

² **Commissioning of the highly granular SiW-ECAL 3 technological prototype**

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⁵ **ABSTRACT:** High precision physics at future colliders as the International Linear Collider (ILC)
⁶ require unprecedented high precision in the determination of the final state of the particles produced
⁷ in the collisions. The needed precision will be achieved thanks to the Particle Flow algorithms (PF)
⁸ which require compact, highly granular and hermetic calorimeters systems. The Silicon-Tungsten
⁹ Electromagnetic Calorimeter (SiW-ECAL) technological prototype design and R&D is oriented
¹⁰ at the baseline design of the ECAL of the International Large Detector (ILD) for the ILC. In this
¹¹ article we present the commissioning and the performance of the prototype in our beam test carried
¹² at DESY in June 2017.

¹³ **KEYWORDS:** Calorimeter methods, calorimeters, Si and pad detectors

14	Contents	
15	1	Introduction
16	2	The SiW-ECAL technological prototype
17	2.1	Silicon sensors
18	2.2	SKIROC: Silicon pin Kalorimeter Integrated ReadOut Chip
19	2.3	Active Sensor Units
20	2.4	Data AcQuisition system
21	2.5	Fully equipped readout modules: the SLABs
22	2.6	The prototype setup
23	3	Commissioning
24	3.1	Tagging and control of the noisy channels.
25	3.2	Optimal trigger threshold determination
26	3.3	S/N ratio in the trigger branch
27	3.4	Prospects
28	4	Performance in a beam test with positrons at DESY
29	4.1	Noise studies and MIP calibration
30	4.1.1	S/N ratio in the charge measurement for MIP interactions
31	4.2	Pedestal and noise stability in a magnetic field
32	4.3	Pedestal stability in electromagnetic shower events
33	5	Summary
34	6	Outlook
35	A	Apendedix: Filtering of fake triggers
		20

36 **1** **Introduction**

37 Future accelerator based particle physics experiments require very precise and detailed reconstruction
38 of the final states produced in the beam collisions. A particular example is the next generation
39 of e^+e^- linear colliders such the ILC[[1–5](#)]. This project will provide collisions of polarized beams
40 with center-of-mass energies (*c.m.e*) of 250 GeV - 1 TeV. These collisions will be studied by two
41 multipurpose detectors: the International Large Detector (ILD) and the Silicon Detector (SiD)[[5](#)].
42 To meet the precision levels required by the ILC physics goals, new techniques relying on single
43 particle separation to make possible the choice of the best information available in the full detector
44 to measure the energy of the final state objects have been developed. These techniques are called

45 Particle Flow (PF) techniques [6–8] and allow to reduce the impact of the poor resolution of the
46 calorimeter systems (compared with trackers) in the overall reconstruction. The PF algorithms
47 impose some special requirements in the design of the detectors. For example, it requires highly
48 granular, compact and hermetic calorimeters.

49 The CALICE collaboration is driving most of the efforts on R&D of highly granular calorime-
50 ters [8] for future linear colliders by investigating and building prototypes for several calorimeter
51 concepts. One of these calorimeters is the silicon-tungsten electromagnetic calorimeter, SiW-
52 ECAL. The SiW-ECAL is the baseline choice for the ILD electromagnetic calorimeter. It consists
53 of a detector (in the barrel region) of $24 X_0$ of thickness which corresponds to $\sim 1 \lambda_I$ (interac-
54 tion length). It has silicon (Si) as active material and tungsten (W) as absorber material. The
55 combination of Si and W choices makes possible the design and construction of a very compact
56 calorimeter with highly granular and compact active layers. It will be built an alveolar structure of
57 carbon fiber into which modules made of tungsten plates and the active sensors will be inserted.
58 The very-front-end (VFE) electronics will be embedded in the detector units. The silicon sensors
59 will be segmented in squared cells (or channels) of 5×5 mm: a total of ~ 100 million readout
60 channels will constitute the ECAL for ILD. The desired signal dynamic range in each channel
61 goes from 0.5 MIP to 3000 MIPs, where the MIP acronym stands for the energy deposited by a
62 minimum-ionizing-particle. To reduce overall power consumption, the SiW-ECAL will exploit
63 the special bunch structure foreseen for the ILC: the e^+e^- bunches trains will arrive in spills of $\sim 1\text{-}2$
64 ms width separated by ~ 200 ms. The data acquisition will be gated during these short windows and
65 during the idle time the bias currents of the electronics will be shut down. This technique is usually
66 denominated power pulsing. In addition to this, to cope with the large amount of channels, the
67 calorimeters should work in self-trigger mode (each channel featuring an internal trigger decision
68 chain) and zero suppression mode.

69 2 The SiW-ECAL technological prototype

70 The first SiW-ECAL prototype was the so called SiW-ECAL physics prototype. It was success-
71 fully tested at DESY, FNAL and CERN running in front of another prototype from the CALICE
72 collaboration, the analogue hadronic calorimeter AHCAL, delivering the proof of concept of the
73 technology and the PF calorimetry. For the physics prototype, the VFE was placed outside the
74 active area with no particular constraints in power consumption. It consisted of 30 layers of Si as
75 active material alternated with tungsten plates as absorber material. The active layers were made of
76 a matrix of 3×3 Si wafers of $500 \mu\text{m}$ thickness. Each of these wafers was segmented in matrices of
77 6×6 squared channels of $1 \times 1 \text{ cm}^2$, allowing for a potential density of 1500 channels/dm 3 assuming
78 the ILD baseline design constraints on the material repartition and compactness. The prototype
79 was divided in 3 modules of 10 layers with different W depth per layer in each of these modules
80 (0.4 , 1.6 and $2.4 X_0$) making a total of $24 X_0$. That very first prototype offered a signal over noise
81 on the measured charge of 7.5 for MIP like particles. More results proving the good performance
82 of the technology and the PF can be found in references [9–14].

83 The current prototype is called the SiW-ECAL technological prototype. It addresses the main
84 technological challenges: compactness, power consumption reduction through power pulsing and
85 VFE inside the detector close to real ILD conditions. It will also provide data to deeply study

the PF and provide input to tune simulation programs as for example GEANT4[15–17] which is widely used in particle physics to simulate the passage of particles through matter. In this section we described in detail the main features and characteristics of the technological prototype.

2.1 Silicon sensors

The sensors consist of high resistivity (bigger than $5000 \Omega\text{-cm}$) silicon wafers with a thickness of $320\mu\text{m}$. The size of the wafers is $9 \times 9 \text{ cm}^2$ and they are each subdivided in an array of 256 PIN diodes of $5 \times 5 \text{ mm}^2$. A MIP traversing the PIN parallel to its normal will create $\sim 80 h^+e^-$ pairs per μm which corresponds to 4.1 fC for particles incident perpendicularly to its surface.

The original design of the silicon wafers included an edge termination made of floating guard-rings. It was observed in beam tests [18, 19] that the capacitive coupling between such floating guard-rings and the channels at the edge created not negligible rates off fake events in tests with high energy beams (pions and electrons with energies larger than 20-40 GeV) An R&D program together with Hamamatsu Photonics (HPK Japan) was conducted to study the guard-rings design as well as the internal crosstalk. It was concluded that using wafers without guard rings and with a width of the peripheral areas lower than $500\mu\text{m}$ thanks to the use of stealth dicing technique, the amount of these squared events can be reduced to be at negligible level.

For the setup described this article we used different solutions for the edge terminations. For all of them, the levels of fake events are at negligible level due to the low energy of the beam used to test the prototype. Therefore, they are not further described here.

2.2 SKIROC: Silicon pin Kalorimeter Integrated ReadOut Chip

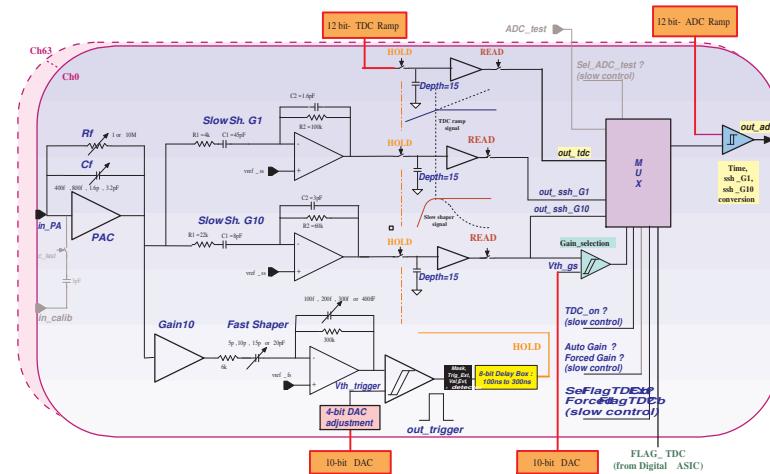


Figure 1. The schematics of the analog part of SKIROC2. High-stack picture (right bottom corner)

The SKIROC[20] (Silicon pin Kalorimeter Integrated ReadOut Chip) is a very front end ASIC (application-specific integrated circuits) designed for the readout of the Silicon PIN diodes. In its version SKIROC2 it consists of 64 channels in AMS $0.35 \mu\text{m}$ SiGe technology. A schematic view of the analog part of the SKIROC2 is shown in Figure 1. Each channel comprises a low noise charge preamplifier of variable gain followed by two branches: a fast shaper for the trigger decision and

111 a set of dual gain slow shaper for charge measurement. The gain can be controlled by modifying
112 the feedback capacitance during the configuration of the detector. With the lowest gain, 6pF, the
113 ASIC will handle a linear dynamic range from 0.1 to up to 1500 MIPs. Finally, a Wilkinson type
114 analogue to digital converter fabricates the digitized charge deposition that can be readout. Once
115 one channel is triggered, the ASIC reads out all 64 channels adding a bit of information to tag
116 them as triggered or not triggered and the information is stored in 15 cell deep physical switched
117 capacitor array (SCA).

118 The SKIROC ASICs can be power-pulsed by taking advantage of the ILC spill structure: the
119 bias currents of the ASIC can be shut down during the idle time between bunch trains. With this
120 method, the ASIC is able to reduce its power consumption down to $25 \mu\text{W}$ per channel, meeting
121 the ILC requirements. The power pulsing feature is used for all the results discussed in this paper
122 and for first time in long periods of data taking in beam test.

123 **2.3 Active Sensor Units**

124 The entity of sensors, thin PCB (printed circuit boards) and ASICs is called Active Signal Units or
125 ASU. An individual ASU has a lateral dimension of $18 \times 18 \text{ cm}^2$. The ASUs are currently equipped
126 further with 16 SKIROC2 ASICs for the read out and features 1024 square pads (64 per ASIC) of
127 $5 \times 5 \text{ mm}$. The channels and ASICs are distributed along the ASU as shown in Figure 2. Each ASU
128 is equipped with 4 silicon wafers as the described in Section 2.1. The high voltage is delivered to
129 the wafers using a HV-kapton sheet that covers the full extension of the wafers.

130 Current version of the PCB is called the FEV11. It has a thickness of 1.6mm and 2.7mm
131 if we include on top the ASICs in its current packaging (1.1 mm thick LFBGA package). With
132 these characteristics, a potential density of 3800 channels/dm³ is achievable keeping the space and
133 interaction length requirements of the the baseline design of the ECAL forthe ILD. This number
134 should be compared with the density achieved in beam tests with the physics prototype: 1500
135 channels/dm³. With the first versions of the technological prototype we reached similar potential
136 density level as in the current version but equipping only a quarter of the ASUs surface [24].

137 **2.4 Data AcQuisition system**

138 The subsequent chain of the data acquisition (DAQ)[21] system consists of three components,
139 enumerate from upstream to downstream from the data flow perspective:

- 140 1. The first component is the so called detector interface (DIF) which is placed at the beginning
141 of each layer holding up to 15 ASUs.
- 142 2. All DIFs are connected by single HDMI cables to the concentrator cards as the second
143 component: the Gigabit Concentrator Cards (GDCCs). These cards are used to control up to
144 7 DIFs. They collect all data from the DIFs and distribute among them the system clock and
145 fast commands.
- 146 3. The most downstream component, is the clock and control card (CCC) which provides a
147 clock, control fan-out of up to 8 GDCCs and accepts and distributes external signals (i.e.
148 signals generated external pulse generator to simulate the ILC spill conditions).

149 The whole system is controlled by the Calicoes and the Pyrame DAQ software version 3 [22, 23].

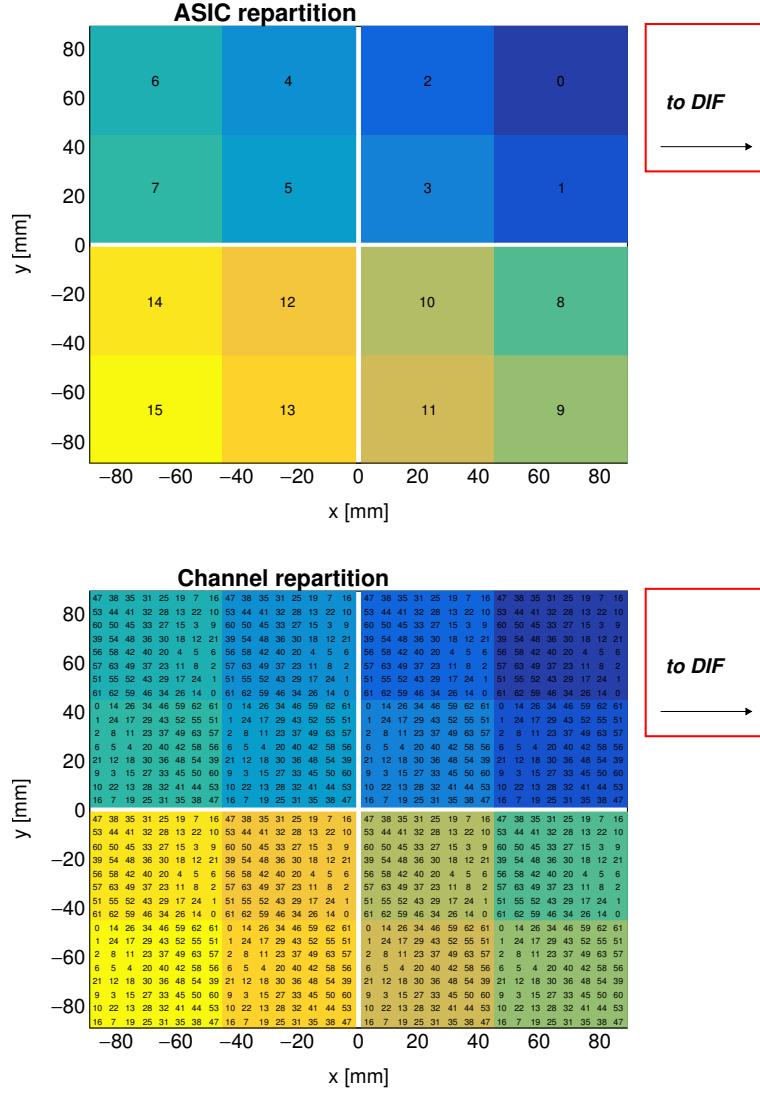


Figure 2. Repartition of the ASIC (up) and channels (down) in one ASU. In this perspective, the Si-Sensors are glued in the back. The channels are separated (in x and y) by 5.5 mm. The empty cross in the middle of the ASU corresponds to the 1 mm separation between the sensors. The areas covered by the different ASICs and channels are labeled with numbers following design and DAQ criteria: from 0-16 in the case of the ASICs and from 0-63 in the case of the channels.

150 2.5 Fully equipped readout modules: the SLABs

151 A full equipped readout module is shown in Fig. 3. These modules are called SLABs and consist
 152 of a chain of one or several fully equipped ASUs connected to a data acquisition system (DAQ)
 153 through an adapter board, called SMBv4. The SMBv4 also serves as to hold other services as power
 154 connectors or the super capacitances used for the power pulsing. These capacitances of 400mF with
 155 16 mΩ of equivalent serial resistance. The capacitances are extra dimensioned to provide enough
 156 local storage of power to assure stable low voltage levels during the power pulsing. The readout
 157 modules are embedded on a "U" shape carbon structure to protect the wafers. The full system is



Figure 3. Open single SLAB with FEV11 ASU, 16 SKIROC 2 and the interface card visibles.

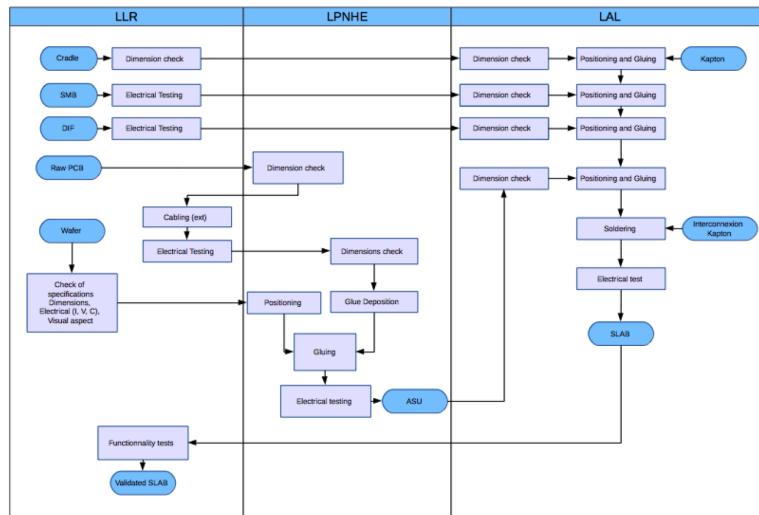


Figure 4. Process flow for the assembly of the SiW-ECAL SLABS.

then covered by two aluminum plates to provide electromagnetic shielding and mechanical stability.
 For the production of the small sample of SLABs studied in this document, a scalable working procedure has been established among several groups [25] profiting from the funding of projects like AIDA2020 or the HIGHTEC emblematic project of the P2IO. A schematic view of this assembly procedure chain can be seen in Figure 4. For more details we refer to Ref.[25]. This process is to be extrapolated to a full assembly procedure for e.g. the ILD detector.

164 2.6 The prototype setup

165 A picture showing the SiW-ECAL technological prototype setup can be seen in Figure 5. The
 166 current prototype consists on 7 layers of SLABs housed in a PVC and aluminum structure that can
 167 host up to 10 layers in slots separated by 15mm each. The first six layers were placed in the first six

168 slots and the last one was in the last slot, with respect to the beam. In the following sections, we
169 will refer to layers number 1 to 7, where the 1 is the closest to the beam pipe and 7 is the farthest.
170 This setup is used for commissioning (Section 3) and for the beam test (Section 4). In both cases,
171 the detector was running in power pulsing mode.

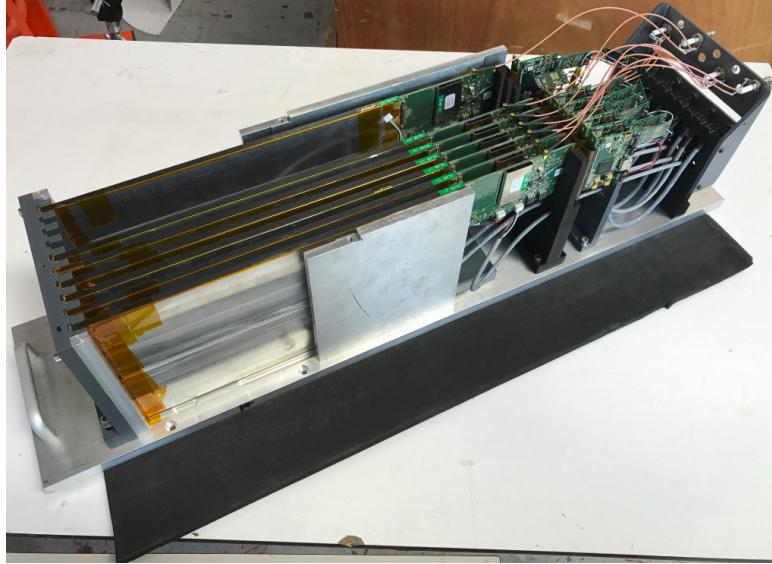


Figure 5. Prototype with 7 layers inside the aluminum stack.

172 3 Commissioning

173 This beam test was prepared by a commissioning phase comprising the debug of the short SLABSS
174 with special emphasis in the control of the noise and the study of the prototype performance in
175 cosmic ray tests.

176 Earlier experiences with the SKIROC2 ASIC are reported in Refs. [24, 26]). Internal SKIROC2
177 parameters reported in these references are adopted in the following unless stated otherwise. For
178 example, a gain value of 1.2pF for the preamplifier is used. With this gain, the SKIROC2 features a
179 linearity better than 90% for 0.5-200 MIPs, which is sufficient for electromagnetic showers created
180 by few GeV electrons or positrons.

181 The main goal of the the commissioning procedure is the optimization of the trigger thresholds
182 to levels in which we are able to record physics signals bellow the MIP level without saturating our
183 DAQ with noise signals. This requires a careful and systematic procedure to:

- 184 1. identify the readout channels that are noisy in high trigger threshold above MIP signal
185 conditions
- 186 2. and select the optimal trigger threshold levels.

187 During the commissioning, we observed the repetition of coherent noise events affecting to
188 several SLABs at the end of acquisitions with long gating time. The situation could be remedied

189 by improving the isolation of the individual SLABs and by reducing the data taking to short gating
190 times.

191 All runs dedicated to the commissioning were characterized by:

- 192 • their short gating windows for the acquisition (1-2ms) at low repetition frequencies (1-5 Hz)
193 to minimize the chances of having real events due to cosmic rays during the data taking and
194 the coherent noise events due to grounding issues;
- 195 • and the relatively high trigger threshold values, between 2 and 0.5 MIPs.

196 **3.1 Tagging and control of the noisy channels.**

197 We found two different types of noisy channels. One set consists of channels randomly distributed
198 along the surface of every ASU and the other consists of channels located in specific areas and
199 systematically noisy in all the ASUs. Preliminary inspections of the PCB layout hint that the
200 channels in the latter set may be noisy due to improvable routing of the PCB. Deeper studies on
201 the PCB routing must be conducted to clarify this. All the noisy channels have been identified
202 and masked and the power of their preamplifiers has been disabled. All the results shown in the
203 following sections are obtained in these conditions.

204 The list of the noisy channels was obtained by means of dedicated data taking runs. In these
205 runs we scan trigger thresholds and progressively mask channels that exhibit counts. In each step,
206 the decision of tagging a channel as noisy was taken following the next rules:

- 207 • if the channel was triggered at rates larger than 0.5-1% of the total number of triggers per
208 ASIC it was added to the list;
- 209 • if a channel was tagged as noisy in at least three of the SLABs, it was tagged as noisy for all
210 and added to the list of channels being suspect of suffer from routing issues.

211 In addition to the different noisy channel types described above, we also have masked full
212 sectors of the SLABs if an ASIC was faulty (at least 70% of channels listed as noisy) or if a Si-wafer
213 was damaged (high leakage currents). The results of this study is summarized in Figure 6.

214 **3.2 Optimal trigger threshold determination**

215 After the noisy channels have been masked, dedicated trigger threshold scan runs are taken, and the
216 results are shown in threshold scan curves where the x-axis represents the threshold value and the
217 y-axis the number of recorded signals normalized to 1. The threshold values are given in internal
218 DAC units which are translated to meaningful physical quantities in Section 3.3. In the absence of
219 external signals (cosmic rays, injected signals, etc) the falling edge position in the threshold scan
220 curves is due to the electronic noise at the output of the fast shaper (the trigger decision branch
221 on the SKIROC) and it depends on the slow clock frequency. These threshold scan curves are
222 approximated by a complementary error function:

$$\frac{2p_0}{\sqrt{\pi}} \int_{\frac{DAC-p_1}{p_2}}^{\infty} e^{-t^2} dt, \quad (3.1)$$

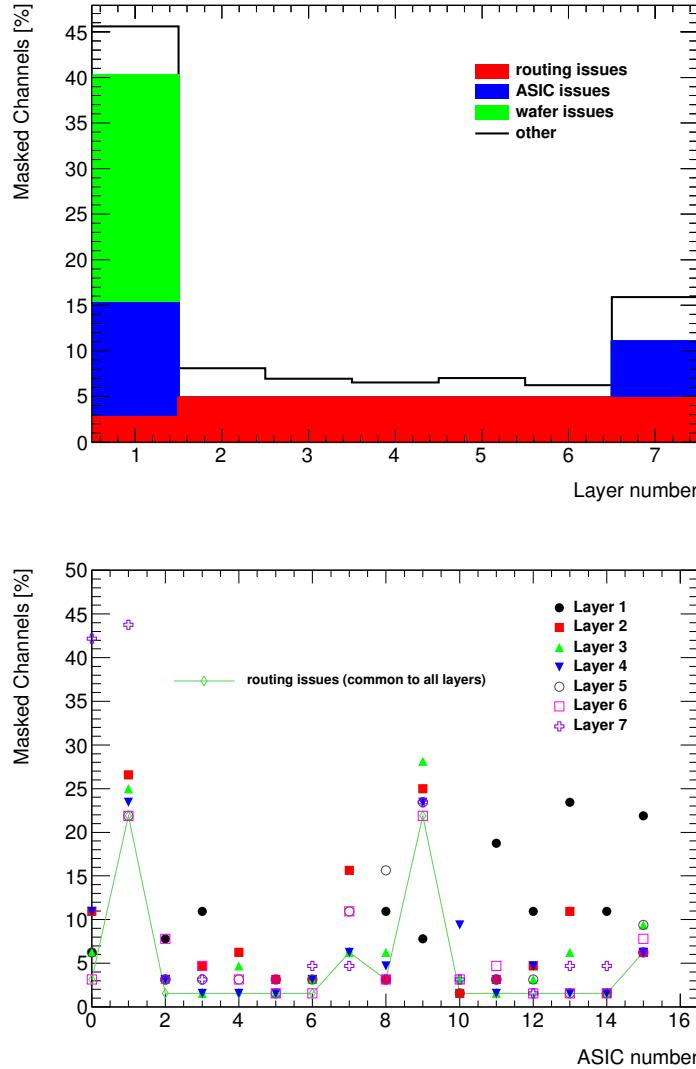


Figure 6. Fraction of channels that are tagged as noisy in all slabs. Top: different type of noisy channels per slab. Bottom: break down of the total number of noisy channels per ASIC. The ASICs 4-7 (wafer issue) and 10 from layer 1 and the ASIC 4 from layer 7 are not included in the second plot since they are fully masked.

where p_0 is 1/2 of the normalization, p_1 is the value in which the noise levels are the 50% of its maximum and p_2 give us the width of the threshold scan curve.

In Figure 7 two threshold scans curves are shown together with the fit by the theoretical function for two different channels from the second layer of the setup are shown.

For every ASICs, after performing the fit of the theoretical curves to the threshold scans, the average values of the p_1 and p_2 are calculated. These are represented by $\langle p_1^{ASIC} \rangle$ in the following. The final threshold value of every ASIC, in DAC units, was chosen using the following formula

$$Threshold_{optimal}^{ASIC} = \text{maximum}(\langle p_1^{ASIC} \rangle + 5 \times \langle p_2^{ASIC} \rangle, 230). \quad (3.2)$$

This formula was applied if at least the 30% of the 64 channels in the ASIC could be fitted. If

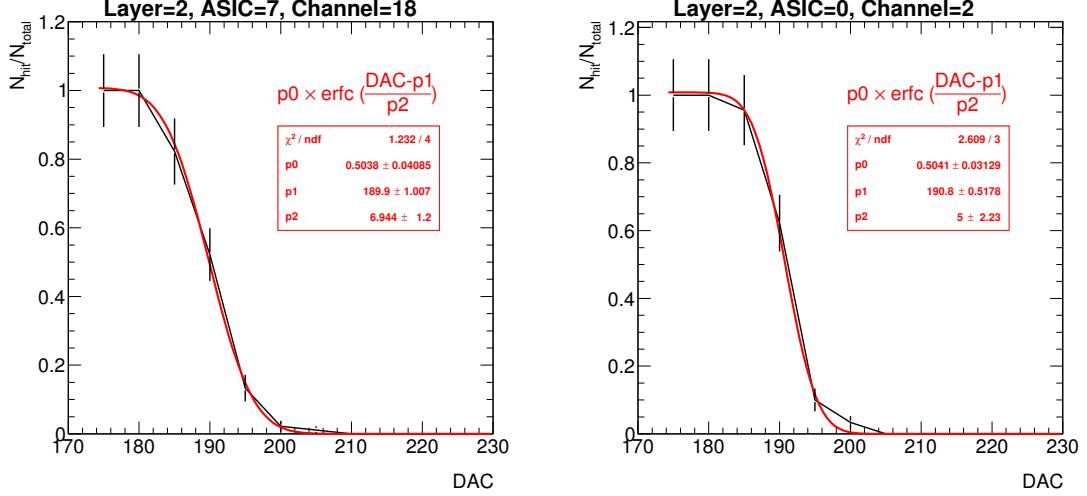


Figure 7. Two threshold scan curves.

not, a global threshold value of 250 was set.

The optimal trigger threshold values for all ASICs are shown in Figure 10, in internal DAC units and in MIPs. In the next section we explain how the conversion is done.

3.3 S/N ratio in the trigger branch

Performing threshold scan scurves using real signals allow to calculate the signal over noise (S/N) ratio to trigger. For that we compare the curves for 1 MIP and 2 MIP injected signals. The S/N is, therefore, defined as the ratio between the distance of both curves at its 50% and the width of the curves. In Figure 8 we see the 1 MIP and 2 MIP curves obtained for several channel in a SKIROC testboard in which a single SKIROC2 in BGA package is placed and the 1 MIP and 2 MIPs signals are directly injected in the preamplifier (via a 3 pF capacitor located in the injection line as shown in Figure 1).

We have obtained similar results using real signals, in this case cosmic rays signals. This is shown in Figure 9 where we show the result of the fit to the threshold scan curves cosmic rays integrated for all channels in one ASIC. For completeness, the fit of threshold scan curves for all channels in the same ASIC are also shown.

From these two results we extract the value of

$$S/N = 12.9 \pm 3.4 \quad (3.3)$$

for the trigger branch. The central value is calculated from the comparison of the blue and red curves in Figure 1 and using the width of the 1 MIP curve in the denominator. The estimated uncertainty has two components: the difference of width between the 1 and 2 MIP curves of injected signals and the differences (width and middle point) between the 1 MIP curves for injected and cosmic ray signals.

Dedicated studies in beam test are needed in order to reduce the uncertainty of this measurement. However, by combining the information contained in the Figs 8 and 9, we can also estimate the

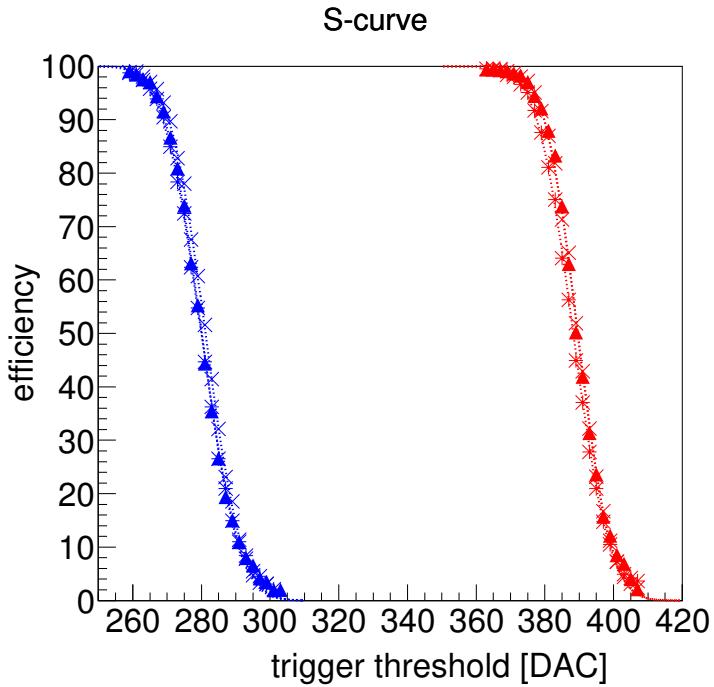


Figure 8. Threshold scan curves with charge injection (1 MIP in blue and 2 MIPs in red) for two different channels in a SKIROC2 testboard.

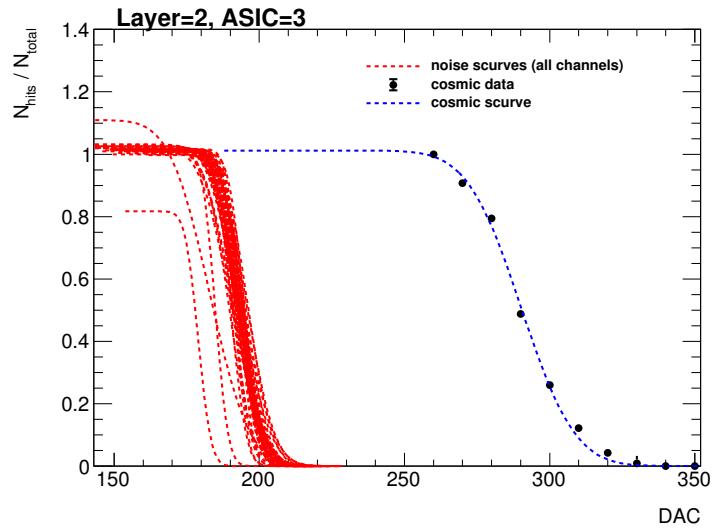


Figure 9. Threshold scan curves for noise (channel by channel, only the result of the fit) and cosmic rays (all channels together) for one ASIC in layer 2.

254 energy that corresponds to a given trigger threshold. This is shown in Figure 10, where the chosen
 255 thresholds of every ASIC being tested in beam are shown.

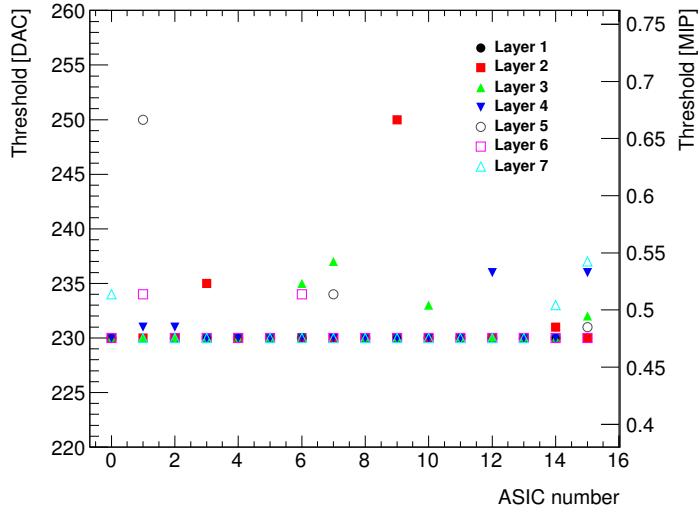


Figure 10. Summary of the trigger threshold settings in internal DAC units and in MIP units.

256 3.4 Prospects

257 The commissioning procedure described above relies on very conservative decisions due to the
 258 presence of unknown noise sources during largest of the commissioning phase. These sources
 259 are now well known and therefore a new “noise commissioning procedure” has been studied. It
 260 will consist on an iterative algorithm that first will identify and mask the channels in which the
 261 number of triggers per channel will be compared with the number of expected triggers assuming
 262 only cosmic rays as signal. This will allow us to have a definition of the noise levels for each
 263 channel independently instead of relative to the total number of triggers recorded by the ASIC.
 264 Finally, once the noisy channels are identified, the threshold are further optimized with a last run
 265 for the identification of the residual noisy channels.

266 Using this new procedure we manage to reduce the number of masked channels by a factor of
 267 two without any loss of performance, at least in the laboratory and using 3 of the 7 SLABs. This new
 268 procedure will also be applied in the next beam test. Also, in order to optimize the commissioning
 269 of the detector, we propose a new set of measurements in the next beam test such as a threshold
 270 scan for the determination of the S/N in the trigger line. The later can be done by the comparison of
 271 threshold curves taken with incident MIP-acting particles and MIP-acting particles traversing the
 272 detector tilted by 45 degrees with respect to the beam direction.

273 4 Performance in a beam test with positrons at DESY

274 The beam line at DESY provides continuous positron beams in the energy range of 1 to 6 GeV
 275 with rates from a few hundreds of Hz to a few KHz with a maximum of \sim 3 KHz for 2-3 GeV. In
 276 addition, DESY gives access to a bore 1 T solenoid, the PCMag.

277 The physics program of the beam test can be summarized in the following points:

- 278 1. Calibration without tungsten absorber using 3 GeV positrons acting MIPs directed to 81
 279 position equally distributed over the modules.
- 280 2. Test in magnetic field up to 1 T using the PCMag. For this test a special PVC structure was
 281 designed and produced to support one single SLAB. The purpose of such test was twofold:
 282 first to prove that the DAQ, all electronic devices and the mechanical consistency of the SLAB
 283 itself are able to handle strong magnetic fields; second to check the quality of the data and
 284 the performance of the detector during the data taking when running in a magnetic field.
- 285 3. Response to electrons of different energies with fully equipped detector, i.e. sensitive parts
 286 and W absorber, with three different repartitions of the absorber material:
- 287 • W-configuration 1: 0.6, 1.2, 1.8, 2.4, 3.6, 4.8 and 6.6 X_0
 288 • W-configuration 2: 1.2, 1.8, 2.4, 3.6, 4.8, 6.6 and 8.4 X_0
 289 • W-configuration 3: 1.8, 2.4, 3.6, 4.8, 6.6, 8.4 and 10.2 X_0

290 First reports on this beam test can be find in Refs. [27, 28]. These results have extended
 291 and are discussed in the following sections. In Section 4.1 we discuss in detail the results of the
 292 pedestal, noise and MIP calibration. We show also results on the pedestal and noise stability when
 293 running inside a magnetic field in Section 4.2 and in electromagnetic shower events in Section 4.3.
 294 The study of the calibration of the prototype in electromagnetic shower events is due to a future
 295 publication.

296 4.1 Noise studies and MIP calibration

297 In Figure 11 we show the signal and pedestal distribution of a single channel after subtracting
 298 the pedestal mean position. The results of the MIP calibration fit are shown in red. The signal
 299 distribution is integrated over all SCAs. For cosmetic reasons the pedestal distribution is shown
 300 only for the first SCA.

301 The pedestal is calculated as the mean position of the distribution of the ADC values for all
 302 channels without trigger. The noise is associated to the width of the distribution. The pedestal
 303 correction is done layer-, chip-, channel- and SCA-wise due to the large spread of values between
 304 pedestals, as observed in Figure 12 (left plot) and Figure 13 (also left plot). For the noise, the
 305 dispersion is much smaller ($\sim 5\%$). This is shown in the right plots of Figures 12 and 13. From
 306 now on, the pedestal correction is applied to all the results presented. The resulting spectra are
 307 fit by a Landau function convoluted with a Gaussian. The most-probable-value of the convoluted
 308 function is taken as the MIP value, allowing thus for a direct conversion from ADC units to energy
 309 in MIP units. The fit succeeded in 98% of the cases and the spread of the resulting MPV is 5%.
 310 The remaining channels will be discarded. Results are summarized in figure 14, leftmost plot.

311 As a sumamry Figure 15 shows the response of all channels integrated over the calibration
 312 run. This plot is obtained after further refinement of the sample by selecting incident tracks. The
 313 maximum peaks at 1 MIP as expected after a good calibration. In addition to this, a second and
 314 a third peaks are visible as shoulders. These shoulder are associated to events involving multiple
 315 particles crossing the detector.

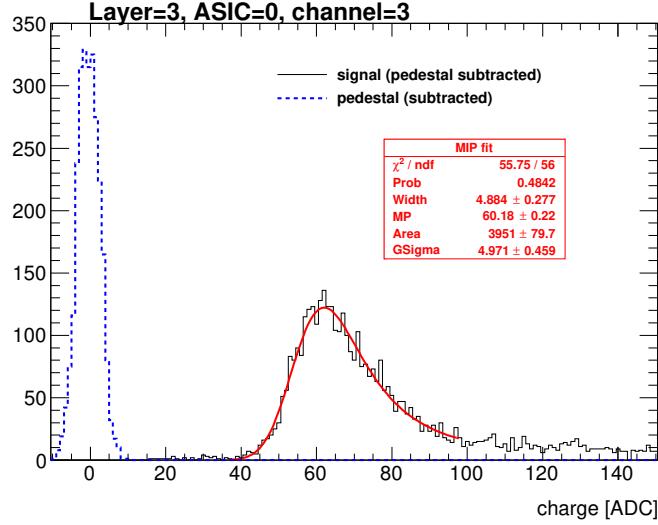


Figure 11. Pedestal (blue dashed line) and signal (black continuous line) distribution for one channel in the third layer.

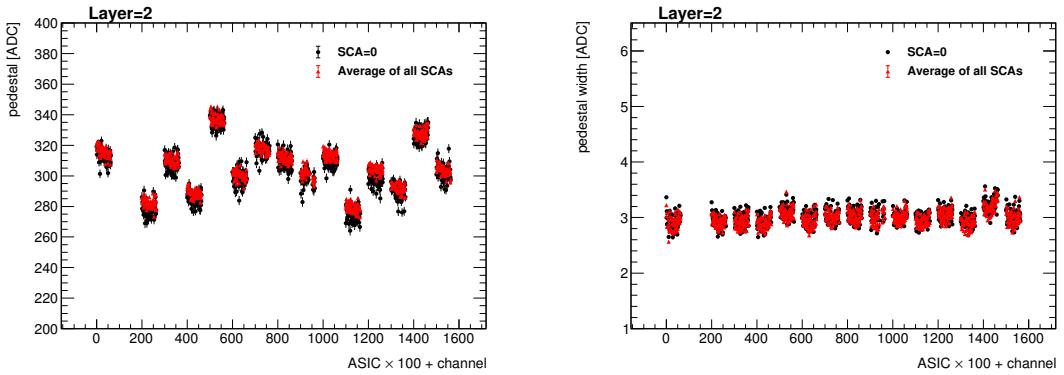


Figure 12. Pedestal mean position (left plot) and width (right plot) for all channels in one layer.

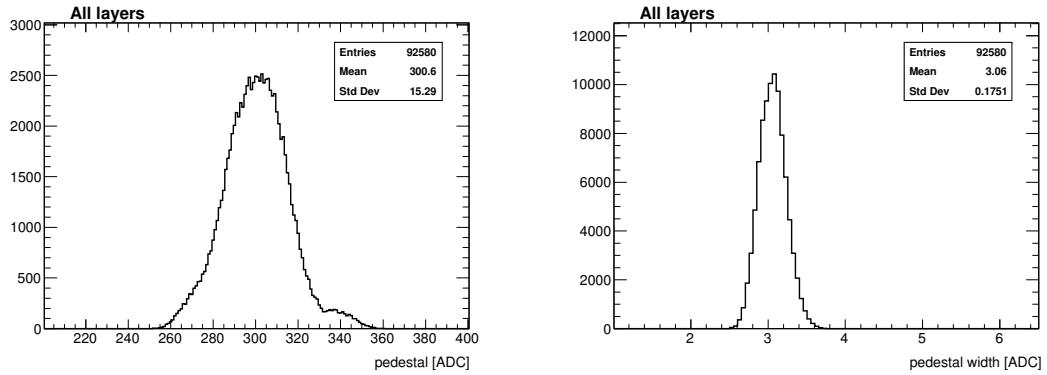


Figure 13. Pedestal mean position (left) and width (right) for all channels and all SCAs in the setup.

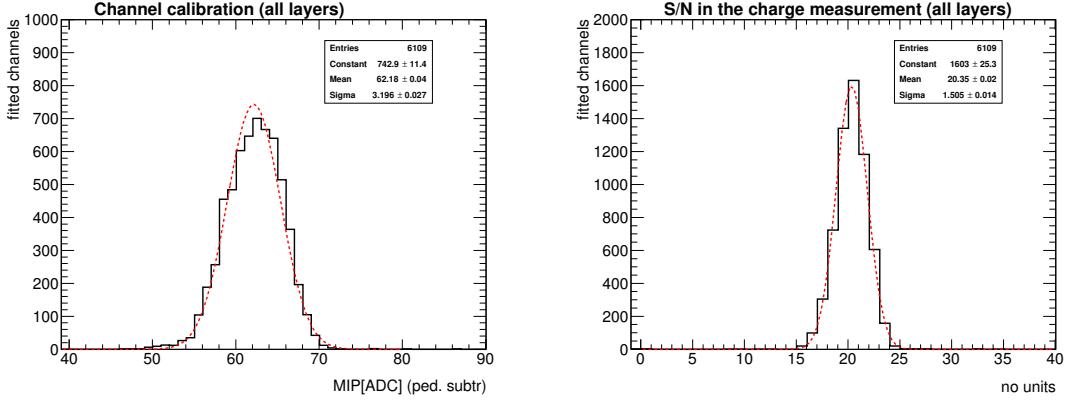


Figure 14. Result of the MIP position calculation and signal over noise calculation for all calibrated channels.

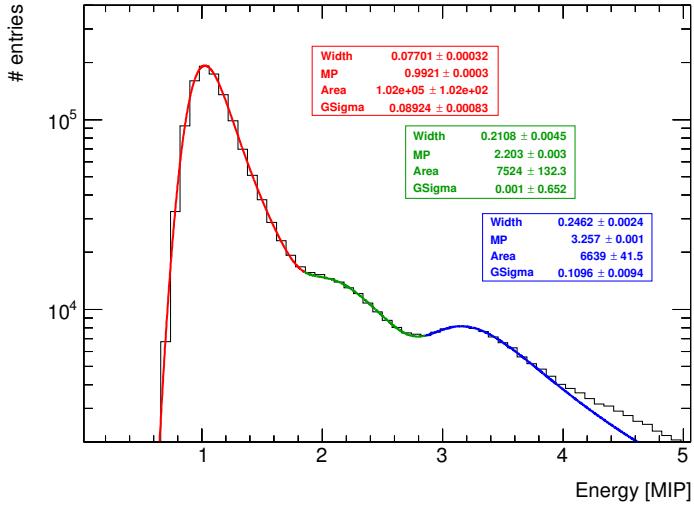


Figure 15. Energy distribution for all calibrated channels when selecting incident tracks of 3 GeV positron acting as MIPs.

To evaluate the single hit detection efficiency we define a high purity sample of events by selecting tracks with at least 4 layers with a hit in exactly the same channel. Afterwards we check which layers have or not a hit in the same or in the closest neighboring channels with energy larger or equal than 0.3 MIP. We repeat this procedure for all channels. The results are shown in Figure 16. Except few exceptions, the efficiency is compatible with 100%. Lower efficiencies in the first layer are related to the presence of noisy channels not spotted during the commissioning. In the last layer we also observe few small deviations which are associated to the outliers channels, hinting for a small misalignment of the last layer.

4.1.1 S/N ratio in the charge measurement for MIP interactions

The signal-over-noise ratio in the charge measurement (corresponding to the slow shaper of the SKIROC2) is defined as the ratio between the most-probable-value of the Landau-gauss function

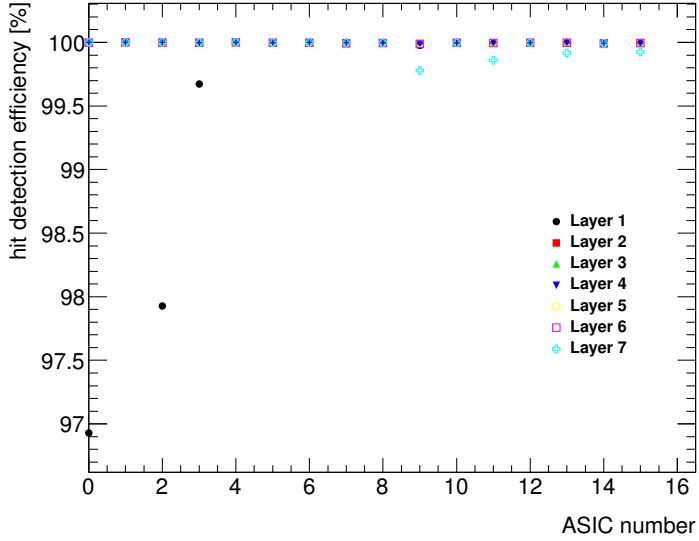


Figure 16. MIP detection efficiency for all layers and ASICS in high purity samples of tracks of MIP-like acting particles.

fit to the data (pedestal subtracted) and the noise (the pedestal width). This quantity has been calculated for all channels and all layers. Results are summarized in Figure 14, rightmost plot.

4.2 Pedestal and noise stability in a magnetic field

The data taking inside the magnetic field has been divided in three runs:

- 331 1. a with a magnetic field of 1 T;
- 332 2. a run with 0.5 T;
- 333 3. and a final run with the magnet off.

334 The beam, 3 GeV positrons, was directed in the area of the PCB readout by the ASIC number
 335 12. The pedestal positions and noise levels of the channels of the ASIC 12 when the SLAB is inside
 336 of the PCMag are compared with the results from the calibration run described in the previous
 337 section. This is shown in Figure 17. We see that the agreement is perfectly good within the
 338 statistical uncertainties. Due to the lower rates in this beam area, the analysis is only done up to few
 339 SCAs.

4.3 Pedestal stability in electromagnetic shower events

341 In this section we discuss the pedestal stability in events with large amount of charge collected by the
 342 ASICS, as are the electromagnetic shower events. All the results shown in this section correspond
 343 to data taken during the tungsten program, using the W-configuration number 2 when shooting the
 344 beam in the area registered by the ASIC 12 (and partially in the 13). For simplicity, only information
 345 recorded by ASIC 12 will be shown. In order to select a high purity of electromagnetic shower like

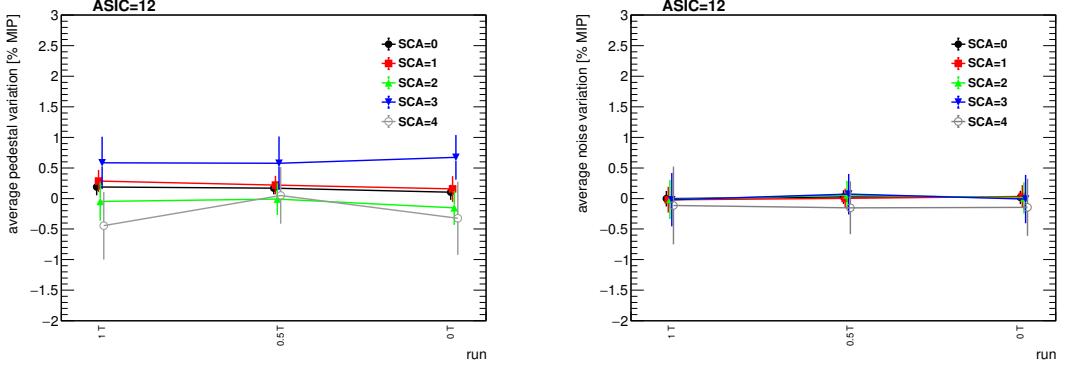


Figure 17. Average deviation of the pedestal mean position (left) and width (right) for all channels in the ASIC 12.

346 the events, we used a simple criteria: select only events with at least 6 of the layers with at least a
347 hit with $E > 0.5$ MIP.

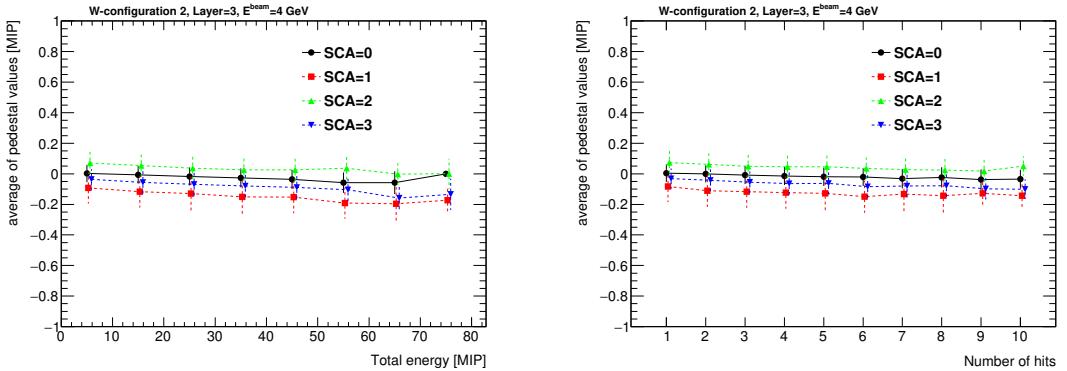


Figure 18. Left: mean position of the projection of the pedestal distribution of all channels calculated when different energies are collected in the ASIC (in bins of 10 MIPs). Right: same but as a function of the number of hits. In both cases, the results are shown for few SCAs. The points for the curves with SCA different than zero are slightly shifted in the x-axis to optimize the visualization.

348 Two main observations have been extracted from the recalculation of the pedestals and its
349 comparison with the values obtained previously during the calibration runs. The first observation
350 consists in a relatively small drift of the pedestal values towards lower values when the collected
351 energy is high *i.e.* when the number of triggered channels is large. This is shown in Figure 18 for
352 several SCAs. A small dependence, in all SCAs, of the pedestal position on the amount of charge
353 collected by the ASIC is observed. This feature is known and it is due to the architecture of the
354 SKIROC2 ASICs where high inrush of currents can slightly shift the baseline of the analogue power
355 supply. The second observation extracted from this analysis can be also seen in Figure 18 but more
356 clearly in Figure 19: in addition to the small drift of the pedestal value an SCA-alternate global
357 shift is observed. We see that the effect is enhanced when large amounts of charge are deposited
358 in the ASIC (*i.e.* at larger beam energies or for the layers in the maximum of the shower profile).
359 We also observed that this alternation is only SCA dependent and does not depends on the time in

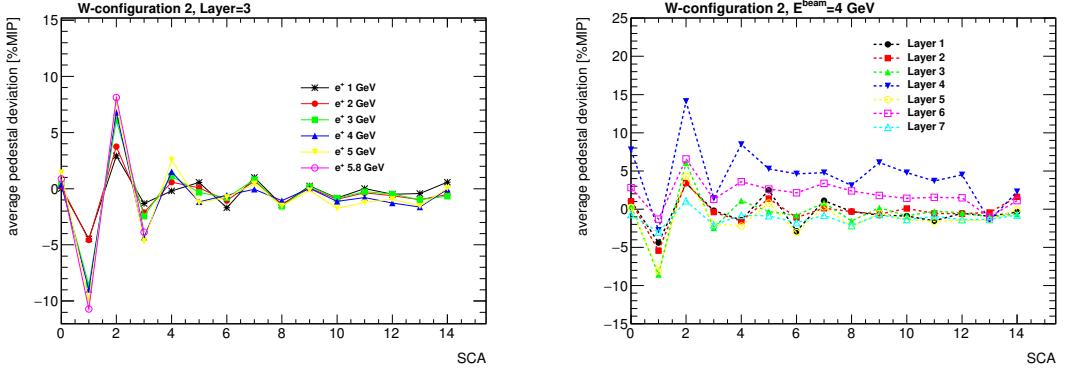


Figure 19. Average value over all channels in ASIC 12 of the pedestals position for each SCA in electromagnetic shower events.

which the deposit of energy occurs within the acquisition. This is not yet fully understood although the fact that the effect is observed in alternate SCAs hints that something is affecting to the digital part of the ASIC (where the SCAs enter in play). Dedicated tests in the laboratory and in the beam are needed in order to clarify this issue.

5 Summary

The R&D program of the highly granular SiW-ECAL detector is in an exciting phase. After the proof of principle of the imaging calorimetry concept using the physics prototype, the technological prototype is being constructed and tested. In this document we describe the commissioning and beam test performance of a prototype built in with the first fully assembled detector elements, in contrast with previous beam tests. In addition, with the setup used in this beam test we reached levels of granularity similar to the targets of the ILD detector for the ILC. This is also the first time that a SiW-ECAL prototype continuously takes data in a beam test running in power pulsing mode, one of the crucial features for the detectors for the ILC. Finally, we tested the performance of the detector modules working for long periods inside magnetic fields.

A very comprehensive and detailed commissioning procedure has been established and optimized allowing us to identify and isolate the different noise sources that could spoil the data taking. The beam test has provided a lot of useful data to study the performance of the detector and to perform a channel by channel calibration, showing a good homogeneity with a spread of the 5% for all channels. The signal over noise, S/N, of the detector has been evaluated to be 12.9 ± 3.4 for the trigger decision and 20.4 ± 1.5 for the charge measurement.

6 Outlook

In parallel to the work described here, several R&D efforts are being carried. One of these efforts is directed to the design and test of new ASICs. In fact, a new generation of SKIROC2, the 2a, has been delivered and it is being tested in the dedicated testboards and it has been integrated in new ASUs. In addition, a new generation of the ASIC, SKIROC3, is foreseen for the final detector construction.

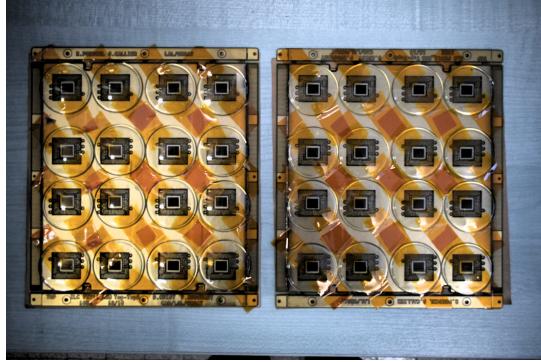


Figure 20. Two FEV11_COB boards with 16 SKIROC2a wire bonded. The ASICS are protected with watch glasses.

385 In contrast with SKIROC2/2a, the new ASIC will be fully optimized for ILC operation, *i.e.* full
 386 zero suppression, reduced power consumption etc.

387 Many efforts are also concentrated in the construction and test of long SLABs made of several
 388 ASUs enchain since we know that the ILD ECAL will host long layers of up to $\sim 2.5\text{m}$. This
 389 device constitutes a technological challenge in both aspects, the mechanical (very thin and long
 390 structure with fragile sensors in the bottom make complicated the assembly procedure and the
 391 handling...) and the electrical (we need to ensure and control the transmission of signals and high
 392 currents along the full device). For example, interconnections between ASUs and between ASU
 393 and interface card are one of the most involved parts of the assembly and require close collaboration
 394 between mechanical and electronic engineers. A first long SLAB prototype of ~ 8 ASUs has been
 395 already tested in beam test also in DESY in 2018.

396 In parallel, a different proposal for a thinner ASU design is being investigated. This is motivated
 397 by the high density of channels demanded by the Particle Flow algorithms. In this alternative PCB
 398 design the ASICS are directly placed on board of the PCB in dedicated cavities. The ASICS will be
 399 in semiconductor packaging and wire bonded to the PCB. This is the so-called COB (chip-on-board)
 400 version of the ASU. A small sample of FEV11_COBs (same connexion pattern with the interface
 401 card than FEV11) with a total thickness of 1.2 mm (to be compared with the 2.7 of the LFBGA
 402 solution) has been produced and tested in the laboratory showing its readiness for tests with particle
 403 beams. A sample can be seen in Figure 20. These new boards maximize the density of channels
 404 ($6000 \text{ channels}/\text{dm}^3$) for the ECAL of the ILD and will allow to satisfy the baseline requirements
 405 of the ECAL for the ILD.

406 Finally, intensive R&D on the compactification of the DAQ to meet the tight space requirements
 407 for the ILD is being done by the SiW-ECAL collaboration.

408 It is foreseen that all these developments, with the exception of the SKIROC3, will be tested
 409 with particle beams during 2018-2019.

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419 Hamburg (Germany), a member of the Helmholtz Association (HGF).

420 A Appendix: Filtering of fake triggers

421 Several types of fake signals have been observed in the technological prototype since its construction
422 and test. A detailed description of them can be found in previous articles, as for example, in Ref.
423 [24]. All these fake signals are easily identified and tagged during the data acquisition and removed
424 afterwards from the analysis not introducing any significance loss of performance as can be seen,
425 for example, in the hit detection efficiency plots (see Section 4.1). In the following, we briefly
426 describe the status of the monitoring, debugging and filtering of such kind of events.

427 Empty triggers

428 Empty trigger events are a well known feature of SKIROC2. The SKIROC2 uses an OR64 signal
429 to mark the change to a new SCA when a signal over threshold is detected. The empty triggers
430 appear when during the acquisition the rising edge of the slow clock falls during the OR64 signal
431 and therefore the change to a new SCA is validated twice. This effect creates around 17% of empty
432 events which are easily filter and removed from the analysis. The ratio of empty triggers in the new
433 SKIROC2a has been reduced to the $\sim 2 - 3\%$ by reducing the length of the OR64 signal.

434 Plane events and retriggers

435 Another well known issue is the appearance of bunches of consecutive fake triggers, called retriggers,
436 that saturates the DAQ. Although the ultimate reason of the appearance of these events remains not
437 clear, it is suspected that they are related to distortions of the power supply baselines. We know
438 that the SKIROC2 and 2a preamplifiers are referenced to the analog power supply level, therefore,
439 any voltage dip can be seen as signal by the preamplifiers. Moreover the presence of a high inrush
440 of current due to many channels triggered at the same time can create these voltage dips and also
441 produce the so called plane events (most of the channels triggered at once). In previous studies
442 the ratio of retriggers and plane events was reduced by improving the power supply stabilization
443 capacitances.

444 Studying the MIP calibration data of this beam test we have noticed that the concentration
445 of the retriggers and plane events in ASICs far from the beam spot is higher than in the ASICs
446 that are reading out the information of real hits. We have also observed that the concentration of
447 these events is higher in the nearby of channels that were masked as suspicious of suffering from
448 routing issues. The ratio these events have been estimated to be of 1 – 3% in the ASICs where
449 high frequency interactions are produced (*i.e.* using 3 GeV positrons at 2-3 KHz) and at higher
450 rates even larger than 40% in other ASICs far from the beam spot. Moreover, it has been noticed a
451 correlation between the time that an ASIC was full and the time of the appearance of some retriggers

452 in other areas of the PCB. This correlation corresponds to $\sim 1.6 \mu\text{s}$ which hints of a distortion on
453 the analogue power supply when the signal that informs the DIF that one ASIC memory is full is
454 transmitted through the PCB.

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