

² **Commissioning of the highly granular SiW-ECAL 3 technological prototype**

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⁵ **ABSTRACT:** High precision physics at future colliders as the International Linear Collider (ILC)
⁶ require unprecedented high precision in the determination of the final state of the particles produced
⁷ in the collisions. The needed precision will be achieved thanks to the Particle Flow algorithms (PF)
⁸ which require compact, highly granular and hermetic calorimeters systems. The Silicon-Tungsten
⁹ Electromagnetic Calorimeter (SiW-ECAL) technological prototype design and R&D is tailored to
¹⁰ the baseline design of the ECAL of the International Large Detector (ILD) for the ILC. In this
¹¹ document we present and discuss the commissioning of the prototype and the performance of the
¹² device in a beam test carried at DESY in June 2017.

¹³ **KEYWORDS:** Calorimeter methods, calorimeters, Si and pad detectors

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37 **1** **Introduction**

38 Future accelerator based particle physics experiments require very precise and detailed reconstruction
39 of the final states produced in the beam collisions. A particular example is the next generation
40 of e^+e^- linear colliders such the ILC[1–5]. This project will provide collisions of polarized beams
41 with centre-of-mass energies (*c.m.e*) of 250 GeV - 1 TeV. These collisions will be studied by two
42 multipurpose detectors: the International Large Detector (ILD) and the Silicon Detector (SiD)[5].
43 To meet the precision levels required by the ILC physics goals, new techniques relying on single
44 particle separation to make possible the choice of the best information available in the full detector
45 to measure the energy of the final state objects have been developed. These techniques are

46 called Particle Flow (PF) techniques [9–11] and allow to reduce the impact of the poor resolution
47 of the calorimeter systems (compared with trackers) in the overall reconstruction. The detectors
48 optimized for PF algorithms have some requirements. In the case of calorimeters: highly granular,
49 compact and hermetic calorimeters. The CALICE collaboration is doing R&D of highly granular
50 calorimeters [11] for future linear colliders.

51 In this document we will focus in the description of the silicon-tungsten electromagnetic
52 calorimeter, SiW-ECAL, its commissioning and its performance in beam test. The SiW-ECAL is
53 the baseline choice for the ILD ECAL. It consists in a detector (in the barrel region) of $24 X_0$ of
54 thickness which corresponds to $\sim 1 \lambda_I$ (interaction length). It has silicon (Si) as active material and
55 tungsten (W) as absorber material. The combination of Si and W choices makes possible the design
56 and construction of a very compact calorimeter with highly granular and compact active layers. It
57 will consist of an alveolar structure of carbon fiber into which modules made of tungsten plates
58 and the active sensors will be inserted. The very-front-end (VFE) electronics will be embedded
59 in the SLABs. The silicon sensors will be segmented in squared cells (or channels) of $5 \times 5 \text{ mm}^2$:
60 a total of ~ 100 million channels will constitute the ECAL for ILD. The desired signal dynamic
61 range in each channel goes from 0.5 MIP to 3000 MIPs. To reduce overall power consumption, the
62 SiW-ECAL will exploit the special bunch structure foreseen for the ILC: the e^+e^- bunches trains
63 will arrive within acquisition windows of $\sim 1\text{-}2 \text{ ms}$ width separated by $\sim 200 \text{ ms}$. During the idle
64 time, the bias currents of the electronics will be shut down. This technique is usually denominated
65 power pulsing. In addition to this, to cope with the large amount of channels, the calorimeters
66 should work in self-trigger mode (each channel featuring an internal trigger decision chain) and
67 zero suppression mode.

68 2 The SiW-ECAL technological prototype

69 The first SiW-ECAL prototype was the so called SiW-ECAL physics prototype. It was success-
70 fully tested at DESY, FNAL and CERN running in front of another prototype from the CALICE
71 collaboration, the analogue hadronic calorimeter AHCAL, delivering the proof of concept of the
72 technology and the PF calorimetry. For the physics prototype, the VFE was placed outside the
73 active area with no particular constraints in power consumption. It consisted of 30 layers of Si as
74 active material alternated with tungsten plates as absorber material. The active layers were made
75 of a matrix of 3×3 Si wafers of $500 \mu\text{m}$ thickness. Each of these wafers was segmented in matrices
76 of 6×6 squared channels of $1 \times 1 \text{ cm}^2$, allowing for density of $1500 \text{ channels/dm}^3$. The prototype was
77 divided in 3 modules of 10 layers with different W depth per layer in each of these modules (0.4,
78 1.6 and $2.4 X_0$) making a total of $24 X_0$. That very first prototype offered a signal over noise on the
79 measured charge of 7.5 for MIP like particles. More results proving the good performance of the
80 technology and the PF can be found in references [12–17].

81 The new generation prototype is called the SiW-ECAL technological prototype. It addresses
82 the main technological challenges: compactness, power consumption reduction through power
83 pulsing and VFE inside the detector close to real ILD conditions. It will also provide data to deeply
84 study the PF and provide input to tune simulation programs as for example GEANT4[18–20] which
85 is widely used in particle physics to simulate the passage of particles through matter. In this section
86 we described in detail the main features and characteristics of the technological prototype.

87 **2.1 Silicon sensors**

88 The sensors consist on floating zone silicon wafers $320\mu\text{m}$ thick with high resistivity (bigger than
89 $5000\ \Omega\cdot\text{cm}$). The size of the wafer is $9\times 9\ \text{cm}^2$ and it is subdivided in an array of 256 PIN diodes
90 of $5\times 5\ \text{mm}^2$. A MIP traversing the PIN parallel to its normal will create $\sim 80\ h^+e^-$ pairs per μm
91 which corresponds to 4.1 fC for particles incident perpendicularly to its surface.

92 The original design of the silicon wafers included an edge termination made of floating guard-
93 rings. It was observed in beam tests [21, 22] that the capacitive coupling between such floating
94 guard-rings and the channels at the edge was not negligible in tests with high energy beams (pions
95 and electrons with energies larger than 20-40 GeV). This coupling lead to fake events in which,
96 at least, the channels in the four edges of the wafer are triggered at the same time. This is why
97 these events are called squared events. An R&D program together with Hamamatsu Photonics
98 (HPK Japan) was conducted to study the guard-rings design as well as the internal crosstalk. It
99 was concluded that using wafers without guard rings and with a width of the peripheral areas lower
100 than $500\ \mu\text{m}$ thanks to the use of stealth dicing technique, the amount of these squared events can
101 be reduced to be almost negligible. This need to be confirmed in beam test. Unfortunately, for the
102 interaction with low energy particles as the delivered at the DESY beam test facility (see Section 4)
103 the amount of squared events is expected to be negligible, therefore we will not discuss this issue
104 in the following.

105 **2.2 SKIROC: Silicon pin Kalorimeter Integrated ReadOut Chip**

106 The SKIROC[23] (Silicon pin Kalorimeter Integrated ReadOut Chip) is a very front end ASIC
107 (application-specific integrated circuits) designed for the readout of the Silicon PIN diodes. In its
108 version SKIROC2 it consists of 64 channels in AMS $0.35\ \mu\text{m}$ SiGe technology. Each channel
109 comprises a low noise charge preamplifier of variable gain followed by two branches: a fast shaper
110 for the trigger decision and a set of dual gain slow shaper for charge measurement. The gain can
111 be controlled by modifying the feedback capacitance during the configuration of the detector. With
112 the slowest gain, 6pF , the ASIC will handle a linear dynamic range from 0.1 to up to 1500 MIPs
113 (a slightly less than the desired final value for the ILC). Finally, a Wilkinson type analogue to
114 digital converter fabricates the digitized charge deposition that can be readout. Once one channel is
115 triggered, the ASIC reads out all 64 channels adding a bit of information to tag them as triggered or
116 not triggered and the information is stored in 15 cell deep physical switched capacitor array (SCA).

117 The SKIROC ASICs can be power-pulsed by taking advantage of the ILC spill structure: the
118 bias currents of the ASIC can be switched off during the idle time between bunch trains. With this
119 method, the ASIC is able to reduce its power consumption down to $25\ \mu\text{W}$ per channel, meeting
120 the ILC requirements. All the results shown in this paper are obtained in power pulsing mode.

121 **2.3 Active Sensor Units**

122 The entity of sensors, thin PCB (printed circuit boards) and ASICs is called Active Signal Units or
123 ASU. An individual ASU has a lateral dimension of $18\times 18\ \text{cm}^2$. The ASUs are currently equipped
124 further with 16 SKIROC2 ASICs for the read out and features 1024 square pads (64 per ASIC) of
125 $5\times 5\ \text{mm}$. The channels and ASICs are distributed along the ASU as shown in Figure 2. Each ASU

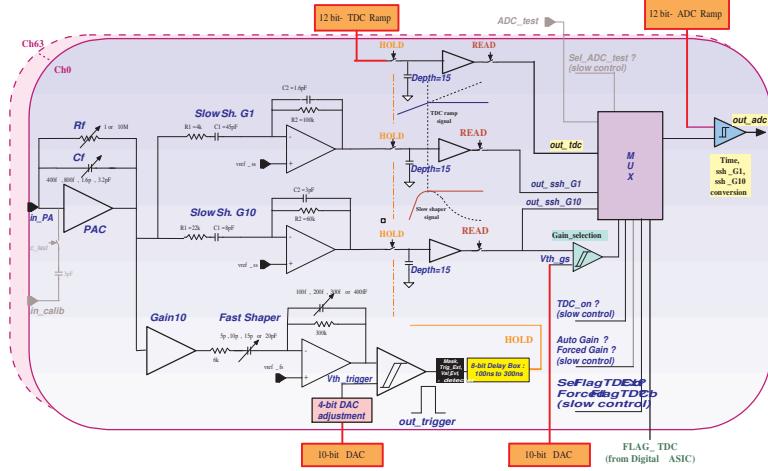


Figure 1. The schematics of the analog part of SKIROC2. High-stack picture (right bottom corner)

is equipped with 4 silicon wafers as the described in Section 2.1. The high voltage is delivered to the wafers using a HV-kapton sheet that covers the full extension of the wafers.

2.4 Data AcQuisition system

The subsequent chain of the data acquisition (DAQ)[24] system is inspired by the ILC. It consists on three modules. The first module is the so called detector interface (DIF) which is placed at the beginning of each layer holding up to 15 ASUs; All DIFs are connected by single HDMI cables to the concentrator cards that make the second module: the Gigabit Concentrator Cards (GDCCs). This cards are used to control up to 7 DIFs collecting all data from them and distributing among them the system clock and fast commands. The last module, the most downstream, is the clock and control card (CCC) which provides a clock, control fan-out of up to 8 GDCCs and accepts and distributes external signals (i.e. signals generated external pulse generator to simulate the ILC spill conditions). The whole system is controlled by the Calicoes and the Pyrame DAQ software version 3 [25, 26].

2.5 Readout layers and SLABs

The readout layers of the SiW-ECAL consist of a chain of ASUs and an adapter board to a data acquisition system (DAQ) at the beginning of the layer. This adapter board is called SMBv4 and it also serves as to hold other services as power connectors or the super capacitances used for the power pulsing. These capacitances of 400mF with 16 mΩ of equivalent serial resistance. The purpose of these capacitances is to provide local storage of the necessary charge to avoid the transport of current pulses over long cables, ensuring in this way the stability of the ASICs during the acquisition.

The readout layers are embedded on a "U" shape carbon structure to protect the wafers. The full system is then covered by two aluminum plates to provide electromagnetic shielding and mechanical stability. This ensemble is denominated SLAB ("short" for 1 ASU ensembles or "long" for several ASUs enchained) and it can be seen in Figure 3. With current SLABs, a potential density of 4000 channels/dm³ is achievable. This number should be compared with the density achieved for previous beam tests: 1500 channels/dm³ [27].

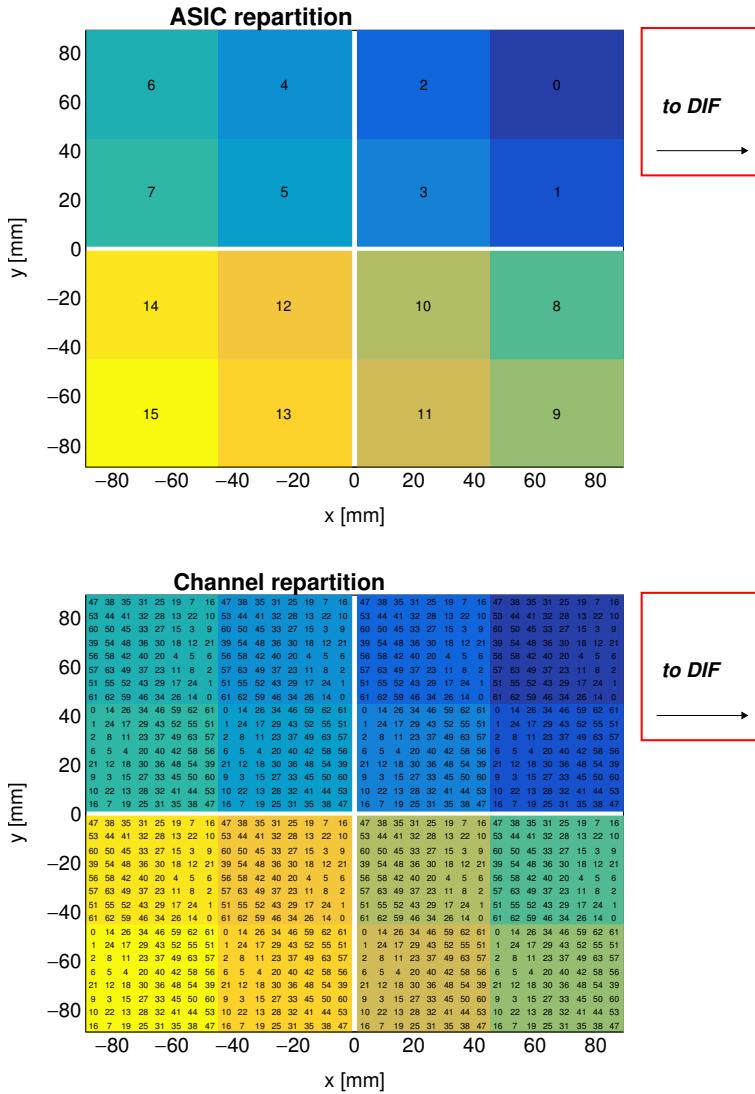


Figure 2. Repartition of the ASIC (up) and channels (down) in one ASU. In this perspective, the Si-Sensors are glued in the back. The channels are separated (in x and y) by 5.5 mm. The empty cross in the middle of the ASU corresponds to the 1 mm separation between the sensors. The areas covered by the different ASICs and channels are labeled with numbers following design and DAQ criteria: from 0-16 in the case of the ASICs and from 0-63 in the case of the channels.

The SiW-ECAL detector designed for the ILD requires of the order of 10^5 highly integrated detection like the ones described in this text. For the production of the small sample of SLABs studied in this document, a scalable working procedure has been established among several groups [28] profiting from the funding of projects like AIDA2020 or the HIGHTEC emblematic project of the P2IO. A schematic view of this assembly procedure chain can be seen in Figure 4. For more details we refer to Ref.[28].

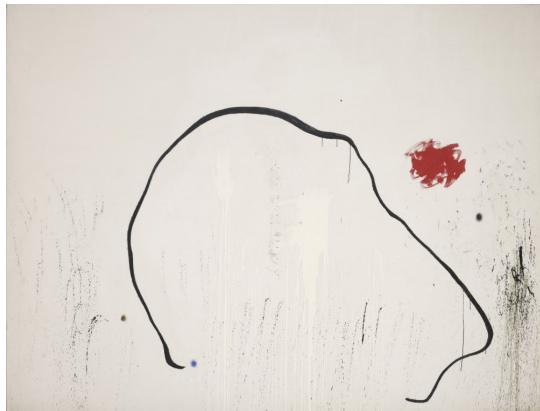


Figure 3. Temporary picture: La Esperanza del Condenado, J. Miró: Open single SLAB with FEV11 ASU, 16 SKIROC 2, interface card and DIF visibles.

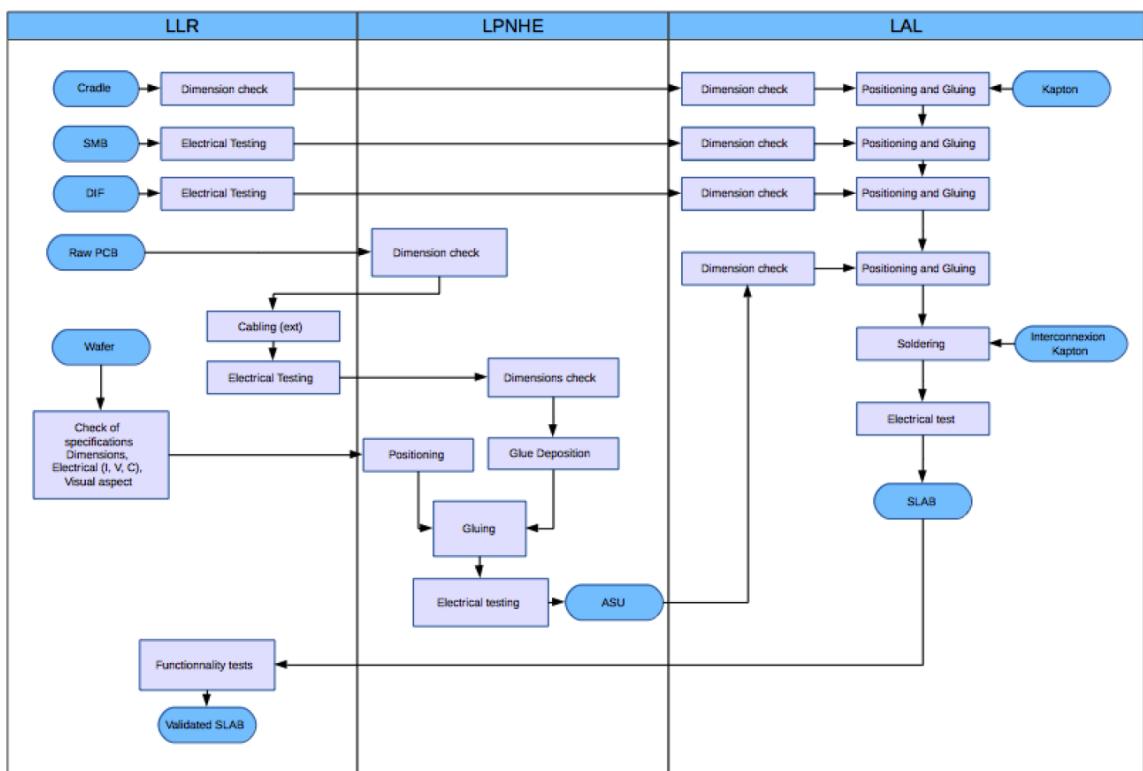


Figure 4. Process flow for the assembly of the SiW-ECAL SLABS.

158 3 Commissioning

159 This beam test was prepared by a careful and comprehensive commissioning comprising the debug
 160 of the short SLABSS with special emphasis in the control of the noise and the study of the prototype
 161 performance in cosmic rays tests.

162 Earlier experiences with the SKIROC2 ASIC are reported in Refs. [27, 29]). Internal SKIROC2
 163 parameters found in these references are adopted in the following except if the opposite is stated.

164 For example, the gain value of 1.2pF for the preamplifier is used. With this gain, the SKIROC2
165 ensures a linearity better than 90% for 0.5-200 MIPs, which is enough for electromagnetic showers
166 created by few GeV electrons or positrons.

167 **3.1 Optimization of noise levels**

168 Studying and control the noise levels is crucial since noisy channels may saturate the DAQ faster
169 than physical signals. Two different types of noise sources were identified: a set of noisy channels
170 randomly distributed in time and noise bursts affecting to all layers at the same time. The outcome
171 of this commissioning is summarized in Figure 5.

172 The first type of noise source, noise events randomly distributed in time, forced us to define a
173 list of channels to be masked in all layers. Again, two different type of noisy channels have been
174 identified. The first group is composed by randomly distributed in space channels. The second group
175 is made of a fixed list of channels, all in the same positions for all SLABs, and all associated to a
176 higher rate of events with underflowed value of the read ADC. A large amount of these channels are
177 located in areas of the PCB where the density of lines (data and power transmission) is higher than
178 in others. This hints for an issue on the routing of the PCB. Therefore, these channels are tagged
179 in Figure 5 with the "routing issues" label although more tests and deeper inspections of the PCB
180 layout are needed to clarify this issue.

181 The list of the noisy channels randomly distributed in time and space was defined by means
182 of dedicated data taking runs. These runs were characterized by: their short acquisition windows
183 (open to data recording for only 1.1 ms) at low repetition frequencies (5 Hz) to minimize the chances
184 of having real events due to cosmic rays hitting the detector during the data taking; and the relatively
185 high trigger threshold values between 250 and 400 DAC (which are equivalent to ~0.5-2 MIP, see
186 Section 3.2 for more information). The full process was an iterative process starting with several
187 repetitions of runs at a high threshold value and then some iterations at lower threshold but always
188 higher than 0.5 MIP. In each of the iterations, the channels identified as noisy were masked. A full
189 run involved 3-5 threshold values and at least two repetitions per value. Again, we decided to follow
190 a conservative approach for listing the noisy channels to be masked: if the channel was triggered at
191 rates larger than 0.5-1% of the total number of triggers per ASIC it was added to the list. These
192 channels are labeled as "other" in the first plot in Figure 5.

193 In addition to the different noisy channel types described above, we also have masked full
194 sectors of the SLABs if an ASIC was faulty (at least 70% of channels listed as noisy) or if a Si-wafer
195 was misworking (high leakage currents). In these cases and in all mentioned above, the masking
196 involved two steps: disabling of the trigger and the disabling of the power of the preamplifier of
197 that channel.

198 The other source of noise mentioned at the beginning of this section consists on noise bursts
199 happening coherently at the same time in all SLABs and it was correlated to occasions when the
200 electrical isolation between SLABs was broken. This is a hint of a system effect as can be the
201 appearance of grounding loops or disturbances in the power supplies. The issue was circumvented
202 by improving the electrical isolation of single layers. We have also observed that the noise bursts
203 happens only at the end of long acquisitions. Therefore, in addition to the improved isolation, we
204 selected short enough acquisition windows (which indeed are the most appropriate to the high

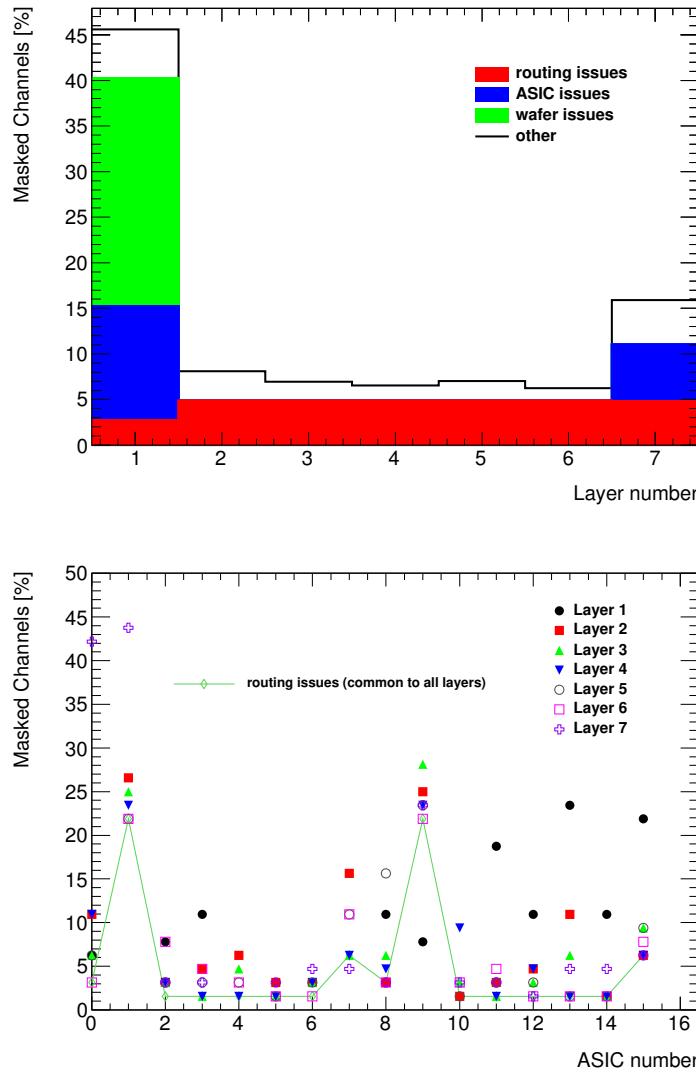


Figure 5. Ratio of channels that are marked as noisy in all slabs. Top: inventory of the different type of noisy channels per slab. Bottom: break down of the total number of noisy channels per ASIC. The ASICs 4-7 (wafer issue) and 10 from layer 1 and the ASIC 4 from layer 7 are not included in the second plot since they are fully masked.

205 rates of particles in the DESY beam). Dedicated studies in the laboratory are currently ongoing in
206 order to fully understand this issue.

207 The list of channels mentioned above is discarded from the data taking from now on.

208 3.2 Threshold determination

209 In order to select the optimal trigger threshold values for the detector operation we perform dedicated
210 scans of trigger threshold values with all channels enabled (excepted the marked as noisy). The
211 threshold values are given in internal DAC units which are translated to meaningful physical
212 quantities in Section 3.3. The threshold scan curves made of the total number of hits normalized

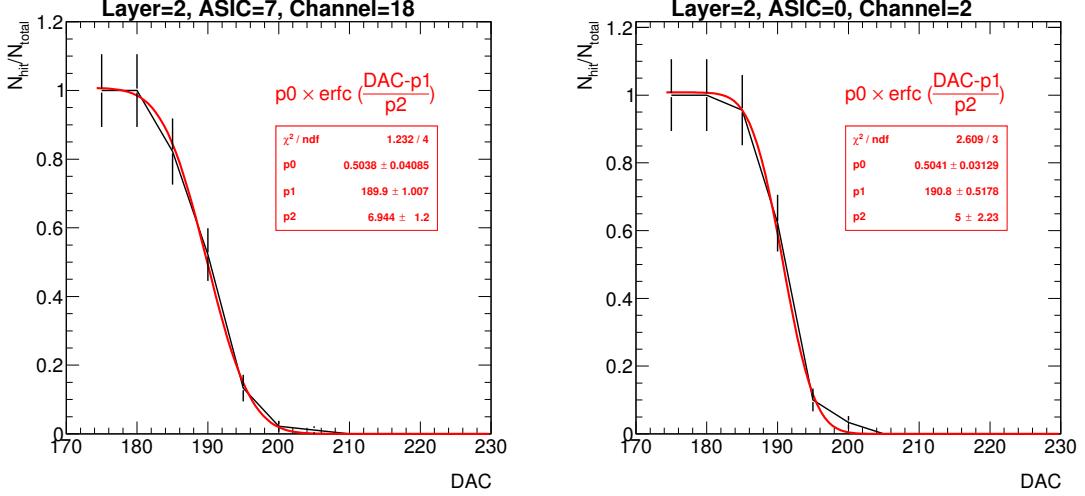


Figure 6. Two threshold scan curves and their associated ThS curves.

213 to 1 vs the threshold for each channel are modeled by a complementary error function called ThS
214 curves from now on:

$$ThS(DAC) = p_0 \times erfc\left(\frac{DAC - p_1}{p_2}\right) = \frac{2p_0}{\sqrt{\pi}} \int_{\frac{DAC-p_1}{p_2}}^{\infty} e^{-t^2} dt, \quad (3.1)$$

215 where p_0 is 1/2 of the normalization, p_1 is the value in which the noise levels are the 50% of its
216 maximum and p_2 give us the width of the ThS curve.

217 In the absence of external signals (cosmic rays, injected signals, etc) these noise ThS curves
218 show the convolution of the envelope of the electronic noise at the output of the fast shaper (the
219 trigger decision branch on the SKIROC). Indeed, the size of this envelope is related to the slow
220 clock frequency.

221 To reduce to the minimum the presence of cosmic rays signals, we perform runs with short open
222 acquisition windows as described in the previous section. In Figure 6 two result of two threshold
223 scans and the fit by a ThS curves for two different channels from the second layer of the setup are
224 shown.

225 The function from equation 3.1 was fitted to all channels data and all the values of p_1 and p_2
226 were saved. The final threshold value of every ASIC, in DAC units, was chosen by taking the

$$\text{maximum}(DAC_{optimal}^{ASIC-j} = < p_1^{ASIC-j} > + 5 \times < p_2^{ASIC-j} >, 230) \quad (3.2)$$

227 if at least the the 30% of the 64 channels ThS curves in the ASIC could be fitted. If only less
228 than the 30% of curves of the 64 channels were successfully fit, a global DAC value of 250 was set.
229 The $<>$ denotes the average over all the channels on the ASIC. The choice of these two values was
230 sustained by previous experiences, see for example [27].

231 The optimal trigger threshold values for all ASICs are shown in Figure 9.

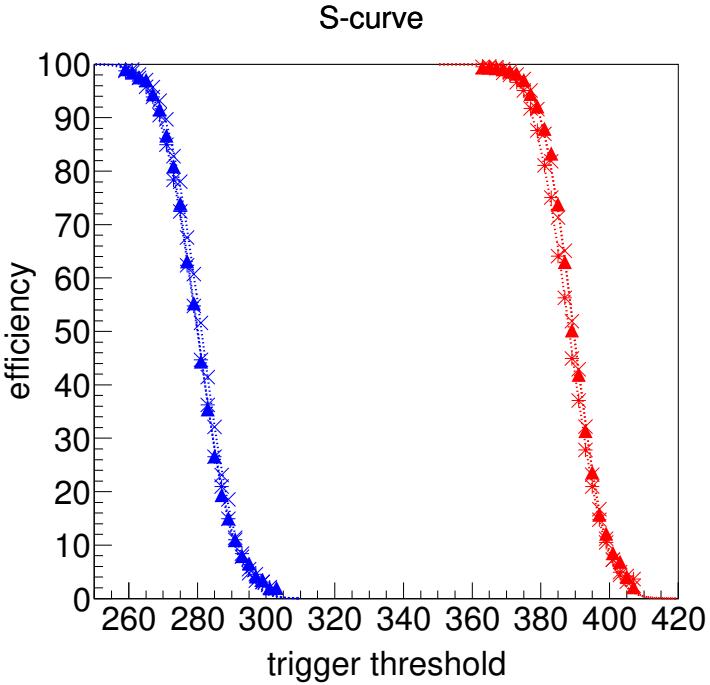


Figure 7. ThS curves with charge injection (1 MIP in blue and 2 MIPs in red) for two different channels in a SKIROC2 testboard. From this plot, we extract a $S/N = 12.8$ in the trigger line.

232 3.3 S/N ratio in the trigger line

233 Similar kind of measurements can be done but using external signals. This will allow to calculate
 234 the signal over noise (S/N) ratio to trigger 1 MIP signals. To calculate the S/N of the trigger we
 235 need to compare the 1 MIP ThS curve and 2 MIP ThS curve. The S/N will be defined as the ratio
 236 between the distance of both ThS curves at its 50% and the width of the ThS curve.

237 In Figure 7 we see the 1 MIP and 2 MIP ThS curves obtained for several channel in a SKIROC
 238 testboard in which a single SKIROC2 in BGA package is placed and the 1 MIP and 2 MIPs signals
 239 are directly injected in the preamplifier (via a 3 pF capacitor located in the injection line as shown
 240 in Figure 1). From this plot we can extract a S/N ratio of ~ 12.8 . We do not expect large differences
 241 with the results that we would obtain with a full equipped SLABs although this board is thought for
 242 commissioning and test of the SKIROC ASICs in an "ideal" environment in contrast with the FEV
 243 ASUS that are optimized to meet the detector requirement and to hold several ASICs at the same
 244 time.

245 We have obtained similar results using real signals, in this case cosmic rays signals by using
 246 very long acquisition windows of 150 ms at 5 Hz. This is shown in Figure 8 where we show the
 247 result of the fit to the noise ThS curves for all channels individually (in red) in one of the ASICs
 248 of the second layer together with the results of the ThS curve obtained with cosmic rays integrated
 249 for all channels (black points and blue line). We expect a broader distribution of the cosmic ThS
 250 curve since muons can traverse the detector at different incidence angles. In addition to this, we
 251 should remember that the noise ThS curve do correspond to the real noise distribution but only to
 252 the envelope of the noise in the fast shaper, therefore the distance between the two ThS curves is

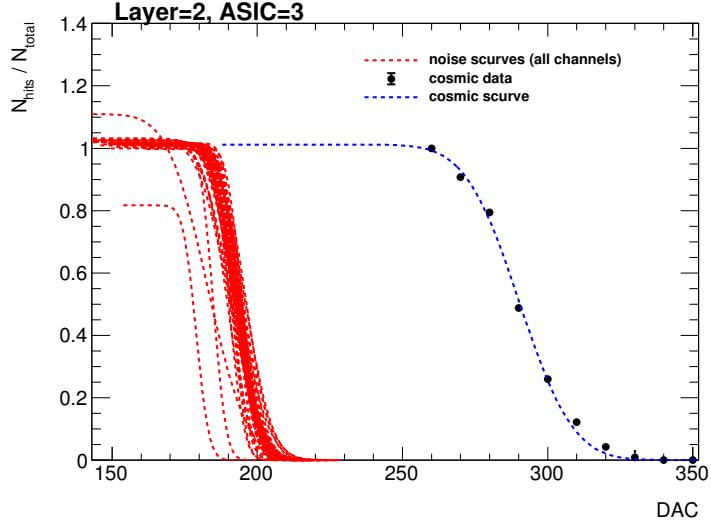


Figure 8. ThS curves for noise (channel by channel, only the result of the fit) and cosmic rays (all channels together) for one ASIC in layer 2.

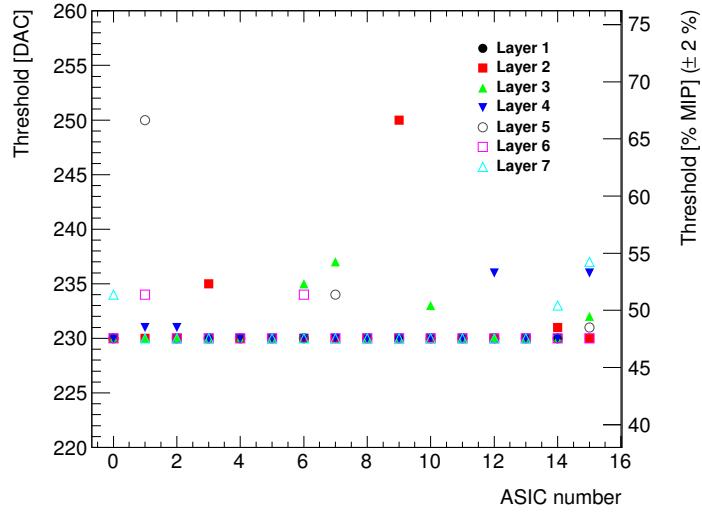


Figure 9. Summary of the trigger threshold settings in internal DAC units and in MIP units.

253 smaller than the real distance between noise and signal. Therefore, if we calculate the S/N using
 254 this plot, the value would be unrealistic but at least provides the comparison between the ThS curve
 255 for 1 MIP real and injected signals.

256 Both ways of estimating the S/N ratio of the trigger have their own limitations and dedicated
 257 studies in beam test are needed in order to precisely determine it. In the meanwhile, combining the
 258 information contained in the Figs 7 and 8, we can estimate the value in energy at which we have set
 259 our trigger threshold. This is shown in Figure 9.

260 **3.4 Prospects**

261 All the commissioning procedure described above relies in very conservative decisions due to
262 the presence of unknown noise sources during most of the commissioning phase. These sources
263 are now well known and isolated and therefore a new “noise commissioning procedure” has been
264 studied. It will consist in an iterative algorithm that first will identify and mask the channels giving
265 underflowed signals and afterwards run a set of acquisitions in which the number of triggers per
266 channel will be compared with the number of expected triggers assuming only cosmic rays as signal.
267 This will allow us to have an unambiguous definition of the noise levels channel per channel instead
268 of defining such levels relatively to the total number of recorded triggers per ASIC. Finally, once
269 that the noisy channels are identified, the optimization of the threshold levels will be performed and
270 a last run for identification of noisy channels will be taken using this optimal threshold.

271 Using this new procedure we manage to reduce the number of masked channels by a factor 2
272 without any loss of performance, at least in the laboratory and using 3 of the 7 SLABs. This new
273 procedure will be tested in the next beam test. Also, in order to optimize the commissioning of the
274 detector, we propose a new set of measurements in the next beam test such as a scan of optimal delay
275 of the hold values of the trigger using MIP like particles and a threshold scan for the determination
276 of the S/N in the trigger line. This later can be done by the comparison of ThS curves taken with 1
277 MIP and $\sqrt{2}$ MIP signals (tilting the detector by 45 degrees).

278 **4 Performance on positron beam test at DESY**

279 The beam test line at DESY provides continuous positron beams in the energy range of 1 to 6 GeV
280 with rates from few hundreds of Hz to few KHz with a maximum of \sim 3 KHz for 2-3 GeV. The
281 particles beam is produced as follows: first, the electron/positron synchrotron DORIS II is used to
282 produce a photon beam via bremsstrahlung when interacting with a carbon fiber target; secondly,
283 these photons are then converted to electron/positron pairs; and, finally, the beam energy is selected
284 with dipole magnets and collimators. In addition, DESY gives access to a bore 1 T solenoid, the
285 PCMag.

286 A photograph showing the SiW-ECAL technological prototype setup can be seen in Figure
287 10. Current prototype consists of 7 layers of SLABs housed by a PVC and aluminum structure
288 that can hold up to 10. For the beam test described in Section 4 all the layers were separated by
289 equal distances of 15 mm except the last one which was at 60 mm of its nearest. In the following
290 sections, we will refer to layers number 1 to 7, where the 1 is the closest to the beam pipe and 7 is
291 the farthest. The detector was exposed to a positron beam in the DESY test beam area (line 24). By
292 means of an external pulse generator we defined the length of the acquisition window to be 3.7 ms
293 at a frequency of 5 Hz. The detector was running in power pulsing mode without any extra active
294 cooling system.

295 The physics program of the beam test can be summarized in the following points:

- 296 1. Calibration without tungsten absorber using 3 GeV positrons acting as minimum ionizing
297 particle (MIPs) directed to 81 position equally distributed over the modules.
- 298 2. Test in magnetic field up to 1 T using the PCMag. For this test a special PVC structure was
299 designed and produced to support one single SLAB. The purpose of such test was twofold:

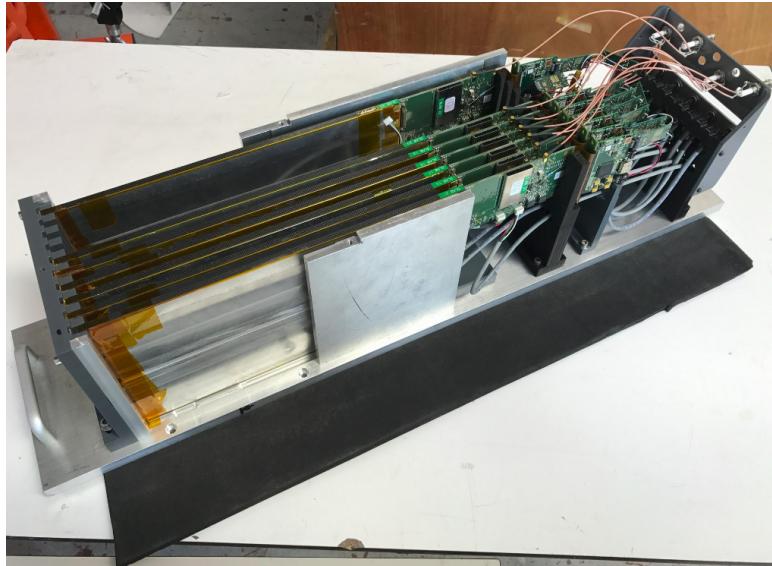


Figure 10. Prototype with 7 layers inside the aluminum stack.

first to prove that the DAQ, all electronic devices and the mechanical consistency of the SLAB itself are able to handle strong magnetic fields; second to check the quality of the data and the performance of the detector during the data taking when running in a magnetic field.

3. Response to electrons of different energies with fully equipped detector, i.e. sensitive parts and W absorber, with three different repartitions of the absorber material:

- W-configuration 1: 0.6, 1.2, 1.8, 2.4, 3.6, 4.8 and 6.6 X_0
- W-configuration 2: 1.2, 1.8, 2.4, 3.6, 4.8, 6.6 and 8.4 X_0
- W-configuration 3: 1.8, 2.4, 3.6, 4.8, 6.6, 8.4 and 10.2 X_0

First reports on this beam test can be find in Refs. [30, 31]. In this paper we discuss in more detail the results of the pedestal, noise and MIP calibration in Section 4.1. We show also results on the pedestal and noise stability when running inside a magnetic field in Section ???. Finally, a first peek to the response and stability of the detector in electromagnetic showers events is discussed in Section 4.3.

4.1 Response to MIP-acting positrons

4.1.1 Pedestal and noise determination

The calibration runs have been used to calculate the pedestal distribution reference values and the noise levels (the width of the pedestal distribution) of each channel. In Figure 11 we show the signal and pedestal distribution of a single channel after subtracting the pedestal mean position. The results of the MIP calibration fit are included (red) and explained in the next version. The pedestal distribution is shown only for the first SCAs to keep the y-axis within a reasonable range. The signal distribution is integrated over all SCAs.

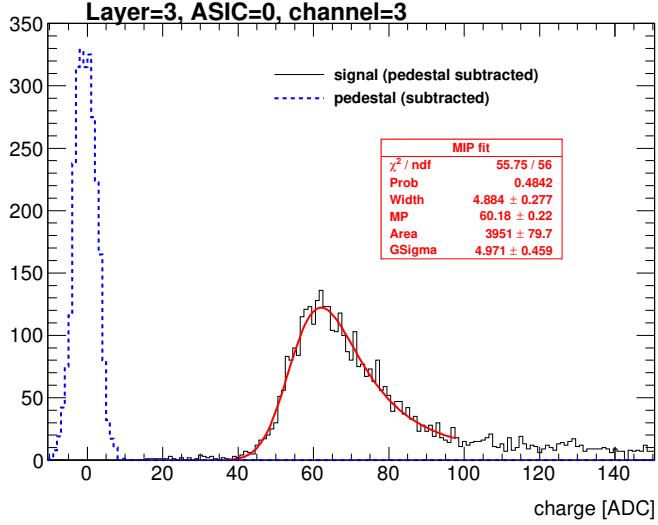


Figure 11. Pedestal (blue dashed line) and signal (black continuous line) distribution for one channel in the third layer.

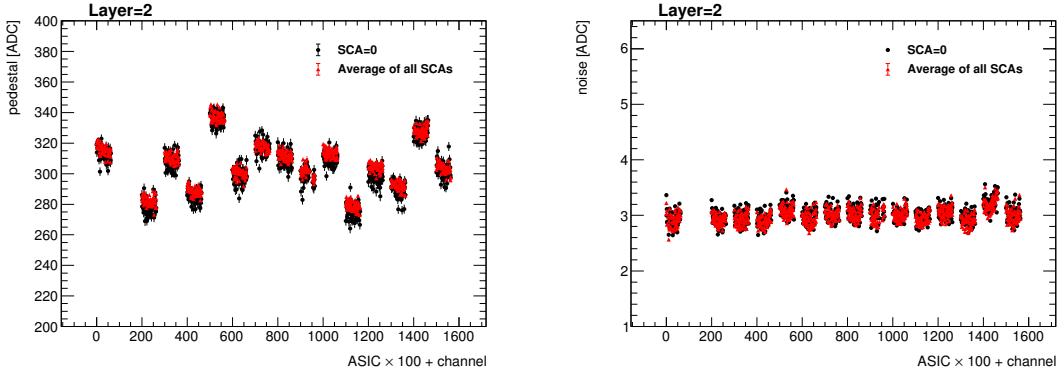


Figure 12. Pedestal mean position (upper plot) and width (lower plot) for all channels in one layer. The data is grouped on bunches in which the value in the x-axis corresponds to the value of the channel number plus the value of the ASIC number multiplied by 100. The black points show the value for the first SCA and the red points show the average value for all the others SCAs (with the standard deviation of the sample as error bar).

321 The pedestal is calculated as the mean position of the ADC distribution of channels without
 322 trigger. The noise is associated to the width of such distribution. The pedestal correction is done
 323 layer-, chip-, channel- and SCA-wisely due to the large spread of values between pedestals, as
 324 observed in Figure 12 (left plot) and Figure 13 (also left plot). For the noise, the dispersion is much
 325 smaller ($\sim 5\%$). This is shown in the right plots of Figures 12 and 13. From now on, the pedestal
 326 correction is applied to all the results presented.

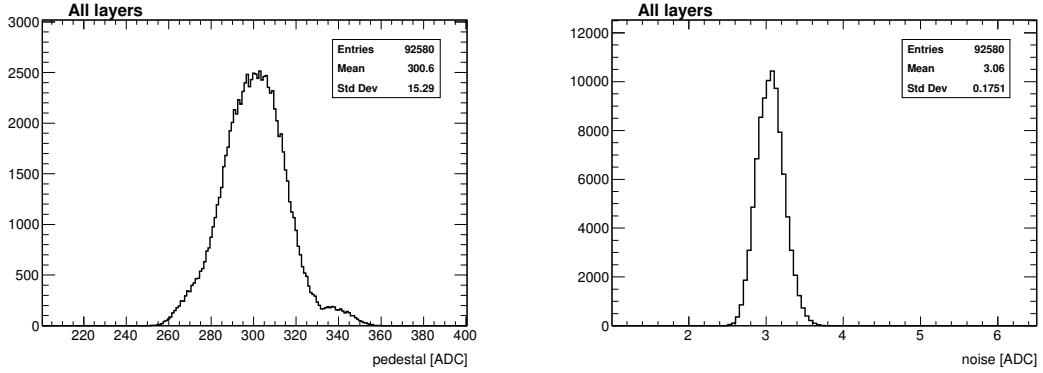


Figure 13. Pedestal mean position (left) and width (right) for all channels and all SCAs in the setup.

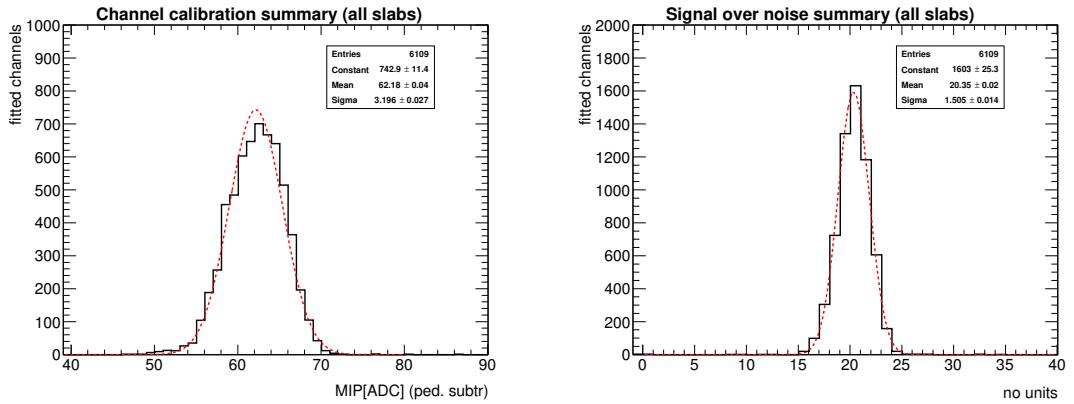


Figure 14. Result of the MIP position calculation and signal over noise calculation for all calibrated channels.

4.1.2 Energy calibration and tracking efficiency

A Landau function convoluted with a Gaussian is fit to the resulting hit distribution. The most-probable-value of the convoluted function is taken as the MIP value, allowing thus for a direct conversion from ADC units to energy in MIP units. We have obtained a raw energy calibration spread of the 5% among all channels with the 98% of all available channels being fitted. Results are summarized in figure 14, leftmost plot.

We checked the MIP calibration in all calibrated channels by selecting tracks incident perpendicular to the layers surface. The results are shown in figure 15 where the single channel energy distribution for MIPs is shown for all calibrated channels in the same distribution. The maximum peaks at 1 MIP as expected after a good calibration. In addition to this, a second and a third peak appear visible. These peaks are due to events involving multiple particles crossing the detector.

To evaluate the single hit detection efficiency we define a high purity sample of events by selecting tracks with at least 4 layers with a hit in exactly the same channel. Afterwards we check if the other layers have or not a hit in the same channel (expanding the search to the closest neighbouring channels) with energy larger or equal than 0.3 MIP. Finally, we repeat this for all layers and channels. The results are shown in Figure 16. Except few exceptions, the efficiency is compatible with 100%. Lower efficiencies in the first layer are related to the presence of noisy

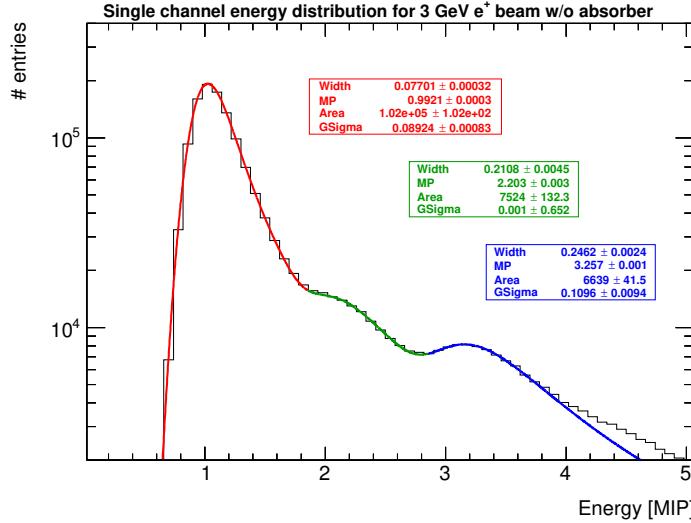


Figure 15. Energy distribution for all calibrated channels when selecting tracks of 3 GeV positron acting as MIPs.

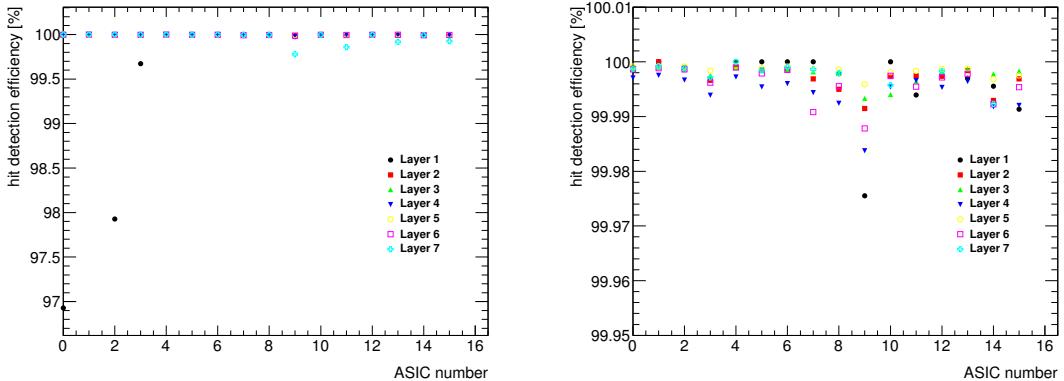


Figure 16. Left: MIP detection efficiency for all layers and ASICs in high purity samples of tracks of MIP-like acting particles. Right: same figures with a zoom in the y-axis. In both cases, the average efficiency of the 64 channels in each ASIC is shown.

344 channels not spotted during the commissioning. In the last layer (separated from the other layers
 345 by four slots of 1.5 cm instead of only one) we also observe few small deviations from the ~ 100%
 346 which are indeed associated to a slight misalignment of the detector. If we remove these channels
 347 from the analysis the full efficiency is recovered.

348 4.1.3 S/N ratio in the charge measurement for MIP interactions

349 The signal-over-noise ratio in the charge measurement (corresponding to the slow shaper of the
 350 SKIROC2) is defined as the ratio between the most-probable-value of the Landau-gauss function
 351 fit to the data (pedestal subtracted) and the noise (the pedestal width). This quantity has been
 352 calculated for all channels and all layers. The average S/N is to 20.4. Results are summarized in

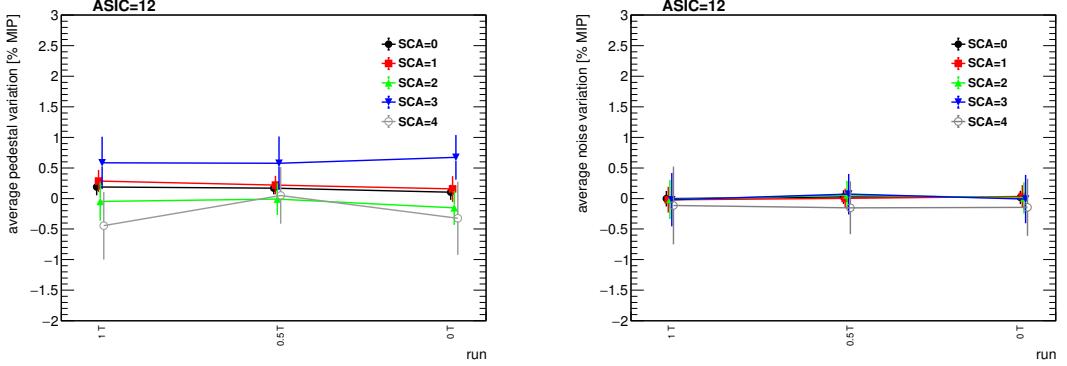


Figure 17. Average deviation of the pedestal mean position (left) and width (right) for all channels in the ASIC 12.

353 Figure 14, rightmost plot.

354 4.2 Pedestal and noise stability in a magnetic field

355 The data taking inside the magnetic field has been divided in three steps: a) a with a magnetic field
 356 of 1 T; b) a run with 0.5 T; c) a final run with the magnet off. The beam, 3 GeV positrons, was
 357 hitting in the area of the PCB readout by the ASIC number 12.

358 The pedestal positions and noise levels of the channels of the ASIC 12 when the SLAB
 359 is inside of the PCMag are compared with the results from the calibration run described in the
 360 previous section. This is shown in Figure 17. We see that the agreement is perfect within the
 361 statistical uncertainties. Due to the lower rates in this beam area, the analysis is only done up to few
 362 SCAs.

363 4.3 Pedestal stability in electromagnetic shower events

364 In this section we discuss the pedestal stability in events with large amount of charge collected by the
 365 ASICs, as are the electromagnetic shower events. All the results shown in this section correspond
 366 to data taken during the tungsten program, using the W-configuration number 2 when shooting the
 367 beam in the area registered by the ASIC 12 (and partially in the 13). Only information recorded
 368 by ASIC 12 is used in the analysis. For other configurations we get comparable results. In order
 369 to select a high purity of electromagnetic shower like the events, we used a simple criteria: select
 370 only events with at least 6 of the layers with at least a hit with $E > 0.5$ MIP.

371 Two main observations have been extracted from the recalculation of the pedestals and its
 372 comparison with the values obtained previously during the calibration runs. The first observation
 373 consists in a relatively small drift of the pedestal values towards lower values when the collected
 374 energy is high (or when the number of triggered channels is large). This is shown in Figure 18 for
 375 several SCAs where the average of the projection of the pedestal distribution for all channels non
 376 triggered in ASIC 12 of layer 3 is plot as a function of the total energy measured by the ASIC (or
 377 the total number of hits). We see that in both cases, the shapes of the curves for each SCA are very
 378 similar. This feature is known and it is due to the architecture of the SKIROC2 ASICs where high
 379 inrush of currents can slightly shift the baseline of the analogue power supply.

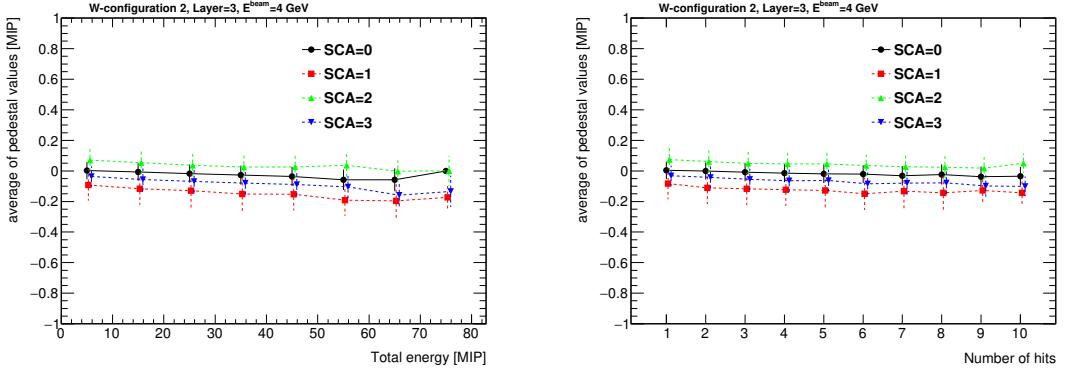


Figure 18. Left: mean position of the projection of the pedestal distribution of all channels calculated when different energies are collected in the ASIC (in bins of 10 MIPs). Right: same but as a function of the number of hits. In both cases, the results are shown for few SCA. The points for the curves with SCA larger than zero are slightly shifted in the x-axis to optimize the visualization.

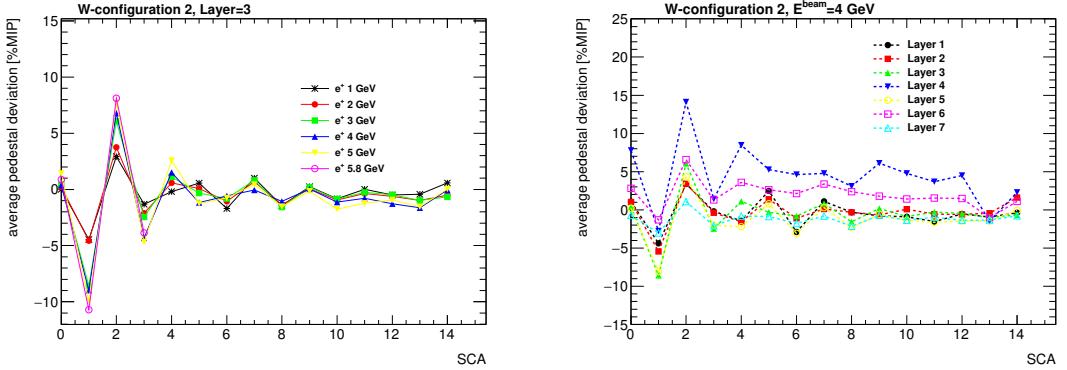


Figure 19. Left: average value on each SCA of the calculated pedestals for all channels of ASIC 12 in the Layer 3 for different energies of the beam. Right: same but fixing the energy of the beam and comparing several layers.

The second observation extracted from this analysis can be also seen in Figure 18 but more clearly in Figure 19: in addition to the small drift of the pedestal value an SCA-alternate global shift is observed. We see that the effect is enhanced when large amounts of charge are deposited in the ASIC (*i.e.* at larger beam energies or for the layers in the maximum of the shower profile). We also observed that this alternation is only SCA dependent and does not depends on the time in which the deposit of energy occurs within the acquisition. This is not yet fully understood although the fact that the effect is observed in alternate SCAs hints that something is affecting to the digital part of the ASIC (where the SCAs enter in play). Dedicated tests in the laboratory and in the beam are needed in order to clarify this issue.

389 5 Summary

The R&D program of the highly granular SiW-ECAL detector is in an exciting phase. After the proof of principle of the imaging calorimetry concept using the physics prototype, the technological

392 prototype is being constructed and tested. In this document we describe the commissioning and
393 beam test performance of a prototype built in with the first fully assembled detector elements.

394 A very comprehensive and detailed commissioning procedure has been established and optimized
395 allowing us to identify and isolate the different noise sources that could spoil the data taking.
396 The beam test has provided a lot of useful data to study the performance of the detector and to
397 perform a channel by channel calibration. A full analysis of the MIP calibration within magnetic
398 field and the response of the prototype in electromagnetic shower events will be covered in a future
399 document. In addition, the results shown here serve as input for ongoing and future R&D.

400 6 Outlook

401 In parallel to the work described here, several R&D efforts are being carried. One of these efforts
402 is directed to the design and test of new ASICs. In fact, a new generation of SKIROC2, the 2a,
403 has been delivered and it is being tested in the dedicated testboards and it has been integrated in
404 new ASUs. In addition, a new generation of the ASIC, SKIROC3, is foreseen for the final detector
405 construction. In contrast with SKIROC2/2a, the new ASIC will be fully optimized for ILC operation,
406 *i.e.* full zero suppression, reduced power consumption etc.

407 Many efforts are also concentrated in the construction and test of long SLABs made of several
408 ASUs enchain since we know that the ILD ECAL will host long layers of up to $\sim 2.5\text{m}$. This
409 device constitutes a technological challenge in both aspects, the mechanical (very thin and long
410 structure with fragile sensors in the bottom, complicated assembly procedure...) and the electrical
411 (*i.e.* transmission of signals and high currents). For example, interconnections between ASUs and
412 between ASU and interface card are one of the most involved parts of the assembly and require
413 close collaboration between mechanical and electronic engineers. The construction and test of a
414 long SLAB prototype of ~ 8 ASUs is currently ongoing.

415 In parallel to the ASUs equipped with BGA packaged ASICs, a different proposal for the ASU
416 design is being investigated. This is motivated by the high density of channels demanded by the
417 Particle Flow algorithms. Indeed, the FEV11 thickness is 1.6 alone and 2.7 mm including the ASICs
418 in its current packaging: 1.1 mm thick LFBGA package. In this alternative PCB design the ASICs
419 are directly placed on board of the PCB in dedicated cavities. The ASICs will be in semiconductor
420 packaging and wire bonded to the PCB. This is the so-called COB (chip-on-board) version of
421 the ASU. A small sample of FEV11_COBs (same connexion pattern with the interface card than
422 FEV11) with a total thickness of 1.2 mm allowing for a potential density of 10000 channels/dm³
423 has been produced and tested in the laboratory showing its readiness for tests with particle beams.
424 A sample can be seen in Figure 20.

425 Finally, many efforts in the compactification of the DAQ and the ASUs (*i.e.* the chip on board
426 versions of the ASUs described in Section 2.3) are being conducted by the SiW-ECAL collaboration.

427 It is foreseen that all these developments, with the exception of the SKIROC3, will be tested
428 with particle beams during 2018-2019.

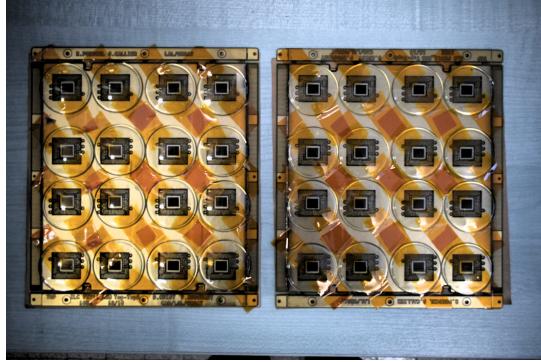


Figure 20. Two FEV11_COB boards with 16 SKIROC2a wire bonded. The ASICs are protected with watch glasses.

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 437 The measurements leading to these results have been performed at the Test Beam Facility at DESY
 438 Hamburg (Germany), a member of the Helmholtz Association (HGF).

439 A Appendix: Filtering of fake triggers

440 Several types of fake signals have been observed in the technological prototype since its construction
 441 and test. A detailed description of them can be found in previous articles, as for example, in Ref.
 442 [27]. All these fake signals are easily identified and tagged during the data acquisition and removed
 443 afterwards from the analysis not introducing any significance loss of performance as can be seen,
 444 for example, in the hit detection efficiency plots (see Section 4.1.2). In the following, we briefly
 445 describe the status of the monitoring, debugging and filtering of such kind of events.

446 Empty triggers

447 Empty trigger events are a well known feature of SKIROC2. The SKIROC2 uses an OR64 signal
 448 to mark the change to a new SCA when a signal over threshold is detected. The empty triggers
 449 appear when during the acquisition the rising edge of the slow clock falls during the OR64 signal
 450 and therefore the change to a new SCA is validated twice. This effect creates around 10-15% of
 451 empty events which are easily filter and removed from the analysis. **The ratio of empty triggers in**
 452 **the new SKIROC2a is reduced to the ~ 3% thanks to to a decrease of the OR64 size by a factor X.**

453 **Plane events and retriggers**

454 Another well known issue is the appearance of bunches of consecutive fake triggers, called retriggers,
455 that saturates the DAQ. These events are also characterized by triggering many channels (some times
456 even all channels of an ASIC) at the same time. Although the ultimate reason of the appearance of
457 these events remains unknown we think that they may be related to some distortion of the power
458 supply baselines. We know that the SKIROC2 and 2a preamplifiers are referenced to the analog
459 power supply level, therefore, any voltage dip can be seen as signal by the preamplifiers. The
460 presence of a high inrush of current due to many channels triggered at the same time can create
461 these voltage dips and produce the so called plane events (most of the channels triggered at once).
462 In previous studies (*i.e.* reference [27]), the ratio of retriggers and plane events was reduced by
463 improving the power supply stabilization capacitances. It is important to remark that all layers and
464 all ASICs analog and digital levels are powered using the same power supply. Moreover, the high
465 voltage power supply for the polarization of the PIN diode it is also common for all layers. Therefore
466 any noise in these power supplies or any overload of an ASIC may participate in the creation of fake
467 signals in different ASICs and layers.

468 Studying the MIP calibration data of this beam test we have noticed that the larger concentration
469 of the retriggers and plane events are originated in ASICs far from the beam spot. Even more, hot
470 spots tend to appear near the channels 37 and the channels masked as suspicious of suffering from
471 routing issues. The amount these events have been estimated to be of 1 – 3% in the ASICs where
472 high frequency interactions are produced (*i.e.* using 3 GeV positrons at 2-3 KHz) and at higher
473 rates even larger than 40% in other ASICs far from the beam spot. Moreover, it has been noticed a
474 correlation between the time that an ASIC was full and the time of the appearance of some retriggers
475 in other areas of the PCB. This correlation corresponds to $\sim 1.6 \mu\text{s}$ which hints of a distortion on
476 the analogue power supply when the signal that informs the DIF that one ASIC memory is full is
477 transmitted through the PCB.

478 All this information and dedicated studies in the laboratory will be used for the improvement
479 of the power supplying system, the PCB design and for further SKIROC developments with the
480 possible approval the ILC in the scope.

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