

² **Commissioning of the highly granular SiW-ECAL 3 technological prototype**

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⁵ **ABSTRACT:** High precision physics at future colliders as the International Linear Collider (ILC)
⁶ require unprecedented high precision in the determination of the final state of the particles produced
⁷ in the collisions. The needed precision will be achieved thanks to the Particle Flow algorithms (PF)
⁸ which require compact, highly granular and hermetic calorimeters systems. The Silicon-Tungsten
⁹ Electromagnetic Calorimeter (SiW-ECAL) technological prototype design and R&D is tailored to
¹⁰ the baseline design of the ECAL of the International Large Detector (ILD) for the ILC. In this
¹¹ document we present and discuss the commissioning of the prototype and the performance of the
¹² device in a beam test carried at DESY in June 2017.

¹³ **KEYWORDS:** Calorimeter methods, calorimeters, Si and pad detectors

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37 **1** **Introduction**

38 Future accelerator based particle physics experiments require very precise and detailed reconstruc-
39 tion of the final states produced in the beam collisions. A particular example is the next generation
40 of e^+e^- linear colliders such the ILC[1–5]. This project will provide collisions of polarized beams
41 with centre-of-mass energies (*c.m.e*) of 250 GeV - 1 TeV. These collisions will be studied by two
42 multipurpose detectors: the International Large Detector (ILD) and the Silicon Detector (SiD)[5].
43 To meet the precision levels required by the ILC physics goals, new techniques relying on single
44 particle separation to make possible the choice of the best information available in the full detector

45 to measure the energy of the final state objects have been developed. These techniques are called
46 Particle Flow (PF) techniques [6–8] and allow to reduce the impact of the poor resolution of the
47 calorimeter systems (compared with trackers) in the overall reconstruction. The PF algorithms
48 impose some special requirements in the design of the detectors. For example, it requires highly
49 granular, compact and hermetic calorimeters.

50 The CALICE collaboration is driving most of the efforts on R&D of highly granular calorime-
51 ters [8] for future linear colliders by investigating and building prototypes for several calorimeter
52 concepts. One of these calorimeters is the silicon-tungsten electromagnetic calorimeter, SiW-
53 ECAL. The SiW-ECAL is the baseline choice for the ILD electromagnetic calorimeter. It consists
54 in a detector (in the barrel region) of $24 X_0$ of thickness which corresponds to $\sim 1 \lambda_I$ (interac-
55 tion length). It has silicon (Si) as active material and tungsten (W) as absorber material. The
56 combination of Si and W choices makes possible the design and construction of a very compact
57 calorimeter with highly granular and compact active layers. It will be built an alveolar structure of
58 carbon fiber into which modules made of tungsten plates and the active sensors will be inserted.
59 The very-front-end (VFE) electronics will be embedded in the detector units. The silicon sensors
60 will be segmented in squared cells (or channels) of $5 \times 5 \text{ mm}$: a total of ~ 100 million channels will
61 constitute the ECAL for ILD. The desired signal dynamic range in each channel goes from 0.5 MIP
62 to 3000 MIPs. To reduce overall power consumption, the SiW-ECAL will exploit the special bunch
63 structure foreseen for the ILC: the e^+e^- bunches trains will arrive within acquisition windows of \sim
64 1-2 ms width separated by ~ 200 ms. During the idle time, the bias currents of the electronics will
65 be shut down. This technique is usually denominated power pulsing. In addition to this, to cope
66 with the large amount of channels, the calorimeters should work in self-trigger mode (each channel
67 featuring an internal trigger decision chain) and zero suppression mode.

68 2 The SiW-ECAL technological prototype

69 The first SiW-ECAL prototype was the so called SiW-ECAL physics prototype. It was success-
70 fully tested at DESY, FNAL and CERN running in front of another prototype from the CALICE
71 collaboration, the analogue hadronic calorimeter AHCAL, delivering the proof of concept of the
72 technology and the PF calorimetry. For the physics prototype, the VFE was placed outside the
73 active area with no particular constraints in power consumption. It consisted of 30 layers of Si as
74 active material alternated with tungsten plates as absorber material. The active layers were made of
75 a matrix of 3×3 Si wafers of $500 \mu\text{m}$ thickness. Each of these wafers was segmented in matrices of
76 6×6 squared channels of $1 \times 1 \text{ cm}^2$, allowing for a potential density of 1500 channels/ dm^3 assuming
77 the ILD baseline design constraints on the material repartition and compactness. The prototype
78 was divided in 3 modules of 10 layers with different W depth per layer in each of these modules
79 ($0.4, 1.6$ and $2.4 X_0$) making a total of $24 X_0$. That very first prototype offered a signal over noise
80 on the measured charge of 7.5 for MIP like particles. More results proving the good performance
81 of the technology and the PF can be found in references [9–14].

82 The new generation prototype is called the SiW-ECAL technological prototype. It addresses
83 the main technological challenges: compactness, power consumption reduction through power
84 pulsing and VFE inside the detector close to real ILD conditions. It will also provide data to deeply
85 study the PF and provide input to tune simulation programs as for example GEANT4[15–17] which

86 is widely used in particle physics to simulate the passage of particles through matter. In this section
87 we described in detail the main features and characteristics of the technological prototype.

88 **2.1 Silicon sensors**

89 The sensors consist on floating zone silicon wafers $320\mu\text{m}$ thick with high resistivity (bigger than
90 $5000\Omega\cdot\text{cm}$). The size of the wafer is $9\times 9\text{ cm}^2$ and it is subdivided in an array of 256 PIN diodes
91 of $5\times 5\text{ mm}^2$. A MIP traversing the PIN parallel to its normal will create $\sim 80 h^+e^-$ pairs per μm
92 which corresponds to 4.1 fC for particles incident perpendicularly to its surface.

93 The original design of the silicon wafers included an edge termination made of floating guard-
94 rings. It was observed in beam tests [18, 19] that the capacitive coupling between such floating
95 guard-rings and the channels at the edge was not negligible in tests with high energy beams (pions
96 and electrons with energies larger than 20-40 GeV). This coupling lead to fake events in which,
97 at least, the channels in the four edges of the wafer are triggered at the same time. This is why
98 these events are called squared events. An R&D program together with Hamamatsu Photonics
99 (HPK Japan) was conducted to study the guard-rings design as well as the internal crosstalk. It
100 was concluded that using wafers without guard rings and with a width of the peripheral areas lower
101 than $500\mu\text{m}$ thanks to the use of stealth dicing technique, the amount of these squared events can
102 be reduced to be almost negligible. This need to be confirmed in beam test. Unfortunately, for the
103 interaction with low energy particles as the delivered at the DESY beam test facility (see Section 4)
104 the amount of squared events is expected to be negligible, therefore we will not discuss this issue
105 in the following.

106 **2.2 SKIROC: Silicon pin Kalorimeter Integrated ReadOut Chip**

107 The SKIROC[20] (Silicon pin Kalorimeter Integrated ReadOut Chip) is a very front end ASIC
108 (application-specific integrated circuits) designed for the readout of the Silicon PIN diodes. In its
109 version SKIROC2 it consists of 64 channels in AMS $0.35\mu\text{m}$ SiGe technology. Each channel
110 comprises a low noise charge preamplifier of variable gain followed by two branches: a fast shaper
111 for the trigger decision and a set of dual gain slow shaper for charge measurement. The gain can
112 be controlled by modifying the feedback capacitance during the configuration of the detector. With
113 the slowest gain, 6pF , the ASIC will handle a linear dynamic range from 0.1 to up to 1500 MIPs
114 (a slightly less than the desired final value for the ILC). Finally, a Wilkinson type analogue to
115 digital converter fabricates the digitized charge deposition that can be readout. Once one channel is
116 triggered, the ASIC reads out all 64 channels adding a bit of information to tag them as triggered or
117 not triggered and the information is stored in 15 cell deep physical switched capacitor array (SCA).

118 The SKIROC ASICs can be power-pulsed by taking advantage of the ILC spill structure: the
119 bias currents of the ASIC can be switched off during the idle time between bunch trains. With this
120 method, the ASIC is able to reduce its power consumption down to $25\mu\text{W}$ per channel, meeting
121 the ILC requirements. All the results shown in this paper are obtained in power pulsing mode. This
122 feature is used for all data discussed in this paper and for first time in long periods of data taking in
123 beam test.

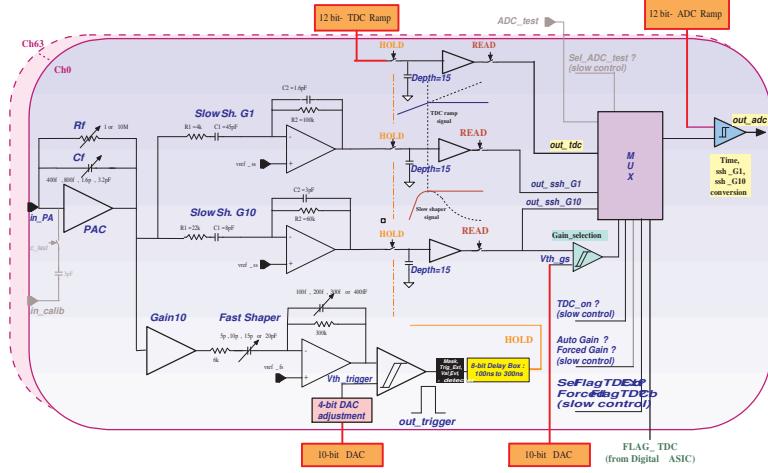


Figure 1. The schematics of the analog part of SKIROC2. High-stack picture (right bottom corner)

2.3 Active Sensor Units

The entity of sensors, thin PCB (printed circuit boards) and ASICs is called Active Signal Units or ASU. An individual ASU has a lateral dimension of $18 \times 18 \text{ cm}^2$. The ASUs are currently equipped further with 16 SKIROC2 ASICs for the read out and features 1024 square pads (64 per ASIC) of $5 \times 5 \text{ mm}$. The channels and ASICs are distributed along the ASU as shown in Figure 2. Each ASU is equipped with 4 silicon wafers as the described in Section 2.1. The high voltage is delivered to the wafers using a HV-kapton sheet that covers the full extension of the wafers.

2.4 Data AcQuisition system

The subsequent chain of the data acquisition (DAQ)[21] system is inspired by the ILC. It consists on three modules. The first module is the so called detector interface (DIF) which is placed at the beginning of each layer holding up to 15 ASUs; All DIFs are connected by single HDMI cables to the concentrator cards that make the second module: the Gigabit Concentrator Cards (GDCCs). This cards are used to control up to 7 DIFs collecting all data from them and distributing among them the system clock and fast commands. The last module, the most downstream, is the clock and control card (CCC) which provides a clock, control fan-out of up to 8 GDCCs and accepts and distributes external signals (i.e. signals generated external pulse generator to simulate the ILC spill conditions). The whole system is controlled by the Calicoes and the Pyrame DAQ software version 3 [22, 23].

2.5 Readout layers and SLABs

The readout layers of the SiW-ECAL consist of a chain of ASUs and an adapter board to a data acquisition system (DAQ) at the beginning of the layer. This adapter board is called SMBv4 and it also serves as to hold other services as power connectors or the super capacitances used for the power pulsing. These capacitances of 400mF with $16\text{ m}\Omega$ of equivalent serial resistance. The purpose of these capacitances is to provide local storage of the necessary charge to avoid the transport of current pulses over long cables, ensuring in this way the stability of the ASICs during the acquisition.

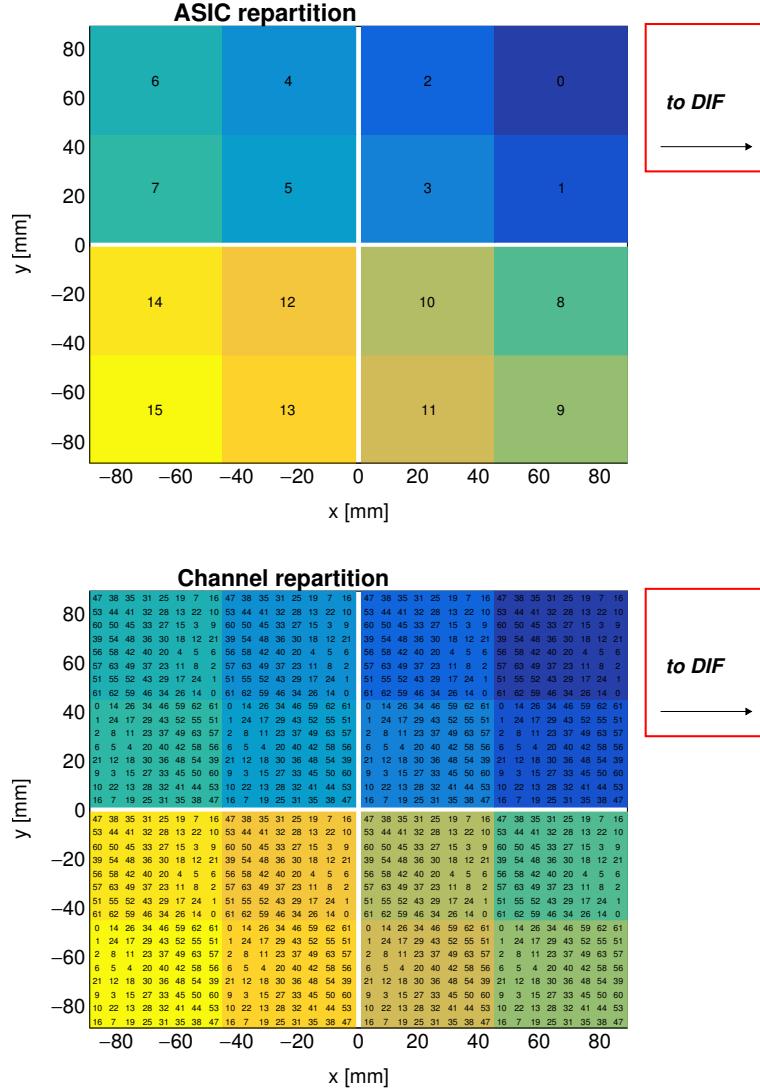


Figure 2. Repartition of the ASIC (up) and channels (down) in one ASU. In this perspective, the Si-Sensors are glued in the back. The channels are separated (in x and y) by 5.5 mm. The empty cross in the middle of the ASU corresponds to the 1 mm separation between the sensors. The areas covered by the different ASICs and channels are labeled with numbers following design and DAQ criteria: from 0-16 in the case of the ASICs and from 0-63 in the case of the channels.

149 The readout layers are embedded on a "U" shape carbon structure to protect the wafers. The
 150 full system is then covered by two aluminum plates to provide electromagnetic shielding and
 151 mechanical stability. This ensemble is denominated SLAB ("short" for 1 ASU ensembles or "long"
 152 for several ASUs enchainable) and it can be seen in Figure 3. The PCB thickness is 1.6 alone and
 153 2.7 mm including the ASICs in its current packaging: 1.1 mm thick LFBGA package. With these
 154 characteristics, a potential density of 3160 channels/dm³ is achievable for the baseline design of
 155 the ILD. This number should be compared with the density achieved in beam tests with the physics
 156 prototype: 1500 channels/dm³. With the first versions of the technological prototype we reached



Figure 3. Open single SLAB with FEV11 ASU, 16 SKIROC 2 and the interface card visibles.

similar potential density level was reached but equipping only a quarter of the ASUs surface [24].
 The SiW-ECAL detector designed for the ILD requires of the order of 10^5 highly integrated detection like the ones described in this text. For the production of the small sample of SLABs studied in this document, a scalable working procedure has been established among several groups [25] profiting from the funding of projects like AIDA2020 or the HIGTEC emblematic project of the P2IO. A schematic view of this assembly procedure chain can be seen in Figure 4. For more details we refer to Ref.[25].

3 Commissioning

This beam test was prepared by a careful and comprehensive commissioning comprising the debug of the short SLABs with special emphasis in the control of the noise and the study of the prototype performance in cosmic rays tests.

Earlier experiences with the SKIROC2 ASIC are reported in Refs. [24, 26]). Internal SKIROC2 parameters found in these references are adopted in the following except if the opposite is stated. For example, the gain value of 1.2pF for the preamplifier is used. With this gain, the SKIROC2 ensures a linearity better than 90% for 0.5-200 MIPs, which is enough for electromagnetic showers created by few GeV electrons or positrons.

3.1 Optimization of noise levels

Studying and control the noise levels is crucial since noisy channels may saturate the DAQ faster than physical signals. Two different types of noise sources were identified: a set of noisy channels randomly distributed in time and noise bursts affecting to all layers at the same time. The outcome of this commissioning is summarized in Figure 5.

The first type of noise source, noise events randomly distributed in time, forced us to define a list of channels to be masked in all layers. Again, two different type of noisy channels have been identified. The first group is composed by randomly distributed in space channels. The second group

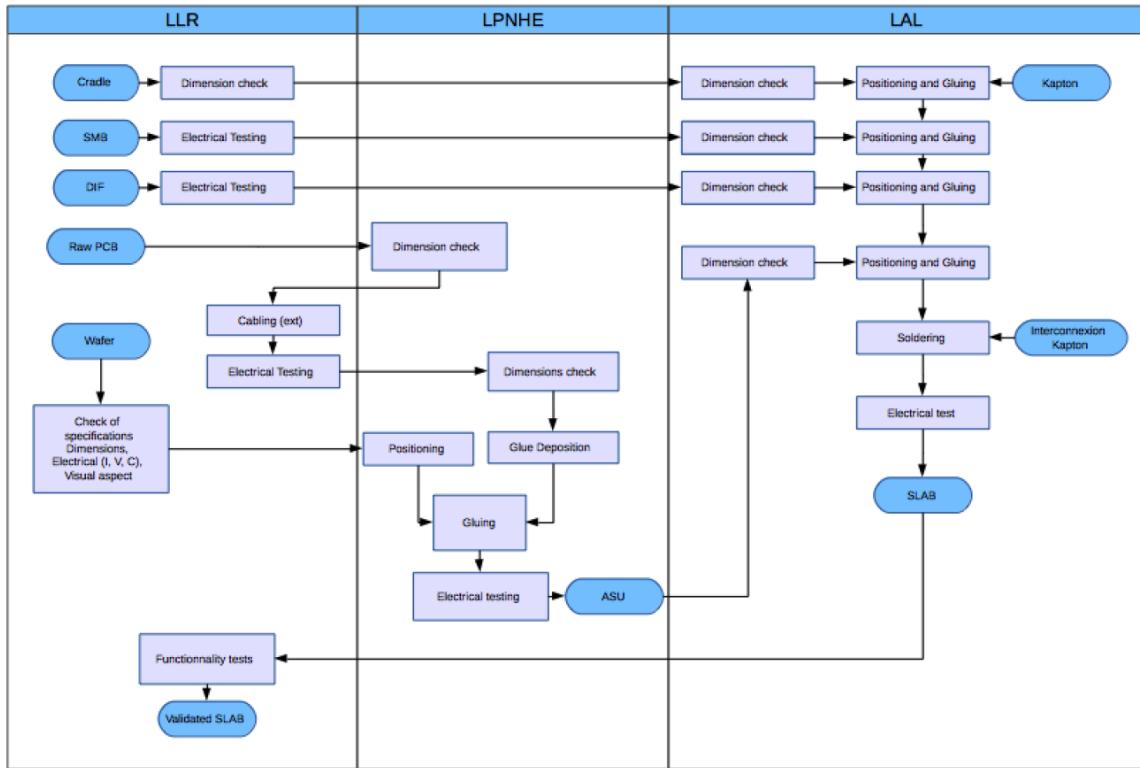


Figure 4. Process flow for the assembly of the SiW-ECAL SLABs.

is made of a fixed list of channels, all in the same positions for all SLABs, and all associated to a higher rate of events with underflowed value of the read ADC. A large amount of these channels are located in areas of the PCB where the density of lines (data and power transmission) is higher than in others. This hints for an issue on the routing of the PCB. Therefore, these channels are tagged in Figure 5 with the "routing issues" label although more tests and deeper inspections of the PCB layout are needed to clarify this issue.

The list of the noisy channels randomly distributed in time and space was defined by means of dedicated data taking runs. These runs were characterized by: their short acquisition windows (open to data recording for only 1.1 ms) at low repetition frequencies (5 Hz) to minimize the chances of having real events due to cosmic rays hitting the detector during the data taking; and the relatively high trigger threshold values between 250 and 400 DAC (which are equivalent to \sim 0.5-2 MIP, see Section 3.2 for more information). The full process was an iterative process starting with several repetitions of runs at a high threshold value and then some iterations at lower threshold but always higher than 0.5 MIP. In each of the iterations, the channels identified as noisy were masked. A full run involved 3-5 threshold values and at least two repetitions per value. Again, we decided to follow a conservative approach for list the noisy channels to be masked: if the channel was triggered at rates larger than 0.5-1% of the total number of triggers per ASIC it was added to the list. These channels are labeled as "other" in the first plot in Figure 5.

In addition to the different noisy channel types described above, we also have masked full sectors of the SLABs if an ASIC was faulty (at least 70% of channels listed as noisy) or if a Si-wafer

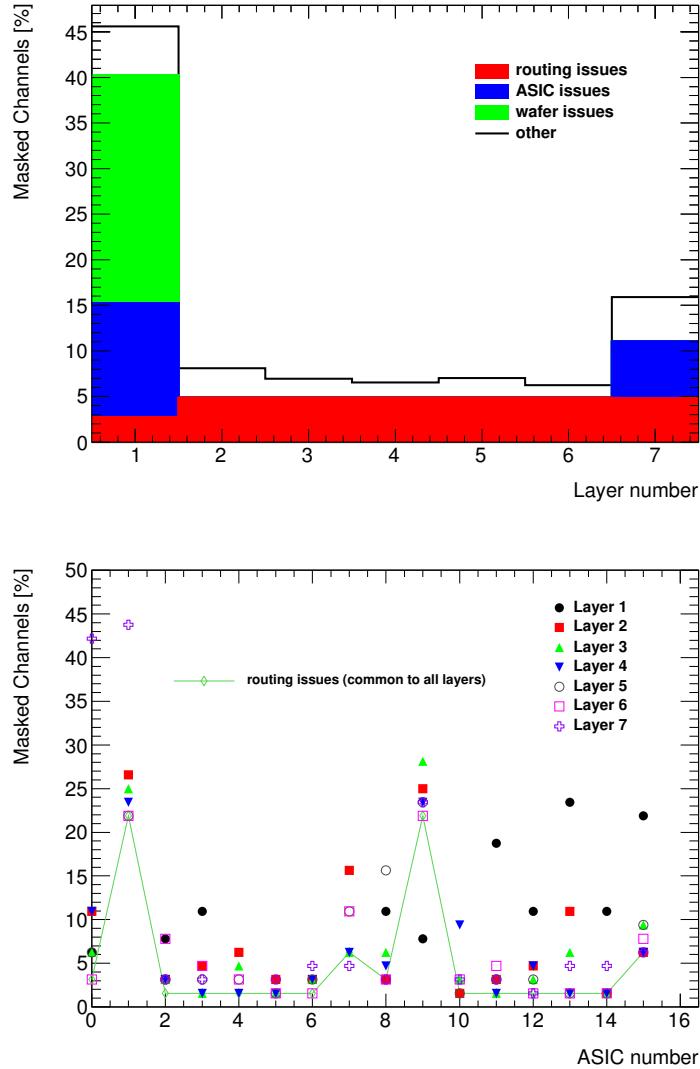


Figure 5. Ratio of channels that are marked as noisy in all slabs. Top: inventory of the different type of noisy channels per slab. Bottom: break down of the total number of noisy channels per ASIC. The ASICs 4-7 (wafer issue) and 10 from layer 1 and the ASIC 4 from layer 7 are not included in the second plot since they are fully masked.

201 was misworking (high leakage currents). In these cases and in all mentioned above, the masking
 202 involved two steps: disabling of the trigger and the disabling of the power of the preamplifier of
 203 that channel.

204 The other source of noise mentioned at the beginning of this section consist on noise bursts
 205 happening coherently at the same time in all SLABS and it was correlated to occasions when the
 206 electrical isolation between SLABS was broken. This is a hint of a system effect as can be the
 207 appearance of grounding loops or disturbances in the power supplies. The issue was circumvented
 208 by improving the electrical isolation of single layers. We have also observed that the noise bursts
 209 happens only at the end of long acquisitions. Therefore, in addition to the improved isolation, we

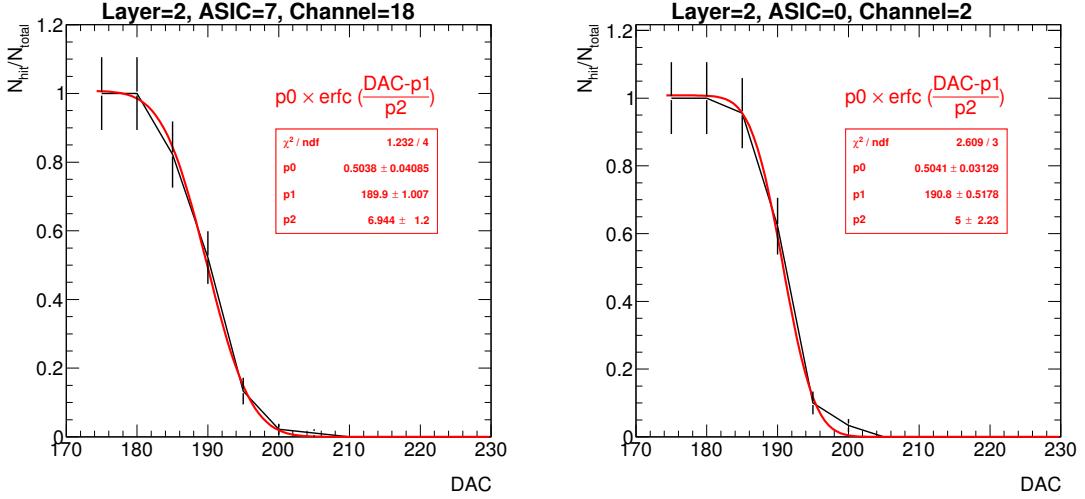


Figure 6. Two threshold scan curves and their associated ThS curves.

selected short enough acquisitions windows (which indeed are the most appropriate to the high rates of particles in the DESY beam). Dedicated studies in the laboratory are currently ongoing in order to fully understand this issue.

The list of channels mentioned above is discarded from the data taking from now on.

3.2 Threshold determination

In order to select the optimal trigger threshold values for the detector operation we perform dedicated scans of trigger threshold values with all channels enabled (excepted the marked as noisy). The threshold values are given in internal DAC units which are translated to meaningful physical quantities in Section 3.3. The threshold scan curves made of the total number of hits normalized to 1 vs the threshold for each channel are modeled by a complementary error function called ThS curves from now on:

$$ThS(DAC) = p_0 \times erfc\left(\frac{DAC - p_1}{p_2}\right) = \frac{2p_0}{\sqrt{\pi}} \int_{\frac{DAC-p_1}{p_2}}^{\infty} e^{-t^2} dt, \quad (3.1)$$

where p_0 is 1/2 of the normalization, p_1 is the value in which the noise levels are the 50% of its maximum and p_2 give us the width of the ThS curve.

In the absence of external signals (cosmic rays, injected signals, etc) these noise ThS curves show the convolution of the envelope of the electronic noise at the output of the fast shaper (the trigger decision branch on the SKIROC). Indeed, the size of this envelope is related to the slow clock frequency.

To reduce to the minimum the presence of cosmic rays signals, we perform runs with short open acquisition windows as described in the previous section. In Figure 6 two result of two threshold scans and the fit by a ThS curves for two different channels from the second layer of the setup are shown.

The function from equation 3.1 was fitted to all channels data and all the values of p_1 and p_2 were saved. The final threshold value of every ASIC, in DAC units, was chosen by taking the

$$\text{maximum}(\text{DAC}_{\text{optimal}}^{\text{ASIC}-j} = \langle p_1^{\text{ASIC}-j} \rangle + 5 \times \langle p_2^{\text{ASIC}-j} \rangle, 230) \quad (3.2)$$

if at least the the 30% of the 64 channels ThS curves in the ASIC could be fitted. If only less than the 30% of curves of the 64 channels were successfully fit, a global DAC value of 250 was set. The $\langle \rangle$ denotes the average over all the channels on the ASIC. The choice of these two values was sustained by previous experiences, see for example [24].

The optimal trigger threshold values for all ASICs are shown in Figure 9.

3.3 S/N ratio in the trigger line

Similar kind of measurements can be done but using external signals. This will allow to calculate the signal over noise (S/N) ratio to trigger 1 MIP signals. To calculate the S/N of the trigger we need to compare the 1 MIP ThS curve and 2 MIP ThS curve. The S/N will be defined as the ratio between the distance of both ThS curves at its 50% and the width of the ThS curve.

In Figure 7 we see the 1 MIP and 2 MIP ThS curves obtained for several channel in a SKIROC testboard in which a single SKIROC2 in BGA package is placed and the 1 MIP and 2 MIPs signals are directly injected in the preamplifier (via a 3 pF capacitor located in the injection line as shown in Figure 1). From this plot we can extract a S/N ratio of ~ 12.8 . We do not expect large differences with the results that we would obtain with a full equipped SLABs although this board is thought for commissioning and test of the SKIROC ASICS in an "ideal" environment in contrast with the FEV ASUS that are optimized to meet the detector requirement and to hold several ASICs at the same time.

We have obtained similar results using real signals, in this case cosmic rays signals by using very long acquisition windows of 150 ms at 5 Hz. This is shown in Figure 8 where we show the result of the fit to the noise ThS curves for all channels individually (in red) in one of the ASICs of the second layer together with the results of the ThS curve obtained with cosmic rays integrated for all channels (black points and blue line). We expect a broader distribution of the cosmic ThS curve since muons can traverse the detector at different incidence angles. In addition to this, we should remember that the noise ThS curve do correspond to the real noise distribution but only to the envelope of the noise in the fast shaper, therefore the distance between the two ThS curves is smaller than the real distance between noise and signal. Therefore, if we calculate the S/N using this plot, the value would be unrealistic but at least provides the comparison between the ThS curve for 1 MIP real and injected signals.

Both ways of estimating the S/N ratio of the trigger have their own limitations and dedicated studies in beam test are needed in order to precisely determine it. In the meanwhile, combining the information contained in the Figs 7 and 8, we can estimate the value in energy at which we have set our trigger threshold. This is shown in Figure 9.

3.4 Prospects

All the commissioning procedure described above relies in very conservative decisions due to the presence of unknown noise sources during most of the commissioning phase. These sources are now well known and isolated and therefore a new "noise commissioning procedure" has been studied. It will consist in an iterative algorithm that first will identify and mask the channels giving

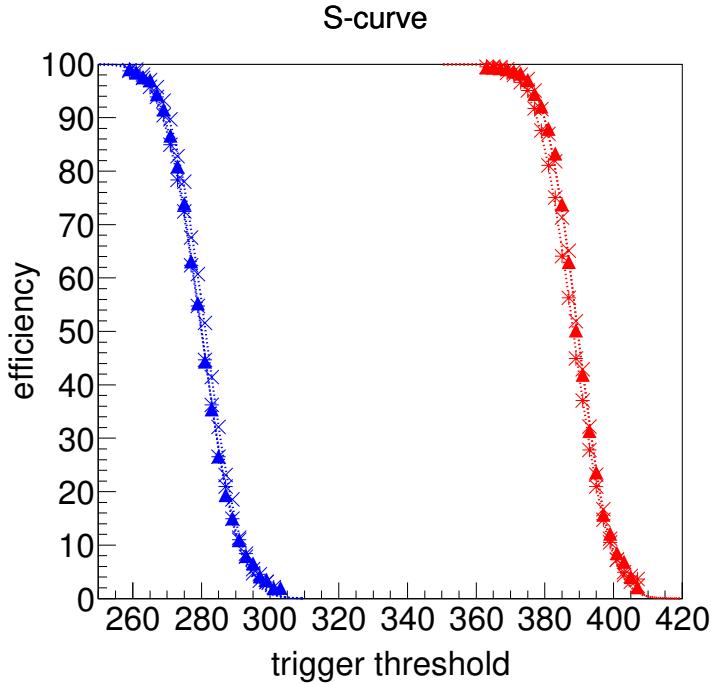


Figure 7. ThS curves with charge injection (1 MIP in blue and 2 MIPs in red) for two different channels in a SKIROC2 testboard. From this plot, we extract a $S/N = 12.8$ in the trigger line.

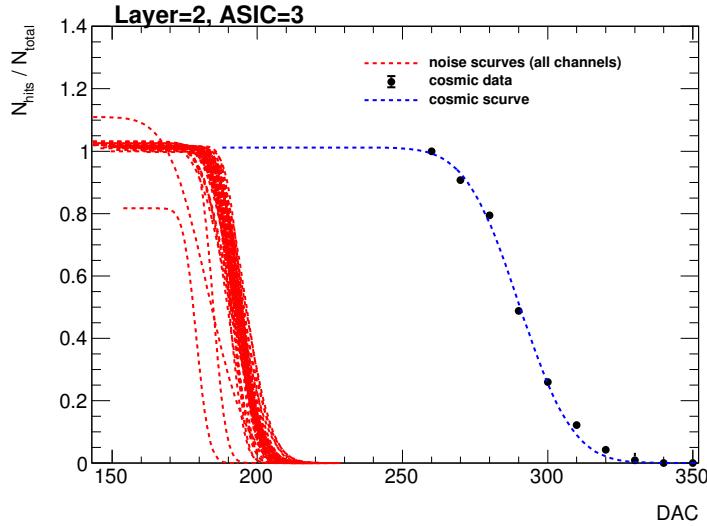


Figure 8. ThS curves for noise (channel by channel, only the result of the fit) and cosmic rays (all channels together) for one ASIC in layer 2.

underflowed signals and afterwards run a set of acquisitions in which the number of triggers per channel will be compared with the number of expected triggers assuming only cosmic rays as signal. This will allow us to have an unambiguous definition of the noise levels channel per channel instead of defining such levels relatively to the total number of recorded triggers per ASIC. Finally, once

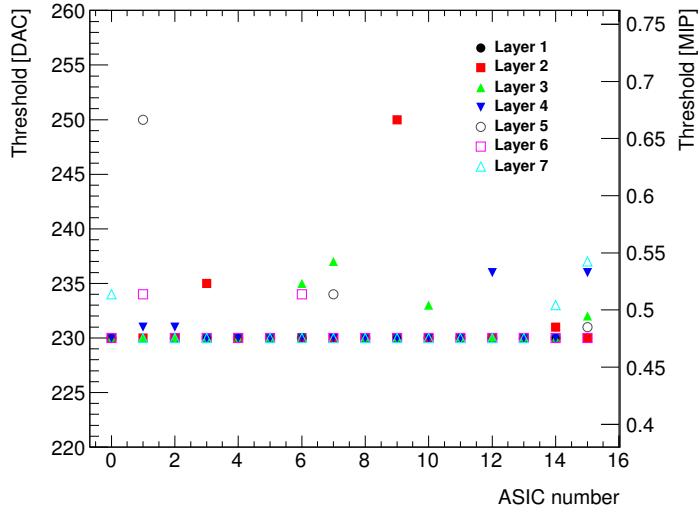


Figure 9. Summary of the trigger threshold settings in internal DAC units and in MIP units.

that the noisy channels are identified, the optimization of the threshold levels will be performed and a last run for identification of noisy channels will be taken using this optimal threshold.

Using this new procedure we manage to reduce the number of masked channels by a factor 2 without any loss of performance, at least in the laboratory and using 3 of the 7 SLABs. This new procedure will be tested in the next beam test. Also, in order to optimize the commissioning of the detector, we propose a new set of measurements in the next beam test such as a scan of optimal delay of the hold values of the trigger using MIP like particles and a threshold scan for the determination of the S/N in the trigger line. This later can be done by the comparison of ThS curves taken with 1 MIP and $\sqrt{2}$ MIP signals (tilting the detector by 45 degrees).

284 4 Performance on positron beam test at DESY

The beam test line at DESY provides continuous positron beams in the energy range of 1 to 6 GeV with rates from few hundreds of Hz to few KHz with a maximum of ~ 3 KHz for 2-3 GeV. The particles beam ies produced as follows: first, the electron/positron synchrotron DORIS II is used to produced a photon beam via bremsstrahlung when interacting with a carbon fiber target; secondly, these photons are then converted to electron/positron pairs; and, finally, the beam energy is selected with dipole magnets and collimators. In addition, DESY gives acces to a bore 1 T solenoid, the PCMag.

A photograph showing the SiW-ECAL technollogical prototype setup can be seen in Figure 10. Current prototype consists on 7 layers of SLABs housed by a PVC and aluminum structure that can hold up to 10. For the beam test described in Section 4 all the layers were separated by equal distances of 15 mm except the last one which was at 60 mm of its nearest. In the following sections, we will refer to layers number 1 to 7, where the 1 is the closest to the beam pipe and 7 is the farthest. The detector was exposed to a positron beam in the DESY test beam area (line 24). By means of an external pulse generator we defined the length of the acquisition window to be 3.7 ms

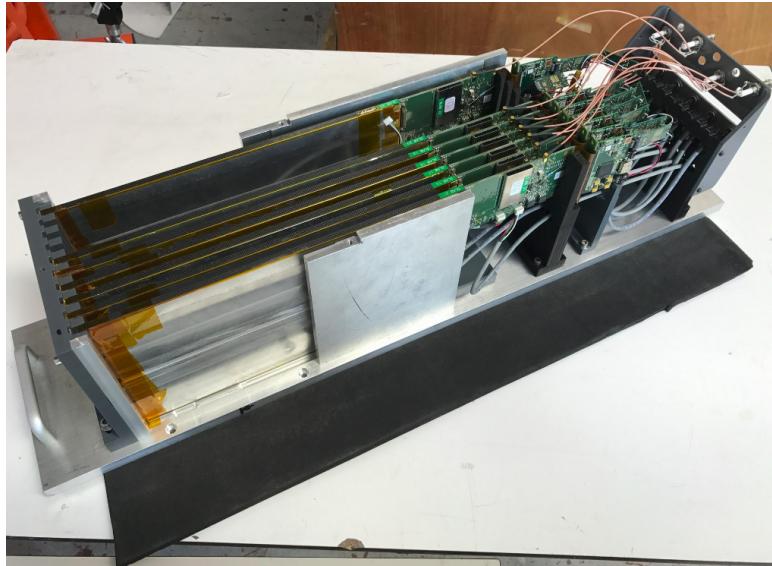


Figure 10. Prototype with 7 layers inside the aluminum stack.

299 at a frequency of 5 Hz. The detector was running in power pulsing mode without any extra active
300 cooling system.

301 The physics program of the beam test can be summarized in the following points:

302 1. Calibration without tungsten absorber using 3 GeV positrons acting as minimum ionizing
303 particle (MIPs) directed to 81 position equally distributed over the modules.

304 2. Test in magnetic field up to 1 T using the PCMag. For this test a special PVC structure was
305 designed and produced to support one single SLAB. The purpose of such test was twofold:
306 first to prove that the DAQ, all electronic devices and the mechanical consistency of the SLAB
307 itself are able to handle strong magnetic fields; second to check the quality of the data and
308 the performance of the detector during the data taking when running in a magnetic field.

309 3. Response to electrons of different energies with fully equipped detector, i.e. sensitive parts
310 and W absorber, with three different repartitions of the absorber material:

- 311 • W-configuration 1: 0.6, 1.2, 1.8, 2.4, 3.6, 4.8 and 6.6 X_0
- 312 • W-configuration 2: 1.2, 1.8, 2.4, 3.6, 4.8, 6.6 and 8.4 X_0
- 313 • W-configuration 3: 1.8, 2.4, 3.6, 4.8, 6.6, 8.4 and 10.2 X_0

314 First reports on this beam test can be find in Refs. [27, 28]. In this paper we discuss in more
315 detail the results of the pedestal, noise and MIP calibration in Section 4.1. We show also results on
316 the pedestal and noise stability when running inside a magnetic field in Section ???. Finally, a first
317 peek to the response and stability of the detector in electromagnetic showers events is discussed in
318 Section 4.3.

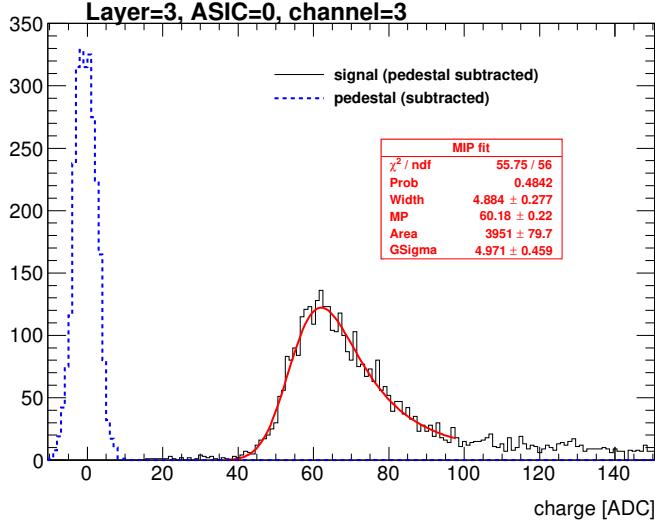


Figure 11. Pedestal (blue dashed line) and signal (black continuous line) distribution for one channel in the third layer.

319 4.1 Response to MIP-acting positrons

320 The calibration runs have been used to calculate the pedestal distribution reference values and the
 321 noise levels (the width of the pedestal distribution) of each channel. In Figure 11 we show the signal
 322 and pedestal distribution of a single channel after subtracting the pedestal mean position. The
 323 results of the MIP calibration fit are shown in red (see Section 4.1.2 for more details). The pedestal
 324 distribution is shown only for the first SCA to keep the y-axis within a reasonable range. The signal
 325 distribution is integrated over all SCAs.

326 4.1.1 Pedestal and noise determination

327 The pedestal is calculated as the mean position of the ADC distribution of channels without trigger.
 328 The noise is associated to the width of such distribution. The pedestal correction is done layer-,
 329 chip-, channel- and SCA-wisely due to the large spread of values between pedestals, as observed
 330 in Figure 12 (left plot) and Figure 13 (also left plot). For the noise, the dispersion is much smaller
 331 ($\sim 5\%$). This is shown in the right plots of Figures 12 and 13. From now on, the pedestal correction
 332 is applied to all the results presented.

333 4.1.2 Energy calibration and tracking efficiency

334 After the pedestals are calculated and subtracted to the hit distributions, those are fit by a Landau
 335 function convoluted with a Gaussian. The most-probable-value of the convoluted function is taken
 336 as the MIP value, allowing thus for a direct conversion from ADC units to energy in MIP units. We
 337 have obtained a raw energy calibration spread of the 5% among all channels with the 98% of all
 338 available channels being fitted. Results are summarized in figure 14, leftmost plot.

339 We checked the MIP calibration in all calibrated channels by selecting tracks incident perpen-
 340 dicillary to the layers surface. The results are shown in figure 15 where the single channel energy

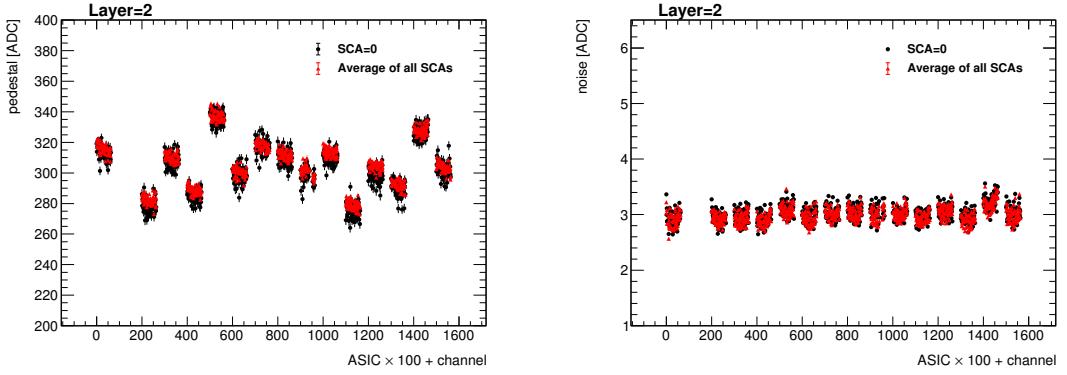


Figure 12. Pedestal mean position (upper plot) and width (lower plot) for all channels in one layer. The data is grouped on bunches in which the value in the x-axis corresponds to the value of the channel number plus the value of the ASIC number multiplied by 100. The black points show the value for the first SCA and the red points show the average value for all the others SCAs (with the standard deviation of the sample as error bar).

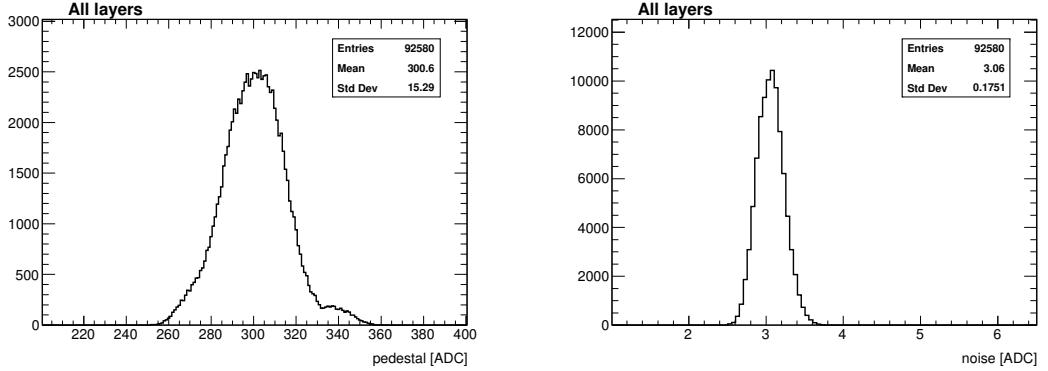


Figure 13. Pedestal mean position (left) and width (right) for all channels and all SCAs in the setup.

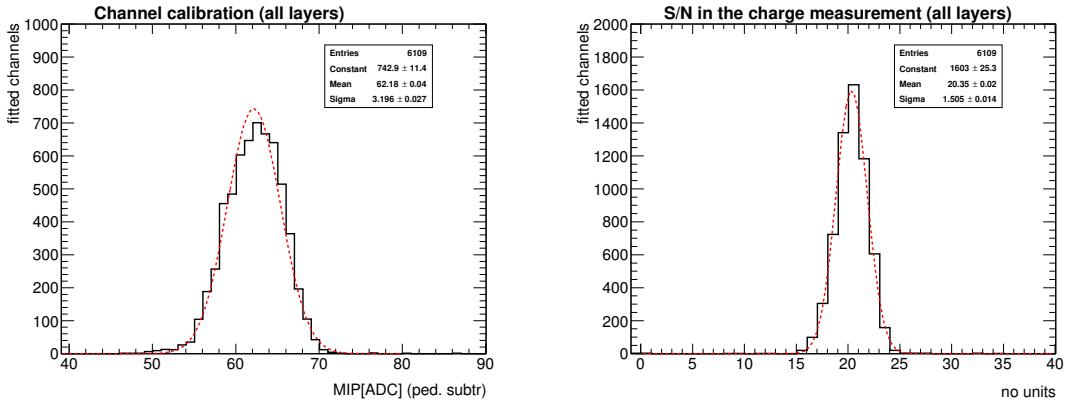


Figure 14. Result of the MIP position calculation and signal over noise calculation for all calibrated channels.

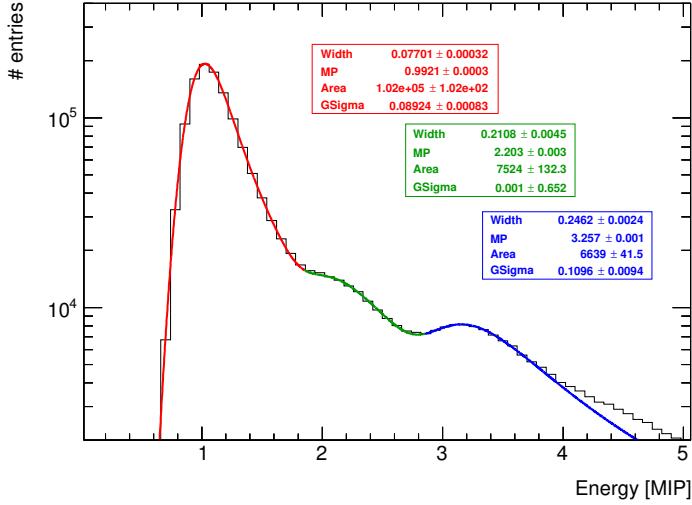


Figure 15. Energy distribution for all calibrated channels when selecting tracks of 3 GeV positron acting as MIPs.

341 distribution for MIPs is shown for all calibrated channels in the same distribution. The maximum
 342 peaks at 1 MIP as expected after a good calibration. In addition to this, a second and a third peak
 343 appear visible. These peaks are due to events involving multiple particles crossing the detector.

344 To evaluate the single hit detection efficiency we define a high purity sample of events by
 345 selecting tracks with at least 4 layers with a hit in exactly the same channel. Afterwards we
 346 check if the other layers have or not a hit in the same channel (expanding the search to the closest
 347 neighbouring channels) with energy larger or equal than 0.3 MIP. Finally, we repeat this for all
 348 layers and channels. The results are shown in Figure 16. Except few exceptions, the efficiency
 349 is compatible with 100%. Lower efficiencies in the first layer are related to the presence of noisy
 350 channels not spotted during the commissioning. In the last layer (separated from the other layers
 351 by four slots of 1.5 cm instead of only one) we also observe few small deviations from the $\sim 100\%$
 352 which are indeed associated to a slight misalignment of the detector. If we remove these channels
 353 from the analysis the full efficiency is recovered.

354 4.1.3 S/N ratio in the charge measurement for MIP interactions

355 The signal-over-noise ratio in the charge measurement (corresponding to the slow shaper of the
 356 SKIROC2) is defined as the ratio between the most-probable-value of the Landau-gauss function
 357 fit to the data (pedestal subtracted) and the noise (the pedestal width). This quantity has been
 358 calculated for all channels and all layers. The average S/N is to 20.4. Results are summarized in
 359 Figure 14, rightmost plot.

360 4.2 Pedestal and noise stability in a magnetic field

361 The data taking inside the magnetic field has been divided in three steps: a) a with a magnetic field
 362 of 1 T; b) a run with 0.5 T; c) a final run with the magnet off. The beam, 3 GeV positrons, was
 363 hitting in the area of the PCB readout by the ASIC number 12.

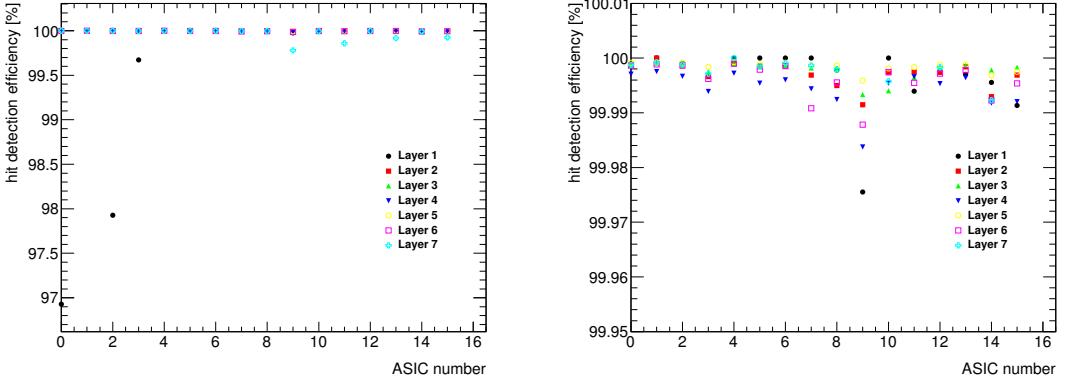


Figure 16. Left: MIP detection efficiency for all layers and ASICS in high purity samples of tracks of MIP-like acting particles. Right: same figures with a zoom in the y-axis. In both cases, the average efficiency of the 64 channels in each ASIC is shown.

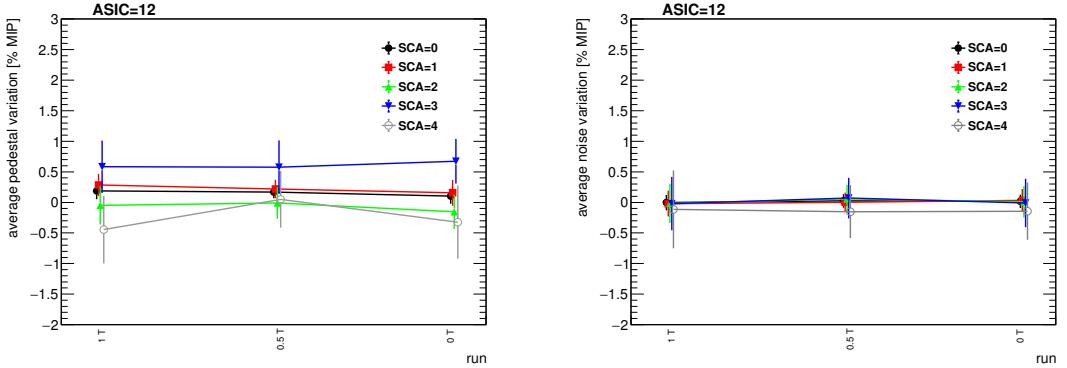


Figure 17. Average deviation of the pedestal mean position (left) and width (right) for all channels in the ASIC 12.

364 The pedestal positions and noise levels of the channels of the ASIC 12 when the SLAB
 365 is inside of the PCMag are compared with the results from the calibration run described in the
 366 previous section. This is shown in Figure 17. We see that the agreement is perfect within the
 367 statistical uncertainties. Due to the lower rates in this beam area, the analysis is only done up to few
 368 SCAs.

369 4.3 Pedestal stability in electromagnetic shower events

370 In this section we discuss the pedestal stability in events with large amount of charge collected by the
 371 ASICS, as are the electromagnetic shower events. All the results shown in this section correspond
 372 to data taken during the tungsten program, using the W-configuration number 2 when shooting the
 373 beam in the area registered by the ASIC 12 (and partially in the 13). Only information recorded
 374 by ASIC 12 is used in the analysis. For other configurations we get comparable results. In order
 375 to select a high purity of electromagnetic shower like the events, we used a simple criteria: select
 376 only events with at least 6 of the layers with at least a hit with $E > 0.5$ MIP.

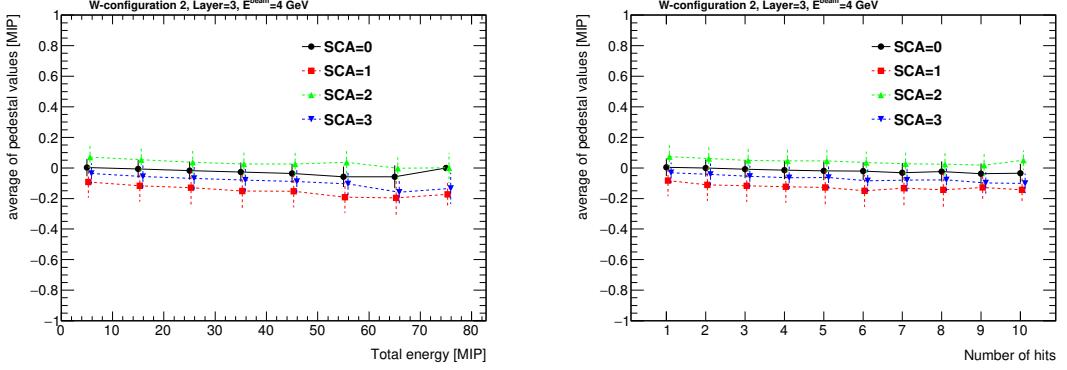


Figure 18. Left: mean position of the projection of the pedestal distribution of all channels calculated when different energies are collected in the ASIC (in bins of 10 MIPs). Right: same but as a function of the number of hits. In both cases, the results are shown for few SCAs. The points for the curves with SCA larger than zero are slightly shifted in the x-axis to optimize the visualization.

377 Two main observations have been extracted from the recalculation of the pedestals and its
 378 comparison with the values obtained previously during the calibration runs. The first observation
 379 consists in a relatively small drift of the pedestal values towards lower values when the collected
 380 energy is high (or when the number of triggered channels is large). This is shown in Figure 18 for
 381 several SCAs where the average of the projection of the pedestal distribution for all channels non
 382 triggered in ASIC 12 of layer 3 is plot as a function of the total energy measured by the ASIC (or
 383 the total number of hits). We see that in both cases, the shapes of the curves for each SCA are very
 384 similar. This feature is known and it is due to the architecture of the SKIROC2 ASICs where high
 385 inrush of currents can slightly shift the baseline of the analogue power supply.

386 The second observation extracted from this analysis can be also seen in Figure 18 but more
 387 clearly in Figure 19: in addition to the small drift of the pedestal value an SCA-alternate global
 388 shift is observed. We see that the effect is enhanced when large amounts of charge are deposited
 389 in the ASIC (*i.e.* at larger beam energies or for the layers in the maximum of the shower profile).
 390 We also observed that this alternation is only SCA dependent and does not depends on the time in
 391 which the deposit of energy occurs within the acquisition. This is not yet fully understood although
 392 the fact that the effect is observed in alternate SCAs hints that something is affecting to the digital
 393 part of the ASIC (where the SCAs enter in play). Dedicated tests in the laboratory and in the beam
 394 are needed in order to clarify this issue.

395 5 Summary

396 The R&D program of the highly granular SiW-ECAL detector is in an exciting phase. After the
 397 proof of principle of the imaging calorimetry concept using the physics prototype, the technological
 398 prototype is being constructed and tested. In this document we describe the commissioning and
 399 beam test performance of a prototype built in with the first fully assembled detector elements.

400 A very comprehensive and detailed commissioning procedure has been established and opti-
 401 mized allowing us to identify and isolate the different noise sources that could spoil the data taking.
 402 The beam test has provided a lot of useful data to study the performance of the detector and to

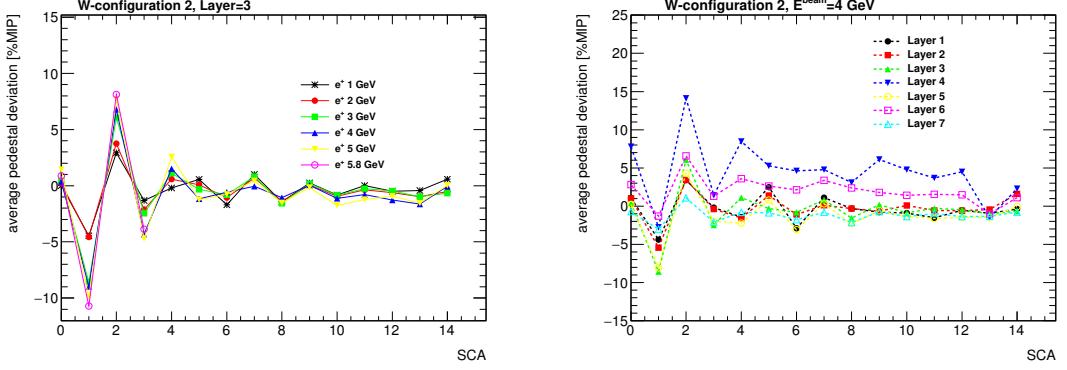


Figure 19. Left: average value on each SCA of the calculated pedestals for all channels of ASIC 12 in the Layer 3 for different energies of the beam. Right: same but fixing the energy of the beam and comparing several layers.

403 perform a channel by channel calibration. A full analysis of the MIP calibration within magnetic
 404 field and the response of the prototype in electromagnetic shower events will be covered in a future
 405 document. In addition, the results shown here serve as input for ongoing and future R&D.

406 6 Outlook

407 In parallel to the work described here, several R&D efforts are being carried. One of these efforts
 408 is directed to the design and test of new ASICs. In fact, a new generation of SKIROC2, the 2a,
 409 has been delivered and it is being tested in the dedicated testboards and it has been integrated in
 410 new ASUs. In addition, a new generation of the ASIC, SKIROC3, is foreseen for the final detector
 411 construction. In contrast with SKIROC2/2a, the new ASIC will be fully optimized for ILC operation,
 412 *i.e.* full zero suppression, reduced power consumption etc.

413 Many efforts are also concentrated in the construction and test of long SLABs made of several
 414 ASUs enchain since we know that the ILD ECAL will host long layers of up to $\sim 2.5\text{m}$. This
 415 device constitutes a technological challenge in both aspects, the mechanical (very thin and long
 416 structure with fragile sensors in the bottom, complicated assembly procedure...) and the electrical
 417 (*i.e.* transmission of signals and high currents). For example, interconnections between ASUs and
 418 between ASU and interface card are one of the most involved parts of the assembly and require
 419 close collaboration between mechanical and electronic engineers. The construction and test of a
 420 long SLAB prototype of ~ 8 ASUs is currently ongoing.

421 In parallel, a different proposal for a thinner ASU design is being investigated. This is motivated
 422 by the high density of channels demanded by the Particle Flow algorithms. In this alternative PCB
 423 design the ASICs are directly placed on board of the PCB in dedicated cavities. The ASICS will be
 424 in semiconductor packaging and wire bonded to the PCB. This is the so-called COB (chip-on-board)
 425 version of the ASU. A small sample of FEV11_COBs (same connexion pattern with the interface
 426 card than FEV11) with a total thickness of 1.2 mm (to be compared with the 2.7 of the LFBGA
 427 solution) has been produced and tested in the laboratory showing its readiness for tests with particle
 428 beams. A sample can be seen in Figure 20. These new boards maximize the density of channels

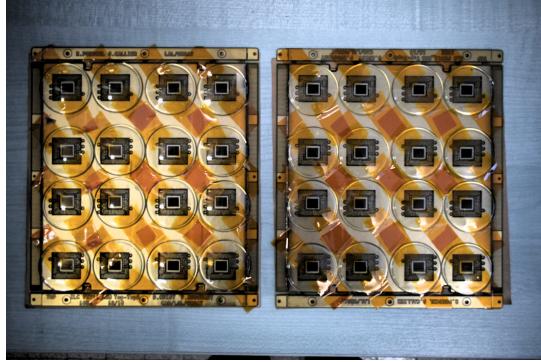


Figure 20. Two FEV11_COB boards with 16 SKIROC2a wire bonded. The ASICs are protected with watch glasses.

429 (4800 channels/dm³) for the ECAL of the ILD and will allow to satisfy the requirement of having
 430 30 active layers in 20 cm length for the barrel areas of the ECAL.

431 Finally, intensive R&D on the compactification of the DAQ towards meeting the ILD tight
 432 space requirements is being done by the SiW-ECAL collaboration.

433 It is foreseen that all these developments, with the exception of the SKIROC3, will be tested
 434 with particle beams during 2018-2019.

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 443 The measurements leading to these results have been performed at the Test Beam Facility at DESY
 444 Hamburg (Germany), a member of the Helmholtz Association (HGF).

445 A Appendix: Filtering of fake triggers

446 Several types of fake signals have been observed in the technological prototype since its construction
 447 and test. A detailed description of them can be found in previous articles, as for example, in Ref.
 448 [24]. All these fake signals are easily identified and tagged during the data acquisition and removed
 449 afterwards from the analysis not introducing any significance loss of performance as can be seen,
 450 for example, in the hit detection efficiency plots (see Section 4.1.2). In the following, we briefly
 451 describe the status of the monitoring, debugging and filtering of such kind of events.

452 Empty triggers

453 Empty trigger events are a well known feature of SKIROC2. The SKIROC2 uses an OR64 signal
 454 to mark the change to a new SCA when a signal over threshold is detected. The empty triggers

455 appear when during the acquisition the rising edge of the slow clock falls during the OR64 signal
456 and therefore the change to a new SCA is validated twice. This effect creates around 17% of empty
457 events which are easily filter and removed from the analysis. The ratio of empty triggers in the new
458 SKIROC2a has been reduced to the $\sim 2 - 3\%$.

459 **Plane events and retriggers**

460 Another well known issue is the appearance of bunches of consecutive fake triggers, called retriggers,
461 that saturates the DAQ. Although the ultimate reason of the appearance of these events remains not
462 clear, it is suspected that they are related to distortions of the power supply baselines. We know
463 that the SKIROC2 and 2a preamplifiers are referenced to the analog power supply level, therefore,
464 any voltage dip can be seen as signal by the preamplifiers. Moreover the presence of a high inrush
465 of current due to many channels triggered at the same time can create these voltage dips and also
466 produce the so called plane events (most of the channels triggered at once). In previous studies (*i.e.*
467 reference [24]), the ratio of retriggers and plane events was reduced by improving the power supply
468 stabilization capacitances. It is important to remark that all layers and all ASICs analog and digital
469 levels are powered using the same power supply. Moreover, the high voltage power supply for the
470 polarization of the PIN diode is also common for all layers and the grounding levels of the low
471 and high voltages supplied are shared within the slab. Therefore any noise in these power supplies
472 or any overload of an ASIC may participate in the creation of fake signals in different ASICs and
473 layers.

474 Studying the MIP calibration data of this beam test we have noticed that the concentration of
475 the retriggers and plane events in ASICs far from the beam spot is higher than in the ASICs that
476 are reading out the information of real hits. Even more, this concentration is even higher near the
477 channels 37 and the channels masked as suspicious of suffering from routing issues. The ratio these
478 events have been estimated to be of 1 – 3% in the ASICs where high frequency interactions are
479 produced (*i.e.* using 3 GeV positrons at 2-3 KHz) and at higher rates even larger than 40% in other
480 ASICs far from the beam spot. Moreover, it has been noticed a correlation between the time that
481 an ASIC was full and the time of the appearance of some retriggers in other areas of the PCB. This
482 correlation corresponds to $\sim 1.6 \mu\text{s}$ which hints of a distortion on the analogue power supply when
483 the signal that informs the DIF that one ASIC memory is full is transmitted through the PCB.

484 We should point out that these events are easily filtered out during the analysis (or even during
485 the online monitoring) and that no impact is observed in the data, *i.e.* in the MIP detection efficiency.

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