

Commissioning and performance in beam tests of the highly granular SiW-ECAL technological prototype for the ILC.

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Abstract

High precision physics at future colliders as the International Linear Collider (ILC) require unprecedented high precision in the determination of the final state of the particles produced in the collisions. The needed precision will be achieved thanks to the Particle Flow algorithms (PF) which require compact, highly granular and hermetic calorimeters systems. The Silicon-Tungsten Electromagnetic Calorimeter (SiW-ECAL) technological prototype design and R&D is tailored to the baseline design of the ECAL of the International Large Detector (ILD) for the ILC. In this document we present and discuss the commissioning of the prototype and the performance of the device in a beam test carried at DESY in June 2017.

Keywords: Calorimeter methods, calorimeters, Si and pad detectors

1. Introduction

Future accelerator based particle physics experiments require very precise and detailed reconstruction of the final states produced in the beam collisions. A particular example is the next generation of e^+e^- linear colliders such the ILC[? ? ? ? ?]. This project will provide collisions of polarized beams with centre-of-mass energies (*c.m.e*) of 250 GeV - 1 TeV. These collisions will be studied by two multipurpose detectors: the International Large Detector (ILD) and the Silicon Detector (SiD)[?]. Another example of an e^+e^- collider project is the Compact Linear Collider (CLIC) project[? ? ?] which will produce collisions with *c.m.e* of 380 GeV - 3 TeV with a detector featuring similar design than the ILD and SiD. Both projects will explore with unprecedented precision the origin of the electroweak symmetry breaking and new physics beyond the standard model by exploring final states with heavy bosons (W, Z and H) and fermions (*i.e.* heavy quarks as c , b and t).

It is known that in a *classical* typical multipurpose detector of a collider experiment the charged particles momentum is better measured by the tracking system the photons energy are only observed in the calorimeter system (mainly in the electromagnetic) if they are not converted and the measurement of the neutral hadrons energy can only be done by involving the full calorimeter systems. To meet the required precision levels by

the ILC or CLIC physics goals, new techniques relying on single particle separation to make possible the choice of the best information available in the full detector to measure the energy of the final state objects have been developed. These techniques are called Particle Flow (PF) techniques [? ? ?] and allow to reduce the impact of the poor resolution of the calorimeter systems (compared with trackers) in the overall reconstruction. For this purpose, detectors optimized for PF algorithms have some requirements. Some of them are summarized here:

- a highly efficient and "transparent" tracking system between the interaction point and the calorimetry systems;
- highly granular (*imaging calorimetry*) and compact calorimeter systems featuring minimum dead material;
- and high power of particle separation¹.

The R&D of highly granular calorimeters for future linear colliders is conducted within the CALICE collaboration and, for now on, we refer the reader to [?] for further information about PF and the CALICE R&D.

In this document we will focus in the description of the silicon-tungsten electromagnetic calorimeter, SiW-ECAL, its commissioning and its performance in beam

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53 test. The SiW-ECAL is the baseline choice for the ILD
 54 ECAL. It consists in a detector (in the barrel region) of
 55 $24 X_0$ of thickness which corresponds to $\sim 1 \lambda_I$ (in-
 56 teraction length). It has silicon (Si) as active material
 57 and tungsten (W) as absorber material. The combina-
 58 tion of Si and W choices makes possible the design and
 59 construction of a very compact calorimeter with highly
 60 granular and compact active layers. It will consist of
 61 an alveolar structure of carbon fiber into which mod-
 62 ules called SLABs made of tungsten plates and the ac-
 63 tive sensors will be inserted. The very-front-end (VFE)
 64 electronics will be embedded in the SLABs. The silicon
 65 sensors will be segmented in squared cells (or channels)
 66 of 5×5 mm: a total of ~ 100 million channels will con-
 67 stitute the ECAL for ILD. The desired signal dynamic
 68 range in each channel goes from 0.5 MIP to 3000 MIPs.
 69 To reduce overall power consumption, the SiW-ECAL
 70 will exploit the special bunch structure foreseen for the
 71 ILC: the e^+e^- bunches trains will arrive within acquisi-
 72 tion windows of $\sim 1\text{-}2$ ms width separated by ~ 200 ms.
 73 During the idle time, the bias currents of the electronics
 74 will be shut down. This technique is usually denom-
 75 inated power pulsing. In addition to this, to cope with the
 76 large amount of channels, the calorimeters should work
 77 in self-trigger mode (each channel featuring an internal
 78 trigger decision chain) and zero suppression mode.

79 The first SiW-ECAL prototype was the so called
 80 SiW-ECAL physics prototype. It was successfully
 81 tested at DESY, FNAL and CERN running in front
 82 of another prototype from the CALICE collaboration,
 83 the analogue hadronic calorimeter AHCAL, delivering
 84 the proof of concept of the technology and the PF
 85 calorimetry. For the physics prototype, the VFE was
 86 placed outside the active area with no particular con-
 87 straints in power consumption. It consisted of 30 lay-
 88 ers of Si as active material alternated with tungsten
 89 plates as absorber material. The active layers were
 90 made of a matrix of 3×3 Si wafers of $500 \mu\text{m}$ thick-
 91 ness. Each of these wafers was segmented in matrices
 92 of 6×6 squared channels of $1 \times 1 \text{ cm}^2$, allowing for den-
 93 sity of 1500 channels/ dm^3 . The prototype was divided in
 94 3 modules of 10 layers with different W depth per layer
 95 in each of these modules (0.4, 1.6 and $2.4 X_0$) making a
 96 total of $24 X_0$. That very first prototype offered a signal
 97 over noise on the measured charge of 7.5 for MIP like
 98 particles. More results proving the good performance of
 99 the technology and the PF can be found in references [? ? ? ? ?].
 100

2. The SiW-ECAL technological prototype

101
 102 The new generation prototype is called the SiW-
 103 ECAL technological prototype. It addresses the main
 104 technological challenges: compactness, power con-
 105 sumption reduction through power pulsing and VFE
 106 inside the detector close to real ILD conditions. It
 107 will also provide data to deeply study the PF and pro-
 108 vide input to tune simulation programs as for example
 109 GEANT4[? ? ?] which is widely used in particle
 110 physics to simulate the passage of particles through mat-
 111 ter.

2.1. Silicon sensors

112
 113 The sensors consist on floating zone silicon wafers
 114 $320 \mu\text{m}$ thick with high resistivity (bigger than 5000
 115 $\Omega\text{-cm}$). The size of the wafer is $9 \times 9 \text{ cm}^2$ and it is sub-
 116 divided in an array of 256 PIN diodes of $5 \times 5 \text{ mm}^2$. A
 117 MIP traversing the PIN parallel to its normal will create
 118 $\sim 80 h^+e^-$ pairs per μm which corresponds to 4.1 fC for
 119 particles incident perpendicularly to its surface.

120
 121 The original design of the silicon wafers included an
 122 edge termination made of floating guard-rings. It was
 123 observed in beam tests [? ?] that the capacitive cou-
 124 pling between such floating guard-rings and the chan-
 125 nels at the edge was not negligible in tests with high
 126 energy beams (pions and electrons with energies larger
 127 than 20-40 GeV). This coupling lead to fake events in
 128 which, at least, the channels in the four edges of the
 129 wafer are triggered at the same time. This is why these
 130 events are called squared events. An R&D program
 131 together with Hamamatsu Photonics (HPK Japan) was
 132 conducted to study the guard-rings design as well as the
 133 internal crosstalk. It was concluded that using wafers
 134 without guard rings and with a width of the peripheral
 135 areas lower than $500 \mu\text{m}$ thanks to the use of stealth dic-
 136 ing technique, the amount of these squared events can
 137 be reduced to be almost negligible. This need to be con-
 138 firmed in beam test. Unfortunately, for the interaction
 139 with low energy particles as the delivered at the DESY
 140 beam test facility (see Section 4) the amount of squared
 141 events is expected to be negligible, therefore we will not
 discuss this issue in the following.

2.2. SKIROC: Silicon pin Kalorimeter Integrated Read- Out Chip

142
 143 The SKIROC[?] (Silicon pin Kalorimeter Integrated
 144 ReadOut Chip) is a very front end ASIC (application-
 145 specific integrated circuits) designed for the readout of
 146 the Silicon PIN diodes. In its version SKIROC2 it con-
 147 sists of 64 channels in AMS $0.35 \mu\text{m}$ SiGe technology.
 148

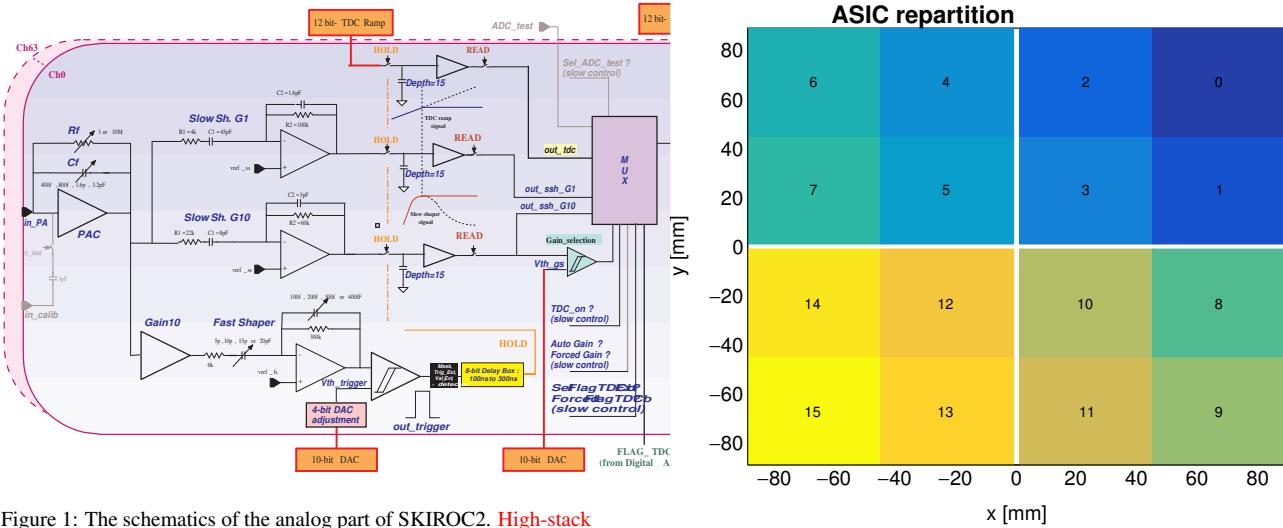


Figure 1: The schematics of the analog part of SKIROC2. **High-stack picture** (right bottom corner)

149 Each channel comprises a low noise charge preamplifier of variable gain followed by two branches: a fast
 150 shaper for the trigger decision and a set of dual gain
 151 slow shaper for charge measurement. The gain can be
 152 controlled by modifying the feedback capacitance during
 153 the configuration of the detector. With the slowest gain,
 154 6pF, the ASIC will handle a linear dynamic range from 0.1 to up to 1500 MIPs (a slightly less than the
 155 desired final value for the ILC). Finally, a Wilkinson
 156 type analogue to digital converter fabricates the digitized
 157 charge deposition that can be readout. Once one
 158 channel is triggered, the ASIC reads out all 64 channels
 159 adding a bit of information to tag them as triggered or
 160 not triggered and the information is stored in 15 cell
 161 deep physical switched capacitor array (SCA).

162 The SKIROC ASICs can be power-pulsed by taking
 163 advantage of the ILC spill structure: the bias currents
 164 of the ASIC can be switched off during the idle time
 165 between bunch trains. With this method, the ASIC is
 166 able to reduce its power consumption down to 25 μ W
 167 per channel, meeting the ILC requirements. All the re-
 168 sults shown in this paper are obtained in power pulsing
 169 mode.

172 2.3. Active Sensor Units

173 The entity of sensors, thin PCB (printed circuit
 174 boards) and ASICs is called Active Signal Units or
 175 ASU. An individual ASU has a lateral dimension of
 176 18x18 cm². The ASUs are currently equipped further
 177 with 16 SKIROC2 ASICs for the read out and features
 178 1024 square pads (64 per ASIC) of 5x5 mm. The chan-
 179 nels and ASICs are distributed along the ASU as shown

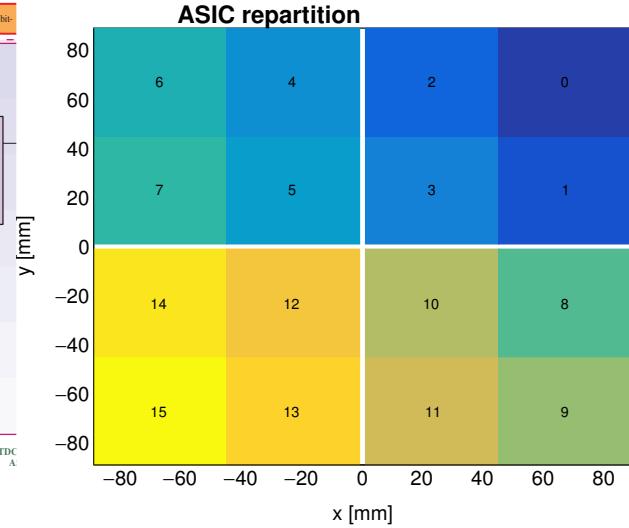


Figure 2: Repartition of the ASIC (up) and channels (down) in one ASU. In this perspective, the Si-Sensors are in glued in the back. The channels are separated (in x and y) by 5.5 mm. The empty cross in the middle of the ASU corresponds to the 1 mm separation between the sensors. The areas covered by the different ASICs and channels are labeled with numbers following design and DAQ criteria: from 0-16 in the case of the ASICs and from 0-63 in the case of the channels.

180 in Figure 2. Each ASU is equipped with 4 silicon wafers
 181 as the described in Section 2.1. The high voltage is de-
 182 livered to the wafers using a HV-kapton sheet that cov-
 183 ers the full extension of the wafers.

184 2.4. Data AcQuisition system

185 The subsequent chain of the data acquisition (DAQ)[?] J system is inspired by the ILC. It consists on three mod-
 186 ules. The first module is the so called detector interface

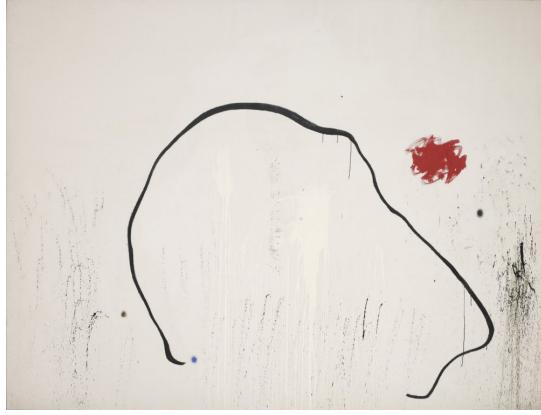


Figure 3: **Temporary picture: La Esperanza del Condenado, J. Miró:** Open single SLAB with FEV11 ASU, 16 SKIROC 2, interface card and DIF visibles.

(DIF) which is placed at the beginning of each layer holding up to 15 ASUs; All DIFs are connected by single HDMI cables to the concentrator cards that make the second module: the Gigabit Concentrator Cards (GDCCs). These cards are used to control up to 7 DIFs collecting all data from them and distributing among them the system clock and fast commands. The last module, the most downstream, is the clock and control card (CCC) which provides a clock, control fan-out of up to 8 GDCCs and accepts and distributes external signals (i.e. signals generated external pulse generator to simulate the ILC spill conditions). The whole system is controlled by the Calicoes and the Pyrame DAQ software version 3 [? ?].

2.5. Readout layers and SLABS

The readout layers of the SiW-ECAL consist of a chain of ASUs and an adapter board to a data acquisition system (DAQ) at the beginning of the layer. This adapter board is called SMBv4 and it also serves as to hold other services as power connectors or the super capacitances used for the power pulsing. These capacitances of 400mF with 16 mΩ of equivalent serial resistance. The purpose of these capacitances is to provide local storage of the necessary charge to avoid the transport of current pulses over long cables, ensuring in this way the stability of the ASICs during the acquisition.

The readout layers are embedded on a "U" shape carbon structure to protect the wafers. The full system is then covered by two aluminum plates to provide electromagnetic shielding and mechanical stability. This ensemble is denominated SLAB ("short" for 1 ASU ensembles or "long" for several ASUs enchainable) and it

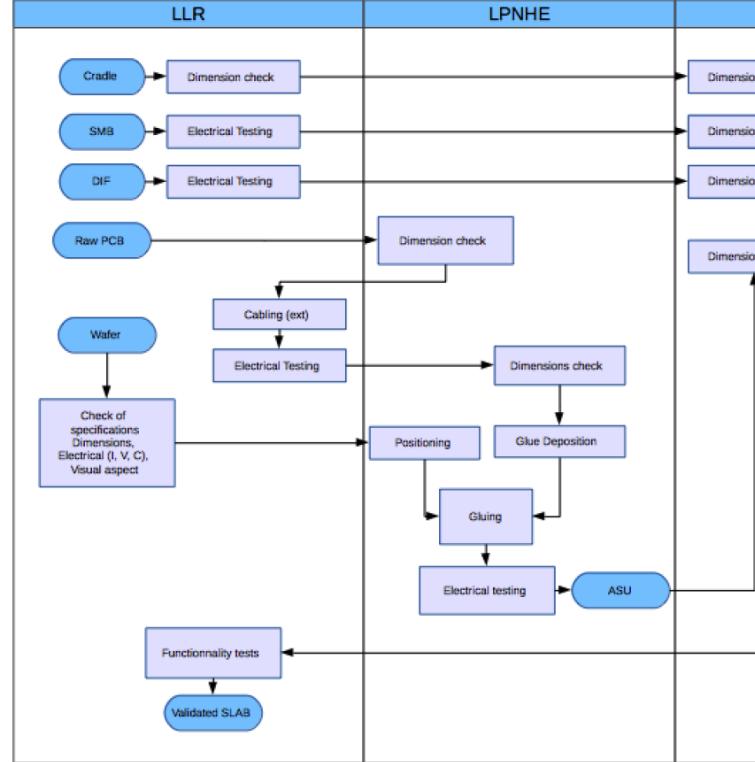


Figure 4: Process flow for the assembly of the SiW-ECAL SLABs.

can be seen in Figure 3. With current SLABs, a potential density of 4000 channels/dm³ is achievable. This number should be compared with the density achieved for previous beam tests: 1500 channels/dm³ [?].

The SiW-ECAL detector designed for the ILD requires of the order of 10⁵ highly integrated detection like the ones described in this text. For the production of the small sample of SLABs studied in this document, a scalable working procedure has been established among several groups [?] profiting from the funding of projects like AIDA2020 or the HIGHTEC emblematic project of the P2IO. A schematic view of this assembly procedure chain can be seen in Figure 4. For more details we refer to Ref.[?].

3. Commissioning

This beam test was prepared by a careful and comprehensive commissioning comprising the debug of the short SLABs with special emphasis in the control of the noise and the study of the prototype performance in cosmic rays tests.

Earlier experiences with the SKIROC2 ASIC are reported in Refs. [? ?]. Internal SKIROC2 parameters

242 found in these references are adopted in the following
 243 except if the opposite is stated. For example, the gain
 244 value of 1.2pF for the preamplifier is used. With this
 245 gain, the SKIROC2 ensures a linearity better than 90%
 246 for 0.5-200 MIPs, which is enough for electromagnetic
 247 showers created by few GeV electrons or positrons.

248 3.1. Optimization of noise levels

249 Studying and control the noise levels is crucial since
 250 noisy channels may saturate the DAQ faster than physical
 251 signals. Two different types of noise sources were
 252 identified: a set of noisy channels randomly distributed
 253 in time and noise bursts affecting to all layers at the
 254 same time. The outcome of this commissioning is sum-
 255 marized in Figure 5.

256 The first type of noise source, noise events randomly
 257 distributed in time, forced us to define a list of channels
 258 to be masked in all layers. Again, two different type
 259 of noisy channels have been identified. The first group
 260 is composed by randomly distributed in space channels.
 261 The second group is made of a fixed list of channels, all
 262 in the same positions for all SLABs, and all associated
 263 to a higher rate of events with underflowed value of the
 264 read ADC. A large amount of these channels are located
 265 in areas of the PCB where the density of lines (data and
 266 power transmission) is higher than in others. This hints
 267 for an issue on the routing of the PCB. Therefore, these
 268 channels are tagged in Figure 5 with the "routing issues"
 269 label although more tests and deeper inspections of the
 270 PCB layout are needed to clarify this issue.

271 The list of the noisy channels randomly distributed in
 272 time and space was defined by means of dedicated data
 273 taking runs. These runs were characterized by: their
 274 short acquisition windows (open to data recording for
 275 only 1.1 ms) at low repetition frequencies (5 Hz) to min-
 276 imize the chances of having real events due to cosmic
 277 rays hitting the detector during the data taking; and the
 278 relatively high trigger threshold values between 250 and
 279 400 DAC (which are equivalent to ~0.5-2 MIP, see Sec-
 280 tion 3.2 for more information). The full process was
 281 an iterative process starting with several repetitions of
 282 runs at a high threshold value and then some iterations
 283 at lower threshold but always higher than 0.5 MIP. In
 284 each of the iterations, the channels identified as noisy
 285 were masked. A full run involved 3-5 threshold values
 286 and at least two repetitions per value. Again, we de-
 287 cided to follow a conservative approach for list the noisy
 288 channels to be masked: if the channel was triggered at
 289 rates larger than 0.5-1% of the total number of triggers
 290 per ASIC it was added to the list. These channels are
 291 labeled as "other" in the first plot in Figure 5.

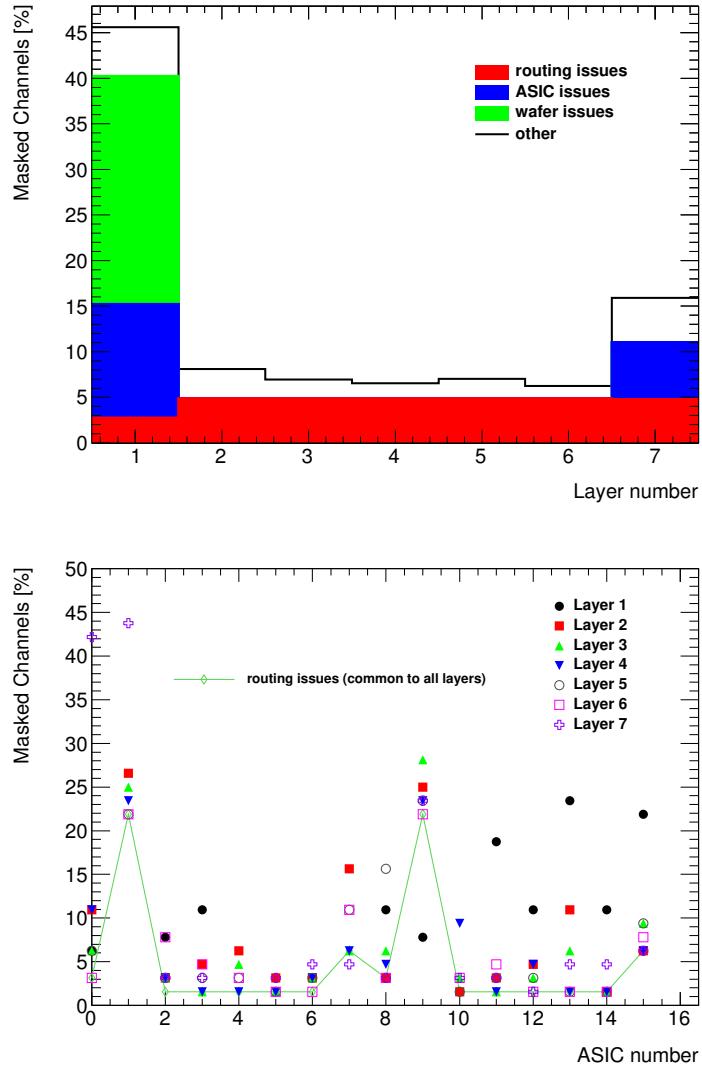


Figure 5: Ratio of channels that are marked as noisy in all slabs. Top: inventory of the different type of noisy channels per slab. Bottom: break down of the total number of noisy channels per ASIC. The ASICs 4-7 (wafer issue) and 10 from layer 1 and the ASIC 4 from layer 7 are not included in the second plot since they are fully masked.

In addition to the different noisy channel types described above, we also have masked full sectors of the SLABs if an ASIC was faulty (at least 70% of channels listed as noisy) or if a Si-wafer was misworking (high leakage currents). In these cases and in all mentioned above, the masking involved two steps: disabling of the trigger and the disabling of the power of the preamplifier of that channel.

The other source of noise mentioned at the beginning of this section consist on noise bursts happening

coherently at the same time in all SLABS and it was correlated to occasions when the electrical isolation between SLABS was broken. This is a hint of a system effect as can be the appearance of grounding loops or disturbances in the power supplies. The issue was circumvented by improving the electrical isolation of single layers. We have also observed that the noise bursts happens only at the end of long acquisitions. Therefore, in addition to the improved isolation, we selected short enough acquisitions windows (which indeed are the most appropriate to the high rates of particles in the DESY beam). Dedicated studies in the laboratory are currently ongoing in order to fully understand this issue.

The list of channels mentioned above is discarded from the data taking from now on.

3.2. Threshold determination

In order to select the optimal trigger threshold values for the detector operation we perform dedicated scans of trigger threshold values with all channels enabled (excepted the marked as noisy). The threshold values are given in internal DAC units which are translated to meaningful physical quantities in Section 3.3. The threshold scan curves made of the total number of hits normalized to 1 vs the threshold for each channel are modeled by a complementary error function called ThS curves from now on:

$$ThS(DAC) = p_0 \times erfc\left(\frac{DAC - p_1}{p_2}\right) = \frac{2p_0}{\sqrt{\pi}} \int_{\frac{DAC-p_1}{p_2}}^{\infty} e^{-t^2} dt, (1)$$

where p_0 is 1/2 of the normalization, p_1 is the value in which the noise levels are the 50% of its maximum and p_2 give us the width of the ThS curve.

In the absence of external signals (cosmic rays, injected signals, etc) these noise ThS curves show the convolution of the envelope of the electronic noise at the output of the fast shaper (the trigger decision branch on the SKIROC). Indeed, the size of this envelope is related to the slow clock frequency.

To reduce to the minimum the presence of cosmic rays signals, we perform runs with short open acquisition windows as described in the previous section. In Figure 6 two result of two threshold scans and the fit by ThS curves for two different channels from the second layer of the setup are shown.

The function from equation 1 was fitted to all channels data and all the values of p_1 and p_2 were saved. The final threshold value of every ASIC, in DAC units, was chosen by taking the

$$\text{maximum}(DAC_{optimal}^{ASIC-j} = < p_1^{ASIC-j} > + 5 \times < p_2^{ASIC-j} >, 250)$$

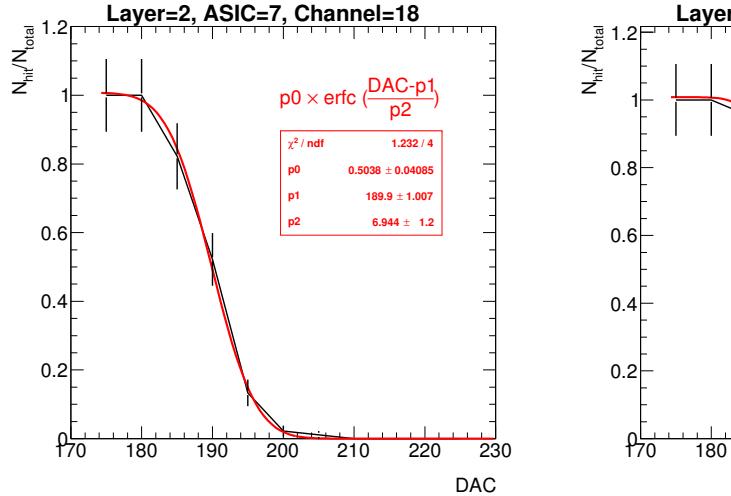


Figure 6: Two threshold scan curves and their associated ThS curves.

if at least the the 30% of the 64 channels ThS curves in the ASIC could be fitted. If only less than the 30% of curves of the 64 channels were successfully fit, a global DAC value of 250 was set. The $<>$ denotes the average over all the channels on the ASIC. The choice of these two values was sustained by previous experiences, see for example [?].

The optimal trigger threshold values for all ASICs are shown in Figure 9.

3.3. S/N ratio in the trigger line

Similar kind of measurements can be done but using external signals. This will allow to calculate the signal over noise (S/N) ratio to trigger 1 MIP signals. To calculate the S/N of the trigger we need to compare the 1 MIP ThS curve and 2 MIP ThS curve. The S/N will be defined as the ratio between the distance of both ThS curves at its 50% and the width of the ThS curve.

In Figure 7 we see the 1 MIP and 2 MIP ThS curves obtained for several channel in a SKIROC testboard in which a single SKIROC2 in BGA package is placed and the 1 MIP and 2 MIPs signals are directly injected in the preamplifier (via a 3 pF capacitor located in the injection line as shown in Figure 1). From this plot we can extract a S/N ratio of ~ 12.8 . We do not expect large differences with the results that we would obtain with a full equipped SLABS although this board is thought for commissioning and test of the SKIROC ASICs in an "ideal" environment in contrast with the FEV ASUS that are optimized to meet the detector requirement and several ASICs at the same time.

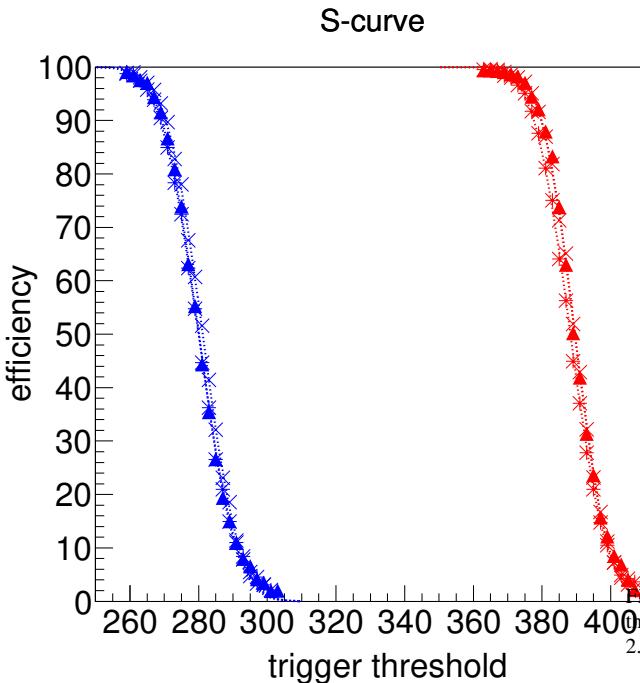


Figure 7: ThS curves with charge injection (1 MIP in blue and 2 MIPs in red) for two different channels in a SKIROC2 testboard. From this plot, we extract a $S/N = 12.8$ in the trigger line.

We have obtained similar results using real signals, in this case cosmic rays signals by using very long acquisition windows of 150 ms at 5 Hz. This is shown in Figure 8 where we show the result of the fit to the noise ThS curves for all channels individually (in red) in one of the ASICs of the second layer together with the results of the ThS curve obtained with cosmic rays integrated for all channels (black points and blue line). We expect a broader distribution of the cosmic ThS curve since muons can traverse the detector at different incidence angles. In addition to this, we should remember that the noise ThS curve do correspond to the real noise distribution but only to the envelope of the noise in the fast shaper, therefore the distance between the two ThS curves is smaller than the real distance between noise and signal. Therefore, if we calculate the S/N using this plot, the value would be unrealistic but at least provides the comparison between the ThS curve for 1 MIP real and injected signals.

Both ways of estimating the S/N ratio of the trigger have their own limitations and dedicated studies in beam test are needed in order to precisely determine it. In the meanwhile, combining the information contained in the Figs 7 and 8, we can estimate the value in energy at

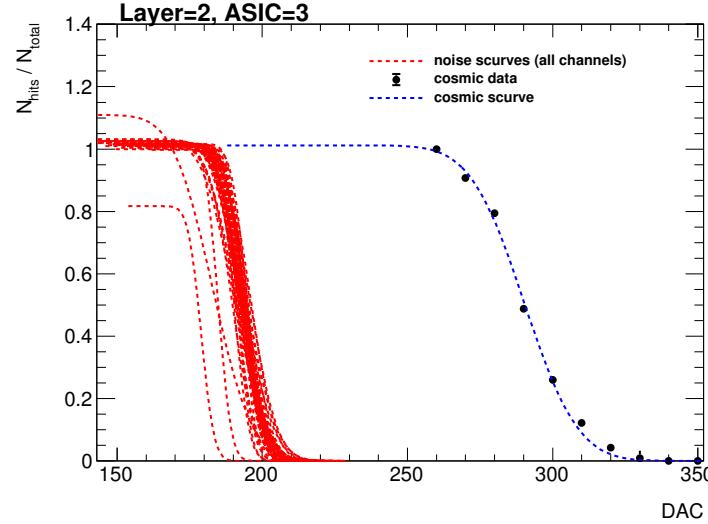


Figure 8: ThS curves for noise (channel by channel, only the result of the fit to the noise) and cosmic rays (all channels together) for one ASIC in layer 2.

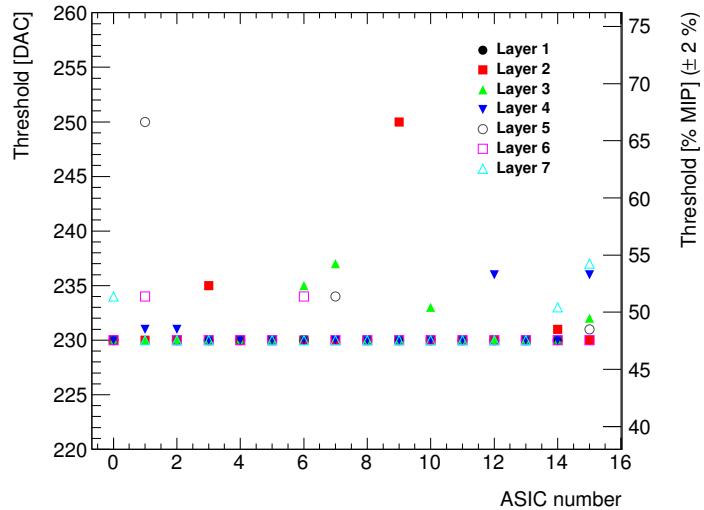


Figure 9: Summary of the trigger threshold settings in internal DAC units and in MIP units.

which we have set our trigger threshold. This is shown in Figure 9.

3.4. Prospects

All the commissioning procedure described above relies in very conservative decisions due to the presence of unknown noise sources during most of the commissioning phase. These sources are now well known and

410 isolated and therefore a new “noise commissioning pro-
 411 cedure” has been studied. It will consist in an iterative
 412 algorithm that first will identify and mask the channels
 413 giving underflowed signals and afterwards run a set of
 414 acquisitions in which the number of triggers per channel
 415 will be compared with the number of expected triggers
 416 assuming only cosmic rays as signal. This will allow
 417 us to have an unambiguous definition of the noise levels
 418 channel per channel instead of defining such levels rela-
 419 tively to the total number of recorded triggers per ASIC.
 420 Finally, once that the noisy channels are identified, the
 421 optimization of the threshold levels will be performed
 422 and a last run for identification of noisy channels will
 423 be taken using this optimal threshold.

424 Using this new procedure we manage to reduce the
 425 number of masked channels by a factor 2 without any
 426 loss of performance, at least in the laboratory and using
 427 3 of the 7 SLABs. This new procedure will be tested
 428 in the next beam test. Also, in order to optimize the
 429 commissioning of the detector, we propose a new set
 430 of measurements in the next beam test such as a scan of
 431 optimal delay of the hold values of the trigger using MIP
 432 like particles and a threshold scan for the determination
 433 of the S/N in the trigger line. This later can be done by
 434 the comparison of ThS curves taken with 1 MIP and $\sqrt{2}$
 435 MIP signals (tilting the detector by 45 degrees).

466 4. Performance on positron beam test at DESY

467 The beam test line at DESY provides continuous
 468 positron beams in the energy range of 1 to 6 GeV with
 469 rates from few hundreds of Hz to few KHz with a max-
 470 imum of ~ 3 KHz for 2-3 GeV. The particles beam
 471 ies produced as follows: first, the electron/positron syn-
 472 chrotron DORIS II is used to produced a photon beam
 473 via bremsstrahlung when interacting with a carbon fiber
 474 target; secondly, these photons are then converted to
 475 electron/positron pairs; and, finally, the beam energy is
 476 selected with dipole magnets and collimators. In add-
 477 tion, DESY gives acces to a bore 1 T solenoid, the
 478 PCMag.

479 A photograph showing the SiW-ECAL technological
 480 prototype setup can be seen in Figure 10. Current proto-
 481 type consists on 7 layers of SLABs housed by a PVC
 482 and aluminum structure that can hold up to 10. For the
 483 beam test described in Section 4 all the layers were sep-
 484 arated by equal distances of 15 mm except the last one
 485 which was at 60 mm of its nearest. In the following sec-
 486 tions, we will refer to layers number 1 to 7, where the 1
 487 is the closest to the beam pipe and 7 is the farthest. The
 488 detector was exposed to a positron beam in the DESY
 489 test beam area (line 24). By means of an external pulse

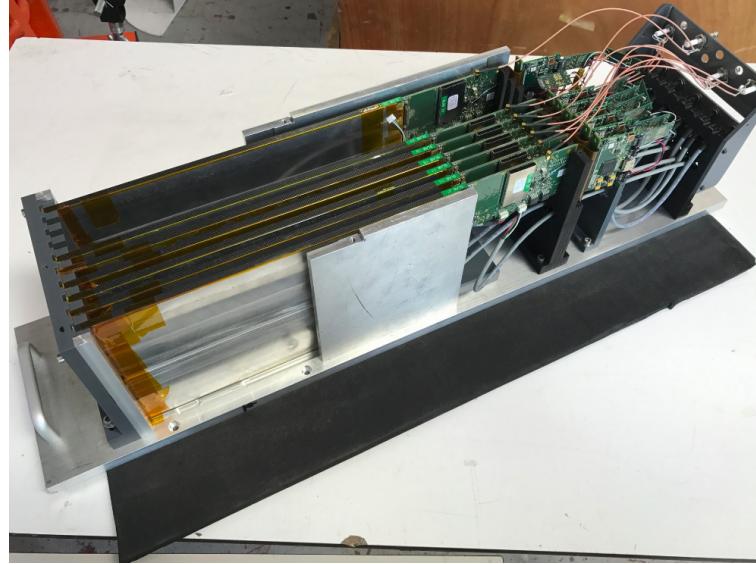


Figure 10: Prototype with 7 layers inside the aluminum stack.

460 generator we defined the length of the acquisition win-
 461 dows to be 3.7 ms at a frequency of 5 Hz. The detector
 462 was running in power pulsing mode without any extra
 463 active cooling system.

464 The physics program of the beam test can be summa-
 465 rized in the following points:

1. Calibration without tungsten absorber using 3 GeV positrons acting as minimum ionizing particle (MIPs) directed to 81 position equally distributed over the modules.
2. Test in magnetic field up to 1 T using the PCMag. For this test a special PVC structure was designed and produced to support one single SLAB. The purpose of such test was twofold: first to prove that the DAQ, all electronic devices and the mechanical consistency of the SLAB itself are able to handle strong magnetic fields; second to check the quality of the data and the performance of the detector during the data taking when running in a magnetic field.
3. Response to electrons of different energies with fully equipped detector, i.e. sensitive parts and W absorber, with three different repartitions of the absorber material:
 - W-configuration 1: 0.6, 1.2, 1.8, 2.4, 3.6, 4.8 and $6.6 X_0$
 - W-configuration 2: 1.2, 1.8, 2.4, 3.6, 4.8, 6.6 and $8.4 X_0$
 - W-configuration 3: 1.8, 2.4, 3.6, 4.8, 6.6, 8.4 and $10.2 X_0$

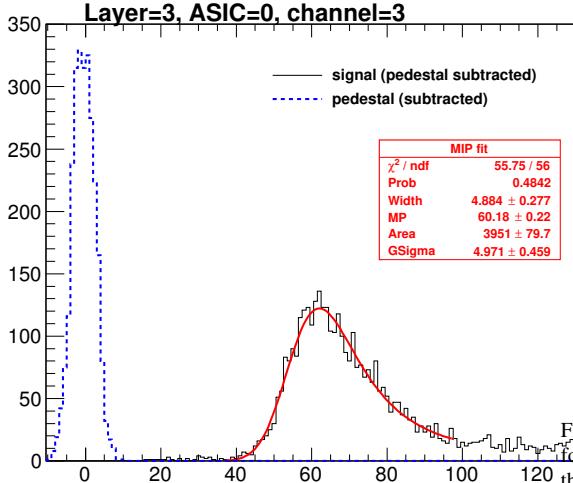


Figure 11: Pedestal (blue dashed line) and signal (black continuous line) distribution for one channel in the third layer.

First reports on this beam test can be find in Refs. [? ?]. In this paper we discuss in more detail the results of the pedestal, noise and MIP calibration in Section 4.1. We show also results on the pedestal and noise stability when running inside a magnetic field in Section ???. Finally, a first peek to the response and stability of the detector in electromagnetic showers events is discussed in Section 4.3.

4.1. Response to MIP-acting positrons

4.1.1. Pedestal and noise determination

The calibration runs have been used to calculate the pedestal distribution reference values and the noise levels (the width of the pedestal distribution) of each channel. In Figure 11 we show the signal and pedestal distribution of a single channel after subtracting the pedestal mean position. The results of the MIP calibration fit are included (red) and explained in the next version. The pedestal distribution is shown only for the first SCA to keep the y-axis within a reasonable range. The signal distribution is integrated over all SCAs.

The pedestal is calculated as the mean position of the ADC distribution of channels without trigger. The noise is associated to the width of such distribution. The pedestal correction is done layer-, chip-, channel- and SCA-wisely due to the large spread of values between pedestals, as observed in Figure 12 (left plot) and Figure 13 (also left plot). For the noise, the dispersion is much smaller ($\sim 5\%$). This is shown in the right plots of Figures 12 and 13. From now on, the pedestal correction is

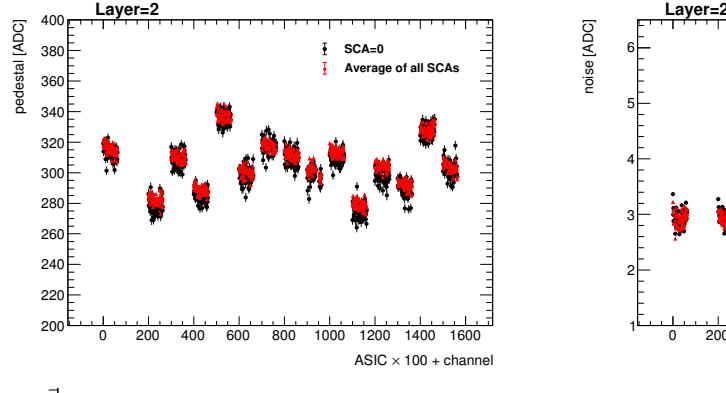


Figure 12: Pedestal mean position (upper plot) and width (lower plot) for all channels in one layer. The data is grouped on bunches in which the value in the x-axis corresponds to the value of the channel number charge [ADC] value of the ASIC number multiplied by 100. The black points show the value for the first SCA and the red points show the average value for all the others SCAs (with the standard deviation of the sample as error bar).

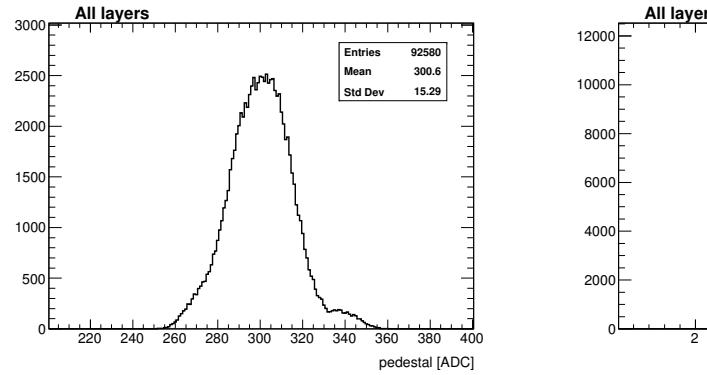


Figure 13: Pedestal mean position (left) and width (right) for all channels and all SCAs in the setup.

applied to all the results presented.

4.1.2. Energy calibration and tracking efficiency

A Landau function convoluted with a Gaussian is fit to the resulting hit distribution. The most-probable-value of the convoluted function is taken as the MIP value, allowing thus for a direct conversion from ADC units to energy in MIP units. We have obtained a raw energy calibration spread of the 5% among all channels with the 98% of all available channels being fitted. Results are summarized in figure 14, leftmost plot.

We checked the MIP calibration in all calibrated channels by selecting tracks incident perpendicularly to the layers surface. The results are shown in figure 15 where the single channel energy distribution for MIPs

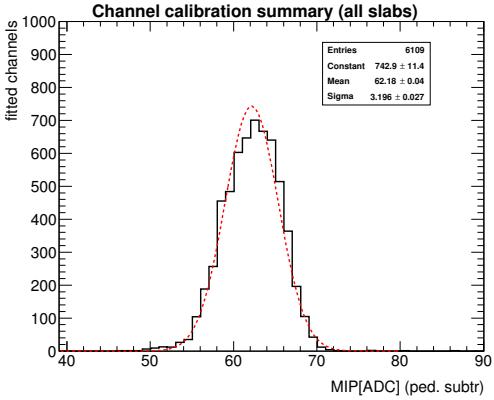


Figure 14: Result of the MIP position calculation and signal over noise calculation for all calibrated channels.

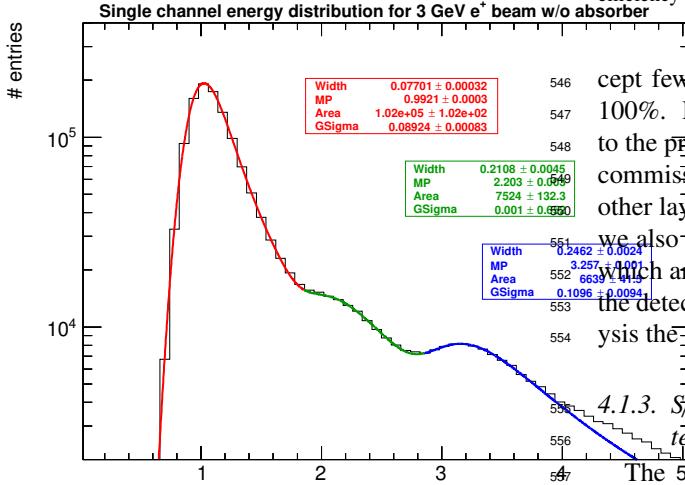


Figure 15: Energy distribution for all calibrated channels when selecting tracks of 3 GeV positron acting as MIPs.

is shown for all calibrated channels in the same distribution. The maximum peaks at 1 MIP as expected after a good calibration. In addition to this, a second and a third peak appear visible. These peaks are due to events involving multiple particles crossing the detector.

To evaluate the single hit detection efficiency we define a high purity sample of events by selecting tracks with at least 4 layers with a hit in exactly the same channel. Afterwards we check if the other layers have or not a hit in the same channel (expanding the search to the closest neighbouring channels) with energy larger or equal than 0.3 MIP. Finally, we repeat this for all layers and channels. The results are shown in Figure 16. Ex-

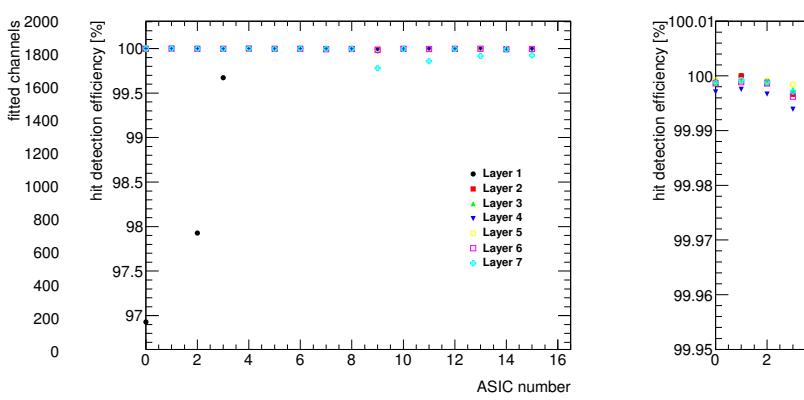


Figure 16: Left: MIP detection efficiency for all layers and ASICs in high purity samples of tracks of MIP-like acting particles. Right: same figures with a zoom in the y-axis. In both cases, the average efficiency of the 64 channels in each ASIC is shown.

cept few exceptions, the efficiency is compatible with 100%. Lower efficiencies in the first layer are related to the presence of noisy channels not spotted during the commissioning. In the last layer (separated from the other layers by four slots of 1.5 cm instead of only one) we also observe few small deviations from the ~ 100% which are indeed associated to a slight misalignment of the detector. If we remove these channels from the analysis the full efficiency is recovered.

4.1.3. S/N ratio in the charge measurement for MIP interactions

The signal-over-noise ratio in the charge measurement (corresponding to the slow shaper of the SKIROC2) is defined as the ratio between the most-probable-value of the Landau-gauss function fit to the data (pedestal subtracted) and the noise (the pedestal width). This quantity has been calculated for all channels and all layers. The average S/N is to 20.4. Results are summarized in Figure 14, rightmost plot.

4.2. Pedestal and noise stability in a magnetic field

The data taking inside the magnetic field has been divided in three steps: a) a with a magnetic field of 1 T; b) a run with 0.5 T; c) a final run with the magnet off. The beam, 3 GeV positrons, was hitting in the area of the PCB readout by the ASIC number 12.

The pedestal positions and noise levels of the channels of the ASIC 12 when the SLAB is inside of the PC-Mag are compared with the results from the calibration run described in the previous section. This is shown in Figure 17. We see that the agreement is perfect within

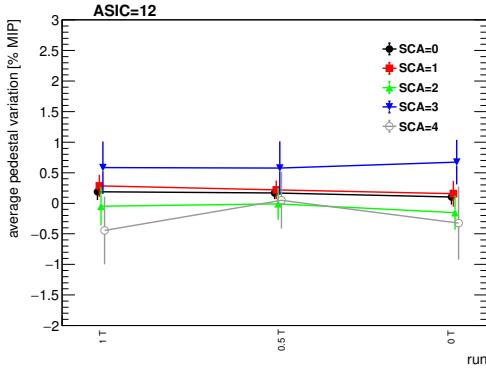


Figure 17: Average deviation of the pedestal mean position (left) and width (right) for all channels in the ASIC 12.

576 the statistical uncertainties. Due to the lower rates in this
577 beam area, the analysis is only done up to few SCAs.

578 4.3. Pedestal stability in electromagnetic shower events

In this section we discuss the pedestal stability in events with large amount of charge collected by the ASICs, as are the electromagnetic shower events. All the results shown in this section correspond to data taken during the tungsten program, using the W-configuration number 2 when shooting the beam in the area registered by the ASIC 12 (and partially in the 13). Only information recorded by ASIC 12 is used in the analysis. For other configurations we get comparable results. In order to select a high purity of electromagnetic shower like the events, we used a simple criteria: select only events with at least 6 of the layers with at least a hit with $E \geq 0.5$ MIP.

Two main observations have been extracted from the recalculation of the pedestals and its comparison with the values obtained previously during the calibration runs. The first observation consists in a relatively small drift of the pedestal values towards lower values when the collected energy is high (or when the number of triggered channels is large). This is shown in Figure 18 for several SCAs where the average of the projection of the pedestal distribution for all channels non triggered in ASIC 12 of layer 3 is plot as a function of the total energy measured by the ASIC (or the total number of hits). We see that in both cases, the shapes of the curves for each SCA are very similar. This feature is known and it is due to the architecture of the SKIROC2 ASICs where high inrush of currents can slightly shift the baseline of the analogue power supply.

The second observation extracted from this analysis can be also seen in Figure 18 but more clearly in Figure

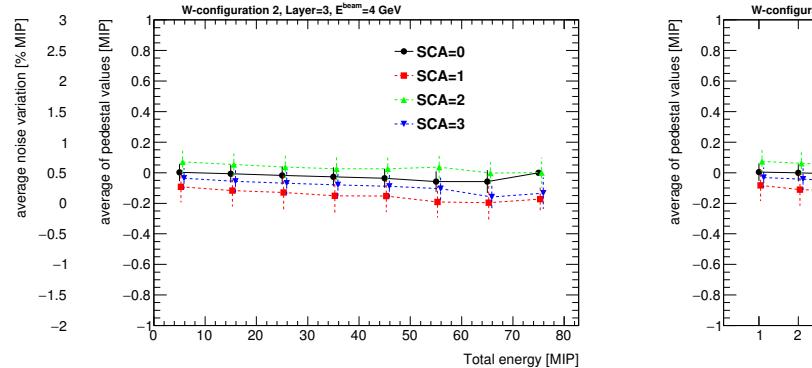


Figure 18: Left: mean position of the projection of the pedestal distribution of all channels calculated when different energies are collected in the ASIC (in bins of 10 MIPs). Right: same but as a function of the number of hits. In both cases, the results are shown for few SCAs. The points for the curves with SCA larger than zero are slightly shifted in the x-axis to optimize the visualization.

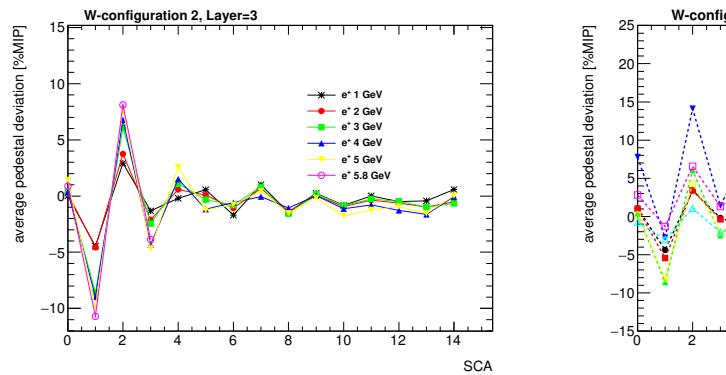


Figure 19: Left: average value on each SCA of the calculated pedestals for all channels of ASIC 12 in the Layer 3 for different energies of the beam. Right: same but fixing the energy of the beam and comparing several layers.

610 19: in addition to the small drift of the pedestal value
611 an SCA-alternate global shift is observed. We see that
612 the effect is enhanced when large amounts of charge are
613 deposited in the ASIC (*i.e.* at larger beam energies or
614 for the layers in the maximum of the shower profile).
615 We also observed that this alternation is only SCA de-
616 pending and does not depends on the time in which the
617 deposit of energy occurs within the acquisition. This is
618 not yet fully understood although the fact that the effect
619 is observed in alternate SCAs hints that something is af-
620 fecting to the digital part of the ASIC (where the SCAs
621 enter in play). Dedicated tests in the laboratory and in
622 the beam are needed in order to clarify this issue.

623 **5. Summary**

624 The R&D program of the highly granular SiW-ECAL
625 detector is in an exciting phase. After the proof of
626 principle of the imaging calorimetry concept using the
627 physics prototype, the technological prototype is being
628 constructed and tested. In this document we describe
629 the commissioning and beam test performance of a pro-
630 totype built in with the first fully assembled detector el-
631 ements.

632 A very comprehensive and detailed commissioning
633 procedure has been established and optimized allowing
634 us to identify and isolate the different noise sources that
635 could spoil the data taking. The beam test has provided
636 a lot of useful data to study the performance of the de-
637 tector and to perform a channel by channel calibration.
638 A full analysis of the MIP calibration within magnetic
639 field and the response of the prototype in electromag-
640 netic shower events will be covered in a future docu-
641 ment. In addition, the results shown here serve as input
642 for ongoing and future R&D.

643 **6. Outlook**

644 In parallel to the work described here, several R&D
645 efforts are being carried. One of these efforts is directed
646 to the design and test of new ASICs. In fact, a new gen-
647 eration of SKIROC2, the 2a, has been delivered and it is
648 being tested in the dedicated testboards and it has been
649 integrated in new ASUs. In addition, a new generation
650 of the ASIC, SKIROC3, is foreseen for the final detec-
651 tor construction. In contrast with SKIROC2/2a, the new
652 ASIC will be fully optimized for ILC operation, *i.e.* full
653 zero suppression, reduced power consumption etc.

654 Many efforts are also concentrated in the construc-
655 tion and test of long SLABs made of several ASUs en-
656 chained since we know that the ILD ECAL will host
657 long layers of up to ~ 2.5 m. This device constitutes a
658 technological challenge in both aspects, the mechan-
659 ical (very thin and long structure with fragile sensors
660 in the bottom, complicated assembly procedure...) and
661 the electrical (*i.e.* transmission of signals and high cur-
662 rents). For example, interconnections between ASUs
663 and between ASU and interface card are one of the most
664 involved parts of the assembly and require close collab-
665 oration between mechanical and electronic engineers.
666 The construction and test of a long SLAB prototype of
667 ~ 8 ASUs is currently ongoing.

668 In parallel to the ASUs equipped with BGA packaged
669 ASICs, a different proposal for the ASU design is be-
670 ing investigated. This is motivated by the high density
671 of channels demanded by the Particle Flow algorithms.

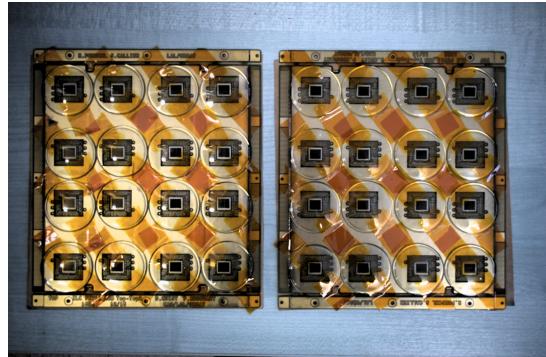


Figure 20: Two FEV11_COB boards with 16 SKIROC2a wire bonded. The ASICS are protected with watch glasses.

672 Indeed, the FEV11 thickness is 1.6 alone and 2.7 mm
673 including the ASICS in its current packaging: 1.1 mm
674 thick LFBGA package. In this alternative PCB design
675 the ASICS are directly placed on board of the PCB in
676 dedicated cavities. The ASICS will be in semiconduc-
677 tor packaging and wire bonded to the PCB. This is the
678 so-called COB (chip-on-board) version of the ASU. A
679 small sample of FEV11_COBs (same connexion pat-
680 tern with the interface card than FEV11) with a total
681 thickness of 1.2 mm allowing for a potential denisty of
682 10000 channels/dm³ has been produced and tested in
683 the laboratory showing its readiness for tests with parti-
684 cle beams. A sample can be seen in Figure 20.

685 Finally, many efforts in the compactification of the
686 DAQ and the ASUs (*i.e.* the chip on board versions of
687 the ASUs described in Section 2.3) are being conducted
688 by the SiW-ECAL collaboration.

689 It is foreseen that all these developments, with the
690 exception of the SKIROC3, will be tested with particle
691 beams during 2018-2019.

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706 The measurements leading to these results have been 753
707 performed at the Test Beam Facility at DESY Ham- 754
708 burg (Germany), a member of the Helmholtz Associa- 755
709 tion (HGF). 756

710 Appendix A. Appendix: Filtering of fake triggers

711 Several types of fake signals have been observed in 760
712 the technological prototype since its construction and 761
713 test. A detailed description of them can be found in 762
714 previous articles, as for example, in Ref. [?]. All 763
715 these 764
716 fake 765
717 signals 766
718 are 767
719 easily 768
720 identified 769
721 and 770
722 tagged 771
723 during 772
724 the 773
725 data 774
726 acquisition 775
727 the 776
728 rising 777
729 edge 778
730 of 779
731 the 780
732 OR64 781
733 size by a factor X.

722 *Empty triggers*

723 Empty trigger events are a well known feature of 772
724 SKIROC2. The SKIROC2 uses an OR64 signal to mark 773
725 the the change to a new SCA when a signal over thresh- 774
726 old is detected. The empty triggers appear when during 775
727 the acquisition the rising edge of the slow clock falls 776
728 during the OR64 signal and therefore the change to a 777
729 new SCA is validated twice. This effect creates around 778
730 10-15% of empty events which are easily filter and 779
731 removed from the analysis. **The ratio of empty triggers in 780
732 the new SKIROC2a is reduced to the ~ 3% thanks to to 781
733 a decrease of the OR64 size by a factor X.**

734 *Plane events and retriggers*

735 Another well known issue is the appearance of bunches 772
736 of consecutive fake triggers, called retriggers, that 773
737 saturates the DAQ. These events are also characterized by 774
738 triggering many channels (some times even all channels 775
739 of an ASIC) at the same time. Although the ultimate 776
740 reason of the appearance of these events remains un- 777
741 known we think that they may be related to some 778
742 distortion of the power supply baselines. We know that 779
743 the SKIROC2 and 2a preamplifiers are referenced to the 780
744 analog power supply level, therefore, any voltage dip 781
745 can be seen as signal by the preamplifiers. The presence 782
746 of a high inrush of current due to many channels trig- 783
747 gered at the same time can create these voltage dips and 784
748 produce the so called plane events (most of the chan- 785
749 nels triggered at once). In previous studies (*i.e.* reference 786
750 [?]), the ratio of retriggers and plane events was re- 787
751duced by improving the power supply stabilization 788
752 capacitors. It is important to remark that all layers and 789

753 all ASICs analog and digital levels are powered using 754
754 the same power supply. Moreover, the high voltage 755
755 power supply for the polarization of the PIN diode it is 756
756 also common for all layers. Therefore any noise in these 757
757 power supplies or any overload of an ASIC may partic- 758
758 ipate in the creation of fake signals in different ASICs 759
759 and layers.

760 Studying the MIP calibration data of this beam test 761
761 we have noticed that the larger concentration of the re- 762
762 triggers and plane events are originated in ASICs far 763
763 from the beam spot. Even more, hot spots tend to ap- 764
764 pear near the channels 37 and the channels masked as 765
765 suspicious of suffering from routing issues. The amount 766
766 these events have been estimated to be of 1 – 3% in the 767
767 ASICs where high frequency interactions are produced 768
768 (*i.e.* using 3 GeV positrons ate 2-3 KHz) and at higher 769
769 rates even larger than 40% in other ASICs far from the 770
770 beam spot. Moreover, it has been noticed a correlation 771
771 between the time that an ASIC was full and the time 772
772 of the appearance of some retriggers in other areas of 773
773 the PCB. This correlation corresponds to $\sim 1.6 \mu s$ which 774
774 hints of a distortion on the analogue power supply when 775
775 the signal that informs the DIF that one ASIC memory 776
776 is full is transmitted through the PCB.

777 All this information and dedicated studies in the 778
778 laboratory will be used for the improvement of the 779
779 power supplying system, the PCB design and for fur- 780
780 ther SKIROC developments with the possible approval 781
781 the ILC in the scope.