

<sup>2</sup> **Commissioning and performance in beam tests of the**  
<sup>3</sup> **highly granular SiW-ECAL technological prototype for the**  
<sup>4</sup> **ILC**

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<sup>6</sup> **ABSTRACT:** High precision physics at future colliders as the International Linear Collider (ILC)  
<sup>7</sup> require unprecedented high precision in the determination of the energy of final state particles.  
<sup>8</sup> The needed precision will be achieved thanks to the Particle Flow algorithms (PF) which require  
<sup>9</sup> compact, highly granular and hermetic calorimeters systems. The Silicon-Tungsten Electromagnetic  
<sup>10</sup> Calorimeter (SiW-ECAL) technological prototype design and R&D is tailored to the baseline design  
<sup>11</sup> of the ECAL of the International Large Detector (ILD) for the ILC. In this document we present  
<sup>12</sup> the latest news on R&D of such prototype with fully embedded very front-end (VFE) electronics.  
<sup>13</sup> Special emphasis is given to the presentation and discussion of the commissioning of the prototype  
<sup>14</sup> for beam test and to the performance of the device in such beam test carried at DESY in June 2017.

<sup>15</sup> **KEYWORDS:** Calorimeter methods, calorimeters, Si and pad detectors

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16	<b>Contents</b>	
17	<b>1 Introduction</b>	<b>1</b>
18	<b>2 The SiW-ECAL technological prototype</b>	<b>3</b>
19	2.1 Silicon sensors	3
20	2.2 SKIROC: Silicon pin Kalorimeter Integrated ReadOut Chip	4
21	2.3 Active Sensor Units	4
22	2.4 Data AcQuisition system	5
23	2.5 Setup	7
24	<b>3 Commissioning of the detector</b>	<b>7</b>
25	3.1 Optimization of noise levels	8
26	3.2 Threshold determination	9
27	3.3 S/N ratio in the trigger line	11
28	3.4 Prospects	12
29	<b>4 Performance on positron beam test at DESY</b>	<b>14</b>
30	4.1 Pedestal and noise studies with the SiW-ECAL in tracker mode	15
31	4.1.1 Pedestal and noise in large magnetic fields	15
32	4.2 MIP response and tracking efficiency with the SiW-ECAL in tracker mode	18
33	4.2.1 S/N ratio in the ADC	19
34	4.3 Pedestal stability in electromagnetic shower events	19
35	4.4 Fake triggers filtering	21
36	<b>5 Summary and prospects</b>	<b>22</b>

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37 **1 Introduction**

38 Future accelerator based particle physics experiments require very precise and detailed reconstruc-  
39 tion of the final states produced in the beam collisions. A particular example is the next generation  
40 of  $e^+e^-$  linear colliders such the ILC[1–5]. This project will provide collisions of polarized beams  
41 with centre-of-mass energies (*c.m.e*) of 250 GeV - 1 TeV. These collisions will be studied by two  
42 multipurpose detectors: the International Large Detector (ILD) and the Silicon Detector (SiD)[5].  
43 Another example of an  $e^+e^-$  collider project is the Compact Linear Collider (CLIC) project[6–8]  
44 which will produce collisions with *c.m.e* of 380 GeV - 3 TeV with a detector featuring similar  
45 design than the ILD and SiD. Both projects will explore with unprecedented precision the origin of  
46 the electroweak symmetry breaking and new physics beyond the standard model by exploring final  
47 states with heavy bosons (W, Z and H) and fermions (*i.e.* heavy quarks as *c*, *b* and *t*).

48 It is known that in a *classical* typical multipurpose detector of a collider experiment the  
49 charged particles momentum is better measured by the tracking system the photons energy are only  
50 observed in the calorimeter system (mainly in the electromagnetic) if they are not converted and  
51 the measurement of the neutral hadrons energy can only be done by involving the full calorimeter  
52 systems. To meet the required precision levels by the ILC or CLIC physics goals, new techniques  
53 relying on single particle separation to make possible the choice of the best information available  
54 in the full detector to measure the energy of the final state objects have been developed. These  
55 techniques are called Particle Flow (PF) techniques [9–11] and allow to reduce the impact of the  
56 poor resolution of the calorimeter systems (compared with trackers) in the overall reconstruction.  
57 For this purpose, detectors optimized for PF algorithms have some requirements. Some of them are  
58 summarized here:

- 59 • a highly efficient and "transparent" tracking system between the interaction point and the  
60 calorimetry systems;
- 61 • highly granular (*imaging calorimetry*) and compact calorimeter systems featuring minimum  
62 dead material;
- 63 • and high power of particle separation<sup>1</sup>.

64 The R&D of highly granular calorimeters for future linear colliders is conducted within the  
65 CALICE collaboration and, for now on, we refer the reader to [11] for further information about PF  
66 and the CALICE R&D.

67 In this document we will focus in the description of the silicon-tungsten electromagnetic  
68 calorimeter, SiW-ECAL, its commissioning and its performance in beam test. The SiW-ECAL is  
69 the baseline choice for the ILD ECAL. It consists in a detector (in the barrel region) of 24  $X_0$  of  
70 thickness which corresponds to  $\sim 1 \lambda_I$  (interaction length). It has silicon (Si) as active material and  
71 tungsten (W) as absorber material. The combination of Si and W choices makes possible the design  
72 and construction of a very compact calorimeter with highly granular and compact active layers.  
73 It will consist of an alveolar structure of carbon fiber into which modules called SLABs made of  
74 tungsten plates and the active sensors will be inserted. The very-front-end (VFE) electronics will  
75 be embedded in the SLABs. The silicon sensors will be segmented in squared cells (or channels)  
76 of 5x5 mm: a total of  $\sim 100$  million channels will constitute the ECAL for ILD. The desired  
77 signal dynamic range in each channel goes from 0.5 MIP to 3000 MIPs. To reduce overall power  
78 consumption, the SiW-ECAL will exploit the special bunch structure foreseen for the ILC: the  $e^+e^-$   
79 bunches trains will arrive within acquisition windows of  $\sim 1\text{--}2$  ms width separated by  $\sim 200$  ms.  
80 During the idle time, the bias currents of the electronics will be shut down. This technique is usually  
81 denominated power pulsing. In addition to this, to cope with the large amount of channels, the  
82 calorimeters should work in self-trigger mode (each channel featuring an internal trigger decision  
83 chain) and zero suppression mode.

84 The first SiW-ECAL prototype was the so called SiW-ECAL physics prototype. It was suc-  
85 cessfully tested at DESY, FNAL and CERN running in front of another prototype from the CALICE

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<sup>1</sup> For that reason the calorimeter systems at ILD will be placed inside the magnetic coil providing magnetic fields of 3.5 T

86 collaboration, the analogue hadronic calorimeter AHCAL, delivering the proof of concept of PF  
87 calorimetry. For the physics prototype, the VFE was placed outside the active area with no particular  
88 constraints in power consumption. It consisted of 30 layers of Si as active material alternated with  
89 tungsten plates as absorber material. The active layers were made of a matrix of 3x3 Si wafers.  
90 Each of these wafers was segmented in matrices of 6x6 squared pixels of  $1 \times 1 \text{ cm}^2$ . The prototype  
91 was divided in 3 modules of 10 layers with different W depth per layer in each of these modules  
92 ( $0.4, 1.6$  and  $2.4 X_0$ ) making a total of  $24 X_0$ . Published results proving the good performance of  
93 the technology and the PF can be found in references [12–17].

## 94 2 The SiW-ECAL technological prototype

95 The new generation prototype is called the SiW-ECAL technological prototype and it addresses the  
96 main technological challenges: compactness, power consumption reduction through power pulsing  
97 and VFE inside the detector close to real ILD conditions. It will also provide data to deeply study  
98 the PF and provide input to tune the Monte Carlo programs.

### 99 2.1 Silicon sensors

100 The sensors consist on float zone silicon wafers  $320 \mu\text{m}$  thick with high resistivity (larger than  $5000$   
101  $\Omega \cdot \text{cm}$ ). The size of the wafer is  $9 \times 9 \text{ cm}^2$  featuring an array of  $256$  PIN diodes of  $5 \times 5 \text{ mm}^2$ . A  
102 MIP traversing the PIN parallel to its normal will create  $\sim 80 h^+ e^-$  pairs per  $\mu\text{m}$  which corresponds  
103 to  $4.1 \text{ fC}$  if the particle traverses the  $320 \mu\text{m}$  perpendicularly to its larger surface.

104 The original design of the silicon wafers included an edge termination made of floating guard-  
105 rings. It was observed in beam tests [18, 19] that the capacitive coupling between such floating  
106 guard-rings and the pixels at the edge was not negligible in tests with high energy beams (pions and  
107 electrons with energies larger than  $20\text{-}40 \text{ GeV}$ ). This coupling lead to fake events in which, at least,  
108 the channels in the four edges of the wafer are triggered at the same time. This is why these events  
109 are so often called squared events. An R&D program together with Hamamatsu Photonics (HPK  
110 Japan) was conducted to study the guard-rings design as well as the internal crosstalk. As outcome  
111 of this R&D program, the technological prototype is equipped with silicon wafers with:

- 112 • N wafers type-X with guard-rings of XXX characteristics (continuous, segmented, segmented  
113 smaller??)
- 114 • N wafers type-Y without guard rings and the width of the peripheral dead areas lower than  
115  $500 \mu\text{m}$  thanks to the use of stealth dicing technique.

116 For the wafers type-Y, the amount of squared events is expected to be reduced by, at least, a  
117 factor XXX. In both cases, for interaction with low energy particles as the delivered at the DESY  
118 beam test facility (see Section 4) the amount of squared events is expected to be negligible, therefore  
119 we will not do any differentiation of our results depending on the wafer type mounted in the detector.

120 **Is this needed? If so, what are the right plots to show?** Before the assembly of the sensors in  
121 the detector, these are characterized one-by-one by measuring the leakage current (of the order of  
122  $1 \text{ nA}$  per single diode) as a function of the bias voltage (I-V curve), the full depletion voltage (of  
123  $40 \text{ V}$ ) extracted from C-V curve and the stability in time (leakage current versus time at a nominal  
124 bias).



**Figure 1.** I-V curve, C-V curve, leakage current vs time. **Temporary picture:** Triptic La Esperanza del Condenado, J. Miró

## 125 2.2 SKIROC: Silicon pin Kalorimeter Integrated ReadOut Chip

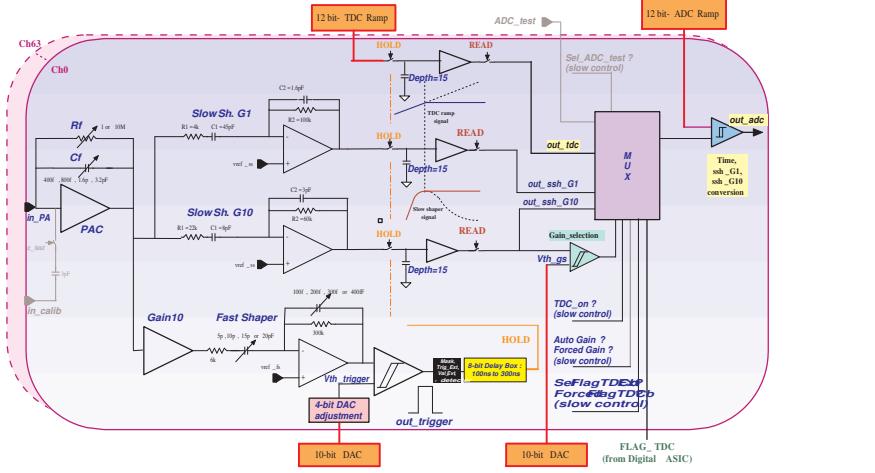
126 SKIROC[20] (Silicon pin Kalorimeter Integrated ReadOut Chip) is the very front end ASIC  
 127 (application-specific integrated circuits) designed for the readout of the Silicon PIN diodes. In  
 128 its version SKIROC2 (and 2a) it consists of 64 channels in AMS 0.35  $\mu\text{m}$  SiGe technology. Each  
 129 channel comprises a low noise charge preamplifier of variable gain followed by two lines: a fast  
 130 shaper for the trigger decision and a set of dual gain slow shaper for charge measurement. The gain  
 131 can be controlled by modifying the feedback capacitance during the configuration of the detector.  
 132 With the slowest gain, 6pF, the ASIC will handle a linear dynamic range from 0.1 to up to 1500  
 133 MIPs (a slightly less than the desired final value for the ILC). Finally, a Wilkinson type analogue to  
 134 digital converter fabricates the digitized charge deposition that can be readout. Once one channel is  
 135 triggered, the ASIC reads out all 64 channels adding a bit of information to tag them as triggered or  
 136 not triggered and the information is stored in 15 cell deep physical switched capacitor array (SCA).  
 137 The trigger threshold can be controlled both globally and locally (channel by channel) although the  
 138 dynamical range for the channel by channel option is too small in the SKIROC version 2 due to a  
 139 mistake in the development. This issue has been solved in the SKIROC2a. The trigger holds the  
 140 voltage of the two slow shapers with a tunable delay and also holds the voltage swept with the slow  
 141 clock trigger to obtain timing information.

142 The SKIROC ASICs can be power-pulsed by taking advantage of the ILC spill structure: the  
 143 bias currents of the ASIC can be switched off during the idle time between bunch trains. With this  
 144 method, the ASIC is able to reduce its power consumption down to 25  $\mu\text{W}$  per channel, meeting the  
 145 ILC requirements. All the results shown in this paper are obtained using the power pulsing feature.

146 Every ASU of the SiW-ECAL prototype is equipped with 16 SKIROCs version 2. A newer  
 147 version, 2a, with some incremental improvements and bug fixing has been produced and will be used  
 148 to equip new layers currently in production. In addition, a new generation of the ASIC, SKIROC3,  
 149 is foreseen for the final detector construction. In contrast with SKIROC2/2a, the new ASIC will be  
 150 fully optimized for ILC operation, *i.e.* full zero suppression, reduced power consumption etc.

## 151 2.3 Active Sensor Units

152 The entity of sensors, thin PCB (printed circuit boards) and ASICs is called Active Signal Units  
 153 or ASU. An individual ASU has a lateral dimension of 18x18 cm<sup>2</sup> and has glued onto it 4 silicon  
 154 wafers (currently with a thickness of 320  $\mu\text{m}$ ). The high voltage is delivered to the wafers using a  
 155 HV-kapton sheet that covers the full extension of the wafers. The ASUs are equipped further with



**Figure 2.** The schematics of the analog part of SKIROC2. High-stack picture (right bottom corner)

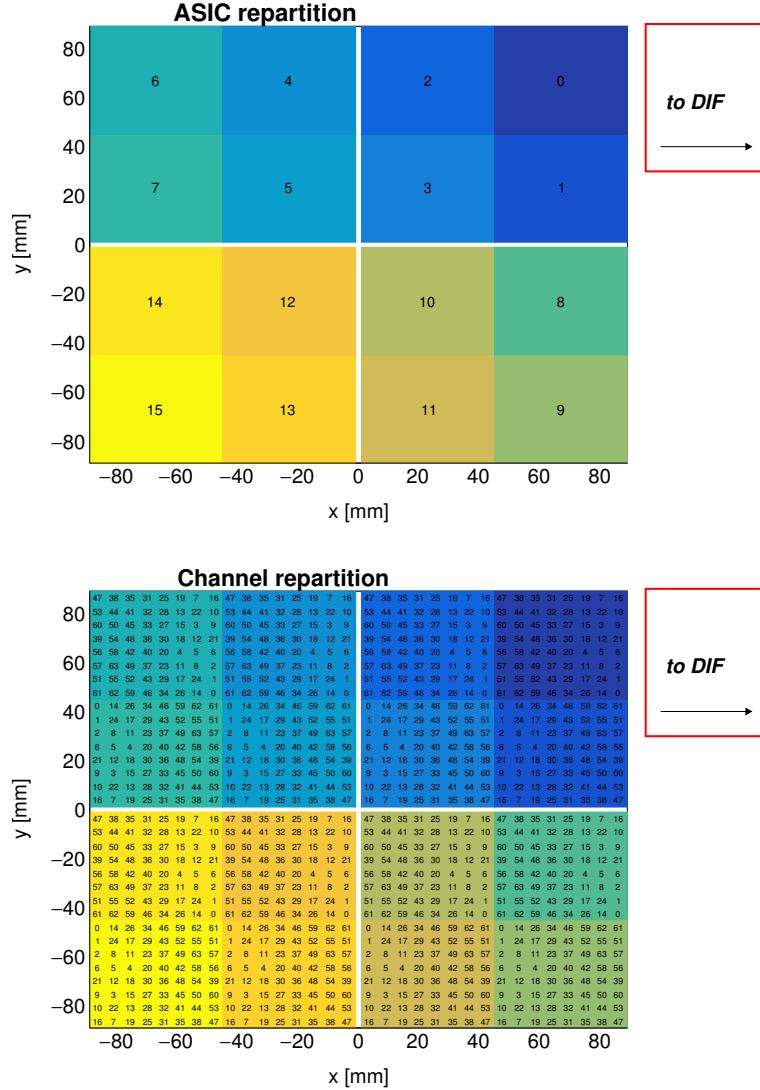
156 16 ASIC for the read out and features 1024 square pads (64 per ASIC) of 5x5 mm. The channels  
 157 and ASICs are distributed along the ASU as shown in Figure 4

158 The readout layers of the SiW-ECAL consist of a chain of ASUs and an adapter board to a data  
 159 acquisition system (DAQ) at the beginning of the layer. This adapter board is called SMBv4 and it  
 160 also serves as a place to sit the power connectors (low voltage to power the analog and digital parts  
 161 of the ASIC and high voltage to bias the PIN diodes) and the super capacitances used for the power  
 162 pulsing. These capacitances of 400mF with 16 mΩ of equivalent serial resistance. The purpose of  
 163 these capacitances is to provide local storage of the necessary charge to avoid the transport of current  
 164 pulses over long cables, ensuring in this way the stability of the ASICs during the acquisition.

165 Currently, the technological prototype layers are built with version of PCB called FEV11 with  
 166 16 SKIROC (see Section 2.4). The FEV11 thickness is 1.6 alone and 2.7 mm including the ASICs  
 167 in its current packaging: 1.1 mm thick LFBGA package. Figure 1 (left) shows a picture of a full  
 168 equipped short slab with FEV11 ASU. There are ongoing R&D activities in an alternative PCB  
 169 design in which the ASICs are directly placed on board of the PCB in dedicated cavities. The  
 170 ASICs will be in semiconductor packaging and wire bonded to the PCB. This is the so-called COB  
 171 (chip-on-board) version of the ASU. A small sample of FEV11\_COBs (same connexion pattern  
 172 with the interface card than FEV11) with a total thickness of 1.2 mm has been produced and tested  
 173 in the laboratory showing its readiness for tests with particle beams. A sample can be seen in Figure  
 174 1 (right).

## 175 2.4 Data AcQuisition system

176 The design of the subsequent chain of the data acquisition (DAQ)[21] system is inspired by the  
 177 ILC. Current DAQ consists of three modules which are designed to be generic enough to cope  
 178 with other applications. The first module is the so called detector interface (DIF) which is placed  
 179 at the beginning of each layer holding up to 15 ASUs. All DIFs are connected by single HDMI  
 180 cables to the concentrator cards: Gigabit Concentrator Card (GDCC). The HDMI connection is  
 181 used to transmit both slow control and data readout. One GDCC controls up to 7 DIFs collecting  
 182 all data from them and distributing among them the system clock and fast commands. The most



**Figure 3.** Repartition of the ASIC (up) and channels (down) in one ASU. In this perspective, the Si-Sensors are glued in the back. The channels are separated (in x and y) by 5.5 mm. The empty cross in the middle of the ASU corresponds to the 1 mm separation between the sensors. The ASICs and channels are labeled with numbers following design and DAQ criteria: from 0-16 in the case of the ASICs and from 0-63 in the case of the channels.

183 downstream module is the clock and control card (CCC). The CCC provides a clock, control fan-out  
184 of up to 8 GDCCs and accepts and distributes external signals (i.e. spill signals).

185 The whole system is controlled by the Calicoes and the Pyrame DAQ software version 3 [22,  
186 23]. The Pyrame framework provides basic blocks (called modules) of control-command or data  
187 acquisition. Calicoes is specific the implementation of these blocks for control-command and data  
188 acquisition of the SiW-ECAL prototype. This new version of the DAQ software implements a new  
189 mechanism to allow any module to treat and publish data in real time. Those data are made available  
190 to any requesting module, in particular to a new online monitor module developed for this beam



**Figure 4.** Left **Temporary picture: La Esperanza del Condenado, J. Miró:** Open single SLAB with FEV11 ASU, 16 SKIROC, interface card and DIF visibles. The silicon sensors are glued to the PCB in the other side. Right: two FEV11\_COB boards with 16 SKIROC2a wire bonded. The ASICs are protected with watch glasses.

191 test, allowing for quick online checks of the data quality and integrity.

## 192 **2.5 Setup**

193 The prototype tested in beam is composed of 7 layers consisting in one short SLAB each. A short  
 194 SLAB is made of: one single ASU FEV11 equipped with 16 SKIROC2 and 4 wafers glued on the  
 195 other side (1024 channels); an interface card SMBv4; and a DIF. All these elements sit on a "U"  
 196 shape carbon structure to protect the wafers. The full system is then covered by two aluminum  
 197 plates to provide electromagnetic shielding and mechanical stability. The 7 layers are supported by  
 198 a PVC and aluminum structure that in which can be inserted to 10 layers. The distance between  
 199 two layer slots is 15 mm and this space is used to place tungsten plates of different thicknesses. For  
 200 the beam test described in Section 4, the layers were placed in positions 1-6 and 10. During the  
 201 commissioning, the slabs have been tested both inside and outside of the structure. A photograph  
 202 showing the prototype can be seen in Figure 5.

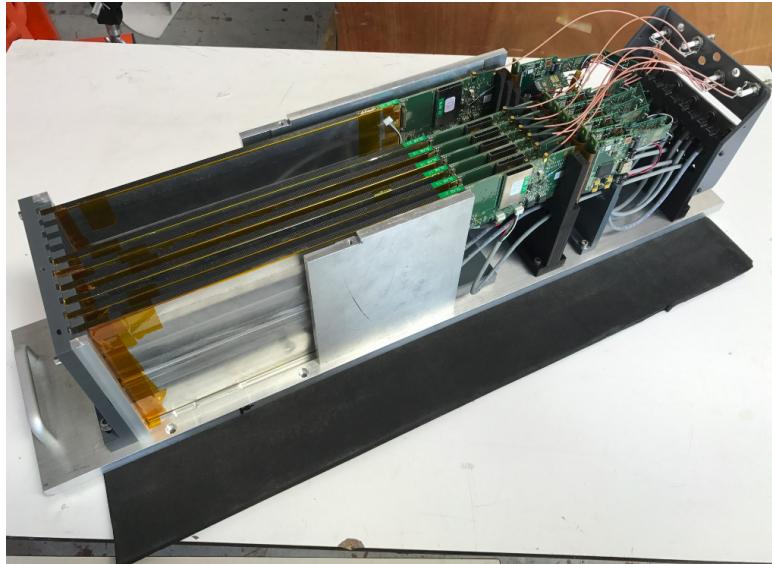
## 203 **3 Commissioning of the detector**

204 This beam test was prepared by a careful and comprehensive commissioning comprising: the debug  
 205 of the single SLABs with special emphasis in the control of the noise and the study of the prototype  
 206 performance in cosmic rays tests.

207 The SKIROC2 has been already commissioned for previous experiences (see for example the  
 208 references [24, 25]). Therefore, all the settings used for the SKIROC2 to obtain the results described  
 209 in this paper are motivated by these previous experiences. For example, the value of 1.2pF for the  
 210 preamplifier. With this gain, the SKIROC2 ensures a linearity better than 90% for 0.5-200 MIPs<sup>2</sup>,  
 211 which is enough for electromagnetic showers created by few GeV electrons or positrons. The delay  
 212 of the trigger signal is the same than in reference [24, 25]: 130 DAC for all ASICs. This value was

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<sup>2</sup>Is this a fact?



**Figure 5.** Prototype with 7 layers inside the aluminum stack.

213 chosen by selecting the delay in which an injected signal of few MIPs of value get the maximum  
214 value of ADC.

### 215 3.1 Optimization of noise levels

216 The purpose of this phase was to monitor and control the noise levels of the prototype. The  
217 commissioning includes the definition of trigger threshold values and a list of noisy channels to be  
218 masked. Studying and control the noise levels is crucial since noisy channels may saturate the DAQ  
219 faster than physical signals. Two different types of noise were identified: randomly distributed in  
220 time noisy channels and noise bursts affecting to all layers at the same time.

221 The first type of noise source (randomly distributed in time) forced us to define a list of channels  
222 to be masked in all layers. Again, two different type of noisy channels have been identified. The first  
223 group is composed by randomly distributed in space channels. The second group is made of a fixed  
224 list of channels, all in the same positions for all SLABs, that were giving underflowed ADC triggers  
225 at high rates. The channels associated to "underflowed-noise" events were identified by means of  
226 the online monitoring tools. Some preliminary inspections of the FEV11 layout hint that the cause  
227 of this "underflowed-noise" events may be in an improvable routing of the lines from the PIN pad to  
228 the SKIROC. For this reason, if a given channel appeared to be associated to "underflowed-noise"  
229 events in one of the SLABs, it was masked in all of them, taking in this way the most conservative  
230 solution. For example, all channels number 37 were masked in all ASICs. More studies in this  
231 respect are to come.

232 The list of the noisy channels randomly distributed in time and space was defined by means of  
233 dedicated data taking runs. These runs were characterized by: their short acquisition windows (of  
234 2.5 ms, only 1.1 ms of effectively data taking time), their low spill frequency (5 Hz) to minimize the  
235 chances of having real events due to cosmic rays hitting the detector during the data taking; and the  
236 relatively high trigger threshold values between 250 and 400 DAC (which is equivalent to ~0.5-2

237 MIP, see Section 3.2 for more information). The full process was an iterative process starting with  
 238 several repetitions of runs at a high threshold value and then some iterations at lower threshold each  
 239 up to 250 DAC. In every of there iterations, the channels identified as noisy were masked. A full run  
 240 involved 3-5 threshold values and at least two repetitions per value. Again, we decided to follow a  
 241 conservative approach for list the noisy channels to be masked: if the channel was triggered at rates  
 242 larger than 0.5-1% of the total number of triggers per ASIC it was added to the list.

243 In addition to the different noisy channel types described above, we also have masked full  
 244 sectors of the SLABs if an ASIC was faulty (at least 70% of channels listed as noisy) or if a Si-wafer  
 245 was misworking (high leakage currents). In these cases and in all mentioned above, the masking  
 246 involved two steps: disabling of the trigger and the disabling of the power of the preamplifier of  
 247 that channel. A summary of the results of the masking procedure is shown in Figure 6.

248 We observed that the noise bursts happening coherently at the same time in all SLABs was  
 249 associated to cases when the electrical isolation between SLABs was broken. This is a hint of a  
 250 system effect as can be the appearance of grounding loops or noise in the power supplies. The issue  
 251 was circumvented by improving the electrical isolation of single layers. We have also observed that  
 252 the noise bursts happened only at the end of long acquisitions therefore, in addition to the improved  
 253 isolation, we selected short enough acquisitions windows (which indeed are the most appropriate to  
 254 the high rates of particles in the DESY beam). However, more studies in the laboratory are needed  
 255 in order to fully understand these issues.

## 256 3.2 Threshold determination

257 Once that the SKIROC main settings have been fixed and the masking of the noisy channels at a  
 258 relatively high threshold value has been done, the final step is the selection of the optimal trigger  
 259 threshold values. For that, we perform dedicated runs in which we scan a reasonable range of  
 260 trigger threshold values (in DAC units) with all channels enabled (excepted the marked as noisy).  
 261 For each of the DAC points we took data only during  $\sim 1$  minute per DAC in order to speed up  
 262 the commissioning. Plotting the total number of hits normalized to the maximum vs the DAC for  
 263 each channel gives the so-called S-curves. In the absence of external signals (cosmic rays, injected  
 264 signals, etc) these noise S-curves show the convolution of the envelope of the electronic noise at  
 265 the output of the fast shaper (the trigger decision line). Indeed, the size of this envelope is related  
 266 to the slow clock frequency (larger periods increase the possibility to find a noise variation over the  
 267 threshold).

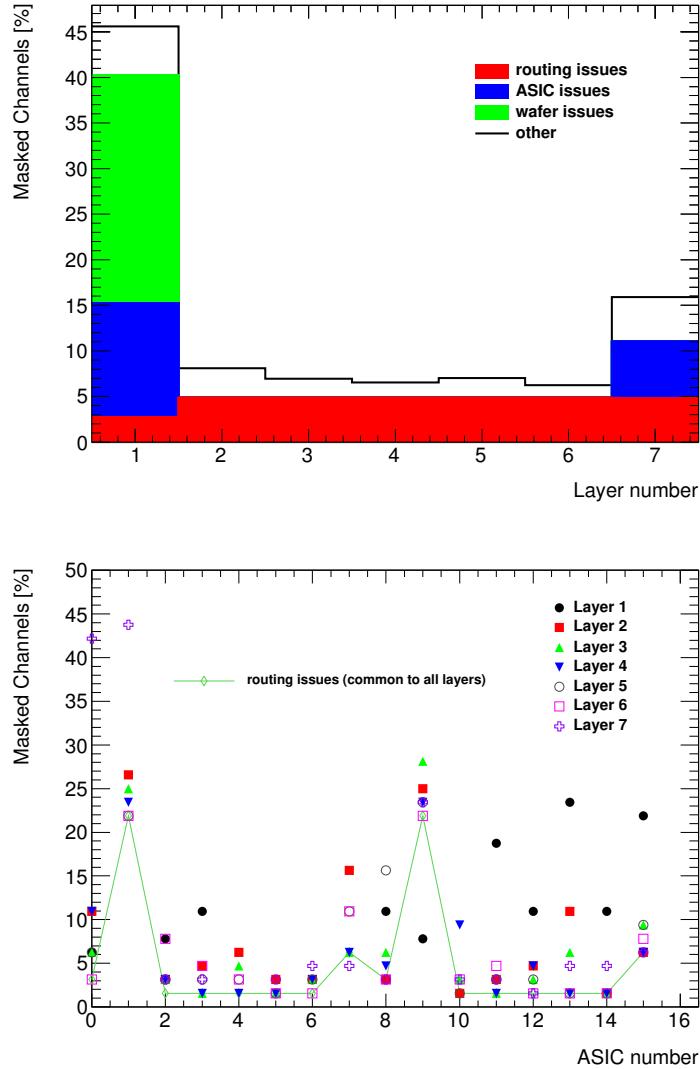
268 To reduce to the minimum the presence of cosmic rays signals, we perform runs with short  
 269 open acquisition windows (1.1 ms)<sup>3</sup>. In Figure 7 two S-curves of two different channels from the  
 270 second layer of the setup are shown.

271 The S-curves are fitted to a complementary error function

$$S(DAC) = p_0 \times erfc\left(\frac{DAC - p_1}{p_2}\right) = \frac{2p_0}{\sqrt{\pi}} \int_{\frac{DAC-p_1}{p_2}}^{\infty} \exp^{-t^2} dt, \quad (3.1)$$

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<sup>3</sup>The acquisition window is defined by means of a external pulse generator that emulates similar spill conditions than at the ILC. For DAQ needs, the actual data recording starts 1.4 ms after rising edge of the spill signal arrives. In this paper we will always refer to the effectively open acquisition window not including the mentioned 1.4 ms.

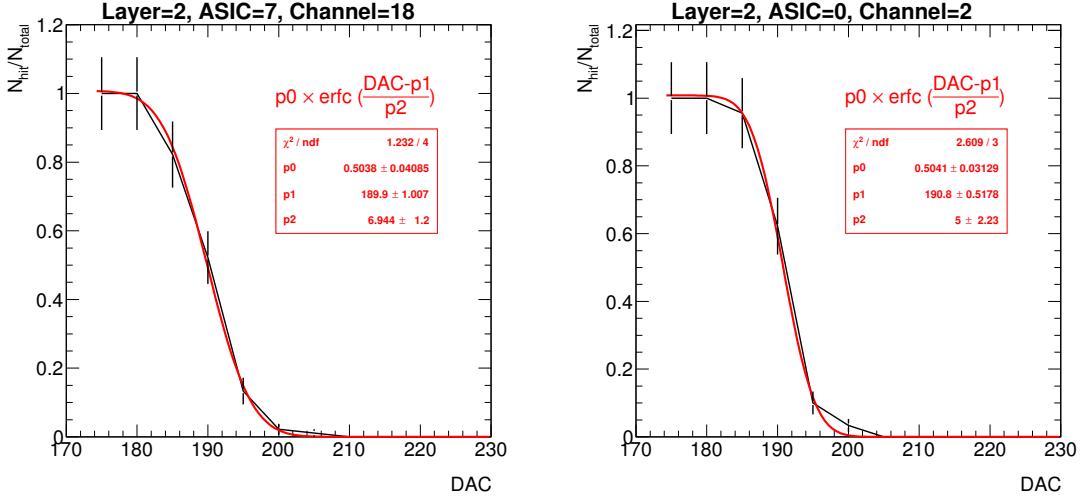


**Figure 6.** Ratio of channels that are marked as noisy in all slabs. Top: inventory of the different type of noisy channels per slab. Bottom: break up of the noisy channels per ASIC. We see two spikes in the number of channels masked due to routing issues in the ASICs 1 and 9. These two ASICs are located near the SMB where the density of lines (data and power transmission) is higher, complicating in this way the routing. The ASICs 4-7 (wafer issue) and 10 from layer 1 and the ASIC 4 from layer 7 are not included in the second plot since they are fully masked.

where  $p_0$  is 1/2 of the normalization,  $p_1$  is the value in which the noise levels are the 50% of its maximum and  $p_2$  give us the width of the S-curve.

The function from equation 3.1 was fitted to all channels data and all the values of  $p_1$  and  $p_2$  were saved. To decide the final trigger threshold value for the full ASIC, we took the maximum between:

$$DAC_{optimal}^{ASIC-j} = \langle p_1^{ASIC-j} \rangle + 5 \times \langle p_2^{ASIC-j} \rangle \quad (3.2)$$



**Figure 7.** Two S-curves obtained during noise runs.

and 230 if at least the the 30% of the 64 channels S-curves in the ASIC could be fitted. If less than the 30% of the channels were fit we took a most conservative value of 250 DAC for the threshold of the ASIC. The election of these two values was sustained by previous experiences, see for example [24].

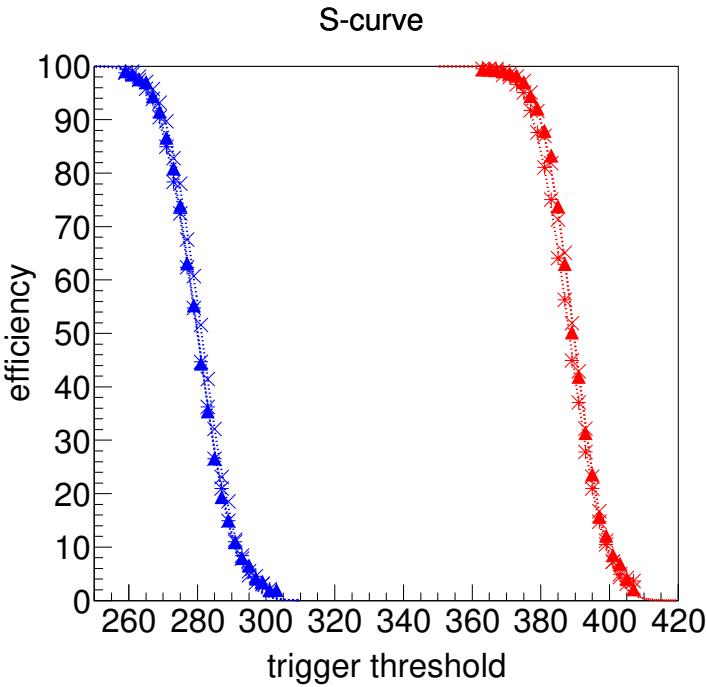
The optimal trigger threshold values for all ASICs are shown in Figure 10.

### 3.3 S/N ratio in the trigger line

Similar kind of measurements can be done but using external signals. This will allow to calculate the signal over noise (S/N) ratio to trigger 1 MIP signals. To calculate the S/N of the trigger we need to compare the 1 MIP S-curve and 2 MIP S-curve. The S/N will be defined as the ratio between the distance of both S-curves at its 50% and the width of the S-curve.

In Figure 8 we see the 1 MIP and 2 MIP S-curves obtained for one channel in a SKIROC testboard in which a single SKIROC2 in BGA package is placed and the 1 MIP and 2 MIPs "fake" signals are directly injected in the preamplifier (via a 3 pF capacitor located in the injection line as shown in Figure 2). From this plot we can extract a S/N ratio of ~12. We don expect large differences with the results that we would obtain with full equipped SLABs although this board is thought for commissioning and test of the SKIROC ASICS in an "ideal" environment in contrast with the FEV ASUS that are optimized to meet detector constraints and to hold several ASICs at the same time. For example: only power pulsing of the analog power is done in this testboard, there is a set of external capacitors on the board connected to some ASIC pins and usually only one channel is tested. This board allows us to commission and debug the SKIROC itself but not the full system.

We have obtained similar results using real signals, in this case cosmic rays signals. This is shown in Figure 9 where we show the result of the fit to the noise S-curves for all channels (in red) in one of the ASICs of the second layer together with the results of the S-curve with cosmic rays (black points and blue line). For the cosmic S-curve we took 30 min of data per point using very long spills (150 ms) in frequencies of 5Hz and we add up the triggers from all channels together. In addition, using the knowledge of the MIP value (see next section), we performed a simple cut



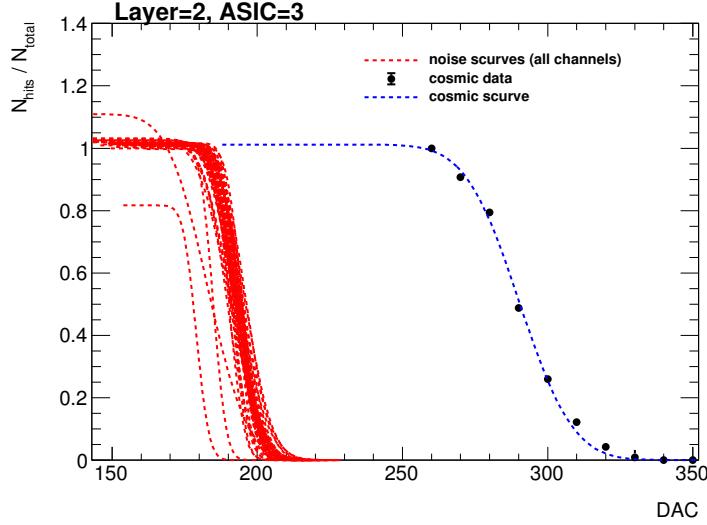
**Figure 8.** S-curves with charge injection (1 MIP in blue and 2 MIPs in red) for two different channels in a SKIROC2 testboard. From this plot, we extract a  $S/N = 12.8$  in the trigger line.

in the ADC to keep only signals corresponding to a MIP (pedestal subtracted)  $\pm 30$  ADC counts. With this cut we try reduce the contribution of muons traversing the wafers with very large angles but we don't have a way to select perpendicular tracks since we were using simple setups with only single slabs. For all these reasons, we expect a broader distribution of the cosmic S-curve. This is one of the reasons why, if we calculate the S/N using this plot, the value would be unrealistic (much lower, indeed). In addition to this, we should remember that the noise S-curve do correspond to the real noise distribution but only to the envelope of the noise in the fast shaper, therefore the distance between the two S-curves is smaller than the real distance between noise and signal.

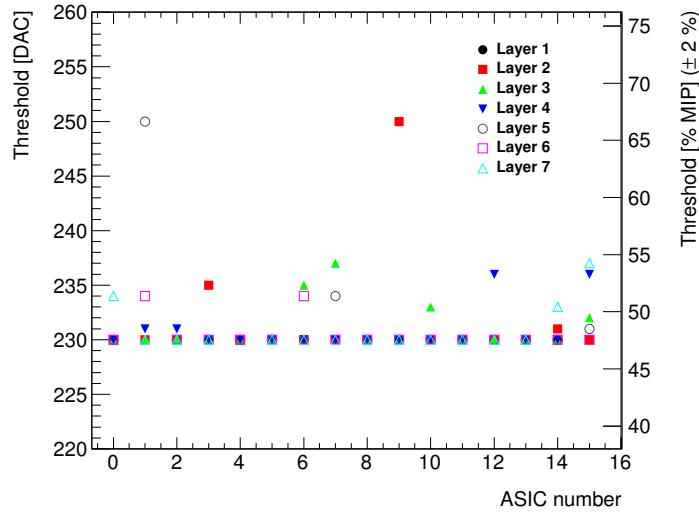
In conclusion, both ways of estimating the S/N ratio of the trigger have their own limitations but in both cases, the 50% of the S-curve of 1 MIP are compatible within  $\pm 10$  ADC. This allow us to, at least, estimate the relative distance between our final trigger threshold for every ASIC and the 1 MIP position by combining the information extracted from Figs 8 and 9. This is shown in Figure 10. Two ASICS ( $\sim 2\%$ ) have a trigger threshold value of 0.67 MIP. The 11% of the ASICs have a trigger threshold between 0.5 and 0.55 MIP and the rest, 87%, have trigger thresholds slightly lower than 0.5 MIP.

### 3.4 Prospects

All the commissioning procedure described above relies in very conservative decisions due to the presence of unknown noise sources during most of the commissioning phase. These sources are now well known and isolated and therefore a new "noise" commissioning procedure has been studied. It will consist in an iterative algorithm that first will identify and mask the "underflowed-noisy"



**Figure 9.** S-curves for noise (channel by channel, only the result of the fit) and cosmic rays (all channels together) for one ASIC in layer 2.



**Figure 10.** Summary of trigger threshold settings for all ASICs in the setup. The values are given in DAC and in estimated MIP units, using the distance between two MIPs from Figure 8. The uncertainty quoted in the right axis is estimated from difference between the 50% position of the S-curve for one MIP extracted from Figure 8 and 9.

323 channels and afterwards run a set of acquisitions in which the number of triggers per channel will  
 324 be compared with the number of expected triggers assuming only cosmic rays as signal. This  
 325 will allow us to have an unambiguous definition of the noise levels channel per channel instead of  
 326 defining such levels relatively to the total number of recorded triggers per ASIC. Finally, once that  
 327 the noisy channels are identified, the optimization of the threshold levels will be performed and a  
 328 last run for identification of noisy channels will be taken using this optimal threshold. In this run,

329 we can decide to mask the noisy channels or to increase its own trigger threshold level if we are  
330 using Skiroc2a.

331 Using this new procedure we manage to reduce the number of masked channels by a factor 2  
332 without any loss of performance, at least in the laboratory and using 3 of the 7 SLABS. This new  
333 procedure will be tested in the next beam test. Also, in order to optimize the commissioning of the  
334 detector, we propose a new set of measurements in the next beam test such as a scan of optimal delay  
335 of the hold values of the trigger using MIP like particles and a threshold scan for the determination  
336 of the S/N in the trigger line. This later can be done comparing 1 MIP and  $\sqrt{2}$  MIP (tilting the  
337 detector by 45 degrees) signals.

## 338 4 Performance on positron beam test at DESY

339 The beam test line at DESY provides continuous positron beams in the energy range of 1 to 6 GeV  
340 with rates from few hundreds of Hz to few KHz with a maximum of  $\sim$  3 KHz for 2-3 GeV. These  
341 positrons are produced in the following way: first, the electron/positron synchrotron DORIS II is  
342 used to produce a photon beam via bremsstrahlung when interacting with a carbon fiber target;  
343 secondly, these photons are then converted to electron/positron pairs; and, finally, the beam energy  
344 is selected with dipole magnets and collimators. In addition, DESY gives access to a bore 1 T  
345 solenoid, the PCMag.

346 The prototype tested in beam in June 2017 consisted of 7 layers as explained in Section 2.5.  
347 The detector was exposed to a positron beam in the DESY test beam area (line 24). By means of an an  
348 external pulse generator we defined the length of the acquisition window to be 3.7 ms at a frequency  
349 of 5 Hz, emulating in this way similar conditions than the ILC will have. The detector was running  
350 in power pulsing mode without any extra active cooling system.

351 The physics program of the beam test can be summarized in the following points:

- 352 • Commissioning and calibration without tungsten absorber using 3 GeV positrons acting as  
353 minimum ionizing particle (MIPs);
- 354 • magnetic field tests up to 1 T in the PCMag;
- 355 • response to electrons with fully equipped detector, i.e. sensitive parts *and* W absorber.

356 For the first two points from above, we used the SiW-ECAL in the tracker mode, *i.e.* without  
357 intercalated tungsten plates. Due to the low material budget of our setup when the tungsten is  
358 not included, a beam of positrons of few GeV of energies provides satisfactory data for calibration  
359 since the positrons deposit the minimum amount of energy by ionization. The calibration of the  
360 detector was realized by directing the 3 GeV positron beam on 81 positions equally distributed over  
361 the surface of the detector. These data were used for pedestal estimation and energy calibration.  
362 Calibration and pedestal analysis was done for all single layers not requiring track reconstruction.  
363 The study of these data is discussed in Section 4.1 for the pedestal and noise studies and Section  
364 4.2 for the results of the calibration.

365 For the tests inside the magnetic field, a special PVC structure was designed and produced to  
366 support one single SLAB. The purpose of such test was twofold: first to prove that the DAQ, all

367 electronic devices and the mechanical slab itself were able to handle strong magnetic fields; second  
368 to prove the stability of the performance during these tests. We took several runs, with 0, 0.5 and 1 T  
369 magnetic fields with and without 3 GeV positron beam and we observed that the pedestal and noise  
370 values are independent of the magnetic field (see Section 4.1.1). The study of the MIP calibration  
371 stability will be discussed in future publications where full studies of the data including comparison  
372 with simulations should be included.

373 To fulfill the last point of the list we inserted W plates of different thicknesses between the  
374 sensitive layers. Then we performed a scan of energies of the positron beam: 1-5.8 GeV. We  
375 tested the response of the detector with three different configurations of the W repartition. The  
376 accumulated amount of tungsten, in radiation length units,  $X_0$ , in front of each of the SLABs was:

- 377 • W-configuration 1: 0.6, 1.2, 1.8, 2.4, 3.6, 4.8 and 6.6  $X_0$
- 378 • W-configuration 2: 1.2, 1.8, 2.4, 3.6, 4.8, 6.6 and 8.4  $X_0$
- 379 • W-configuration 3: 1.8, 2.4, 3.6, 4.8, 6.6, 8.4 and 10.2  $X_0$

380 Preliminary results of the raw electromagnetic shower profiles look promising but will not be  
381 discussed in this article since deeper analysis and comparison with montecarlo simulations will be  
382 needed to extract conclusive results from the data. This will be the topic of a future article, possibly  
383 combining data with future beam tests that are currently in preparation. What it is included in this  
384 article, in Section 4.3 is the study of the pedestals in this events.

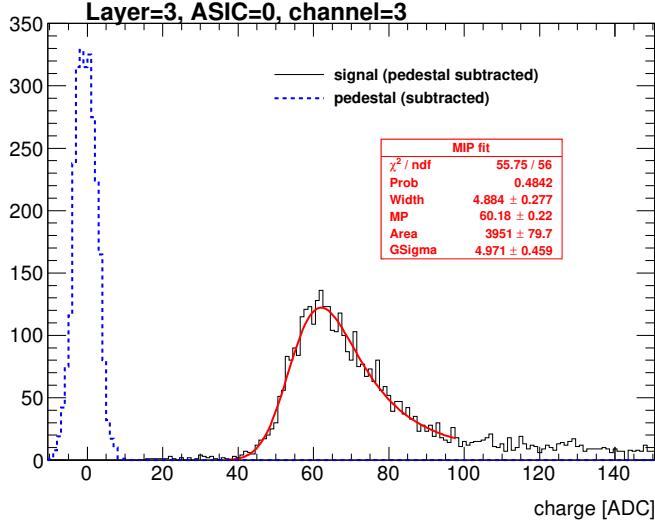
#### 385 4.1 Pedestal and noise studies with the SiW-ECAL in tracker mode

386 Due to the way that the SKIROC2 ASICs work, it is possible to extract the pedestals simultaneously  
387 to the recording of signals from particle interactions. Indeed, when a channel is triggered, the rest  
388 are read out at the end of the slow clock period (usually called BCID - for bunch crossing identity)  
389 and marked as non triggered channels. This allows us to reconstruct the pedestal distribution for all  
390 channels and for all SCAs. These distributions are fitted with a Gaussian and the pedestal value are  
391 associated with the mean of the result of the fit. These values will be, afterwards, subtracted to the  
392 ADC recorded by the SKIROC2 for all channels and SCAs. The noise is associated to the width of  
393 the pedestal distribution. The calibration runs have been used to calculate the pedestal distribution  
394 reference values of the detector. In Figure 11 we show the signal and pedestal distribution of a  
395 single channel after subtracting the pedestal mean position.

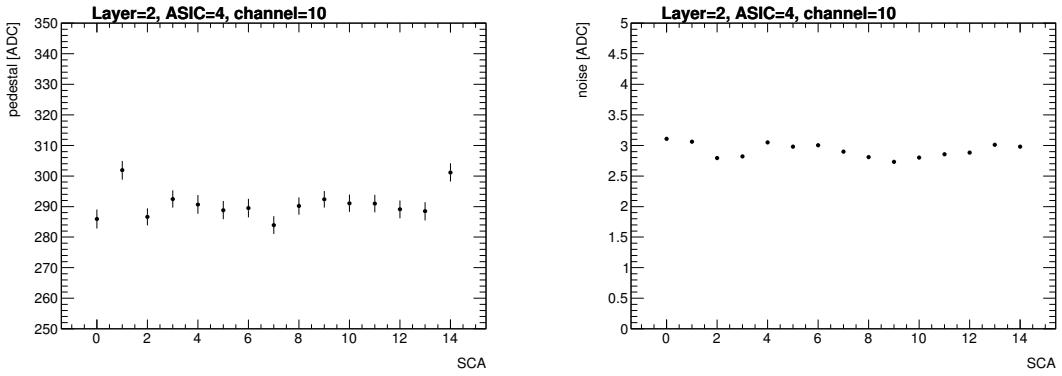
396 In Figure 12 (left) we observe that both the pedestal position for each SCA in the same channel  
397 can be different in few %. In the case of the pedestal mean position, these differences are even larger  
398 between different ASICs in the same layer (Figure 13, left plot) or between layers (Figure 14, left).  
399 This is the reason of performing the pedestal correction layer-, chip-, channel- and SCA-wisely. For  
400 the noise, the dispersion is much smaller ( $\sim 5\%$ ). This is shown in the right plots of Figures 12, 13  
401 and 14.

##### 402 4.1.1 Pedestal and noise in large magnetic fields

403 For the tests inside the magnetic field we used the SLAB of the first layer in the special PVC struture  
404 mentioned at the begining of this section. We should also mention that the PCMag is in a different



**Figure 11.** Pedestal (blue dashed line) and signal (black continuous line) distribution for one channel in the third layer. The results of the MIP calibration fit are included (red). The pedestal distribution is shown only for the first SCA to keep the y-axis within a reasonable range. The signal distribution is integrated over all SCAs.

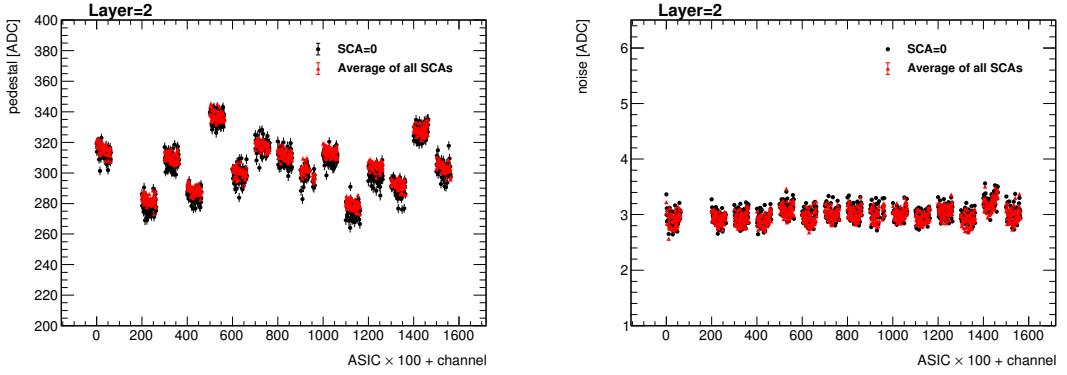


**Figure 12.** Pedestal mean position (left) and width (right) for one channel in the second layer.

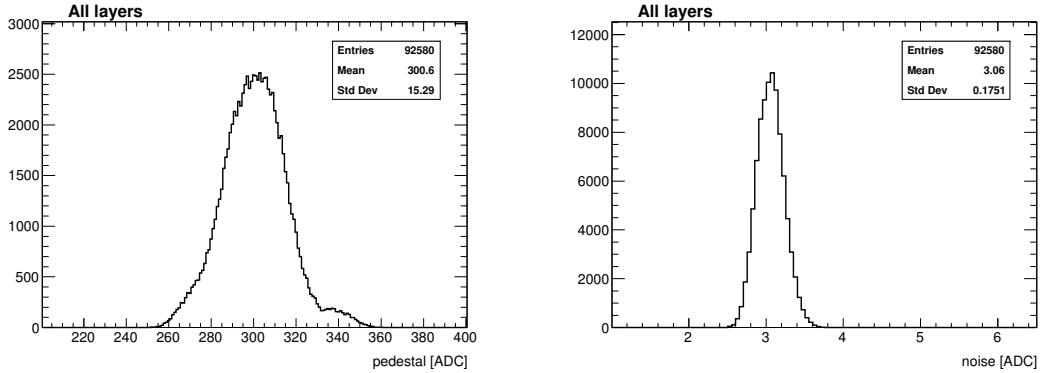
area (downstream) on the same beam line, therefore, due to the presence of additional collimators the beam rates are lower.

We divided the data taking in 3 stages in this order: a long run (13h) with a magnetic field of 1 T, a second and shorter run of 3 hours with 0.5 T and a final run with the magnet off. In the cases were we had beam, we used the 3 GeV positron beam settings impacting in the ASIC number 12.

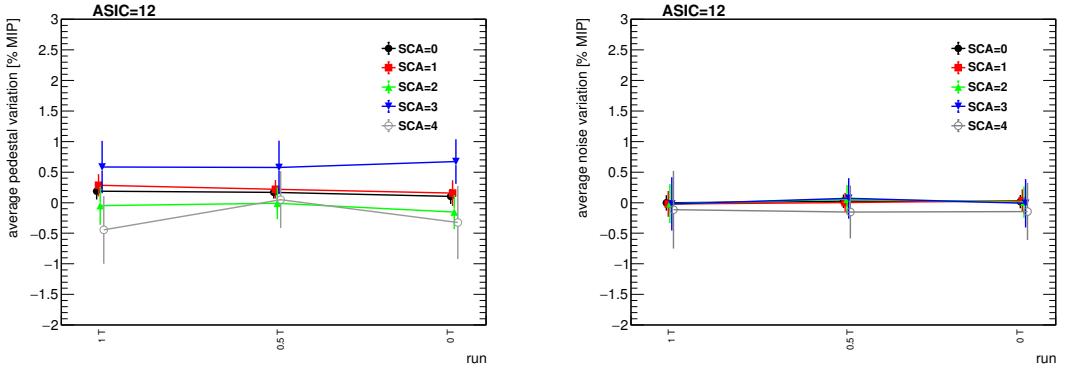
The comparison of the pedestal values and noise levels between the reference run in the stack and the different runs in the magnetic field are shown in Figure 15. We see that in both cases, the agreement is perfect within the statistical uncertainties. Due to the lower rates in this beam area, the analysis is only done up to few SCAs.



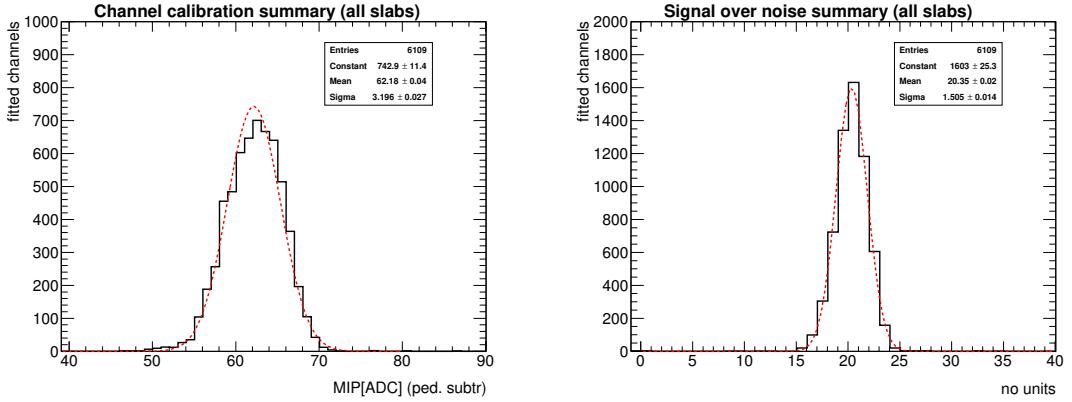
**Figure 13.** Pedestal mean position (upper plot) and width (lower plot) for all channels in one layer. The data is grouped on bunches in which the value in the x-axis corresponds to the value of the channel number plus the value of the ASIC number multiplied by 100. The black points show the value for the first SCA and the red points show the average value for all the others SCAs (with the standard deviation of the sample as error bar).



**Figure 14.** Pedestal mean position (left) and width (right) for all channels and all SCAs in the setup.



**Figure 15.** Average deviation of the pedestal mean position (left) and width (right) for all channels in the ASIC 12. The values are given in MIP units obtained from calibration (see Section 4.2).



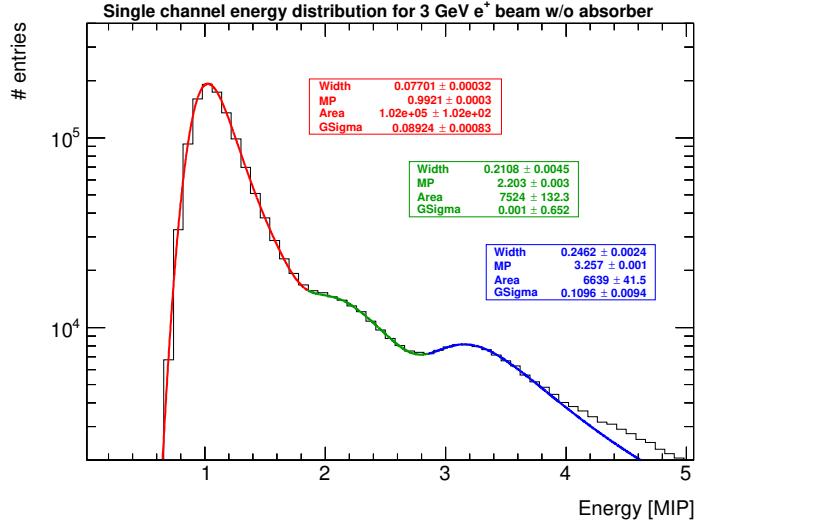
**Figure 16.** Result of the MIP position calculation and signal over noise calculation for all calibrated channels.

#### 414    4.2 MIP response and tracking efficiency with the SiW-ECAL in tracker mode

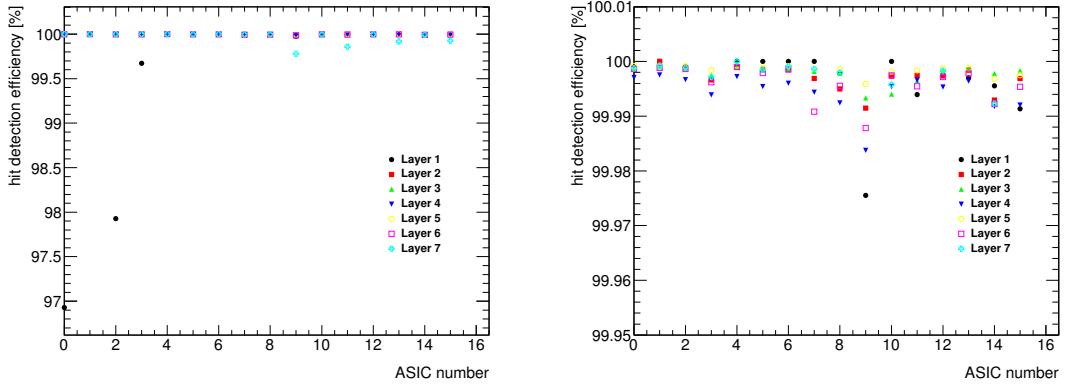
415    After the calculation of the pedestals for each channels and SCA, these are subtracted and the same  
 416    data (without track recognition) are used for the calibration. A Landau function convoluted by  
 417    a Gaussian is fit to the resulting hit distribution in ADC units. The most-probable-value of the  
 418    convoluted function is taken as the MIP value, allowing thus for a direct conversion from ADC to  
 419    energy. We have obtained a raw energy calibration spread of the 5% among all channels with the  
 420    98% of all available channels being fitted. Results are summarized in figure 16, leftmost plot.

421    We checked the MIP calibration by selecting tracks that cross the detector parallel to its  
 422    normal and filling a histogram with the energy measured by each channel with a hit. We did  
 423    this for all calibration runs together. The results are shown in figure 17 where the single channel  
 424    energy distribution for MIPs is shown for all calibrated channels in the same distribution. The  
 425    distribution nicely fits in the 1 MIP spectrum, showing in that way the good performance of our  
 426    default calibration that, for simplicity, was done without requiring tracking reconstruction. The  
 427    distribution also reveals the presence of a second and third peak due to events involving multiple  
 428    particles crossing the detector.

429    To evaluate the single hit detection efficiency we define a high purity sample of events of  
 430    positrons traversing the detector perpendicularly by selecting tracks with at least 4 layers (of 7  
 431    possible) with a hit in exactly the same channel. Afterwards we check if the other layers have or not  
 432    a hit in the same channel (expanding the search to the closest neighbouring channels) with energy  
 433    larger or equal than 0.3 MIP. Finally, we repeat this for all layers and channels. The results are shown  
 434    in Figure 18. Except few exceptions, the efficiency is compatible with 100%. Lower efficiencies in  
 435    the first layer are related to the presence of noisy channels not well identified in the commissioning  
 436    phase that boosted the filling of the the 15 SCAs of three ASICs. In the last layer (separated from  
 437    the other layers by four slots of 1.5 cm instead of only one) we also observe few small deviations  
 438    from the ~ 100% which are indeed associated to a slight misalignment of the tracks visible only in  
 439    the outliers channels. If we remove these channels from the analysis the full efficiency is recovered.



**Figure 17.** The single channel energy distribution (for all calibrated channels) for 3 GeV positron tracks acting as MIPs.



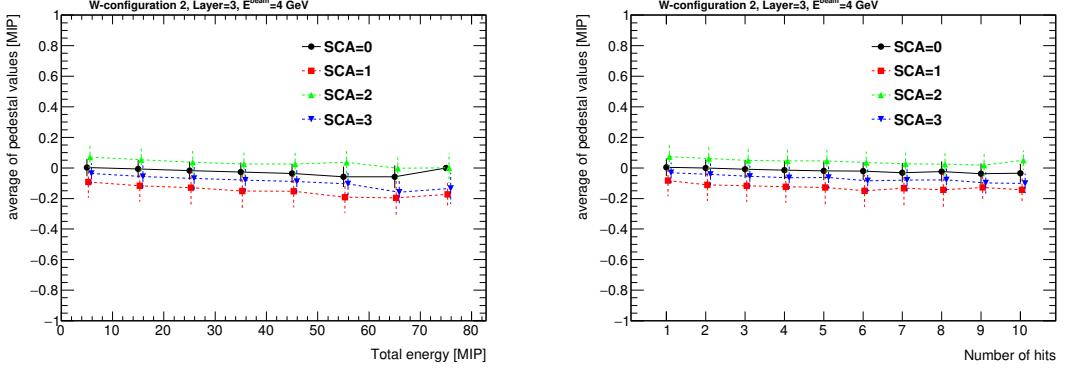
**Figure 18.** Left: MIP detection efficiency for all layers and ASICs in high purity samples of tracks of MIP-like acting particles. Right: same figures with a zoom in the y-axis. In both cases, the average efficiency of the 64 channels in each ASIC is shown.

#### 4.2.1 S/N ratio in the ADC

The signal-over-noise ratio in the ADC (corresponding to the slow shaper of the SKIROC2) is defined as the ratio between the most-probable-value of the Landau-gauss function fit to the data (pedestal subtracted) and the noise (the pedestal width). This quantity has been calculated for all channels and all slabs and, in average, it corresponds to 20.4. Results are summarized in Figure 16, rightmost plot.

### 4.3 Pedestal stability in electromagnetic shower events

The pedestal stability in events with large amount of charge deposited by the ASICs, as are the electromagnetic shower events, has been also calculated. All the results shown in this section



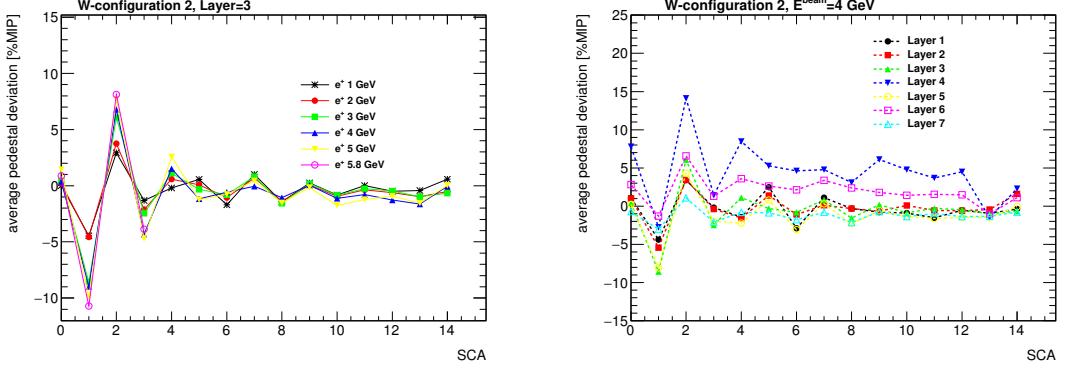
**Figure 19.** Left: mean position of the projection of the pedestal distribution of all channels of ASIC 12 in the Layer 3 calculated when different energies are collected in the ASIC (in bins of 10 MIPs). Right: same but as a function of the number of hits. In both cases, the results are shown for few SCA. The points for the curves with SCA larger than zero are slightly shifted in the x-axis to optimize the visualization.

449 correspond to data taken during the tungsten program, using the W-configuration number 2 when  
 450 shooting the beam in the ASIC 12 (and partially in the 13). Only the ASIC 12 is used in the  
 451 analysis. For other configurations and positions of the beam we get comparable results. We used  
 452 also a calibrated data sample where the pedestal values have been subtracted and the MIP calibration  
 453 has been applied. Therefore, all energy measurements are given in MIP units and the pedestal  
 454 values are expected to be equal to zero. In order to select a high purity of electromagnetic shower  
 455 like the events, we used a simple criteria: select only events with at least 6 of the layers with at least  
 456 a hit with  $E > 0.5$  MIP.

457 Two main observations have been extracted from the recalculation of the pedestals and its  
 458 comparison with the values obtained previously during the calibration runs. The first observation  
 459 consists in a relatively small drift of the pedestal values towards lower values when the collected  
 460 energy is high (or when the number of triggered channels is large). This is shown in Figure 19 for  
 461 several SCAs where the average of the projection of the pedestal distribution for all channels non  
 462 triggered in ASIC 12 of layer 3 is plotted as a function of the total energy measured by the ASIC (or  
 463 the total number of hits). We see that in all cases, the slopes of the curves for each SCA are very  
 464 similar. This feature is known and it is due to the architecture of the SKIROC2 (and 2a) ASICs  
 465 where high inrush of currents can slightly shift the baseline of the analogue power supply. This  
 466 feature is foreseen to be removed from the SKIROC3 ASICs.

467 The second observation extracted from this analysis can be also seen in Figure 19 but more  
 468 clearly in Figure 20: in addition to the small drift of the pedestal value an SCA-alternate global  
 469 shift is observed. We see that the effect is enhanced when large amounts of charge are deposited in  
 470 the ASIC (*i.e.* at larger beam energies or for the layers in the maximum of the shower profile). We  
 471 also observed that this alternation is only SCA dependent and not BCID dependent. This is not yet  
 472 fully understood although the fact that the effect is observed in alternate SCAs hints to some issue  
 473 affecting the digital part of the ASIC (where the SCAs enter in play).

474 Dedicated tests in the laboratory and in the beam are needed in order to clarify this issue.



**Figure 20.** Left: average value on each SCA of the calculated pedestals for all channels of ASIC 12 in the Layer 3 for different energies of the beam. Right: same but fixing the energy of the beam and comparing several layers.

#### 475 4.4 Fake triggers filtering

476 Several types of fake signals have been observed in the technological prototype since its construction  
 477 and test. A detailed description of them can be found in previous articles, as for example, in Ref.  
 478 [24]. All these fake signals are easily identified and tagged during the data acquisition and removed  
 479 afterwards from the analysis not introducing any significance loss of performance as can be seen,  
 480 for example, in the hit detection efficiency plots (see Section 4.2). In the following, we briefly  
 481 describe the status of the monitoring, debugging and filtering of such kind of events.

#### 482 Empty triggers

483 Empty trigger events are a well known feature of SKIROC2. The SKIROC2 uses an OR64 signal  
 484 to mark the the change to a new SCA when a signal over threshold is detected. The empty triggers  
 485 appear when during the acquisition the rising edge of the slow clock falls during the OR64 signal  
 486 and therefore the change to a new SCA is validated twice. This effect creates around 10-15% of  
 487 empty events which are easily filter and removed from the analysis. **The ratio of empty triggers in**  
 488 **the new SKIROC2a is reduced to ~ 3% due to a decrease of the OR64 by a factor X.**

#### 489 Plane events and retriggers

490 Another well know issue is related to the appearance of bunches of consecutive fake triggers that  
 491 quickly fill several SCA in consecutive slow clock periods. These events are also characterized by  
 492 triggering many channels (some times even all channels of an ASIC) at the same time. Although  
 493 the ultimate reason of the appearance of these events remains unknown we think that they may  
 494 be related to some distortion of the power supply baselines. We know that the SKIROC2 and 2a  
 495 preamplifiers are referenced to the analog power supply level, therefore, any voltage dip can be  
 496 seen as signal by the preamplifiers. The presence of a high inrush of current due to many channels  
 497 triggered at the same time can create these voltage dips. In previous studies (*i.e.* reference [24]),  
 498 the ratio of retriggers and plane events was reduced by improving the power supply stabilization  
 499 capacitances. It is important to remark that all layers and all ASICs analog and digital levels are  
 500 powered using the same power supply. Moreover, the high voltage power supply for the polarization

501 of the PIN diode it is also common for all layers. Therefore any noise in these power supplies or any  
502 overload of an ASIC may participate in the creation of fake signals in different ASICs and layers.

503 Studying the MIP calibration data of this beam test we have noticed that most of the retriggers  
504 and plane events are originated in ASICs far from the beam spot. Even more, hot spots tend to appear  
505 near the channels 37 and the channels tagged as “underflowed” during the commissioning phase.  
506 The amount these events have been estimated to be of 1 – 3% in the ASICs where high frequency  
507 interactions are produced (*i.e.* using 3 GeV positrons ate 2-3 KHz) and at higher rates even larger  
508 than 40% in other ASICs far from the beam spot. Moreover, it has been noticed a correlation  
509 between the time that an ASIC was full and the time of the appearance of some retriggers in other  
510 areas of the PCB. This correlation corresponds to  $\sim 8$  BCIDs (1.6  $\mu$ s) which hints of a distortion on  
511 the analogue power supply when the signal that informs the DIF that one ASIC memory has been  
512 filled is transmitted through the PCB.

513 All this information and dedicated studies in the laboratory will be used for the improvement  
514 of the power delivery, the PCB design and for further SKIROC developments with the possible  
515 approval the ILC in the scope.

## 516 5 Summary and prospects

517 The R&D program of the highly granular SiW-ECAL detector is in an exciting phase. After the  
518 proof of principle of the imaging calorimetry concept using the physics prototype, the technological  
519 prototype is being constructed and tested. In this document we describe the commissioning and  
520 beam test performance of a prototype built in with the first fully assembled detector elements (still  
521 only 7 over the total of  $\sim 10000$  to be in the ILD).

522 A very comprehensive and detailed commissioning procedure has been established and opti-  
523 mized allowing us to identify and isolate the different noise sources that could spoil the data taking.  
524 The beam test has provided a lot of useful data, allowing first for the study of the performance  
525 of the detector and secondly for its channel by channel calibration. A full analysis including the  
526 comparison with simulations of the second part of the data taking program (the electromagnetic  
527 showers) is to come. During both phases, the commissioning and the beam test, we have collected  
528 a good amount of data and results that will serve as input for future improvements on the design of  
529 the ASUs, the SKIROC and the upstream DAQ.

530 In parallel to the work described here, several R&D efforts are being carried. For example, we  
531 know that the ILD ECAL will host long layers of up to  $\sim 2.5$ m. A long layer constitutes a techno-  
532 logical challenge in both aspects, the mechanical (very thin and long structure with fragile sensors  
533 in the bottom, complicated assembly procedure...) and the electrical (*i.e.* transmission of signals  
534 and high currents). For example, interconnections between ASUs and between ASU and interface  
535 card are one of the most involved parts of the assembly and require close collaboration between  
536 mechanical and electronic engineers. Therefore, many efforts are focused in the construction and  
537 test of such long layers made of chains of ASUs (up to  $\sim 15$  ASU) as well as in the standardization  
538 of the interconnections. In addition, many efforts in the compactification of the DAQ and the ASUs  
539 (*i.e.* the chip on board versions of the ASUs described in Section 2.3) are being conducted by the  
540 SiW-ECAL collaboration.

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551 **References**

- 552 [1] T. Behnke, J. E. Brau, B. Foster, J. Fuster, M. Harrison, J. M. Paterson et al., *The International Linear*  
553 *Collider Technical Design Report - Volume 1: Executive Summary*, [1306.6327](#).
- 554 [2] H. Baer, T. Barklow, K. Fujii, Y. Gao, A. Hoang, S. Kanemura et al., *The International Linear*  
555 *Collider Technical Design Report - Volume 2: Physics*, [1306.6352](#).
- 556 [3] C. Adolphsen, M. Barone, B. Barish, K. Buesser, P. Burrows, J. Carwardine et al., *The International*  
557 *Linear Collider Technical Design Report - Volume 3.I: Accelerator & in the Technical Design Phase*,  
558 [1306.6353](#).
- 559 [4] C. Adolphsen, M. Barone, B. Barish, K. Buesser, P. Burrows, J. Carwardine et al., *The International*  
560 *Linear Collider Technical Design Report - Volume 3.II: Accelerator Baseline Design*, [1306.6328](#).
- 561 [5] H. Abramowicz et al., *The International Linear Collider Technical Design Report - Volume 4:*  
562 *Detectors*, [1306.6329](#).
- 563 [6] M. Aicheler, P. Burrows, M. Draper, T. Garvey, P. Lebrun, K. Peach et al., *A Multi-TeV Linear*  
564 *Collider Based on CLIC Technology*, .
- 565 [7] L. Linssen, A. Miyamoto, M. Stanitzki and H. Weerts, *Physics and Detectors at CLIC: CLIC*  
566 *Conceptual Design Report*, [1202.5940](#).
- 567 [8] P. Lebrun, L. Linssen, A. Lucaci-Timoce, D. Schulte, F. Simon, S. Stapnes et al., *The CLIC*  
568 *Programme: Towards a Staged e+e- Linear Collider Exploring the Terascale : CLIC Conceptual*  
569 *Design Report*, [1209.2543](#).
- 570 [9] J.-C. Brient and H. Videau, *The Calorimetry at the future e+ e- linear collider*, *eConf* **C010630**  
571 (2001) E3047, [[hep-ex/0202004](#)].
- 572 [10] V. Morgunov and A. Raspereza, *Novel 3-D clustering algorithm and two particle separation with tile*  
573 *HCAL*, in *Linear colliders. Proceedings, International Conference, LCWS 2004, Paris, France, April*  
574 *19-23, 2004*, pp. 431–436, 2004. [physics/0412108](#).
- 575 [11] F. Sefkow, A. White, K. Kawagoe, R. Pöschl and J. Repond, *Experimental Tests of Particle Flow*  
576 *Calorimetry*, *Rev. Mod. Phys.* **88** (2016) 015003, [[1507.05893](#)].
- 577 [12] CALICE collaboration, C. Adloff, J. Blaha, J. J. Blaising, C. Drancourt, A. Espargiliere, R. Galione  
578 et al., *Tests of a particle flow algorithm with CALICE test beam data*, *JINST* **6** (2011) P07005,  
579 [[1105.3417](#)].

- 580 [13] CALICE collaboration, J. Repond et al., *Design and Electronics Commissioning of the Physics*  
 581 *Prototype of a Si-W Electromagnetic Calorimeter for the International Linear Collider*, *JINST* **3**  
 582 (2008) P08001, [[0805.4833](#)].
- 583 [14] CALICE collaboration, C. Adloff et al., *Response of the CALICE Si-W electromagnetic calorimeter*  
 584 *physics prototype to electrons*, *Nucl. Instrum. Meth. A* **608** (2009) 372–383, [[0811.2354](#)].
- 585 [15] C. Adloff et al., *Study of the interactions of pions in the CALICE silicon-tungsten calorimeter*  
 586 *prototype*, *JINST* **5** (2010) P05007, [[1004.4996](#)].
- 587 [16] CALICE collaboration, C. Adloff et al., *Effects of high-energy particle showers on the embedded*  
 588 *front-end electronics of an electromagnetic calorimeter for a future lepton collider*, *Nucl. Instrum.*  
 589 *Meth. A* **654** (2011) 97–109, [[1102.3454](#)].
- 590 [17] CALICE collaboration, B. Bilki et al., *Testing hadronic interaction models using a highly granular*  
 591 *silicon-tungsten calorimeter*, *Nucl. Instrum. Meth. A* **794** (2015) 240–254, [[1411.7215](#)].
- 592 [18] CALICE collaboration, R. Cornat and R. Pöschl, *Technological prototype of a silicon-tungsten*  
 593 *imaging electromagnetic calorimeter*, *JINST* **10** (2015) C06015.
- 594 [19] CALICE collaboration, R. Cornat, *Semiconductor sensors for the CALICE SiW EMC and study of the*  
 595 *cross-talk between guard rings and pixels in the CALICE SiW prototype*, *J. Phys. Conf. Ser.* **160**  
 596 (2009) 012067.
- 597 [20] S. Callier, F. Dulucq, C. de La Taille, G. Martin-Chassard and N. Seguin-Moreau, *SKIROC2, front*  
 598 *end chip designed to readout the Electromagnetic CALorimeter at the ILC*, *JINST* **6** (2011) C12040.
- 599 [21] F. Gastaldi, R. Cornat, F. Magniette and V. Boudry, *A scalable gigabit data acquisition system for*  
 600 *calorimeters for linear collider*, *PoS TIPP2014* (2014) 193.
- 601 [22] M. Rubio-Roy, F. Thiant and F. Magniette, *Flexible online monitoring for high-energy physics with*  
 602 *Pyrame*, *J. Phys. Conf. Ser.* **898** (2017) 032009.
- 603 [23] CALICE collaboration, F. Magniette and A. Irles, *Pyrame 3, an online framework for Calice*  
 604 *SiW-Ecal*, *JINST* **13** (2018) C03009.
- 605 [24] M. S. Amjad et al., *Beam test performance of the SKIROC2 ASIC*, *Nucl. Instrum. Meth. A* **778** (2015)  
 606 78–84.
- 607 [25] T. Suehara et al., *Performance study of SKIROC2/A ASIC for ILD Si-W ECAL*, *JINST* **13** (2018)  
 608 C03015, [[1801.02024](#)].