Chapter 2
Review of AC–AC Frequency Converters

2.1 Introduction

As mentioned above, frequency converters convert AC electrical power of one frequency into AC electrical power of another frequency [51]. Additionally, this kind of converter also has the capability to control the load voltage amplitude, the load displacement angle relative to source voltage, the displacement angle between source currents and voltages (input power factor) and the capability to control bi-directional (or only unidirectional) power flow through the converter [51]. Figure 2.1 shows a generic three-phase PWM AC–AC frequency converter diagram and functional representation of such frequency converters.

To the input terminal of the frequency converter are connected voltage sinusoidal AC sources, with constant amplitude U_S and constant frequency f_S. These applied voltages are converted into output voltage waves with set amplitude U_L , frequency f_L and displacement angle of the load voltages relative to source voltages L_S. These output voltages are applied to the load. The load current amplitudes I_L and phase angles φ_L are determined by the impedance characteristic of the loads. During bi-directional power flow control in the case of direction from output terminals to input terminals, the frequency converter converts the load current waves of frequency f_L, into input current waves of frequency f_S.

AC–AC frequency converter topologies can be broadly classified into three categories, depending upon the type of AC–AC conversion. Figure 2.2 shows a classification tree for frequency converters. The classification of AC–AC frequency converters in the technical literature is varied, because the development of the converters discussed is still in progress [16, 81, 83, 84, 126]. The latter classified as indirect structures with main DC energy storage elements, direct structures without DC energy storage element and hybrid structures with small local DC energy storage elements. The first group includes the most popular and widely used in industry and households, i.e. direct frequency converters with voltage source inverters (VSI) or

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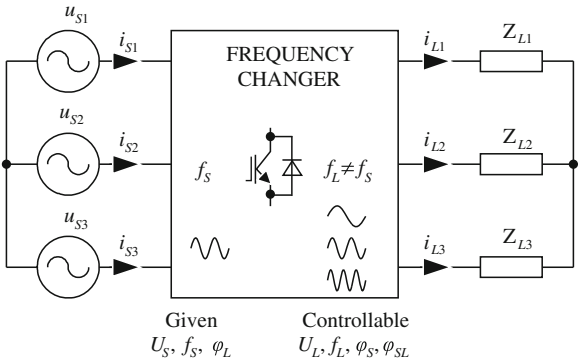


Fig. 2.1 Generic diagram of three-phase PWM AC–AC frequency converter and its functionality

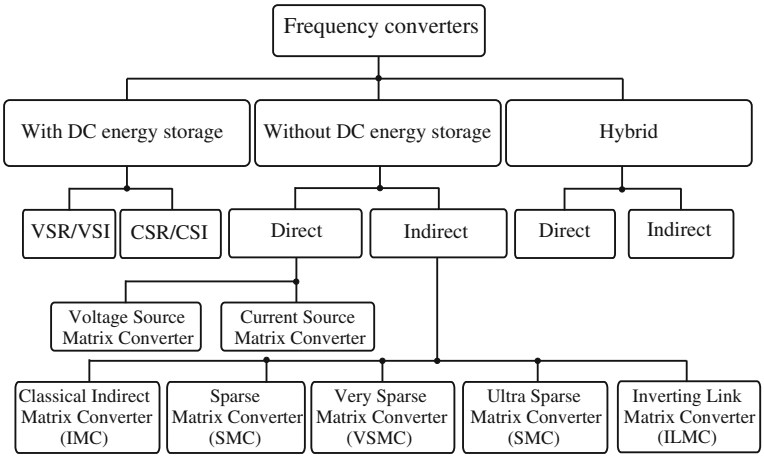


Fig. 2.2 Classification of three-phase AC–AC converter topologies

current source inverters (CSI). The second group consists of alternative topologies of direct frequency converters. These topologies have no DC energy storage elements and basically consist of an array of static power switches connected between the source and load terminals. For good performance direct frequency converters have small capacitors and inductors, such as high frequency component filters or small regenerative AC energy storage. The last group is a combination of direct frequency converters with small-sized local DC energy storage elements or an additional module with a DC–DC boost converter.

2.2 Frequency Converters with a DC Energy Storage Element

The most traditional AC–AC power converter topology is a pulse width modulated (PWM) voltage source inverter (PWM-VSI) with a front-end diode rectifier and a DC link capacitor, as shown in Fig. 2.3 [59, 72]. The frequency converter presented in Fig. 2.3 is also called a two-level indirect converter with voltage source inverter (VSI). An indirect converter consists of two converter stages and energy storage element, which convert input AC into DC and then reconvert DC back into output AC with variable amplitude and frequency. The DC-link capacitor decouples two AC power conversion stages and ensures the independent control of two stages. The control of the output is achieved by modulating the duty cycles of the devices in the inverter stage so as to produce near-sinusoidal output currents in the inductive load, at a desired amplitude and frequency. The source current in this converter is highly distorted, containing high amounts of low-order harmonics (5th and 7th) [11]. Through the impedance of the mains, the low-order current harmonics may distort the voltage at the point of common coupling, which may further interfere with other electric systems in the network. As the current direction in a diode rectifier cannot reverse, some mechanism must be implemented to handle an eventual energy flow reversal, such as during an electromagnetic braking of a motor, in order to prevent the DC bus voltage reaching destructive levels. Such mechanisms are always dissipative ones (in a braking resistor) and hence they can be effectively employed only when the energy to be dissipated is low [72]. The solution to the problem is to use an IGBT bridge as a supply rectifier. This converter is called back-to-back inverter (B2B VSI) and is presented in Fig. 2.4 [145]. The back-to-back converter consists simply of a force-commutated rectifier and a force-commutated inverter connected by a common DC-link, making their separate control possible. The line-side converter may be operated to give sinusoidal source currents, and the braking energy can be fed back to the power grid. It is a boost-type converter, i.e. its DC-link side voltage has to be higher than the peak value of the supply line-to-line voltage. In the back-to-back VSI, source filter inductors are also required. These inductors are a big problem

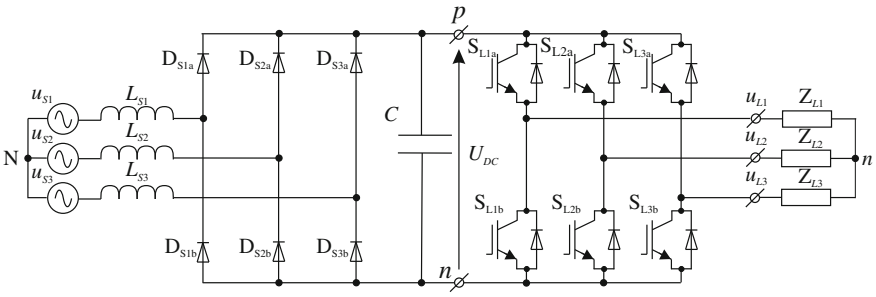


Fig. 2.3 Two-level indirect frequency converter with voltage source inverter and diode bridge rectifier

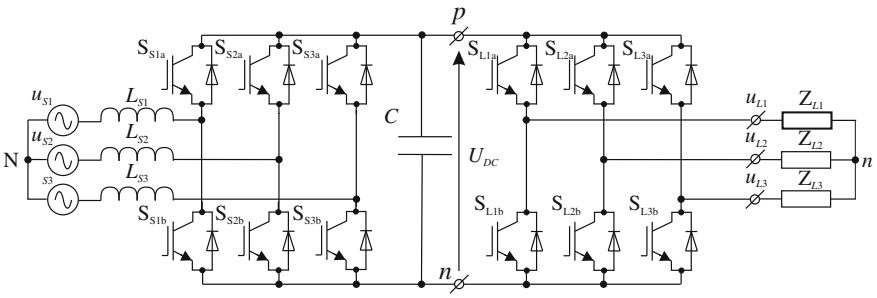


Fig. 2.4 Back-to-back converter (BB-VSI)

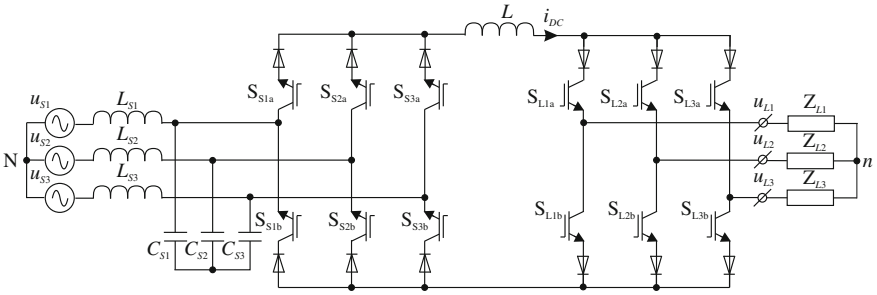


Fig. 2.5 Two-level indirect frequency converter with current source inverter

because the inductors are bulkier and heavier than the DC link capacitor in low and medium power converters.

An alternative solution to a frequency converter with voltage source inverter is the solution with PWM current source inverter (CSI), presented in Fig. 2.5 [34, 59]. The CSI produces sinusoidal supply current waveforms similar to the back-to-back VSI. The CSC contains a DC link inductor, which is generally larger and heavier than the link capacitor in voltage source converters. In the CSI, a source filter is also required. This is a low-pass LC-type filter, and the physical size of CSI source filter is smaller than used in a B2B VSI. Furthermore, the CSI usually requires series-connected diodes with every IGBT. This increases semiconductor conduction losses and the complexity of the main circuit.

The DC energy storage in the presented indirect frequency converters is a bulky component. In the solution with VSI the DC link capacitors are relatively large compared to the size of the rectifier and inverter semiconductor components, at the same time reducing the speed of response. Electrolytic capacitors typically occupy from 30 to 50 % of the total volume of the converter for power levels greater than a few kW and in addition to this they are a component with a limited lifetime. It should be noted that the electrolytic capacitor has by far the shortest lifetime of any element, active or passive, used in power electronic converters. In addition, the presence of the capacitor significantly limits the power converter to high temperature applications

up to 300 °C, because these capacitors are temperature sensitive. Capacitors also cause higher maintenance costs of the conversion system. Furthermore, high power conventional capacitors cannot be used in some special applications, such as in aeronautics, aircraft and deep-sea or space systems [12, 15, 19, 31, 141]. In the case of the CSI, the DC-link inductors are generally bulkier and heavier than the link capacitor in voltage source converters. However, frequency converters with VSI, (diode rectifier stage and back-to-back) are well known and widely used in industry.

The classical VSI generates a low-frequency output voltage with controllable magnitude and frequency by programming high-frequency voltage pulses. Of the various pulse-programming methods, the carrier-based pulse width modulation (PWM) methods are the preferred approach in most applications [52]. Two main implementation techniques exist in the control of load voltages: The first is the triangle intersection technique, where the reference modulation wave is compared with a triangular carrier wave and the intersections define the switching instants. The second is based on space vector modulation (SVM). In this method, the time length of the inverter states are precalculated for each carrier cycle by employing space-vector theory [50, 132].

In the classical three-phase VSI stage in the frequency converter shown in Figs. 2.3 and 2.4 is identified as eight switch combinations, which are connected in Table 2.1. Two of these states are a short circuit of the output terminals while the other six produce active voltages. In the three-phase CSI stage shown in Fig. 2.5, there is possible six active switch combinations and three with zero output current. The switch combinations in CSI are presented in Table 2.2.

In the space-vector approach, employing the complex variable transformation, the time domain load voltage and current signals are translated to the complex reference voltage or current vector, which rotates in the complex coordinates with the angular speed shown in the following:

$$\underline{\mathbf{u}}_L = \frac{2}{3}(u_{L1} + \underline{a}u_{L2} + \underline{a}^2 u_{L3}), \tag{2.1}$$

$$\underline{\mathbf{i}}_L = \frac{2}{3}(i_{L1} + \underline{a}i_{L2} + \underline{a}^2 i_{L3}), \tag{2.2}$$

Table 2.1 Switch configurations and corresponding load voltages in VSI

No.	S_{L1a}	S_{L2a}	S_{L3a}	S_{L1b}	S_{L2b}	S_{L3b}	u_{L1n}	u_{L2n}	u_{L3n}
1	1	1	0	0	0	1	$\frac{1}{3}U_{\mathrm{DC}}$	$\frac{1}{3}U_{\mathrm{DC}}$	$-\frac{2}{3}U_{\mathrm{DC}}$
2	1	0	0	0	1	1	$\frac{2}{3}U_{\mathrm{DC}}$	$-\frac{1}{3}U_{\mathrm{DC}}$	$-\frac{1}{3}U_{\mathrm{DC}}$
3	0	1	0	1	0	1	$-\frac{1}{3}U_{\mathrm{DC}}$	$\frac{2}{3}U_{\mathrm{DC}}$	$-\frac{1}{3}U_{\mathrm{DC}}$
4	0	1	1	1	0	0	$-\frac{2}{3}U_{\mathrm{DC}}$	$\frac{1}{3}U_{\mathrm{DC}}$	$\frac{1}{3}U_{\mathrm{DC}}$
5	0	0	1	1	1	0	$-\frac{1}{3}U_{\mathrm{DC}}$	$-\frac{1}{3}U_{\mathrm{DC}}$	$\frac{2}{3}U_{\mathrm{DC}}$
6	1	0	1	0	1	0	$\frac{1}{3}U_{\mathrm{DC}}$	$-\frac{2}{3}U_{\mathrm{DC}}$	$\frac{1}{3}U_{\mathrm{DC}}$
7	1	1	1	0	0	0	0	0	0
8	0	0	0	1	1	1	0	0	0

Table 2.2 Switch configurations and corresponding load current in CSI

No.	S_{L1a}	S_{L2a}	S_{L3a}	S_{L1b}	S_{L2b}	S_{L3b}	i_{L1}	i_{L2}	i_{L3}
1	1	0	0	0	0	1	I_{DC}	0	$-I_{DC}$
2	0	1	0	0	0	1	0	I_{DC}	$-I_{DC}$
3	0	1	0	1	0	0	$-I_{DC}$	I_{DC}	0
4	0	0	1	1	0	0	$-I_{DC}$	0	I_{DC}
5	0	0	1	0	1	0	0	$-I_{DC}$	I_{DC}
6	1	0	0	0	1	0	I_{DC}	$-I_{DC}$	0
7	1	0	0	1	0	0	0	0	0
8	0	1	0	0	1	0	0	0	0
9	0	0	1	0	0	1	0	0	0

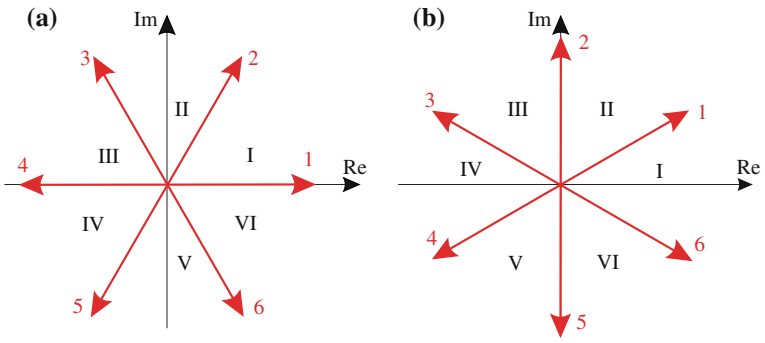


Fig. 2.6 Active stationary vector on dq plane for three-phase: **a** VSI (Table 2.1), **b** CSI (Table 2.2)

where: $\underline{a} = e^{j\frac{2\pi}{3}}$, $\mathbf{u}_L, \mathbf{i}_L$-vectors of load voltages and load current, respectively; U_L, I_L-magnitude of those vectors; α_L, β_L-phase angle of load voltage and load current vectors, respectively. Each active switch configuration in VSI and CSI corresponds to active space vectors, while the zero configuration corresponds to zero space vectors. Active vectors are represented in the dq plane as shown in Fig. 2.6, and spaced equally at 60° intervals around the complex plane [59].

2.3 Frequency Converters Without DC Energy Storage Element

2.3.1 Introduction

The main aim of this subsection is to describe the general characteristics of AC–AC frequency converters without DC energy storage elements. As is presented in Fig. 2.2 these converters are divided into three groups. The first group contains a classical

direct matrix converter which operates in two modes: as a voltage source matrix converter and a current source matrix converter, similarly as in converters with DC energy storage elements. The second group contains indirect converters with fictitious DC-link (but without DC storage elements). The third group is converters based on matrix-reactance choppers with source or load synchronous switches connected as in a matrix converter. This concept is based on regenerative AC energy storage elements such as small capacitors or inductors. In these elements the average energy during the source (or load) voltage time period is equal to zero.

The main focus is given to the presented fundamentals of the matrix converter, which are the fundamental structures in AC–AC frequency converters without DC energy storage. Furthermore, matrix-frequency converters, as the main object of this book will be described in detail in the following chapters.

2.3.2 Direct AC–AC Frequency Converters: Matrix Converter

As mentioned above, the groups of direct frequency converters include matrix converter (MC) structures. The MC, depending on the kind of power supply (voltage or current character), can work as a voltage source matrix converter (VSMC) or a current source matrix converter (CSMC), respectively. The main technical papers presented at conferences and in journals concern the matrix converter in VSMC mode, and commonly this structure is referred to as a matrix converter.

Generally, the matrix converter is a single-stage converter which has an array of $m \times n$ bi-directional power switches to connect, directly, an m-phase voltage source to an n-phase load [1, 2, 135, 142], which is presented in Fig. 2.7. In three-phase systems, an MC is an array of nine bi-directional switches that allow any load phase to be connected to any source phase (Fig. 2.8). In the case of voltage sources on the input side there are voltage source matrix converters (VSMC), the schemes of which are depicted in Figs. 2.7 and 2.8 [87].

For good performance, the VSMC should have a source filter. The source filter is generally needed to minimise the high frequency components in the input currents and reduce the impact of the perturbations from the input grid. Their size is inversely proportional to the matrix converter switching frequency. The major advantage of matrix converters is the absence of the DC link capacitor, which may increase the efficiency and the lifetime of the converter. The development of MCs started when Venturini and Alesina proposed the basic principles of operation in the early 1980s [135]. The authors proposed in [135] a high switching frequency control algorithm and the development of a rigorous mathematical analysis to describe the low-frequency behaviour of the converter.

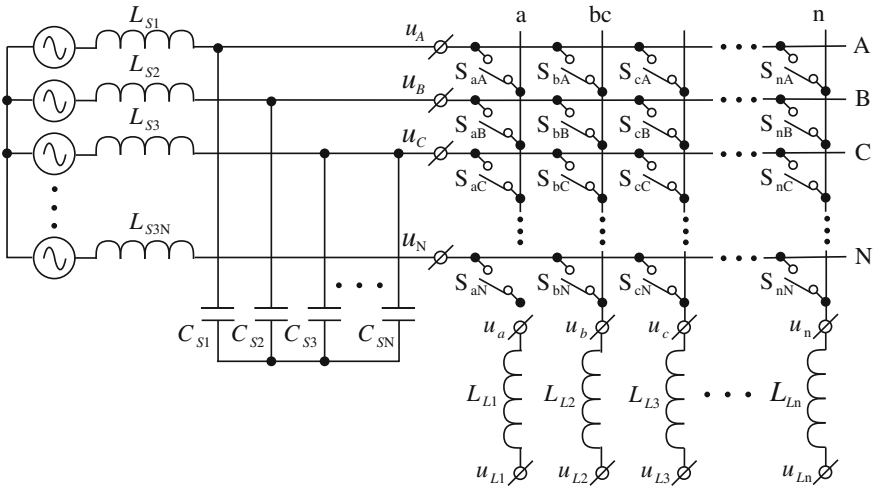


Fig. 2.7 Simplified circuit of m × n phase matrix converter

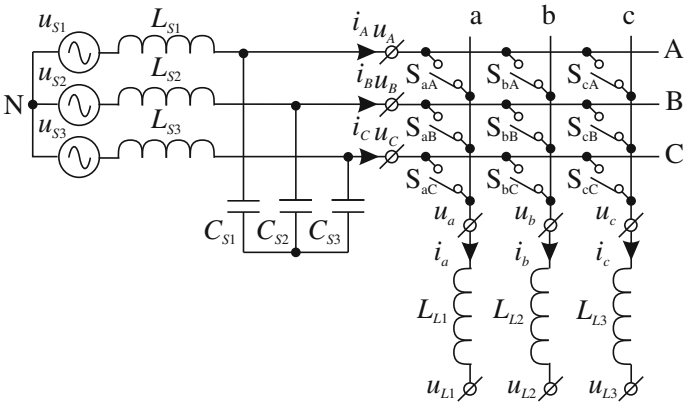


Fig. 2.8 Simplified circuit of three-phase matrix converter

Basic principles of matrix converter

The switching function of a single switch is defined as follows [135]:

$$s_{jK} = \begin{cases} 1, \text{ switch } s_{jK} \text{ turn-on} \\ 0, \text{ switch } s_{jK} \text{ turn-off} \end{cases}, \tag{2.3}$$

where $j \in \{a, b, c\}$ is the name of the output phase, $K \in \{A, B, C\}$ is the name of the input phase. Taking into account that the input phases must never be short-circuited and that the output currents must never be interrupted, the constraints can

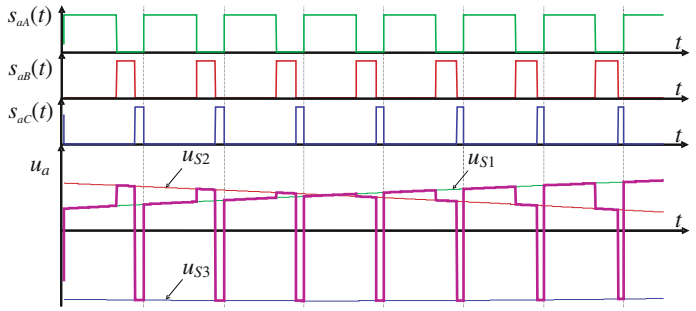


Fig. 2.9 Synthesis of matrix converter output voltages

be expressed as [135]:

$$s_{jA} + s_{jB} + s_{jC} = 1. \tag{2.4}$$

With these restrictions, the three-phase matrix converter has 27 allowed switching states, with 512 (2^9) which are possible [25, 110, 142]. If the load and source voltages are referenced to the supply neutral point "N" then the input/output relationship of voltages and current can be described as follows:

$$\begin{bmatrix} u_a(t) \\ u_b(t) \\ u_c(t) \end{bmatrix} = \begin{bmatrix} s_{aA}(t) & s_{aB}(t) & s_{aC}(t) \\ s_{bA}(t) & s_{bB}(t) & s_{bC}(t) \\ s_{cA}(t) & s_{cB}(t) & s_{cC}(t) \end{bmatrix} \begin{bmatrix} u_A(t) \\ u_B(t) \\ u_C(t) \end{bmatrix}, \tag{2.5}$$

$$\begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix} = \begin{bmatrix} s_{aA}(t) & s_{bA}(t) & s_{cA}(t) \\ s_{aB}(t) & s_{bB}(t) & s_{cB}(t) \\ s_{aC}(t) & s_{bC}(t) & s_{cC}(t) \end{bmatrix} \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix}, \tag{2.6}$$

$$\begin{bmatrix} u_{ab}(t) \\ u_{bc}(t) \\ u_{ca}(t) \end{bmatrix} = \begin{bmatrix} s_{aA}(t) - s_{bA}(t) & s_{aB}(t) - s_{bB}(t) & s_{aC}(t) - s_{bC}(t) \\ s_{bA}(t) - s_{cA}(t) & s_{bB}(t) - s_{cB}(t) & s_{bC}(t) - s_{cC}(t) \\ s_{cA}(t) - s_{aA}(t) & s_{cB}(t) - s_{aB}(t) & s_{cC}(t) - s_{aC}(t) \end{bmatrix} \begin{bmatrix} u_A(t) \\ u_B(t) \\ u_C(t) \end{bmatrix}. \tag{2.7}$$

The graphical interpretation of MC output voltages formation from pieces of source voltages is presented in Fig. 2.9.

Topologies of bi-directional switches

The three-phase MC topology is constructed using nine bi-directional four-quadrant switches arranged in a matrix, which are capable of conducting currents and blocking voltages of both polarities. There are four main topologies for bi-directional switches, which are shown in Fig. 2.10 [6, 60, 126, 142, 149]. The most simple switch cell is a single-phase diode bridge with an IGBT connected at the centre (Fig. 2.10a). The main advantage of this switch is that only one active device is needed. This approach reduces the cost of the power circuit and the complexity of

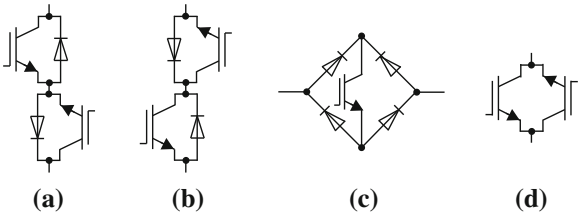


Fig. 2.10 Bi-directional switch cell configuration: **a** diode bridge with an IGBT configuration, **b** common emitter anti-paralleled IGBT configuration, **c** common emitter anti-paralleled IGBT configuration, **d** anti-paralleled reverse blocking IGBTs (RB-IGBT) configuration

the control. Only one transistor gate drive circuit is needed for each switch cell. The disadvantage is that the conduction losses are relatively high. During the conduction stage, the three devices are conducted (two diodes and IGBT transistor). Moreover, the direction of current through the switch cell cannot be controlled. The two most commonly used configurations of switch cell are named the common emitter anti-paralleled IGBT configuration (Fig. 2.10b) and the common collector anti-paralleled IGBT configuration (Fig. 2.10c). Each of these switch cells consist of two diodes and two IGBT switches that are connected in an anti-parallel arrangement. The diodes are included to provide reverse blocking capability, whereas, the IGBTs enable the independent control of the current direction. Compared to the diode bridge switch cell (Fig. 2.10a), here conduction losses are reduced, because only two devices are conducted in each conduction path. Its disadvantage is the requirement of two gate drive circuits for each IGBTs. For the arrangement shown in Fig. 2.10b, due to its common emitter arrangement, one isolated power supply is required for each bi-directional switch cell. Furthermore, by using common collector bi-directional switch cells (Fig. 2.10c), the number of isolated power supplies required for the gate drive circuits can be reduced to six. Finally, the switch cell is the anti-paralleled reverse blocking IGBTs (RB-IGBT) [130], an arrangement shown in Fig. 2.10d [123, 149]. The main feature of the RB-IGBT is its reverse voltage blocking capability, which eliminates the use of diodes. For this reason there is a reduction in the number of discrete devices and conduction losses. At any instant, there is only one device conducting current in any direction. In this configuration, 18 gate drive circuits and six isolated power supplies is required. Therefore, an anti-paralleled RB-IGBT configuration is generally preferred for creating matrix converter bi-directional switch cells. The element complexity of matrix converters with different switches cells is described in Table 2.3 [21].

Furthermore, other switching devices, besides IGBT, could be used in MCs. If the switching devices used for the bi-directional power switch have a reverse voltage blocking capability, then it is possible to build bi-directional switches. For example, MOS turn-off thyristor (MTOs), GTO thyristor and pure JFET may be an applicable [93].

The first key problem is related to the practical realisation of bi-directional switches. Currently, there are no small bi-directional power switches that are

commercially available, so discrete devices need to be used to construct suitable switch cells. These realisations require much more chip area and they produce higher switching losses compared to a completely integrated solution. However, in recent times several different configurations of bi-directional switch cells have appeared on the commercial market. The 1,200 V/200 A IGBT commercially available bi-directional switch cell sample chip, created by Dynex Semiconductor, is shown in Fig. 2.11. This module is a relatively high power device. In the small power semiconductor market this kind of switch module is not available.

From a commercial point of view, it is worth noting that several manufacturers have already produced integrated power modules for MC. The traditional solution tends to concentrate on a single power module, with the switches corresponding to one leg of the converter. The prototype of one-phase leg of an MC with RB-IGBTs is shown in Fig. 2.12 [123, 149]. The power modules included six 600 V/100 A RB-IGBTs, connected as shown in Fig. 2.13.

However, it is also possible to find modules containing the whole power stage of the MC. This arrangement leads to a very compact converter with the potential for substantial improvements in efficiency. The first three-phase-to-three-phase matrix switch power module was built by Eupec in co-operation with Siemens, using transistors connected in the common collector configuration [60, 122]. It contains all 18 necessary IGBTs and diodes of the 3×3 switch matrix in a single housing (Fig. 2.14). This module is named EconoMAC [60]. This type of packaging will have important benefits in terms of circuit losses. The stray inductance and connect resistances can be minimised.

Table 2.3 The MC element complexity with different switch cells

Switch cell configuration	Transistors	Diodes	Isolated power supply	Gate drive circuits
Figure 2.10a	9	36	9	9
Figure 2.10b	18	9	9	18
Figure 2.10c	18	9	6	18
Figure 2.10d	18	0	6	18

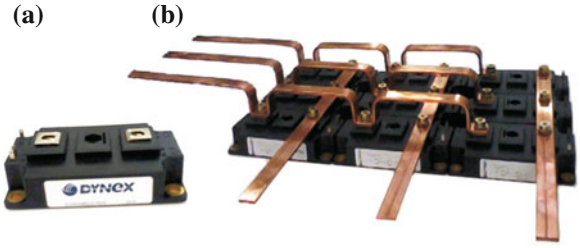


Fig. 2.11 Chip of commercially available bi-directional switch cell: **a** single switch, **b** matrix-connected nine switches

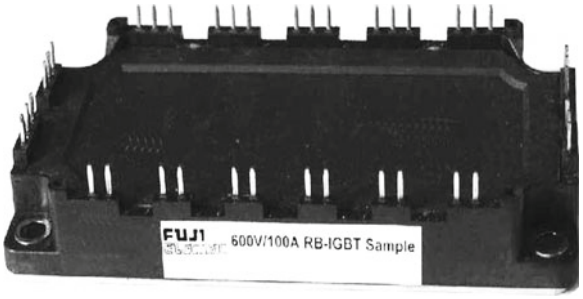


Fig. 2.12 Prototype of 600 V/100 A RB-IGBT module—photograph [123]

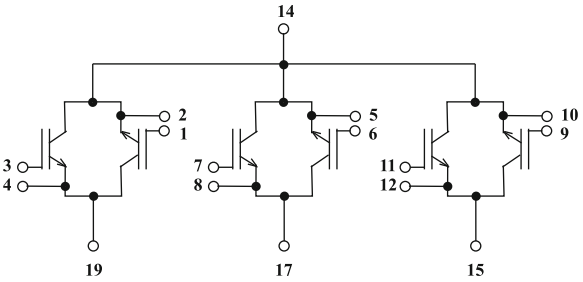


Fig. 2.13 Prototype of 600 V/100 A RB-IGBT module—topology structure [123]

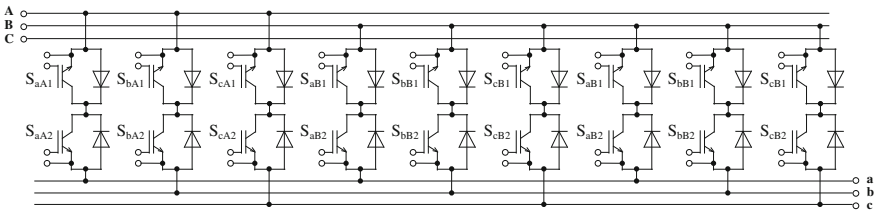


Fig. 2.14 Power stage configuration of EconoMAC module [60]

The all-in-one MC configuration prototype module with RB-IGBTs was introduced by FUJI Electric in 2011. The prototype 1,200 V/50 A module is shown in Fig. 2.15, whereas the internal structure is depicted in Fig. 2.16 [100].

Nowadays, several bi-directional switches, one-phase leg matrix converter or three-phase matrix configuration power switch modules are proposed by various companies [25, 26, 60, 100, 122, 123, 149]. Based on the above review it can be said that the number of power semiconductors for matrix converter application will systematically increase over time. The market for these devices depends on the development of MC technology. The main focus of development is the reduction of costs, size and increase in reliability [6, 98, 99].

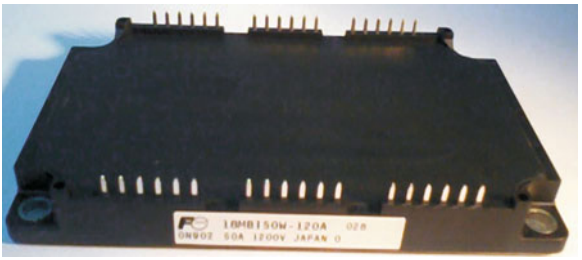


Fig. 2.15 Photography of RB-IGBT matrix configuration module

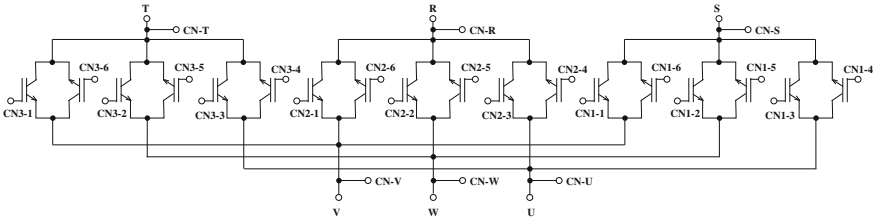


Fig. 2.16 Power stage configuration of RB-IGBT matrix configuration module

Commutation strategies

One of the main issues in control of the MC is the current commutation [25, 142]. The switches used in the MC are not protected by the DC-link capacitor, which is typical of the classical VSI, since there are no natural freewheeling paths. The current commutation between switches in the MC is more difficult to achieve than the VSI [105]. When considering commutation strategies for matrix converters two general rules must be adhered [29, 135]:

1. commutation should not cause a short circuit between the two input phases, because the consequent high circulating current might destroy the switches;
2. commutation should not cause an interruption of the output current because the consequent overvoltage might likely destroy the switches.

The switches have to be capable of being turned on and turned off in such a way as to avoid short circuits and sudden current interruptions. The commutation has to be actively controlled at all times with respect to the two above-mentioned basic rules. In order to explain the strategy it is helpful to refer to the simplified commutation circuit shown in Fig. 2.17 [142]. Taking into consideration the basic rules, it is important that no two bi-directional switches are switched on at any given instant (Fig. 2.17a). When the switches are turned on simultaneously, then the voltage sources will be shorted directly and the switches will be damaged due to over-currents. In the case where all the switches are turned off simultaneously (Fig. 2.17b), in the first instant after the switching-off an over-voltage will be generated which could destroy the semiconductors. The spikes of over-voltage depend on load current and duration of current interruption ($u_{\text{spikes}} = L\mathrm{d}i_L/\mathrm{d}t$). These two considerations

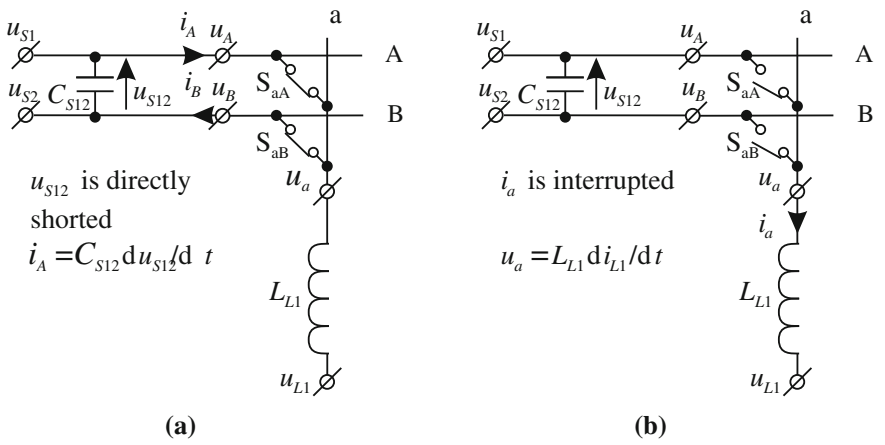


Fig. 2.17 Disallowed switch configurations in MC: **a** short circuit of capacitive input, **b** open circuit of inductive load

cause a conflict since semiconductor devices cannot be switched instantaneously between states because of propagation delays and finite switching times.

Various methods have been proposed to avoid this difficulty and to ensure successful commutation. To fulfil commutation requirements some knowledge of the commutation conditions is mandatory, e.g. the polarity of input voltage between the involved bi-directional switches or the polarity of load current. This part of the chapter offers an overview of different current commutation strategies in the MC. The first and second presented commutation methods intentionally break the rules of MC current commutation, which are mentioned above, and need extra circuitry to avoid destruction of the switches.

The first is based on a dead-time method which is commonly used in inverter systems. Using dead-time commutation would cause an open circuit of the load [32, 142]. This would result in large voltage spikes across the switches. This necessitates the use of snubbers or clamping devices across the switch cells to provide a path for the load current. In this method the commutation losses are relatively high. All commutation energy is lost in snubbers or clamping devices. Furthermore, the clamping devices increase converter volume. The MC snubbers are more complicated than snubbers in the VSI, due the bi-directional nature of the switch cells.

The second current commutation is known as the overlap commutation method [32]. This method also breaks the rules of MC current commutation. In overlap current commutation, the incoming switch is turned on before the outgoing switch is turned off [13]. During the overlap period extra line inductance is added to slow the rise of the current. The inductors are in the main conduction path, and the conduction losses will be increased. Furthermore, during the overlap period the load voltages are deformed. The switching time for each commutation is increased and will vary

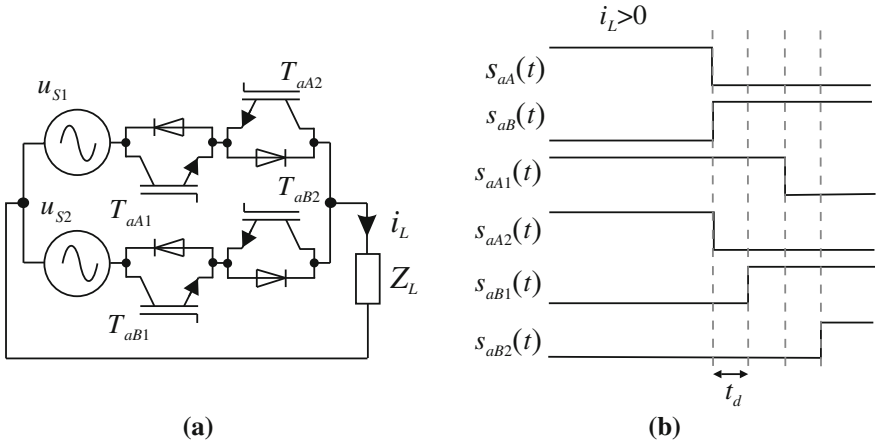


Fig. 2.18 For step commutation of bi-directional switches based on current direction for $i_L > 0$: **a**general commutation circuit of two bi-directional switches, **b** timing diagram

with level of voltage and inductor value. As a consequence, the switching frequency is decreased.

These two current commutation methods have disadvantages. Therefore, it is preferable to use advanced commutation methods. The commutation problem has been solved with the development of several multistep commutation strategies that allow safe operation of the switches. The most common solution is the four-step commutation strategy (or semi-soft current commutation) introduced by Burany in 1989 [20]. In this method the direction of current flow through the commutation cells can be controlled. In order to explain the strategy it is helpful to refer to the simplified commutation circuit shown in Fig. 2.18. The strategy assumes that when the output phase is connected to an input phase, both the IGBTs of the bi-directional switch S_1 have to be turned on simultaneously. The following example assumes that the load current ($i_L > 0$) is in the direction as shown in Fig. 2.18a and the upper bi-directional switch (S_1) is closed. In this method, the current direction is used to determine which device in the active switch cell is not current conducting. The commutation process is shown as a timing diagram in Fig. 2.18b. In the beginning, both IGBTs of switch S_1 are turned on in the same instant. In the first step, the IGBT T_{aA2}, which is not conducting the load current, is turned off. In the second step, after delay interval time t_d, the transistor T_{aB1} that will conduct the current is turned on. This allows both cells to be turned on without short circuiting the input phases and provides a path for the load current. Depending on the instantaneous input voltages, there are two kinds of commutation process after the second step. If $u_{S2} > u_{S1}$ and $i_L > 0$, then the conducting diode of switch cell S_1 could be reverse biased and a natural commutation could take place. In the third step the IGBT T_{aA1} is turned off. If there is no natural commutation during the second step, then a hard commutation happens when, in the third step, IGBT T_{aB1} is turned off. A short time later, in the fourth

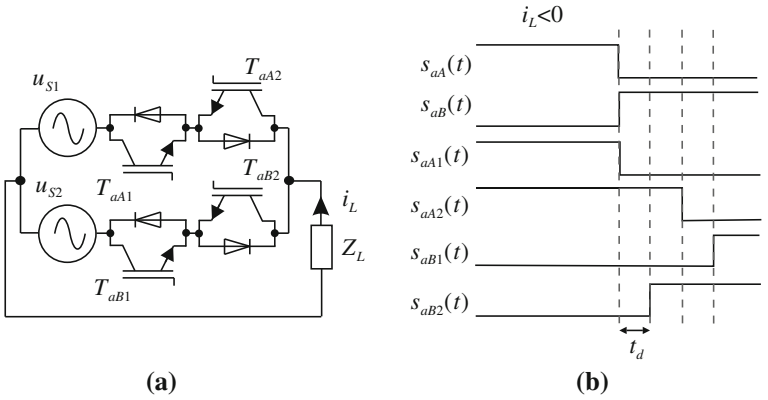


Fig. 2.19 For step commutation of bi-directional switches based on current direction for $i_L < 0$: **a** general commutation circuit of two bi-directional switches, **b** timing diagram

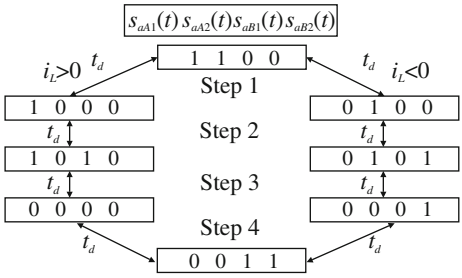


Fig. 2.20 Four-step commutation based on current direction switching diagram for two bi-directional switches from Fig. 2.18a ($i_L > 0$) and from Fig. 2.19a ($i_L < 0$)

step, transistor T_{aB2} is turned on to also allow the conduction of negative currents. The time delay has to be set to a value higher than the maximum propagation time of the IGBT signals. In this commutation method half of the commutation process is soft switching and half is hard switching. As a result this method is often called semi-soft current commutation [142]. Problems occur, however, at low current levels when the direction of the current is not certain and incorrect decisions are made as to which switches conduct the load current. This can be a problem if no protection device is employed. The simplified commutation circuit and timing diagram for the second condition $i_L < 0$ is shown in Fig. 2.19. A state diagram of the commutation process for a four-step commutation sequence between two bi-directional switches from Figs. 2.18a and 2.19a is shown in Fig. 2.20.

A simplification of the four-step current commutation method is to only gate the conducting device in the active switch cell [105, 124]. The non-conducting IGBTs are turned off during the commutation process and steady-state condition. Then there is created a simple two-step current commutation strategy, as shown in Fig. 2.21a. Current reversal is achieved by turning on the reverse transistor in the switch cell when the current falls below a threshold level (Fig. 2.21b). If the current achieves a value above the threshold level in the opposite direction, the initial device is turned

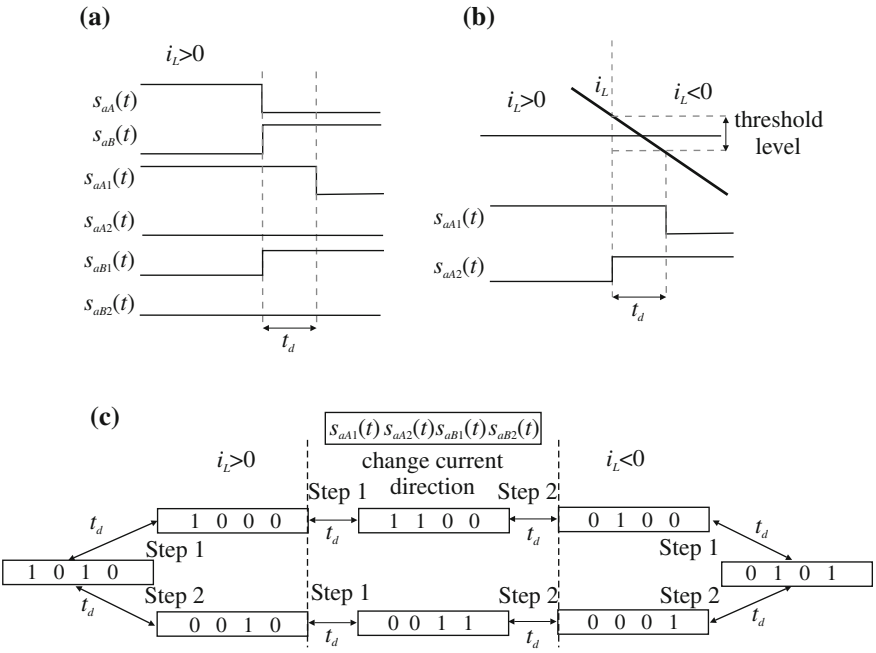


Fig. 2.21 Simple two-step current commutation: **a** timing diagram for commutation between two switches, **b** current reversal using threshold detection, **c** state diagram for the commutation process

off. A state diagram for the commutation process for a simple two-step commutation sequence between two bi-directional switches from Fig. 2.18a is shown in Fig. 2.21c.

This commutation method has practical limitations. During the current reversal period the current direction is unknown, because the current reversal switch is subject to hysteresis. During this time period the commutation cannot take place. Since the direction of current is unknown, the correct device that will conduct the current cannot be determined. The second disadvantage is that current direction can be difficult to determine, especially in high power drives when the levels of current are low and when the load current has to be within a threshold level. Then the threshold level may also be relatively large. This may result in a distorted current waveform.

For current commutation techniques it is required to know the load phase current direction. High precision determination of the direction of current is a key issue. Any inaccuracies cause errors, which result in switching losses and the possibility of destroying switch cells. To solve this problem a new technique has been developed [33]. This technique uses the voltage across the bi-directional switch to determine the current direction. This conception is based on an intelligent gate drive circuit. In addition, to control the IGBT this gate driver can also detect the current direction and enables the exchange of information between other gate driver devices. This process ensures that all gate drivers can operate with safe commutation.

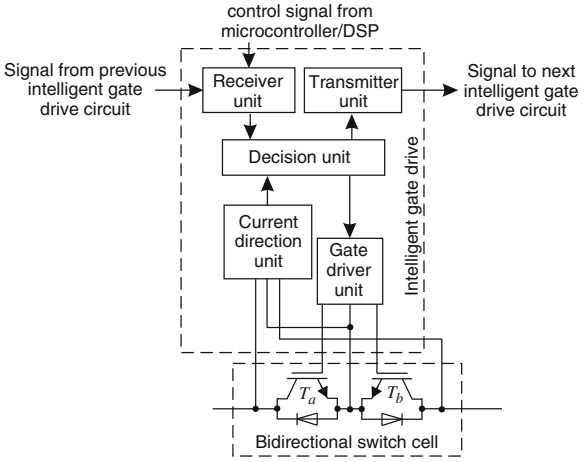
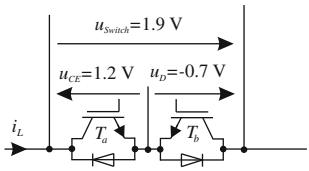


Fig. 2.22 Simplified block diagram of intelligent gate driver

Fig. 2.23 Voltage measurements in switch cell



A simplified block diagram of the intelligent gate driver is shown in Fig. 2.22 [33]. Current direction detection is based on voltage measurements across each of the devices in the commutation cell (Fig. 2.23). In the case which is shown in Fig. 2.23 the voltages are defined as follows: $u_{CE} = 1.2\,\mathrm{V}$ and depends on transistors used, $u_D = -0.7\,\mathrm{V}$. When load current is in the opposite direction the reverse situation exists. The current polarity is detected and can be calculated on the basis of the measured results. Information about current direction is sent to all intelligent gate drivers on the same output line.

The commutation process is as follows [33, 140]. Taking into consideration the current direction as shown in Fig. 2.18 and with the switch cell S_1 conducting (T_{aA1} is turned on), then the current direction information from the cell S_1 gate drive is passed to the gate drive for cell S_2. Transistor T_{aB1} is turned on and after delay time the transistor T_{aA1} is turned off. After a short time interval the current direction information is taken from the detection circuit in switch cell "B" rather than switch cell "A". The commutation is now complete. A timing diagram and state diagram for the commutation process for a two-step commutation sequence between two bidirectional switches with intelligent gate driver is shown in Fig. 2.24a, b, respectively. In this commutation method the current direction is known at any instant. If the detection circuit determines that the load current has fallen to zero then the intelligent gate driver sends this information to another gate driver.

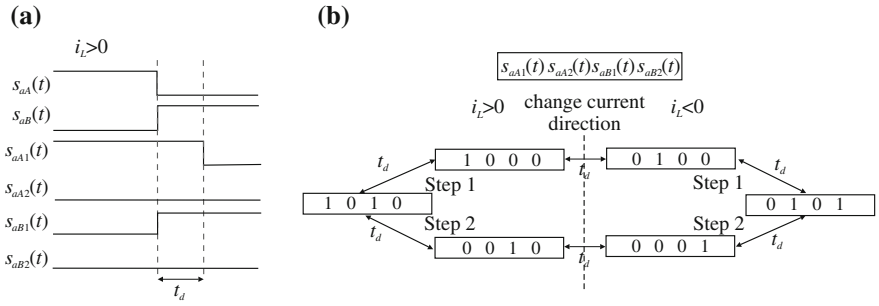


Fig. 2.24 Two-step current commutation with intelligent gate driver: **a** timing diagram for commutation between two switches, **b** state diagram for the commutation process

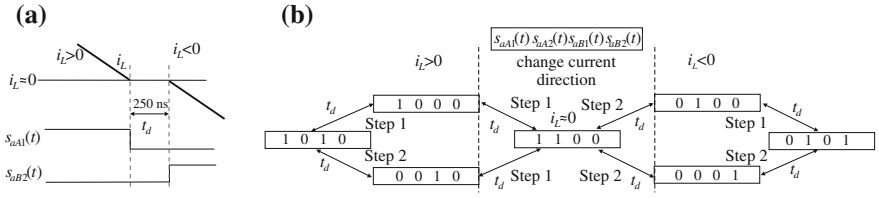


Fig. 2.25 Two-step current commutation with intelligent gate driver including propagation delay compensation: **a** timing diagram for commutation between two switches, **b** state diagram for the commutation process

A two-step current commutation method with intelligent gate driver also has special cases, where a potential difficulty occurs. One such case is when a commutation between switch cells occurs and the load current changes direction. The problem is due to the propagation delay in sending the data on the current direction to the next gate drive switch cell [33]. If a commutation between switch cells occurs first and then the information about the current direction reaches the next gate driver, then the wrong switch is turned on. This problem is solved by having a short dead time when the current reaches zero. During this time period no switches are turned on, as shown in Fig. 2.25. The reverse device is not gated until the new information is received by the other gate drivers. This delay time is small and only depends on the propagation delay inherent in the communication lines (typically 250 ns). This small dead time does not unduly distort the load current waveforms. A state diagram for the commutation process for a two-step commutation sequence between two bi-directional switches with intelligent gate driver and propagation delay compensation is shown in Fig. 2.25 [32, 33].

Some commutation was based on input voltage polarity measurements. To introduce this method input line-to-line voltages have to be measured in order to detect the polarity of the voltage across the two bi-directional switches involved in the commutation process. The operating principle is to provide, by proper control of active devices, the output current with freewheeling paths. Similar to the commutation

method based on current direction there are different number of commutation steps. The first is a four-step commutation strategy, which was presented in [3]. In general, the switching sequence depends on the voltage level switches involved in the commutation process. In this strategy both IGBTs of the conducting bi-directional switch are turned on. When commutation between switch cells occurs, the first stage is to determine the voltage level at the turned on and the turned off switch cells. This is needed to identify within the two commutating bi-directional switches the active devices that will operate as freewheeling devices. In general, the freewheeling devices are as follows:

1. the devices which allow the current flow from source to load in the lower input voltage phase;
2. the devices which allow the current flow from load to source in the higher input voltage phase.

After determination of freewheeling devices, the second action is switch commutation in the following four steps:

Step 1: the freewheeling device of the incoming switch is turned on;
Step 2: the non-freewheeling device of the outgoing switch is turned off;
Step 3: the non-freewheeling devices of the incoming switch is turned on;
Step 4: the freewheeling device of the outgoing switch is turned off.

The above described commutation process is depicted in Fig. 2.26a. A state diagram of the commutation process for a four-step commutation sequence between two bi-directional switches with voltage polarity measurement is shown in Fig. 2.26b [29].

Another input voltage measurement-based commutation strategy was presented by Ziegler and Hofmann in [152]. It is based on the basic operating principle of providing a freewheeling path for both output current polarities at any given time, for devices with either steady- or transient-state combinations. This commutation method is called METZI and is based on the detection of the six time intervals as

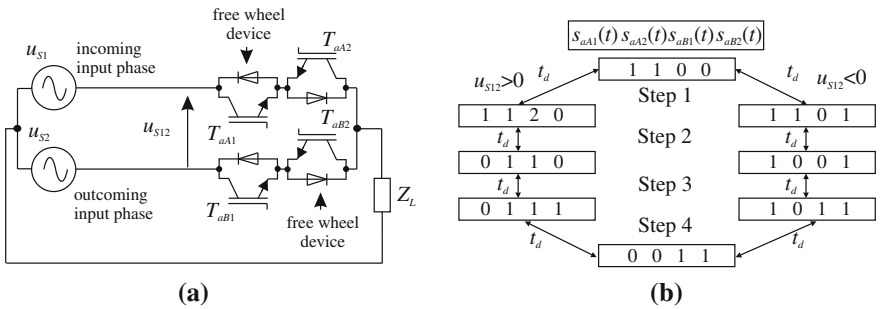


Fig. 2.26 Four-step voltage polarity measurement commutation method; **a** general commutation circuit, **b** switching diagram

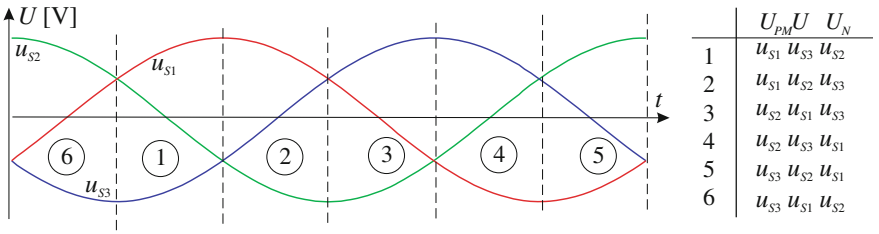


Fig. 2.27 Description of input voltages intervals in METZI method

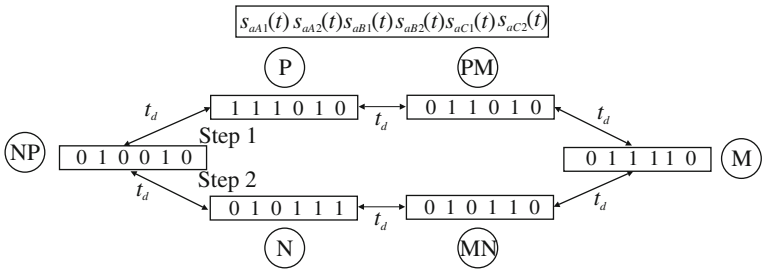


Fig. 2.28 Switching diagram for two-step METZI commutation method

shown in Fig. 2.27. METZI commutation is considered for each load phase. The two-step commutation is obtained by using more active devices in either steady or transient states. Four of the six switches are turned on in every major state. Two switches are turned on to ensure a bi-directional path for the load current, and the redundant two switches are turned on for two-step commutation. In every time interval (Fig. 2.27) one input line has the highest voltage U_P, one the lowest U_N and one the middle U_M. There are six switching states, three major states (P, M, N) and three intermediate states (PM, MN, NP) for each output phase, as shown in the state diagram in Fig. 2.28. Then two-step commutation rules are defined as follows [58]:

Step 1: turn off all switches which will not be switched on in the target base state; the auxiliary state will be reached;
Step 2: turn on the switches of the target base state; the target state will be reached.

Figure 2.29 shows the example of commutation from phase P to phase M with METZI commutation method.

The implementation of this method requires a very accurate measurement of the input voltage. When implementing this method, some problems are presented at the zero crossing points of the line-to-line voltage, as depicted in Fig. 2.30. The improved commutation method, which takes into account critical regions during the zero crossing point of the line to line voltage, is presented in [150]. The critical sequence is replaced by two uncritical sequences which will be commutated to the

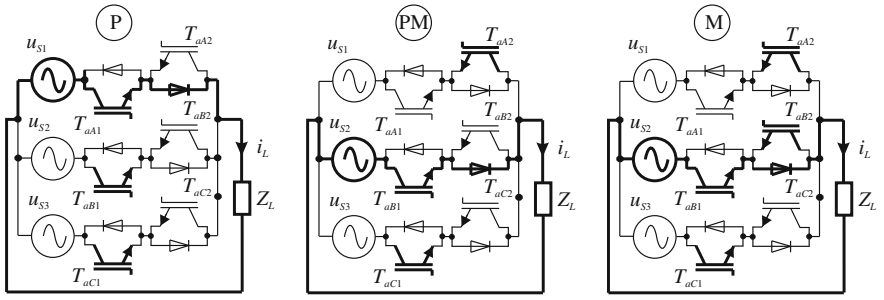


Fig. 2.29 Two-step METZI commutation from phase P to phase M

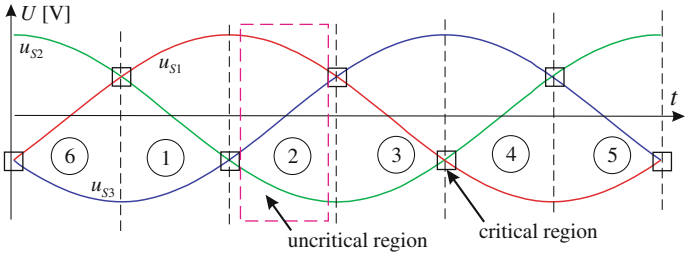


Fig. 2.30 Critical regions for commutation strategies based on the voltage polarity detection

remaining third input phase and then to the desired destination phase. A few other solutions of commutation in critical regions are presented in papers [53, 96, 97, 118].

The disadvantages of the previously presented commutation strategies can be partially avoided by using a commutation strategy where both output current and input line-to-line voltage sign are measured. This strategy was proposed in [29] and is realised by three steps. The first key advantage of this commutation strategy is that output current commutates between the off-going and on-going bi-directional switch always at the same instant with respect to the beginning of the commutation process. The second advantage of the proposed three-step commutation strategy is to decrease the value of the minimum duty cycle the converter is able to apply.

The strategy assumes that when the output phase is connected to an input phase both the IGBTs of the bi-directional switch S_1 have to be turned on simultaneously, allowing an automatic output current reversal. With the knowledge of the output current direction and line-to-line input voltage polarity between off-going and on-going phases the commutation rules are defined. There are two different three-step switching sequences, which depend on the voltage polarity. If the output current is positive, then the following two-switching sequences are used, where u_{S12} is denoted as in Fig. 2.26 [29]:

Sequence 1 $u_{S12} > 0$: In the first step the IGBT that is not carrying the current in the off-going switch cell is turned off and simultaneously the IGBTs that will carry the current in the on-going switch cell is turned on. Then, in the second step, the IGBT

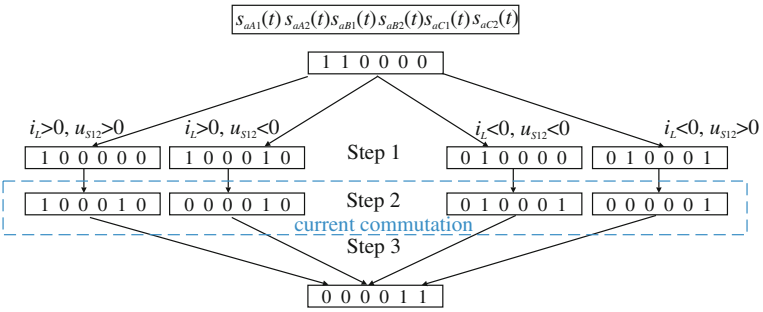


Fig. 2.31 Switching diagram for both three-step voltage and current polarity measurement commutation method

still gated in the off-going switch cell is turned off. In the last step the IGBTs that will not carry the current in the on-going switch-cell are turned on.

Sequence 2 $u_{S12} < 0$: In the first step the IGBT that is not carrying the current in the off-going switch cell is turned off first. In the second step, the IGBT that will carry the current in the on-going switch cell is turned on. In the last step the IGBT still gated in the off-going switch cell is turned off and simultaneously the IGBT that will not carry the current in the on-going switch cell is turned on.

A state diagram for the commutation process for a three-step commutation sequence between two bi-directional switches with both voltage and current polarity measurement is shown in Fig. 2.31. The dashed contour indicates the state of the switching sequences in which the current commutates. In Fig. 2.31 the commutation sequence for negative polarity of output current is also shown. Detailed information about the advantages of a three-step commutation strategy is presented in [29].

The commutation strategies presented above are the most well known and concern the bi-directional switch cell with IGBT and reverse diodes. In the literature can be found more variants of the presented commutation with different numbers of steps [56, 58, 118, 119, 137, 139, 151].

Recently, a reverse-blocking insulated gate bipolar transistor (RB-IGBT) was developed as an alternative solution for MC bidirectional switches [67]. This RB-IGBT is based on the ultrathin-wafer technology, and one unique feature is that its reverse leakage current is closely related to u_{GE}. When the RB-IGBT operates in reverse blocking condition, then a positively biased u_{GE} can reduce the reverse leakage current significantly. In an MC with the anti-parallel RB-IGBT, the previously presented commutation methods based on load current direction measurements or input voltages polarity measurements can be used, as presented in [67, 71]. However, a novel commutation method for an MC with RB-IGBT has been developed. A detailed description of this method is shown in [123], and it is based on RB-IGBT properties in reverse blocking condition. This method is implemented by utilizing load current direction signals and input voltage relations. A simplified commutation circuit of RB-IGBT is shown in Fig. 2.32. Taking into account the circuit in Fig. 2.32,

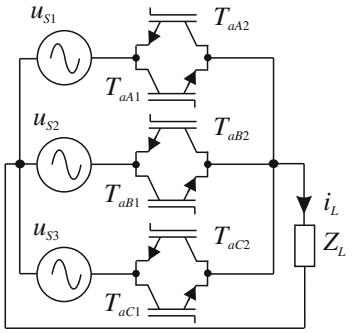


Fig. 2.32 Simplified commutation circuit with RB-IGBT

for different combinations of load current direction, and input voltage relationship, there are eight possibilities altogether, as summarised in Table 2.4 [123].

Soft switching is the commutation method which removes the switching losses associated with hard switching, allowing for higher switching frequencies to be used with reduced EMC emissions. Soft switching is the switching of devices when either a zero voltage or zero current condition occurs. The theory of soft commutation in MC is well known. The techniques developed fall into two categories: resonant switch circuits [32, 107, 136] and auxiliary resonant circuits [14, 18, 30, 57, 131].

The example of a resonant switch cell with common emitter connected IGBT and diode bridge arrangement is shown in Fig. 2.33. The soft switched cell shown in Fig. 2.33a consists of a standard common emitter anti-parallel IGBT and diode cell with one extra IGBT, two diodes, a capacitor, inductor and voltage source [32, 136]. For the following explanation, a simplified commutation circuit is connected similar to that in Fig. 2.26, but using a soft switch cell (cell one and cell two are assumed to be the incoming and outgoing switches, respectively). All transistors are turned on and turned off simultaneously. In the commutation between incoming and outgoing switches current flows from the supply of cell one through C_R and also through D_3, L_R, E, T_A and D_2. Current also flows through C_R of cell two and capacitor voltage u_{CR} charges linearly until it equals E. The element L_R and C_R of both cells forms a resonant circuit. When u_{CR} is equal to zero, D_1 starts to conduct ($I_{D1} = I_{LR} - I_L$). and inductor L_R discharges linearly through D_1 and D_3. When $I_{LR} = I_L$ transistor T_1 starts to conduct ($I_{T1} = I_L - I_{LR}$), and the inductor current is still linearly discharging. When $I_{LR} = 0$, transistor T_2 conducts the full i_L. This ensures that the main switches switch under zero voltage conditions and that the auxiliary switch switches under zero current conditions. The major problem with this soft switch is that the voltage source E is difficult to realise in a practical system.

It is seen from Fig. 2.33b that the presented bi-directional switch consists of a bridge rectifier (D_1, D_2, D_3, D_4), two transistors (T_1, T_2) a small inductor (L_R) and a capacitor (C_R). The transistors are turned on and turned off simultaneously. Current direction of inductor L_R and voltage polarity of capacitor C_R are unidirectional. The

Table 2.4 Commutation method of RB-IGBT

Condition	$u_{S1} > u_{S2}$ and $u_{S1} > u_{S3}$ and $i_L > 0$							$u_{S1} > u_{S2}$ and $u_{S1} > u_{S3}$ and $i_L < 0$						
		T_{aA1}	T_{aA2}	T_{aB1}	T_{aB2}	T_{aC1}	T_{aC2}		T_{aA1}	T_{aA2}	T_{aB1}	T_{aB2}	T_{aC1}	T_{aC2}
	Initial state:	1	1i	0	1	0	1	Initial state:	1i	1	0	1	0	1
	Step 1:	1	0	0	1i	0	0	Step 1:	1i	0	0	1	0	0
	Step 2:	1	0	1	1i	0	0	Step 2:	1	0	1i	1	0	0
Condition	$u_{S1} < u_{S2}$ and $u_{S1} > u_{S3}$ and $i_L > 0$							$u_{S1} < u_{S2}$ and $u_{S1} > u_{S3}$ and $i_L < 0$						
		T_{aA1}	T_{aA2}	T_{aB1}	T_{aB2}	T_{aC1}	T_{aC2}		T_{aA1}	T_{aA2}	T_{aB1}	T_{aB2}	T_{aC1}	T_{aC2}
	Initial state:	1	1i	1	0	0	1	Initial state:	1i	1	1	0	0	1
	Step 1:	0	1i	1	0	0	1	Step 1:	0	1	1i	0	0	1
	Step 2:	0	1	1	1i	0	1	Step 2:	0	1	1i	1	0	1
Condition	$u_{S1} > u_{S2}$ and $u_{S1} < u_{S3}$ and $i_L > 0$							$u_{S1} > u_{S2}$ and $u_{S1} < u_{S3}$ and $i_L < 0$						
		T_{aA1}	T_{aA2}	T_{aB1}	T_{aB2}	T_{aC1}	T_{aC2}		T_{aA1}	T_{aA2}	T_{aB1}	T_{aB2}	T_{aC1}	T_{aC2}
	Initial state:	1	1i	0	1	1	0	Initial state:	1i	1	0	1	1	0
	Step 1:	1	0	0	1i	1	0	Step 1:	1i	0	0	1	1	0
	Step 2:	1	0	1	1i	1	0	Step 2:	1	0	1i	1	1	0
Condition	$u_{S1} < u_{S2}$ and $u_{S1} < u_{S3}$ and $i_L > 0$							$u_{S1} < u_{S2}$ and $u_{S1} < u_{S3}$ and $i_L < 0$						
		T_{aA1}	T_{aA2}	T_{aB1}	T_{aB2}	T_{aC1}	T_{aC2}		T_{aA1}	T_{aA2}	T_{aB1}	T_{aB2}	T_{aC1}	T_{aC2}
	Initial state:	1	1i	1	0	1	0	Initial state:	1i	1	1	0	1	0
	Step 1:	0	1i	1	0	0	0	Step 1:	0	1	1i	0	0	0
	Step 2:	0	1	1	1i	0	0	Step 2:	0	1	1i	1	0	0

where *1* RB-IGBT turn-on and non-conducting current, *1i* RB-IGBT turn-on and conducting current, *0* RB-IGBT turn-off

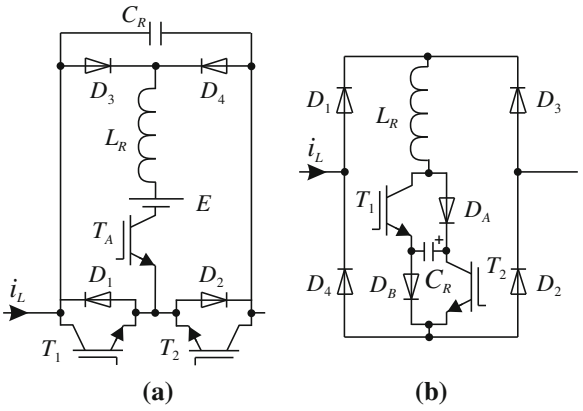


Fig. 2.33 Soft switched cell with: **a** common emitter connected IGBT, **b** diode bridge arrangement

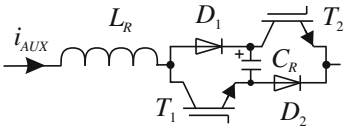


Fig. 2.34 Unidirectional auxiliary resonant components

circuit operation from Fig. 2.33b is described in [32, 107]. The capacitor voltage polarity before turning on is shown as in Fig. 2.33b, to reverse biasing diodes D_A and D_B. When T_1 and T_2 are turned on, i_{T1} and i_{T2} will increase from zero resulting in zero current switching. The voltage of C_R decays to zero and the diodes D_A and D_B become forward biased. Then the current flows through both IGBT and its series diode D_A and D_B. Next, the turning off process is as follows. When T_1 and T_2 are turned off, the switch voltages (U_{T1} and U_{T2}) will increase from zero resulting in zero voltage switching. Hence, the capacitor serves as a snubber to eliminate the voltage spike. The inductor current will fall to zero and the capacitor will be charged ready for the another turning on process.

In the solution with the presented soft switch cells the switching losses are decreased but the conduction losses are increased due to the extra devices in the main conduction path. Another disadvantage of this switch configuration is the increase in the number of components.

The second soft commutation idea is to use auxiliary resonant components on each output phase of the matrix converter in the attempt to force the current or voltage to zero during commutation [18]. The proposed circuit using auxiliary resonant switches is shown in Fig. 2.34 [18]. Two such switches are used for each output phase, one for positive load current and one for negative load current as shown in Fig. 2.35.

The circuit operation of Fig. 2.34 is similar to that of the circuit in Fig. 2.33b. The auxiliary resonant switch in the configuration shown in Fig. 2.35 is to conduct the

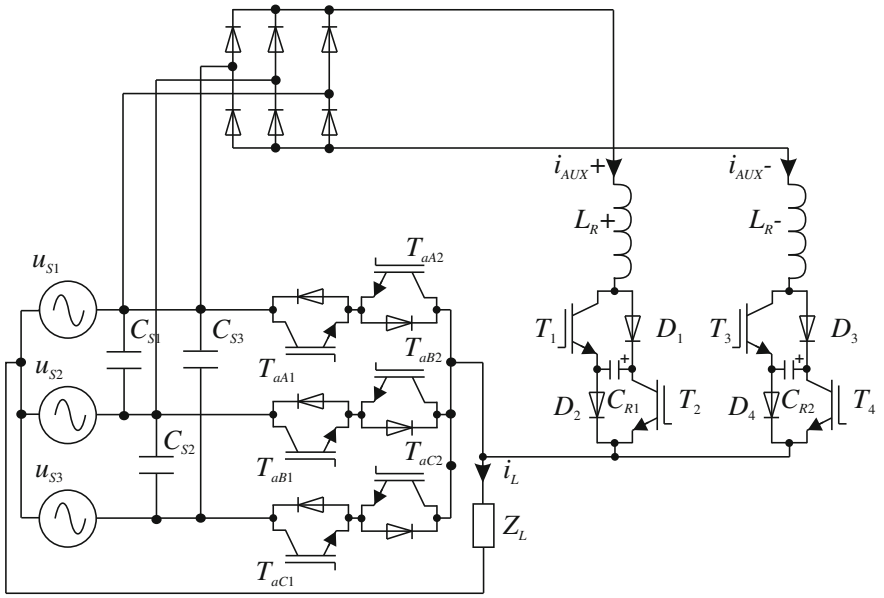


Fig. 2.35 Single phase of MC with the auxiliary resonant components

load current during commutation allowing ZCS of the main switches. Because of this, the conduction loss will not be significantly increased compared to a converter using non-resonant techniques. Auxiliary resonant circuits will also increase the component count but not to the same extent as circuits using soft switching cells. An advantage of this type of circuit is that the auxiliary resonant components can be disabled when operating at low voltage or current. Another concept of auxiliary resonant components on each output phase of the MC is presented in [57].

Another concept of soft switching with auxiliary resonant components is the auxiliary resonant commutated pole structure (ARCP), which has been fully analysed in [14, 30, 131]. Three different ARCP-MC topologies previously proposed are shown in Fig. 2.36. Unfortunately, the control complexity of the ARCP-MC is significantly higher than that of the MC. The number of elements is also increased.

All these soft switching circuits (Figs. 2.33, 2.34, 2.35, Fig. 2.36) significantly increase the component count in the MC, and increase conduction losses. Furthermore, a modification of the MC control algorithm is required.

Protection Issues

In the previous subsection a convenient manner of commutating the IGBTs was discussed. It was noted that in some cases there are over-voltages that should be managed appropriately to avoid semiconductor destruction [95, 105]. Other sources of over-voltages are grid perturbations and fault states in the load and, therefore, it is important to have a method of dealing with these phenomena. An effective and

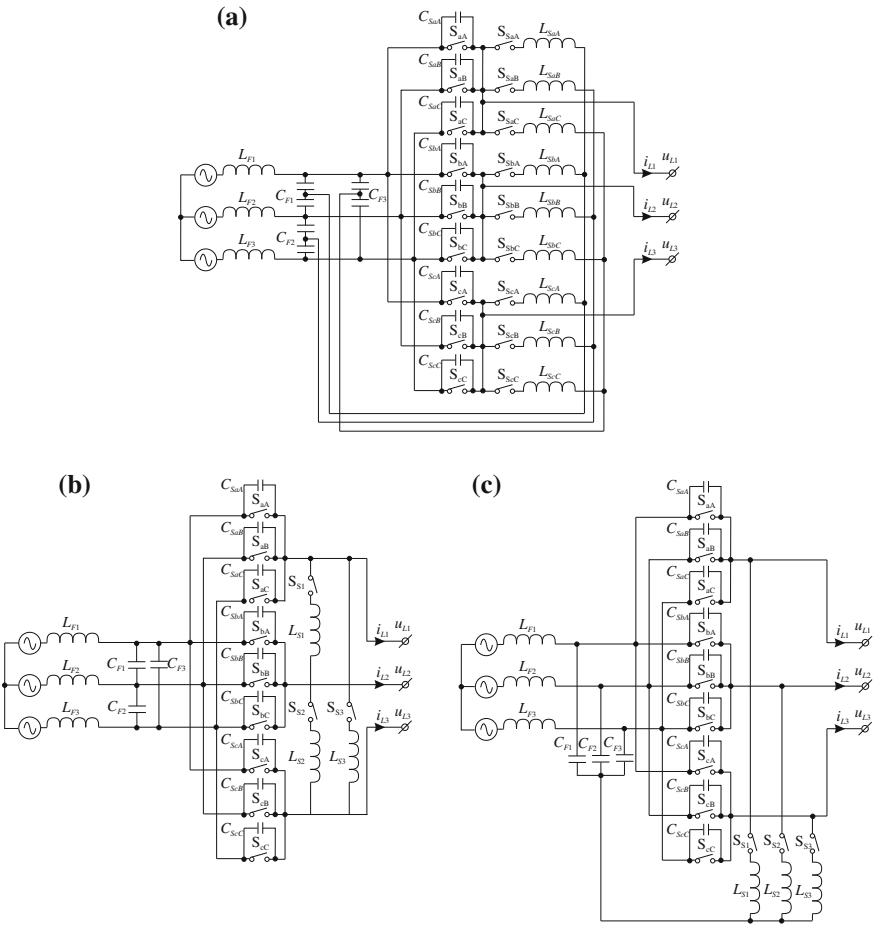


Fig. 2.36 MC auxiliary resonant commutated pole (MC-ARCM), **a** concept I, **b** concept II, **c** concept III [131]

robust protection scheme is an important element in the implementation of a stable and reliable power stage in MCs.

In [135] the first protection circuit was proposed, consisting of input and output diode bridges, an electrolytic capacitor and its charge and discharge circuit. Figure 2.37 shows this over-voltage circuit [94, 95], which is the most common solution for avoiding over-voltages coming from the grid and from the motor. This clamp configuration uses 12 fast-recovery diodes to connect the capacitor to the input and output terminals. Then a capacitor takes the commutation energy and the resistor can discharge the capacitor. When over-voltage occurs, (in the case of a hard commutation and abnormal operation of the motor) the diode conducts and the *RC* circuit maintains the voltage level at a safe value. In normal operation, the diodes

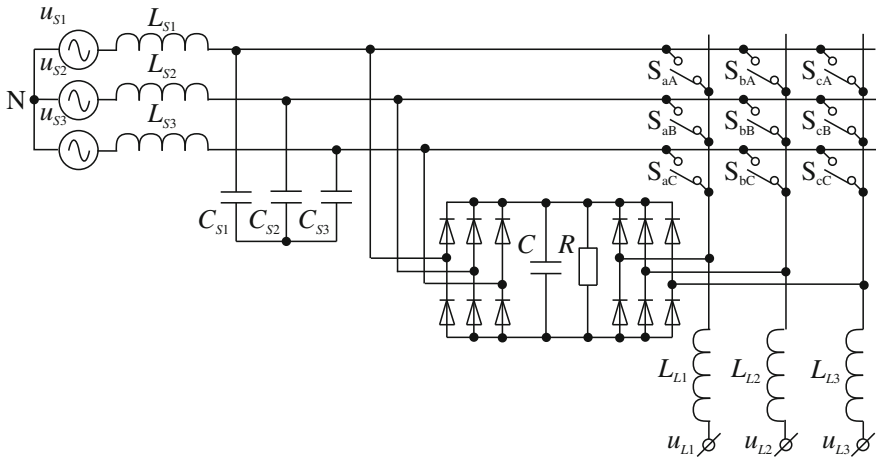


Fig. 2.37 Matrix converter with a 12-diode protected clamp circuit

are off and the clamp circuit has no influence on the MC operation. In the case of a drive system, when all the switches are turned off, the current in the load is suddenly interrupted. The energy stored in the motor leakage inductance has to be discharged without creating dangerous over-voltages. Then, a shut-down of the converter can be made by reducing the power to the machine, causing no interruption of the motor current.

The energy stored in DC capacitors is discharged in the resistor [5, 6, 75] or is used to feed the control electronics and to magnetise the motor-ride-through capability [74]. This over-voltage protection circuit has the advantages of being very simple, it has low hardware requirements and simple control strategies. However, this circuit (Fig. 2.37) has some drawbacks, such as the high number of required semiconductor devices (12 fast-recovery auxiliary diodes). The reduction of diodes to six is possible in the over-voltage protection circuit, depicted in Fig. 2.38. In this topology six additional diodes for the power bi-directional switches are used [101]. In both these protected circuits the electrolytic capacitor has a large volume which constrains the lifetime of the system. The discharge circuit by a DC chopper increases the number of power devices.

On the other hand, a varistor protection and a suppressor diode protection were proposed in [95]. Figure 2.39 shows the varistor location. Varistors are connected at the input and at the output terminals of MC. These protections are very useful for a small capacity system, but not suitable for a large capacity system. The protection strategy with varistor over-voltage protection allows the removal of the large and expensive diode clamp. The input varistor has to protect the converter switches from the voltage surges coming from the AC mains. At the output side, the varistor protect the MC power stage devices from a hard converter shut-down or a converter error during a commutation process. During normal operations the losses caused

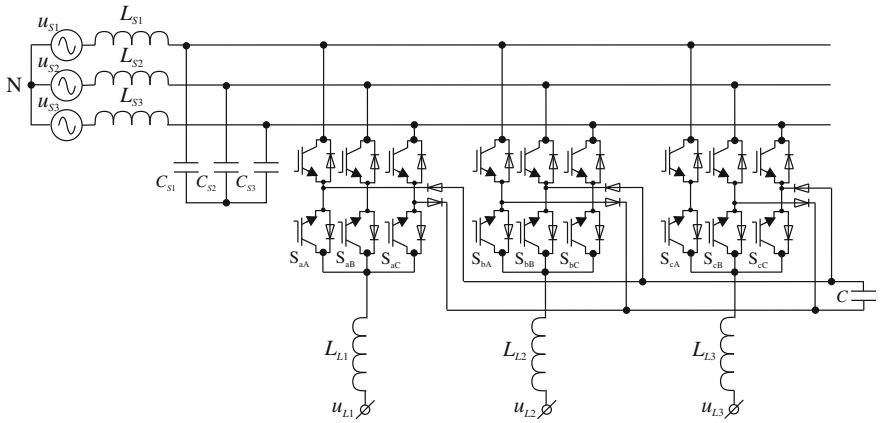


Fig. 2.38 Matrix converter with a 6-diode protected clamp circuit

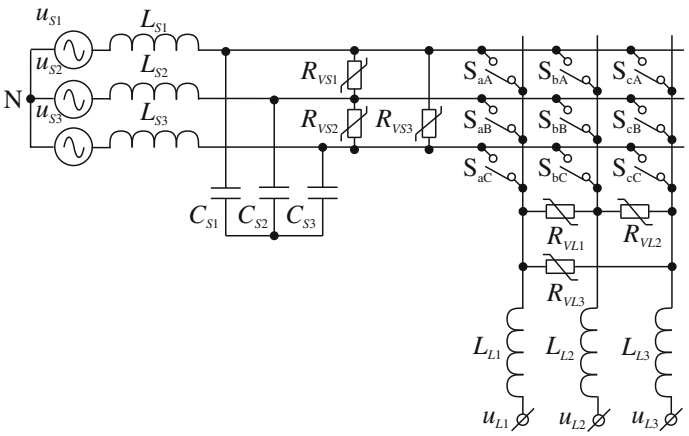


Fig. 2.39 Matrix converter with varistor protection

by the varistors are not worth mentioning. Unfortunately, the varistor triangles by themselves are not sufficient to guarantee during a converter shut-down a reliable protection of the IGBTs. Then a simple extra circuit to protect each IGBT is required. A problem occurs when a turning off bi-directional switch achieves its blocking capability with a certain delay in respect to the others. The neighbouring IGBT having its full blocking capability may get the maximum clamping voltage of the varistor, causing damage to this device. In order to protect the single IGBT, a circuit made up with a suppressor diode is added to any IGBTs. Figure 2.40 shows the IGBT with a suppressor diode. To ensure a good performance and lifetime of the MC a combination of both varistor and suppressor diode protection is required [95].

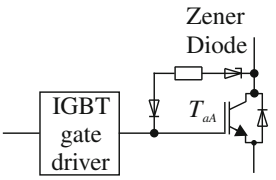


Fig. 2.40 IGBT gate driver with suppressor diode protection

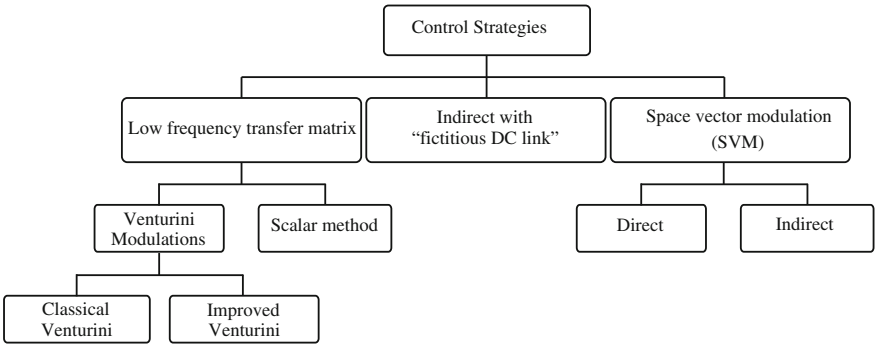


Fig. 2.41 Classification of MC modulation techniques [126]

As shown in Fig. 2.40, the protection IGBT circuit with suppressor diode uses the Zener diode, with a high breakdown voltage [95]. But the Zener breakdown voltage has to be lower than the maximum blocking voltage of the IGBT. Then, the operation of the suppressor diode is as follows: if the collector–emitter voltage of the IGBT increases to a value higher than that of the breakdown voltage of the suppressor diode, this diode becomes conductive. The gate of the IGBT is charged again. Each IGBT can be protected in this way because the IGBT becomes conductive and destructive voltage is eliminated.

Modulation techniques

The complexity of the matrix converter topology makes the study and the determination of suitable modulation strategies a hard task. A review of the well-known modulation techniques is presented in this paragraph. From this unitary point of view, some modulation techniques are described and compared with reference to maximum voltage transfer ratio. Several modulation strategies have been proposed in previous work [3, 4, 17, 21–28, 54, 55, 61, 62, 65, 106, 108–113, 133–135, 142, 148, 155, 156]. These modulation strategies give different voltage conversion ratios and the number of commutations employed in each modulation strategy is different. A modulation strategy can be broadly classified into three categories, depending upon the type of calculation of switch states. Figure 2.41 shows the tree of such classification of MC modulation techniques [126].

The MC bi-directional power switches work with a high switching frequency. A low frequency load voltage of variable amplitude and frequency can be generated by modulating the duty cycle of the switches using their respective switching functions

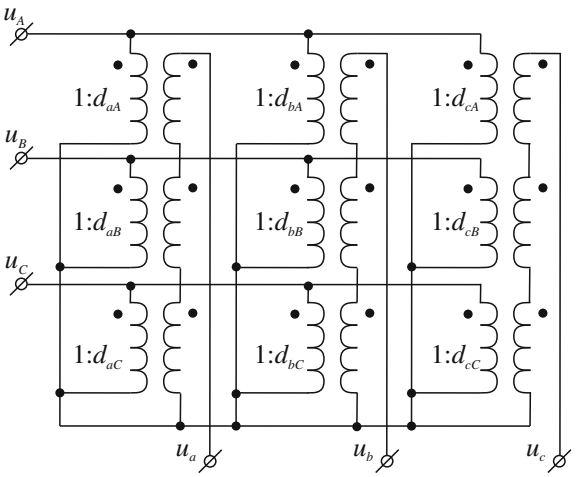


Fig. 2.42 Matrix converter averaged-switching-cycle representation

s_{jK}. A modulation duty cycle should be defined for each switch in order to determine the average behaviour of the MC output voltage waveform [110, 135, 142]. The modulation duty cycle is defined by:

$$d_{jK}(t) = \frac{t_{jK}}{T_{\text{Seq}}}, \tag{2.8}$$

where t_{jK} represents the time when switch S_{jK} is turned on and T_{Seq} represents the time of the complete sequence in the PWM pattern, and $0 < d_{jK} < 1$. Based on the switch duty-ratios, the averaged output voltages and the averaged input currents can be related to the input voltages and the output currents, respectively, as [142]:

$$\bar{\mathbf{u}}_L = \mathbf{M}(t)\mathbf{u}_S, \qquad \bar{\mathbf{i}}_S = \mathbf{M}^T(t)\bar{\mathbf{i}}_L, \tag{2.9}$$

where:

$$\mathbf{M}(t) = \begin{bmatrix} d_{aA}(t) & d_{aB}(t) & d_{aC}(t) \\ d_{bA}(t) & d_{bB}(t) & d_{bC}(t) \\ d_{cA}(t) & d_{cB}(t) & d_{cC}(t) \end{bmatrix}. \tag{2.10}$$

The matrix $\mathbf{M}(t)$ is known as the modulation matrix or low-frequency transfer matrix. Based on these relationships in (2.9) and (2.10), a matrix converter on a switching-cycle averaged basis can be represented by nine ideal transformers with varying turn-ratios, as shown in Fig. 2.42 [115].

Venturini Modulation Techniques

In 1980, Venturini and Alesina presented a PWM modulation method for the control of MCs [135]. The proposed method by these authors is known as the classical Venturini modulation or the direct transfer function approach. The modulation problem assumes that a set of sinusoidal load voltages, $u_L = [u_{L1}(t), u_{L2}(t), u_{L3}(t)]^T$ and source currents, $i_S = [i_{S1}(t), i_{S2}(t), i_{S3}(t)]^T$ are required:

$$\mathbf{u}_L = qU_{Lm}\begin{bmatrix}\cos(\omega_L t)\\ \cos(\omega_L t - 120)\\ \cos(\omega_L t + 120)\end{bmatrix}, \quad \mathbf{i}_S = qI_{Sm}\begin{bmatrix}\cos(\omega t + \varphi)\\ \cos(\omega t - 120 + \varphi)\\ \cos(\omega t + 120 + \varphi)\end{bmatrix}. \tag{2.11}$$

A set of input voltages and an assumed set of output currents are described as follows:

$$\mathbf{u}_S = U_{Sm}\begin{bmatrix}\cos(\omega_L t)\\ \cos(\omega_L t - 120)\\ \cos(\omega_L t + 120)\end{bmatrix}, \quad \mathbf{i}_L = I_{Lm}\begin{bmatrix}\cos(\omega t + \varphi)\\ \cos(\omega t - 120 + \varphi)\\ \cos(\omega t + 120 + \varphi)\end{bmatrix}, \tag{2.12}$$

where: q is the voltage transfer ratio, ω and ω_L are the input and output pulsation, respectively, and φ_S and φ_L are the input and output phase displacement angles, respectively. The low-frequency transfer matrix proposed by Venturini is described in [135] as:

$$\mathbf{M}(t) = \mathbf{M}^+(t) + \mathbf{M}^-(t), \tag{2.13}$$

where:

$$\mathbf{M}^+(t) = \frac{\alpha_1}{3}\begin{bmatrix}1+2qm^+(0) & 1+2qm^+(-\frac{2\pi}{3}) & 1+2qm^+(-\frac{4\pi}{3})\\ 1+2qm^+(-\frac{4\pi}{3}) & 1+2qm^+(0) & 1+2qm^+(-\frac{2\pi}{3})\\ 1+2qm^+(-\frac{2\pi}{3}) & 1+2qm^+(-\frac{4\pi}{3}) & 1+2qm^+(0)\end{bmatrix}, \tag{2.14}$$

$$\mathbf{M}^-(t) = \frac{\alpha_2}{3}\begin{bmatrix}1+2qm^-(0) & 1+2qm^-(-\frac{2\pi}{3}) & 1+2qm^-(-\frac{4\pi}{3})\\ 1+2qm^-(-\frac{2\pi}{3}) & 1+2qm^-(-\frac{4\pi}{3}) & 1+2qm^-(0)\\ 1+2qm^-(-\frac{4\pi}{3}) & 1+2qm^-(0) & 1+2qm^-(-\frac{2\pi}{3})\end{bmatrix}, \tag{2.15}$$

$$m^+ = \cos(\omega_m t + x), \quad m^- = \cos(-(\omega_m + 2\omega)t + x), \quad \omega_m = \omega_L - \omega, \tag{2.16}$$

$$\alpha_1 = \frac{1}{2}\left(1 + \frac{\tan(\varphi_S)}{\tan(\varphi_L)}\right), \quad \alpha_2 = \frac{1}{2}\left(1 - \frac{\tan(\varphi_S)}{\tan(\varphi_L)}\right). \tag{2.17}$$

Considering only the solution (2.14) ($\alpha_1 = 1, \alpha_2 = 0$), the phase displacement at the input is the same as at the output because $\varphi_S = \varphi_L$, whereas the solution (2.15) ($\alpha_1 = 0, \alpha_2 = 1$), yields $\varphi_S = -\varphi_L$ giving reversed phase displacement

at the input. If both solutions are combined (2.13), the result provides the means for input displacement factor control [142]. If $\alpha_1 = \alpha_2$ the input displacement factor at the converter terminals is unity, regardless of the loads character (load displacement factor). Through the choice of α_1 and α_2, there are the possibility to input displacement factor control [110, 142].

The solution presented by Eqs. (2.13)–(2.17) is characterised as a limitation of voltage transfer ratio q. In this approach, during each switch sequence time (T_{Seq}), the average load voltage is equal to the target voltage. For this to be possible it is clear that the target voltages must fit within the source voltage envelope for any load frequency (Fig. 2.43). Then, the voltage ratio is limited to $q_{\max} = 0.5$ [3, 4].

An improvement in the achievable voltage ratio to 0.866 ($\sqrt{3}/2$) is possible by adding common mode voltages to the target load voltages, as defined by Eq. (2.18) and as shown in Fig. 2.44. The matrix u_L of the target output voltages includes third harmonics of the source and load voltages. This new strategy is known as Venturini's optimum or improved method. The general conception of the improved Venturini control strategy is presented in research papers [3] and [4].

$$\mathbf{u}_L = \begin{bmatrix} U_{L1}\cos(\omega_L t) + U_{S1}\frac{\cos(3\omega t)}{4} - U_{L1}\frac{\cos(3\omega_L t)}{6} \\ U_{L2}\cos(\omega_L t + \frac{2\pi}{3}) + U_{S2}\frac{\cos(3\omega t)}{4} - U_{L2}\frac{\cos(3\omega_L t)}{6} \\ U_{L3}\cos(\omega_L t + \frac{4\pi}{3}) + U_{S3}\frac{\cos(3\omega t)}{4} - U_{L3}\frac{\cos(3\omega_L t)}{6} \end{bmatrix}. \tag{2.18}$$

According to [3] and [4] the transfer matrix in Venturini's improved modulation is described as follows:

$$\mathbf{M}(t) = \begin{bmatrix} m(0,\ 0,\ 0,\ 0,\ 0,\ 0)\ m(2,\ 4,\ 2,\ 4,\ 2,\ 4)\ m(4,\ 2,\ 4,\ 2,\ 4,\ 2) \\ m(2,\ 2,\ 0,\ 0,\ 0,\ 0)\ m(4,\ 0,\ 2,\ 4,\ 2,\ 4)\ m(0,\ 4,\ 4,\ 2,\ 4,\ 2) \\ m(4,\ 4,\ 0,\ 0,\ 0,\ 0)\ m(0,\ 2,\ 2,\ 4,\ 2,\ 4)\ m(2,\ 0,\ 4,\ 2,\ 4,\ 2) \end{bmatrix}, \tag{2.19}$$

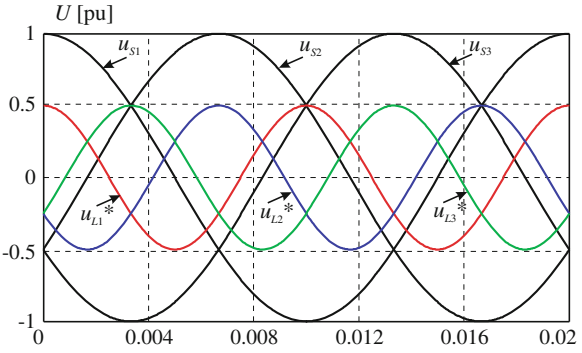


Fig. 2.43 Illustrating maximum voltage ratio of 0.5 for classical Venturini modulation

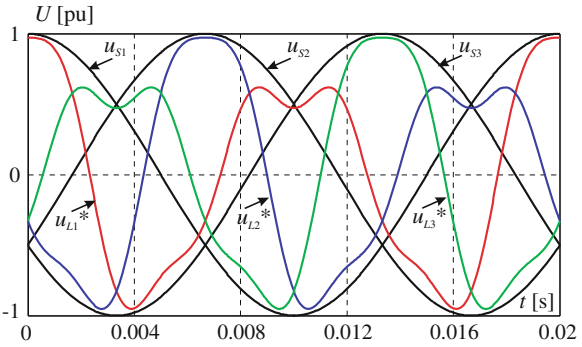
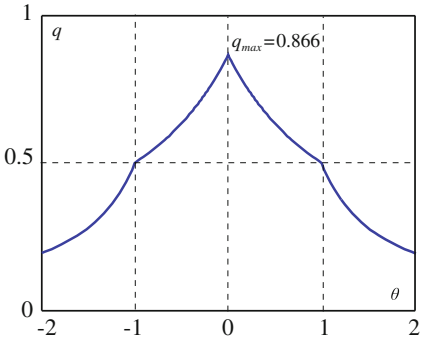


Fig. 2.44 Illustrating maximum voltage ratio of 0.866 for Venturini's improved modulation for $f_L = 100\,\text{Hz}$

Fig. 2.45 Voltage transfer ratio in MC with Venturini's optimum modulation as a function of input displacement factor



$$
\begin{aligned}
&m(x_1,\ x_2,\ x_3,\ x_4,\ x_5,\ x_6)\\
&\quad=\frac{1}{3}\left\{1+\frac{\sqrt{3}}{2}p\left[Z_1^1(x_1)+Z_1^{-1}(x_2)-\frac{1}{6}Z_3^1(x_3)-\frac{1}{6}Z_3^{-1}(x_4)\right.\right.\\
&\qquad\left.\left.+\operatorname{sign}(p)\left(-\frac{1}{6\sqrt{3}}Z_0^4(x_5)+\frac{7}{6\sqrt{3}}Z_0^2(x_6)\right)\right]+a_1Z_1^1(x_1)+a_2Z_1^{-1}(x_2)\right\},
\end{aligned}
\tag{2.20}
$$

$$
Z_\alpha^\beta(\gamma,t)=\cos\left((\alpha\omega_L+\beta\omega)t+\gamma\frac{\pi}{3}\right),
\tag{2.21}
$$

$$
a=2|\theta|q,\qquad p=\frac{1}{\sqrt{3}}(2q-a),\qquad \theta=\frac{\tan(\varphi_S)}{\tan(\varphi_L)},
\tag{2.22}
$$

and: ($a_1 = a$ i $a_2 = 0$) where $\theta < 0$, ($a_2 = a$ i $a_1 = 0$) where $\theta > 0$, ($a_1 = a_2$) where $\theta = 0$.

An input displacement factor can be a control which uses Eqs. (2.18)–(2.22). Unfortunately, if the input displacement factor is different from unity, the voltage ratio limit will be reduced from 0.866 to a small value, which depends on the displacement

factor achieved in the input site. The maximum voltage ratio is described by Eq. (2.23) and is shown in Fig. 2.45.

$$2q\left[|\theta|\left(1-\frac{\text{sign}(p)}{\sqrt{3}}\right)+\frac{\text{sign}(p)}{\sqrt{3}}\right]\leq 1, \tag{2.23}$$

where: $\text{sign}(p)=\begin{cases}1, & p\geq 1\\ -1, & p\leq 0\end{cases}$.

Scalar modulation methods

A second type of MC modulation based on a low-frequency transfer matrix is the scalar method. The basic rules of this control were first proposed by Roy, in 1987 [113]. In the proposed modulation method the switch actuation signals are calculated directly from measurements of the source phase voltages. According to [111–113], the value of any instantaneous load phase voltage may be expressed by the following equations:

$$u_L=U_{Lm}\cos(\omega_L t)=\frac{1}{T_{\text{Seq}}}(t_K u_K+t_L u_L+t_M u_M), \tag{2.24}$$

$$t_K+t_L+t_M=T_{\text{Seq}}, \tag{2.25}$$

where K–L–M are names of subscripts which change according to the rules below:

Rule 1: At any instant, the source phase voltage which has a polarity different from both others is assigned to "M".
Rule 2: The two source phase voltages which share the same polarity are assigned to "K" and "L", the smallest one of the two (in absolute value), being "K".

Then t_K and t_L are chosen such that:

$$\frac{t_K}{t_L}=u_K u_L=\rho_{KL}\qquad 0\leq\rho_{KL}\leq 1. \tag{2.26}$$

In a balanced three-phase system, the pulse duty factors are given as:

$$\begin{aligned} m_{jL}&=\frac{t_L}{T_{\text{Seq}}}=\frac{(u_j-u_M)u_L}{1.5U_{Sm}^2}\\ m_{jK}&=\frac{t_K}{T_{\text{Seq}}}=\frac{(u_j-u_M)u_K}{1.5U_{Sm}^2}\\ m_{jM}&=\frac{t_K}{T_{\text{Seq}}}=1-\frac{t_K+t_L}{T_{\text{Seq}}}=1-(m_{jL}+m_{jK}) \end{aligned}, \tag{2.27}$$

where: $j=\{\text{a, b, c}\}$ which is the name of load phase.

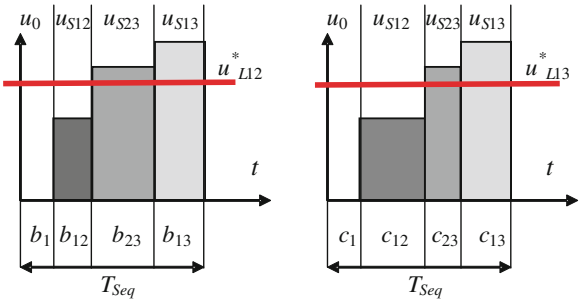


Fig. 2.46 Synthesising of output line-to-line voltages by three line-to-line source voltages in MC witch scalar modulation

The presented MC scalar modulation provides a voltage transfer ratio equal to 0.5 similar to Venturini modulation. Again, common mode addition is used with the target output voltages, to achieve a 0.866 voltage ratio capability.

Development of the Roy concept is presented by Ishiguro et al. in [65]. In the proposed modulation method the switch actuation signals are calculated directly from measurements of the line-to-line source voltages and from the demands of the load line-to-line voltages. The requirements of the output line-to-line voltages u^*_{L12} and u^*_{L13} are synthesised in each sequence period T_{Seq} by using the three input line-to-line voltages u_{S12}, u_{S23}, u_{S31} and zero voltage u_0 as follows (Fig. 2.46):

$$\begin{aligned} u^*_{L12} &= b_{12}u_{S12} + b_{23}u_{S23} + b_{13}u_{S13} + b_1u_0 \\ u^*_{L13} &= c_{12}u_{S12} + c_{23}u_{S23} + c_{13}u_{S13} + c_1u_0 \end{aligned}, \tag{2.28}$$

where:

$$\begin{aligned} b_{12} + b_{23} + b_{13} + b_1 &= 1 \\ c_{12} + c_{23} + c_{13} + c_1 &= 1 \end{aligned}, \tag{2.29}$$

and $0 \le b_{12} \le 1, 0 \le b_{23} \le 1, 0 \le b_{13} \le 1, 0 \le b_1 \le 1, 0 \le c_{12} \le 1, 0 \le c_{23} \le 1,$ $0 \le c_{13} \le 1, 0 \le c_1 \le 1$.

The values of coefficients are defined by (2.30)–(2.32). In this MC scalar modulation method the achieved voltage transfer ratio is equal to 0.75.

$$\begin{aligned} b_{12} &= \frac{u_{S12}u^*_{L12}}{u^2_{S12} + u^2_{S23} + u^2_{S13}}, \quad b_{23} = \frac{u_{S23}u^*_{L12}}{u^2_{S12} + u^2_{S23} + u^2_{S13}}, \\ b_{13} &= \frac{u_{S13}u^*_{L12}}{u^2_{S12} + u^2_{S23} + u^2_{S13}}, \end{aligned} \tag{2.30}$$

$$c_{12} = \frac{u_{S12}u^*_{L13}}{u^2_{S12} + u^2_{S23} + u^2_{S13}}, \quad c_{23} = \frac{u_{S23}u^*_{L13}}{u^2_{S12} + u^2_{S23} + u^2_{S13}},$$
$$c_{13} = \frac{u_{S13}u^*_{L13}}{u^2_{S12} + u^2_{S23} + u^2_{S13}}, \tag{2.31}$$

$$b_1 = 1 - b_{12} - b_{23} - b_{13}, \quad c_1 = 1 - c_{12} - c_{23} - c_{13}. \tag{2.32}$$

When only two line-to-lines are taken into account for calculation of control signals the achieved voltage transfer ratio is equal to 0.866, and according to [65] the control strategy is described as follows:

$$\begin{aligned} u^*_{L12} &= b_2 u_{S12} + b_3 u_{S13} + b_1 u_0 \\ u^*_{L13} &= c_2 u_{S12} + c_3 u_{S13} + c_1 u_0 \end{aligned}, \tag{2.33}$$

$$b_1 + b_2 + b_3 = 1, \quad c_1 + c_2 + c_3 = 1, \tag{2.34}$$

where: $0 \le b_1 \le 1, 0 \le b_2 \le 1, 0 \le b_3 \le 1, 0 \le c_1 \le 1, 0 \le c_2 \le 1, 0 \le c_3 \le 1$. The values of coefficient are defined by Eqs. (2.35) and (2.36). Synthesis of the output line-to-line voltages in sample sequence period T_{Seq}, are shown in Fig. 2.47.

$$b_2 = \frac{(u_{S12} - u_{S23})u^*_{L12}}{u^2_{S12} + u^2_{S23} + u^2_{S13}}, \quad b_3 = \frac{(u_{S23} - u_{S31})u^*_{L12}}{u^2_{S12} + u^2_{S23} + u^2_{S13}}, \quad b_1 = 1 - b_2 - b_3, \tag{2.35}$$

$$b_2 = \frac{(u_{S12} - u_{S23})u^*_{L13}}{u^2_{S12} + u^2_{S23} + u^2_{S13}}, \quad b_3 = \frac{(u_{S23} - u_{S31})u^*_{L13}}{u^2_{S12} + u^2_{S23} + u^2_{S13}}, \quad c_1 = 1 - c_2 - c_3. \tag{2.36}$$

These scalar methods have limitations in input displacement factor control (input power factor). A comprehensive treatment of both voltage transfer ratio and input power factor aspects of the scalar method is contained in [106]. The maximum voltage transfer ratio is also equal to 0.866, but with a wider range of input displacement factor control.

Indirect modulation

The idea of an undirected control of a matrix converter makes the series connection of rectifier and inverter an equivalent circuit to a matrix converter, and is shown in Fig. 2.48. This technique, proposed in 1983 [109], consists of a simple control strategy where the most positive and the most negative input voltages, called here u_p and u_n, respectively, are used to synthesize the output reference voltage. In this equivalent circuit model, all kinds of significant pulse width modulation (PWM) algorithms for the rectifier and inverter can contribute to the control of the matrix converter. This concept is also known as modulation with "fictitious DC link" [142]. Then, the modulation with indirect transfer function was developed by Ziogas et al. [155, 156] and Huber et al. [61, 62].

The modulation process is divided into two steps. To attain the above features, a mathematical approach is employed as indicated in (2.37) [142].

$$\overline{\mathbf{u}}_L = (\mathbf{A}\mathbf{u}_I)\mathbf{B}, \tag{2.37}$$

where:

$$\mathbf{A} = K_A \begin{bmatrix} \cos(\omega t) \\ \cos(\omega t - 120°) \\ \cos(\omega t - 240°) \end{bmatrix}^T, \qquad \mathbf{B} = K_B \begin{bmatrix} \cos(\omega_L t) \\ \cos(\omega_L t - 120°) \\ \cos(\omega_L t - 240°) \end{bmatrix}. \tag{2.38}$$

According to (2.38) and (2.38), after some rearranging there is:

$$\overline{\mathbf{u}}_L = \frac{3K_A K_B U_{Sm}}{2} \begin{bmatrix} \cos(\omega_L t) \\ \cos(\omega_L t - 120°) \\ \cos(\omega_L t - 240°) \end{bmatrix}, \tag{2.39}$$

where K_A and K_B are modulation indexes. In a simple way, the technique operation is the following. First multiplication $\mathbf{A}\mathbf{u}_S$ in (2.37) corresponds to "rectifier transformation". A "fictitious DC-link" is obtained as a result of this multiplication. Then, the second step is generally referred to as the "inverter transformation". A practical realisation of this mathematical approach is discussed in detail in [155, 156]. Generally, in the indirect modulation approach, the maximum voltage transfer ratio is equal to $q = 6\sqrt{3}/\pi^2 = 1.053$. The voltage ratio obtainable is obviously greater than that of other methods. Unfortunately, this achievement comes with low-order harmonics (low frequency distortion) of source currents, or load voltages or both. For $q < 0.866$, the indirect method yields very similar results to the direct methods.

Space vector modulation

The space vector modulation (SVM) technique is based on the instantaneous space vector representation of source and/or load voltages and/or currents in power

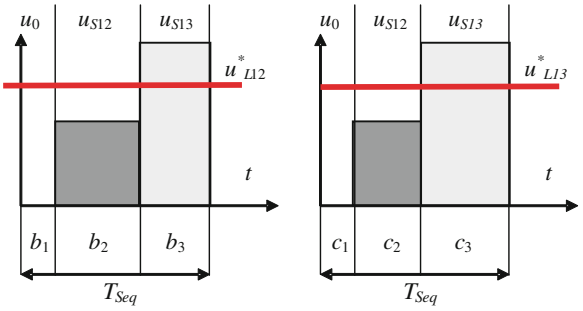


Fig. 2.47 Synthesizing of output line-to-line voltages by two line-to-line source voltages in MC with scalar modulation

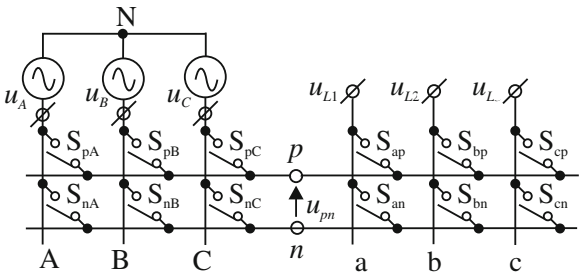


Fig. 2.48 Indirect equivalent structure of MC

converters [50, 59]. The SVM is a control technique that has been widely used in adjustable speed drives. Generally, in conventional DC-link VSI, the SVM technique is used to provide the reference output voltage vector $\overrightarrow{u}_{L\text{ref}}$. This vector is obtained by basic voltage vectors generated by the different inverter configurations. The SVM modulation for MCs is able to synthesize the reference output voltage vector $\overrightarrow{u}_{L\text{ref}}$ and due to the direct source voltages connection, it can also control the source current displacement angle [22, 121]. The SVM is probably the most used modulation strategy for MCs. Several control strategies based on the SVM technique for MCs have been proposed in the literature [17, 21–28, 54, 55, 61, 62, 121]. Basically, two methods for the implementation of SVM for MCs are used. The first one is defined as the "indirect method," because the MC is described as a two-stage system with virtual DC-link [61, 62]. The second approach to SVM for MCs is based on a direct approach [17, 21–28, 54, 55, 121]. The basic principles of direct SVM for MCs are described below.

For the space-vector modulation of the matrix converter it is convenient to define the following four space vectors [23]:

$$\begin{aligned} \underline{u}_O &= \tfrac{2}{3}(u_{L1} + \underline{a}u_{L2} + \underline{a}^2 u_{L3}) \\ \underline{u}_S &= \tfrac{2}{3}(u_{S1} + \underline{a}u_{S2} + \underline{a}^2 u_{S3}) \\ \underline{i}_O &= \tfrac{2}{3}(i_{L1} + \underline{a}i_{L2} + \underline{a}^2 i_{L3}) \\ \underline{i}_S &= \tfrac{2}{3}(i_{S1} + \underline{a}i_{S2} + \underline{a}^2 i_{S3}) \end{aligned}, \tag{2.40}$$

where u_S is the space-vector representation for the input phase voltage, u_O is the space-vector representation for the output phase voltage, i_S is the space-vector representation for the input phase current and i_O is the space-vector representation for the output phase current and $\underline{a} = e^{j(2\pi/3)}$.

Taking into account that in MCs the input phases must never be short-circuited and the output currents must never be interrupted, there are 27 possible switching configurations [21]. These switching states and the resulting output voltages and source current are tabulated in Table 2.5. These combinations are depicted in Fig. 2.49 [54, 55].

Table 2.5 Switching configuration for a MC and resulting output voltages and source current

No.	Vector No.	a	b	c	S_{aA}	S_{aB}	S_{aC}	S_{bA}	S_{bB}	S_{bC}	S_{cA}	S_{cB}	S_{cC}	u_{ab}	u_{bc}	u_{ca}	i_A	i_B	i_C
1	0_A	A	A	A	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0
2	0_B	B	B	B	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0
3	0_C	C	C	C	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0
4	−3	A	C	C	1	0	0	0	0	1	0	0	1	$-u_{CA}$	0	u_{CA}	i_a	0	$-i_a$
5	+2	B	C	C	0	1	0	0	0	1	0	0	1	u_{BC}	0	$-u_{BC}$	0	i_a	$-i_a$
6	−1	B	A	A	0	1	0	1	0	0	1	0	0	$-u_{AB}$	0	u_{AB}	$-i_a$	i_a	0
7	+3	C	A	A	0	0	1	1	0	0	1	0	0	u_{CA}	0	$-u_{CA}$	$-i_a$	0	i_a
8	−2	C	B	B	0	0	1	0	1	0	0	1	0	$-u_{BC}$	0	u_{BC}	0	$-i_a$	i_a
9	+1	A	B	B	1	0	0	0	1	0	0	1	0	u_{AB}	0	$-u_{AB}$	i_a	$-i_a$	0
10	−6	C	A	C	0	0	1	1	0	0	0	0	1	u_{CA}	$-u_{CA}$	0	i_b	0	$-i_b$
11	+5	C	B	C	0	0	1	0	1	0	0	0	1	$-u_{BC}$	u_{BC}	0	0	i_b	$-i_b$
12	−4	A	B	A	1	0	0	0	1	0	1	0	0	u_{BA}	$-u_{BA}$	0	$-i_b$	i_b	0
13	+6	A	C	A	1	0	0	0	0	1	1	0	0	$-u_{CA}$	u_{CA}	0	$-i_b$	0	i_b
14	−5	B	C	B	0	1	0	0	0	1	0	1	0	u_{BC}	$-u_{BC}$	0	0	$-i_b$	i_b
15	+4	B	A	B	0	1	0	1	0	0	0	1	0	$-u_{AB}$	u_{AB}	0	i_b	$-i_b$	0
16	−9	C	C	A	0	0	1	0	0	1	1	0	0	0	u_{CA}	$-u_{CA}$	i_c	0	$-i_c$
17	+8	C	C	B	0	0	1	0	0	1	0	1	0	0	$-u_{BC}$	u_{BC}	0	i_c	$-i_c$
18	−7	A	A	B	1	0	0	1	0	0	0	1	0	0	u_{AB}	$-u_{AB}$	$-i_c$	i_c	0
19	+9	A	A	C	1	0	0	1	0	0	0	0	1	0	$-u_{CA}$	u_{CA}	$-i_c$	0	i_c
20	−8	B	B	C	0	1	0	0	1	0	0	0	1	0	u_{BC}	$-u_{BC}$	0	$-i_c$	i_c
21	+7	B	B	A	0	1	0	0	1	0	1	0	0	0	$-u_{AB}$	u_{AB}	i_c	$-i_c$	0
22	–	A	B	C	1	0	0	0	1	0	0	0	1	u_{AB}	u_{BC}	u_{CA}	i_a	i_b	i_c
23	–	A	C	B	1	0	0	0	0	1	0	1	0	$-u_{CA}$	$-u_{BC}$	$-u_{AB}$	i_a	i_c	i_b
24	–	B	A	C	0	1	0	1	0	0	0	0	1	$-u_{AB}$	$-u_{CA}$	$-u_{BC}$	i_b	i_a	i_c
25	–	B	C	A	0	1	0	0	0	1	1	0	0	u_{BC}	u_{CA}	u_{AB}	i_c	i_a	i_b
26	–	C	A	B	0	0	1	1	0	0	0	1	0	u_{CA}	u_{AB}	u_{BC}	i_b	i_c	i_a
27	–	C	B	A	0	0	1	0	1	0	1	0	0	$-u_{BC}$	$-u_{AB}$	$-u_{CA}$	i_c	i_b	i_a

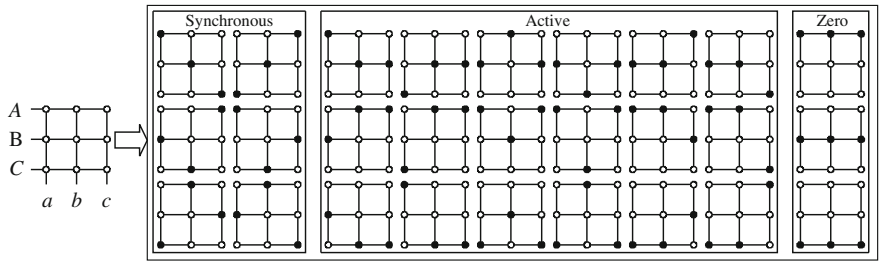


Fig. 2.49 Allowed switch combinations in a MC

Analyzing the Table 2.5, the switch configuration may be categorised as one of the three groups [21].

Group 1 – 3 combinations giving null output voltage and input current vectors, will be named "zero configurations". All three output phases are connected to the same input phase in these combinations.
Group 2 – 6 combinations in which each output phase is connected to a different input phase, will be named "synchronous configurations". In this case, the output voltage and input current vectors have variable directions and cannot be usefully used to synthesise the reference vectors.
Group 3 – 18 combinations where the output voltage and the input current vectors have fixed directions and will be named "active configurations." The magnitude of these vectors depends upon the instantaneous values of the input line-to-line voltages and output line currents, respectively. In this case, two output lines are connected to the same input line.

In Fig. 2.50 the output voltage and input current vectors corresponding to the 18 active configurations are shown. In this figure, the scheme of how the complex space vector plane is divided into sectors is also presented. S_O denotes the sector containing the output voltage vector and S_i denotes the sector containing the input current vector. The active configurations are split into three sub-groups as shown in Table 2.5 and Fig. 2.50. The configurations in each sub-group produce a space voltage and current vectors in a defined direction, which change every 120°. The amplitude and polarity of the space vectors along the defined direction depend on which of the line-to-line voltages is used.

The SVM algorithm for an MC is able to synthesize the reference output voltage vector and to control the phase angle of the input current vector selecting four non-zero configurations, which are applied for a suitable time period within each sequence T_{Seq} as is determined by the following equation [27]:

$$\underline{u}_O = d_I \underline{u}_I + d_{II} \underline{u}_{II} + d_{III} \underline{u}_{III} + d_{IV} \underline{u}_{IV}, \tag{2.41}$$

where $\underline{u}_I$, $\underline{u}_{II}$, $\underline{u}_{III}$ and $\underline{u}_{IV}$ are the output voltage vectors corresponding to the four selected configurations, and d_I, d_{II}, d_{III} and d_{IV} are their duty cycles, defined as:

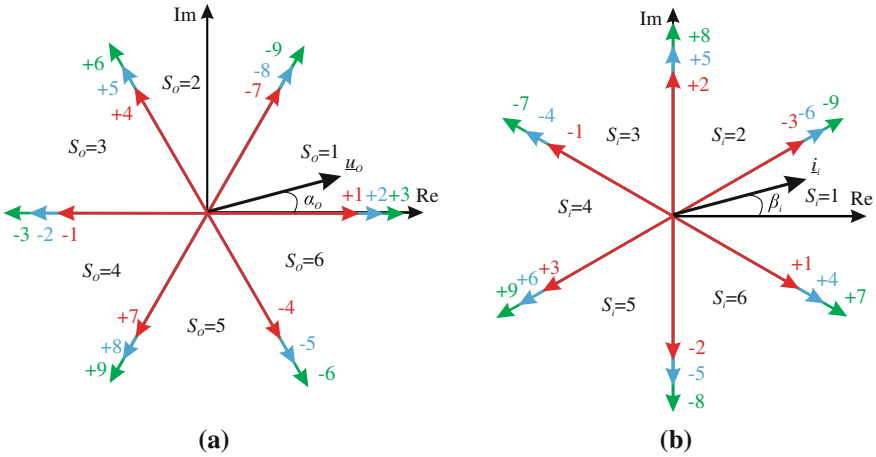


Fig. 2.50 Graphical interpretation of: **a** sectors and direction of the output voltage vectors, **b** sectors and directions of the input line current vectors

$$d_k = \frac{t_k}{T_{\text{Seq}}}, \qquad k = I, II, III, IV. \tag{2.42}$$

Finally, the zero configurations are applied to complete T_{Seq}, where:

$$d_0 = 1 - d_I - d_{II} - d_{III} - d_{IV}. \tag{2.43}$$

The rotating vectors of Group 3 are not used in SVM.

The main task of the SVM technique is to calculate the duty cycles and define the switching pattern. Several control strategies based on the SVM technique for the MC with a different sequence of the switches have been proposed in the literature [22–24, 27, 28, 54, 55, 102]. The presented types of switching sequences have been mainly focused on the possibility of reducing the number of commutations in each switching period T_{Seq} [102] and the power losses [54, 55], to improve the waveform of the output voltage and to eliminate the current distortion [22–24, 27] or to extend the operating region [28].

In order to explain the basic SVM algorithm, an example of synthesis of the reference output voltage vector and input current vector, with both lying in Sector 1, is shown in Fig. 2.51. Figure 2.51 clearly shows that the reference output voltage $\underline{u}_O$ is resolved into the components $\underline{u}'_O$ and $\underline{u}''_O$ along the two adjacent vector directions. The vector of source currents i_S is also resolved into components, along the two adjacent current directions [23]. The $\underline{u}'_O$ component can be synthesised using two voltage vectors having the same direction of u_O, whereas the $\underline{u}''_O$ component can be synthesised using two voltage vectors having the opposite direction, as follows [28]:

$$\begin{aligned}\underline{u}'_O &= d_I\underline{u}_I + d_{II}\underline{u}_{II} = 2/\sqrt{3}U_O\cos(\alpha_O - \pi/3)e^{j[(S_O-1)\pi/3+\pi/3]} \\ \underline{u}''_O &= d_{III}\underline{u}_{III} + d_{IV}\underline{u}_{IV} = 2/\sqrt{3}U_O\cos(\alpha_O + \pi/3)e^{j[(S_O-1)\pi/3]}\end{aligned}, \tag{2.44}$$

where d_I, d_{II}, d_{III} and d_{IV} are the on-time ratios of individual switch combinations corresponding to vectors $\underline{u}_I$, $\underline{u}_{II}$, $\underline{u}_{III}$ and $\underline{u}_{IV}$, α_O is the angle of the output voltage vector measured from the bisecting line of the corresponding sectors and is defined by (2.51) [23]. The requirements of the reference input current displacement angle are defined [28]

$$\begin{aligned}(d_I\underline{i}_I + d_{II}\underline{i}_{II})je^{j\beta_i}e^{j(S_i-1)\pi/3} &= 0 \\ (d_{III}\underline{i}_{III} + d_{IV}\underline{i}_{IV})je^{j\beta_i}e^{j(S_i-1)\pi/3} &= 0\end{aligned}, \tag{2.45}$$

where β_i is the angle input current vector measured from the bisecting line of the corresponding sectors and is defined by (2.51) [23], where i_I, i_{II}, i_{III}, i_{IV} are the source current vectors corresponding to the four selected configurations.

For example from Fig. 2.51 ($S_i = 1$, $S_O = 1$), possible switching states that can be utilised to synthesise the resolved voltage and current components are

$$\begin{aligned}\underline{u}^1 &: \pm7, \pm8, \pm9, \quad \underline{u}^2 : \pm1, \pm2, \pm3, \\ \underline{i}^1 &: \pm1, \pm4, \pm7, \quad \underline{i}^2 : \pm3, \pm6, \pm9.\end{aligned} \tag{2.46}$$

Then, to simultaneously synthesise the output voltage and the input current vectors, common switching states ±9, ±7, ±1and ± 3 are selected. From two switching states with the same number but opposite polarity, only one should be used. If the duty cycle is positive, the switching state with a positive polarity is selected; otherwise, the one with a negative polarity is selected. The required modulation duty cycles for the switching configurations I, II, III and IV are given by Eqs. (2.47)–(2.50) [23]:

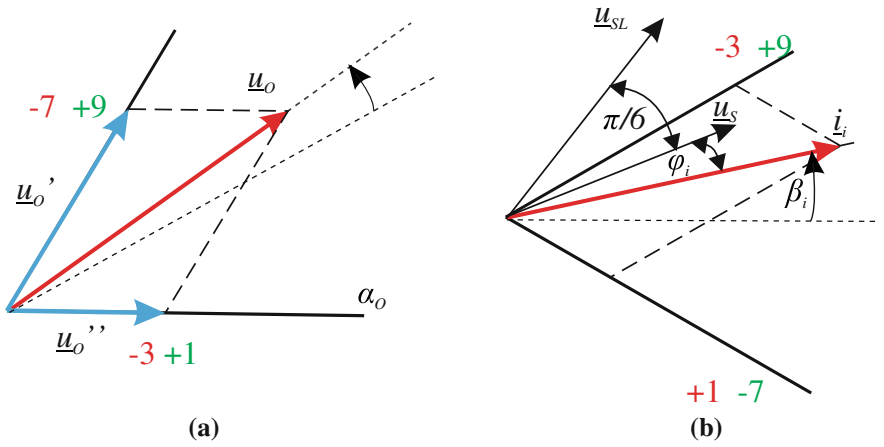


Fig. 2.51 Synthesis of: **a** reference output voltage vector, **b** reference input current vector

$$d_I = (-1)^{(S_O+S_i+1)} \frac{2}{\sqrt{3}} q \frac{\cos(\alpha_O - \frac{\pi}{3}) \cos(\beta_i - \frac{\pi}{3})}{\cos(\varphi_i)}, \tag{2.47}$$

$$d_I = (-1)^{(S_O+S_i)} \frac{2}{\sqrt{3}} q \frac{\cos(\alpha_O - \frac{\pi}{3}) \cos(\beta_i + \frac{\pi}{3})}{\cos(\varphi_i)}, \tag{2.48}$$

$$d_I = (-1)^{(S_O+S_i)} \frac{2}{\sqrt{3}} q \frac{\cos(\alpha_O + \frac{\pi}{3}) \cos(\beta_i - \frac{\pi}{3})}{\cos(\varphi_i)}, \tag{2.49}$$

$$d_I = (-1)^{(S_O+S_i+1)} \frac{2}{\sqrt{3}} q \frac{\cos(\alpha_O + \frac{\pi}{3}) \cos(\beta_i + \frac{\pi}{3})}{\cos(\varphi_i)}. \tag{2.50}$$

In (2.44)–(2.50) φ_i is the input phase displacement angle, α_O and β_i are the angles of the output voltage and input current vectors measured from the bisecting line of the corresponding sectors, and are limited as follows [23]:

$$-\frac{\pi}{6} \leq \alpha_O \leq \frac{\pi}{6}, \qquad -\frac{\pi}{6} \leq \beta_i \leq \frac{\pi}{6}. \tag{2.51}$$

Equations (2.47)–(2.50) have a general validity for any combination of the output voltage sector S_O and the input current sector S_i. Table 2.6 provides the four switch configurations to be used within the cycle period T_{Seq} [23]. The sectors are defined as shown in Fig. 2.50.

Subject to the constraints:

$$|d_I| + |d_{II}| + |d_{III}| + |d_{IV}| \leq 1, \tag{2.52}$$

the voltage ratio is defined by

$$q \leq \frac{\sqrt{3}|\cos(\varphi_i)|}{2\cos(\beta_i)\cos(\alpha_O)}. \tag{2.53}$$

In the particular case of balanced supply voltages and balanced output voltages, the maximum voltage transfer ratio is equal

$$q \leq \frac{\sqrt{3}}{2}|\cos(\varphi_i)|. \tag{2.54}$$

This means that the maximum voltage transfer ratio of MC is equal to 0.866 if the unity input power factor is set [142].

Current source matrix converter

As mentioned previously, the MC depends on the power supply (with voltage or current character) which is used—a voltage source matrix converter (VSMC) or current source matrix converter (CSMC), respectively. In the ideal case, the current source matrix converter consists of current at the input side and voltage source at the output side. In the practical realisation of CSMC, the converter includes nine

Table 2.6 Selection of the switching configurations for each combination of output voltage and input current sectors

		Sector of the output voltage vector S_O																							
		1				2				3				4				5				6			
Sector S_i of the input current vector	1	+9	−7	−3	+1	−6	+4	+9	−7	+3	−1	−6	+4	−9	+7	+3	−1	+6	−4	−9	+7	−3	+1	+6	−4
	2	−8	+9	+2	−3	+5	−6	−8	+9	−2	+3	+5	−6	+8	−9	−2	+3	−5	+6	+8	−9	+2	−3	−5	+6
	3	+7	−8	−1	+2	−4	+5	+7	−8	+1	−2	−4	+5	−7	+8	+1	−2	+4	−5	−7	+8	−1	+2	+4	−5
	4	−9	+7	+3	−1	+6	−4	−9	+7	−3	+1	+6	−4	+9	−7	−3	+1	−6	+4	+9	−7	+3	−1	−6	+4
	5	+8	−9	−2	+3	−5	+6	+8	−9	+2	−3	−5	+6	−8	+9	+2	−3	+5	−6	−8	+9	−2	+3	+5	−6
	6	−7	+8	+1	−2	+4	−5	−7	+8	−1	+2	+4	−5	+7	−8	−1	+2	−4	+5	+7	−8	+1	−2	−4	+5
Index of d_k		I	II	III	IV	I	II	III	IV	I	II	III	IV	I	II	III	IV	I	II	III	IV	I	II	III	IV

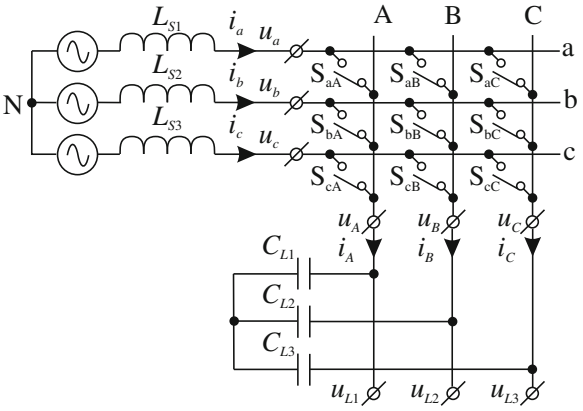


Fig. 2.52 Current source matrix converter

bidirectional switch cells and three AC capacitors that are located at the load-side of the converter. The current source realization includes a three-phase ideal voltage source (u_{S1}, u_{S2}, u_{S3}) in series with an R–L impedance per phase. Figure 2.52 shows the topology of a CSMC. In the literature, the CSMC is not often considered. Only a few papers present the principle of CSMC [48, 49, 70, 87, 88, 103].
The relationship between the converter source-side and load-side currents and voltages is

$$\begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix} = \begin{bmatrix} s_{aA}(t) & s_{bA}(t) & s_{cA}(t) \\ s_{aB}(t) & s_{bB}(t) & s_{cB}(t) \\ s_{aC}(t) & s_{bC}(t) & s_{cC}(t) \end{bmatrix} \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix}, \tag{2.55}$$

$$\begin{bmatrix} u_a(t) \\ u_b(t) \\ u_c(t) \end{bmatrix} = \begin{bmatrix} s_{aA}(t) & s_{aB}(t) & s_{aC}(t) \\ s_{bA}(t) & s_{bB}(t) & s_{bC}(t) \\ s_{cA}(t) & s_{cB}(t) & s_{cC}(t) \end{bmatrix} \begin{bmatrix} u_A(t) \\ u_B(t) \\ u_C(t) \end{bmatrix}. \tag{2.56}$$

The main objective of CSMC is to control directly the magnitude, frequency and phase-angle of the load current. Furthermore, indirectly, the output voltage is controlled. It is possible to obtain a voltage gain greater than one. The voltage gain strictly depends on the load. The CSMC also controls the phase-angle of the voltages (u_a, u_b and u_c) at the input side of the matrix switches. In this way, it is possible to control the input power factor.

The major disadvantage of the CSMC is the realisation of a practical current source—a large inductance value is needed. Moreover, the energy accumulated in source inductors is dangerous in the case when turning-off all converter switches. An additional circuit to discharge this energy is required. Another drawback of CSMC is that the voltage gain is dependent on load change. In large loads, the output voltages can be much smaller than the source one.

On the load side, the CSMC can be considered as a voltage source MC. Due to this fact, in the CSMC there can be used, with small modifications, all of the modulation methods, commutation strategies and protection strategies which are used in the VSMC. An exemplary solution of a CSMC with a Venturini control strategy is presented in [87], in which the low-frequency modulation matrix is transposed in accordance with classical Venturini modulation [135]. In the solution of a CSMC with SVM [48], the voltage sectors are dependent on input voltages (u_a, u_b and u_c), and current sectors are calculated from output current, inversely, as in the VSMC. The commutation method is based on input current measurements [48].

The matrix of nine bi-directional switches with capacitors connected on the input side terminals is versatile. Depending on the source character—voltage or current—the source can be connected to the input or output sides of the matrix switches. In this way, we obtain the universal converter which is connected between voltage and current sources, and which can transfer energy in both directions. These beneficial properties of matrix-connected switches are introduced in a new family of matrix-reactance frequency converters, which are the main goal of this book and are presented in the following chapters.

Multilevel matrix converter

As mentioned in the introduction, the multilevel concept of a direct matrix converter is also proposed. It is well-known that multilevel technology is a good solution in medium or high voltage power conversion [59]. The multilevel matrix converter (MLMC) is obtained by replacing each switch in a direct MC by two or more series connected switches, and flying capacitors which are introduced to clamp the voltage over the switches as shown in Fig. 2.53 [120, 143, 147]. Similarly to a MC, the MLMC must fulfil the same constraints on the switching pattern to avoid short circuit on the input side or open circuits on the output side. An additional problem is voltage control across the flying capacitor which changes periodically in line with the input voltage. The voltages must be controlled to keep a sinusoidal shape. Because of this, the modulation methods and commutation strategies are complex. This kind of converter is not a classical direct AC–AC frequency converter without DC energy storage elements, because the flying capacitors are used as a local energy storage. The advantages of MLMC is the possibility to apply it in high voltage range systems with low maintenance costs and few voltage device components. Furthermore, the MLMC gives an improved output voltage waveform quality. The maximum voltage transfer ratio in a MLMC is less than one. In the case with Venturini modulation, it is equal to 0.5 [120, 147] and with SVM it is equal to 0.8 [91, 114, 146].

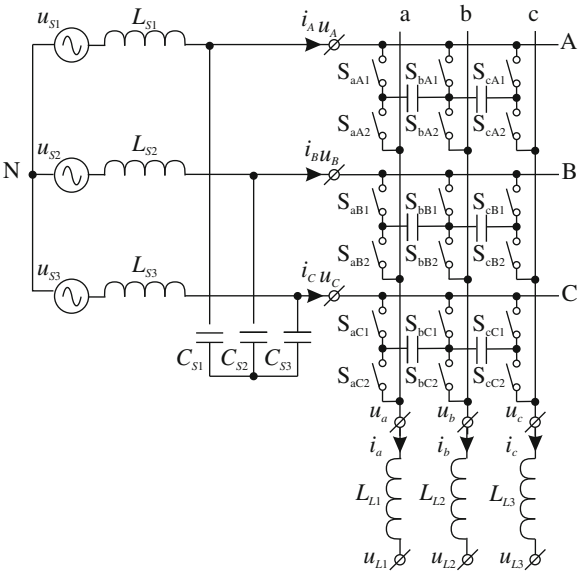


Fig. 2.53 Three level matrix converter

2.3.3 Indirect AC–AC Frequency Converters Without DC Energy Storage Elements

The second group of frequency converters without DC energy storage elements is the indirect converter with fictitious DC link (Fig. 2.2). This converter is obtained from the classical matrix converter structure. Systems with MC modulation schemes can be classified under direct frequency conversion schemes [21, 126, 135, 142] and indirect frequency conversion schemes [61, 62, 155, 156]. In the latter modulation concept, the converter is divided into two parts with fictitious DC link. There is a fictitious voltage-fed rectifier on the input side and a fictitious voltage source inverter on the output side. The input rectifier and output inverter are directly connected on the DC side. The indirect matrix converters with fictions DC link is a hardware implementation of this basic idea. Such a converter was suggested in [64] and investigated in more detail in [63, 68, 69, 76]. Figure 2.54 shows the circuit of indirect matrix converters (IMC). The main circuit consists of the PWM rectifier section (CSR—current source rectifier), PWM-inverter section (VSI) and the AC source filter. The cascaded connection of two bridge converters (CSR and VSI) provides separation of the modulation process on the input and output sides. The synchronisation of the modulation process of CSR and VSI is necessary for system balance with sinusoidal supply current because of the absence of the DC energy storage element. The IMC offers the same benefits and disadvantages as the classical direct MC, and is also called a two-stage matrix converter.

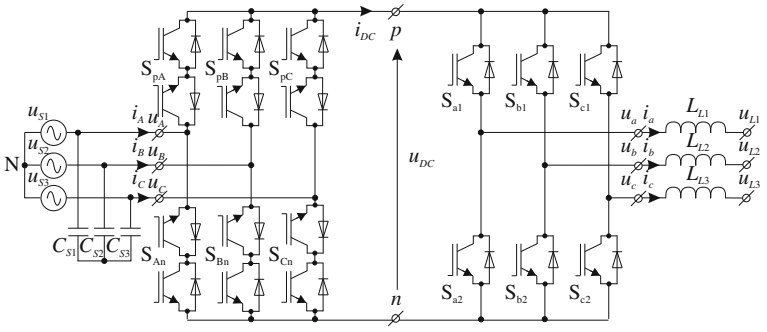


Fig. 2.54 Indirect matrix converter

MCs are inherently bi-directional and therefore can regenerate energy back into the mains from the load side. However, the DC voltage in an IMC has only positive polarity. In order to allow bi-directional current flow (four-quadrant operation), in the input bridge of the IMC bi-directional active switches are needed as shown in Fig. 2.54. On the output side, the classical voltage source inverter (Fig. 2.3) [59, 72] is used to form output voltages. The IMC employs 18 IGBTs and 18 diodes similar to those in the classical direct MC. However, the physical realisation is much easier, because the inverter stage could be realised by a conventional six-pack power module as compared to a fully discrete realisation of a direct MC.

Similarly as in the conventional MC, commutation methods are needed to avoid shorting of input phases without cutting load current path. The four-step commutation is commonly used in the IMC. The modulation strategies are based on an indirect concept which is presented in [61, 62, 155, 156]. Both vector and triangular wave modulation have been developed and are presented in [63, 64, 68, 69, 76]. In the modulation strategies, the 72 basic switch configurations are used. In Table 2.7, output voltages and source currents resulting from the different switch combinations are tabulated [81].

In Ref. [81] the authors show new topologies of IMC with reduced number of active switches on the line bridge. The input stage of the IMC is realised with four-quadrant switches, as shown in Fig. 2.54. In this circuit configuration, the bi-directional power flow could in principle be obtained with positive and negative DC link voltage. If assumed that the DC link voltage is positive polarity, a reduction in the number of active switch devices is possible. The derivation of a simplified bridge branch structure of the IMC is shown in Fig. 2.55. The new topology is called by the authors a sparse matrix converter (SMC), and is shown in Fig. 2.56. A detailed description of derivation is presented in [81, 83, 84, 116]. SMC are functionally equivalent to IMC, but are characterised by a lower realisation effort and a lower control complexity. The SMC topology employs 15 IGBTs and 18 diodes.

If a unidirectional power flow is required, a more simplified version of the system is possible. Such a circuit is shown in Fig. 2.57 [81, 83, 84, 117]. This converter is

Table 2.7 Switching configuration for an IMC and resulting output voltages and source current

No.	a	b	c		S_{pA}	S_{pB}	S_{pC}	S_{An}	S_{Bn}	S_{Cn}	S_a	S_b	S_c	u_{ab}	u_{bc}	u_{ca}	u_{DC}	i_A	i_B i_C
1	p	p	p	X	X	X	X	X	X	1	1	1	0	0	0	–	0	0	0
10	n	n	n	X	X	X	X	X	X	0	0	0	0	0	0	–	0	0	0
19	X	X	X	1	0	0	1	0	0	X	X	X	0	0	0	0	0	0	0
25	X	X	X	0	1	0	0	1	0	X	X	X	0	0	0	0	0	0	0
31	X	X	X	0	0	1	0	0	1	X	X	X	0	0	0	0	0	0	0
37	A	C	C	1	0	0	0	0	1	1	0	0	$-u_{CA}$	0	u_{CA}	$-u_{CA}$	i_a	0	$-i_a$
38	A	C	C	0	0	1	1	0	0	0	1	1	$-u_{CA}$	0	u_{CA}	u_{CA}	i_a	0	$-i_a$
39	B	C	C	0	1	0	0	0	1	1	0	0	u_{BC}	0	$-u_{BC}$	u_{BC}	0	i_a	$-i_a$
40	B	C	C	0	0	1	0	1	0	0	1	1	u_{BC}	0	$-u_{BC}$	$-u_{BC}$	0	i_a	$-i_a$
41	B	A	A	0	1	0	1	0	0	1	0	0	$-u_{AB}$	0	u_{AB}	$-u_{AB}$	$-i_a$	i_a	0
42	B	A	A	1	0	0	0	1	0	0	1	1	$-u_{AB}$	0	u_{AB}	u_{AB}	$-i_a$	i_a	0
43	C	A	A	0	0	1	1	0	0	1	0	0	u_{CA}	0	$-u_{CA}$	u_{CA}	$-i_a$	0	i_a
44	C	A	A	1	0	0	0	0	1	0	1	1	u_{CA}	0	$-u_{CA}$	$-u_{CA}$	$-i_a$	0	i_a
45	C	B	B	0	0	1	0	1	0	1	0	0	$-u_{BC}$	0	u_{BC}	$-u_{BC}$	0	$-i_a$	i_a
46	C	B	B	0	1	0	0	0	1	0	1	1	$-u_{BC}$	0	u_{BC}	u_{BC}	0	$-i_a$	i_a
47	A	B	B	1	0	0	0	1	0	1	0	0	u_{AB}	0	$-u_{AB}$	u_{AB}	i_a	$-i_a$	0
48	A	B	B	0	1	0	1	0	0	0	1	1	u_{AB}	0	$-u_{AB}$	$-u_{AB}$	i_a	$-i_a$	0
49	C	A	C	1	0	0	0	0	1	0	1	0	u_{CA}	$-u_{CA}$	0	$-u_{CA}$	i_b	0	$-i_b$
50	C	A	C	0	0	1	1	0	0	1	0	1	u_{CA}	$-u_{CA}$	0	u_{CA}	i_b	0	$-i_b$
51	C	B	C	0	1	0	0	0	1	0	1	0	$-u_{BC}$	u_{BC}	0	u_{BC}	0	i_b	$-i_b$
52	C	B	C	0	0	1	0	1	0	1	0	1	$-u_{BC}$	u_{BC}	0	$-u_{BC}$	0	i_b	$-i_b$
53	A	B	A	0	1	0	1	0	0	0	1	0	u_{AB}	$-u_{AB}$	0	$-u_{AB}$	$-i_b$	i_b	0
54	A	B	A	1	0	0	0	1	0	1	0	1	u_{AB}	$-u_{AB}$	0	u_{AB}	$-i_b$	i_b	0
55	A	C	A	0	0	1	1	0	0	0	1	0	$-u_{CA}$	u_{CA}	0	u_{CA}	$-i_b$	0	i_b
56	A	C	A	1	0	0	0	0	1	1	0	1	$-u_{CA}$	u_{CA}	0	$-u_{CA}$	$-i_b$	0	i_b
57	B	C	B	0	0	1	0	1	0	0	1	0	u_{BC}	$-u_{BC}$	0	$-u_{BC}$	$-i_b$	i_b	0

(continued)

Table 2.7 (continued)

No.	a	b	c		S_{pA}	S_{pB}	S_{pC}	S_{An}	S_{Bn}	S_{Cn}	S_a	S_b	S_c	u_{ab}	u_{bc}	u_{ca}	u_{DC}	i_A	i_B i_C
58	B	C	B	0	0	1	0	1	0	1	0	1	u_{BC}	$-u_{BC}$	0	u_{BC}	0	$-i_b$	i_b
59	B	A	B	1	0	0	0	1	0	0	1	0	$-u_{AB}$	u_{AB}	0	u_{AB}	i_b	$-i_b$	0
60	B	A	B	0	1	0	1	0	0	1	0	1	$-u_{AB}$	u_{AB}	0	$-u_{AB}$	i_b	$-i_b$	0
61	C	C	A	1	0	0	0	0	1	0	0	1	0	u_{CA}	$-u_{CA}$	$-u_{CA}$	i_c	0	$-i_c$
62	C	C	A	0	0	1	1	0	0	1	1	0	0	u_{CA}	$-u_{CA}$	u_{CA}	i_c	0	$-i_c$
63	C	C	B	0	1	0	0	0	1	0	0	1	0	$-u_{BC}$	u_{BC}	u_{BC}	0	i_c	$-i_c$
64	C	C	B	0	0	1	0	1	0	1	1	0	0	$-u_{BC}$	u_{BC}	$-u_{BC}$	0	i_c	$-i_c$
65	A	A	B	0	1	0	1	0	0	0	0	1	0	u_{AB}	$-u_{AB}$	$-u_{AB}$	$-i_c$	i_c	0
66	A	A	B	1	0	0	0	1	0	1	1	0	0	u_{AB}	$-u_{AB}$	u_{AB}	$-i_c$	i_c	0
67	A	A	C	0	0	1	1	0	0	0	0	1	0	$-u_{CA}$	u_{CA}	u_{CA}	$-i_c$	0	i_c
68	A	A	C	1	0	0	0	0	1	1	1	0	0	$-u_{CA}$	u_{CA}	$-u_{CA}$	$-i_c$	0	i_c
69	B	B	C	0	0	1	0	1	0	0	0	1	0	u_{BC}	$-u_{BC}$	$-u_{BC}$	0	$-i_c$	i_c
70	B	B	C	0	1	0	0	0	1	1	1	0	0	u_{BC}	$-u_{BC}$	u_{BC}	0	$-i_c$	i_c
71	B	B	A	1	0	0	0	1	0	0	0	1	0	$-u_{AB}$	u_{AB}	u_{AB}	i_c	$-i_c$	0
72	B	B	A	0	1	0	1	0	0	1	1	0	0	$-u_{AB}$	u_{AB}	$-u_{AB}$	i_c	$-i_c$	0

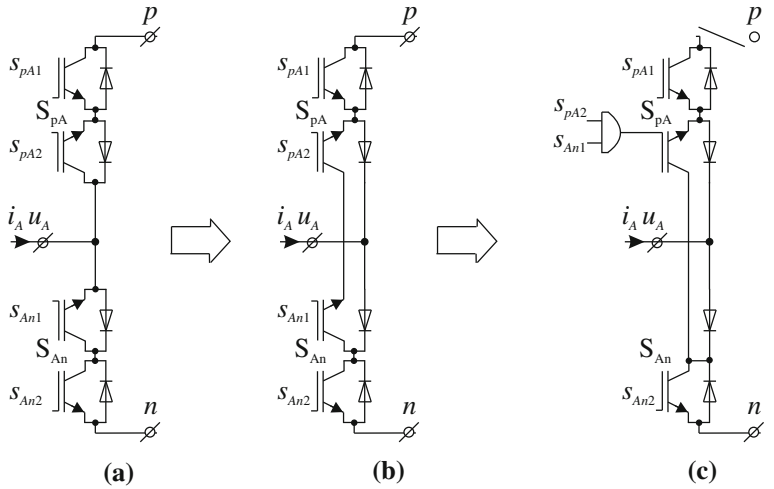


Fig. 2.55 Derivation of the bridge branch **a** branch for IMC, **b** idea of reduction of branch transistors, **c** branch for SMC

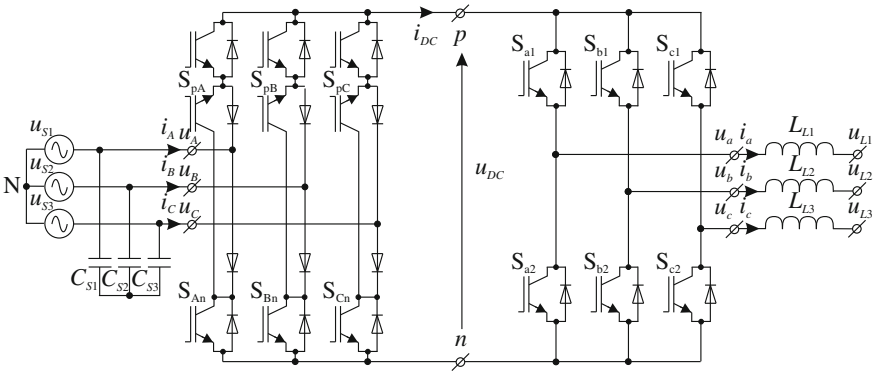


Fig. 2.56 Sparse matrix converter (SMC)

named as an ultra sparse matrix converter (USMC). The source bridge consists of only three IGBTS and 12 diodes.

The structures of IMC, SMC and USMC require the use of the multistep switch commutation method to fulfil commutation rules. In another topology previously presented in paper [138], a simplified commutation is possible. This converter is named a very sparse matrix converter (VSMC) and is shown in Fig. 2.58. The rectifier bridge consists of bi-directional switches with IGBT and diode bridge configuration. This switching connection provides the zero DC-link current commutation strategy [81]. In VSMC, only a safety interval dead time is required between switch-off of one four-quadrant switch and the switch-on of the next four-quadrant switch. This topology provides an option to reduce the number of IGBTs, but the number of power

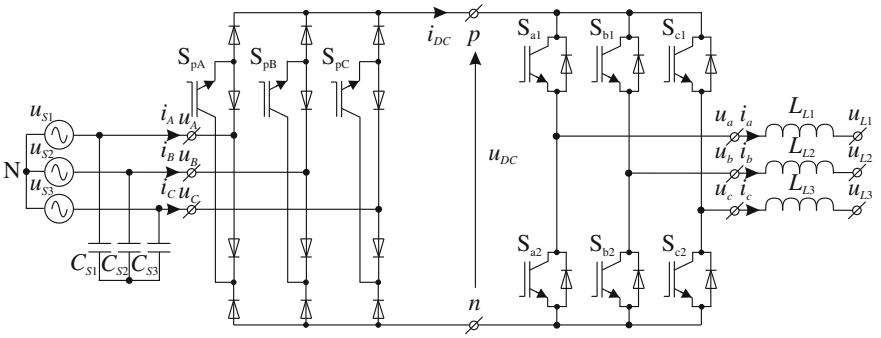


Fig. 2.57 Ultra sparse matrix converter (USMC)

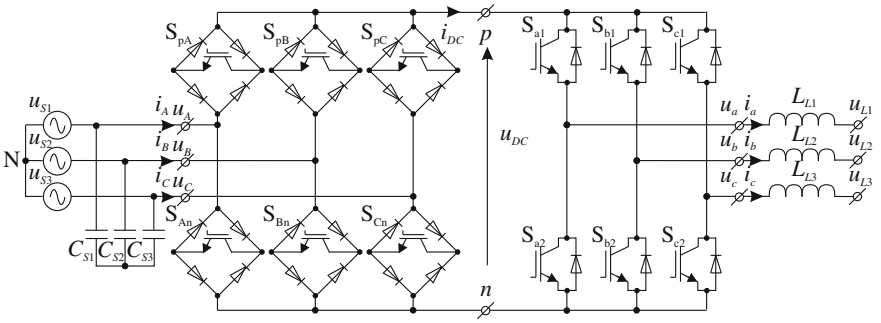


Fig. 2.58 Very sparse matrix converter (VSMC)

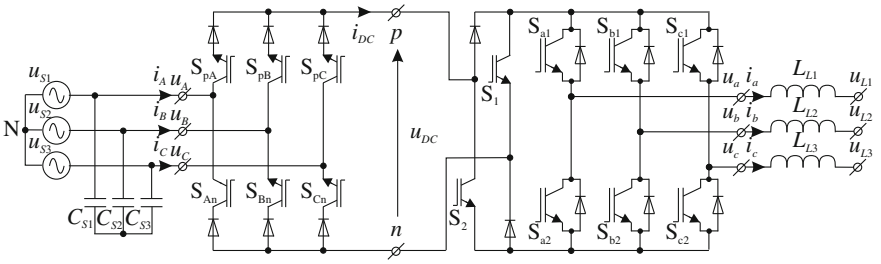


Fig. 2.59 Inversing link matrix converter (ILMC)

diodes is increased. In the VSMC structure, the 12 IGBTs and 30 diodes is employed. This topology is functionally similar to IMC.

Zero DC link current commutation and bidirectional power flow also would allow the employment of the circuit topology of the inverting link matrix converter (ILMC) presented in [81] and shown in Fig. 2.59. Here, the bidirectional current carrying capability of the input stage is achieved by connecting an input rectifier and a voltage inverter through two power transistors and two diodes. Unfortunately, the inversion

of the voltages has to be performed with high frequency. Then the switching losses are high. Additionally the modulation process is complex. Therefore, the literature on the ILMC will not be considered in more detail.

The topologies of the sparse, very sparse, ultra sparse and inverting link matrix converter are characterised by a voltage transfer ratio also less than one, with its maximal level equal to 0.866.

Indirect matrix converters have also been extended into multilevel structures. Multilevel indirect matrix converters (MIMC) is an emerging topology that integrates the multilevel concept into the indirect matrix converter topology. Having the ability to generate multilevel output voltages, the MIMC is able to produce better quality output waveforms than IMC in terms of harmonic content, but at the cost of a higher number of power semiconductor devices requirement and more complicated modulation strategy. In the literature there are presented two main topologies, a three-level-output-stage indirect matrix converter [81, 90, 92] and an indirect three-level sparse matrix converter [89]. The first one applies the three-level neutral-point-clamped voltage source inverter concept [59] to the inversion stage of an indirect matrix converter topology and is shown in Fig. 2.60. The rectified DC-link voltage, u_{DC} is transformed into dual voltage supplies, $+u_{\mathrm{DC}}$ and $-u_{\mathrm{DC}}$, by connecting the DC link middle point of the three-level neutral-point-clamped voltage source inverter to the neutral-point "N" of the star-connected input filter capacitors. Then, there are three voltage levels at the DC links: $+u_{\mathrm{DC}}$, 0 V and $-u_{\mathrm{DC}}$. Based on these voltage levels, the inversion stage can be modulated to generate the multilevel output voltage waveforms.

The second MIMC applies simplified three-level neutral-point-clamped voltage source inverter concept with neutral-point chopper, to the inversion stage of an IMC topology (Fig. 2.61) [89]. This converter topology has a simpler circuit configuration than converter from Fig. 2.60 and is also able to generate three-level output voltages.

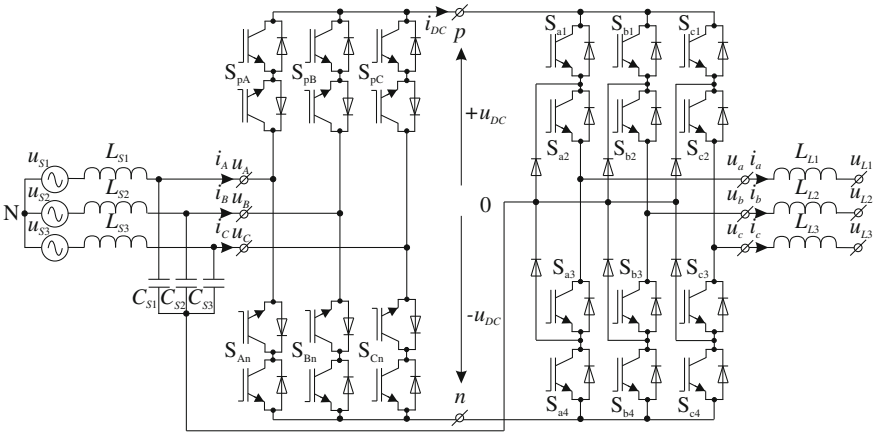


Fig. 2.60 Three-level-output-stage indirect matrix converter

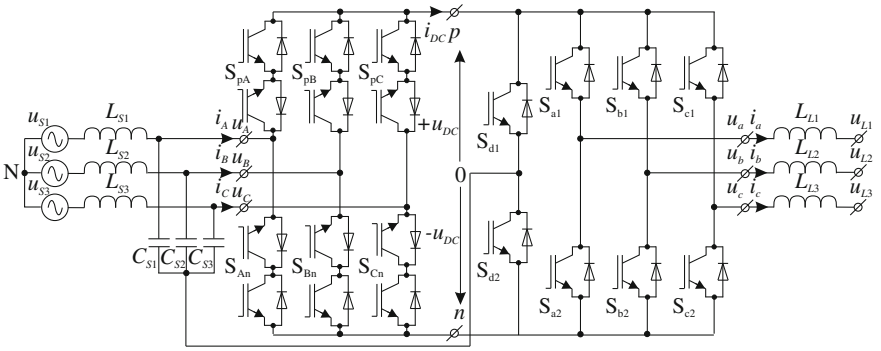


Fig. 2.61 Indirect three-level sparse matrix converter

In this circuit, two additional unidirectional switches are connected as an additional inverter leg. The main task of this leg is a device of neutral-point commutator.

2.3.4 AC–AC Frequency Converters Based on Matrix-Reactance Chopper Topologies

The first study of topologies of frequency converters based on matrix-reactance chopper topologies was presented in 1993 by Antic et al. in [8–10]. The proposed topology consists of a three phase AC–AC buck-boost chopper with an integrated matrix-converter—Fig. 2.62a. This topology has only a small regenerative AC energy storage, and was proposed for low frequency operation in drive systems with induction motors.

Another concept of frequency converters based on a MRC, but with a different switch realisation is proposed by Zinoviev et al. [104, 153, 154] (Fig. 2.62b). The principle of operation of this new voltage controller is similar to the operation of a buck-boost AC–AC chopper with the possibility to change the output voltage frequency.

Further, detailed analysis of this kind of topologies was carried out by Fedyczak et al. in a series of papers: [36–47, 85, 86, 125–129]. As a result, the new family of AC–AC frequency converters based on matrix-reactance chopper topologies was presented [45, 46, 126]. Those converters are named matrix-reactance frequency converters (MRFC) and are the main object of this book. The analysis of properties of MRFC will be presented in the following chapters. In Chap. 3, the topology generation is presented. Chapter 4 shows the modeling concept. Whereas in further chapters, there are presented the test results of theoretical analysis, simulation and experimental investigations. In this book, all the structures of frequency converters based on MRC topologies are subsequently named as matrix-reactance frequency converters.

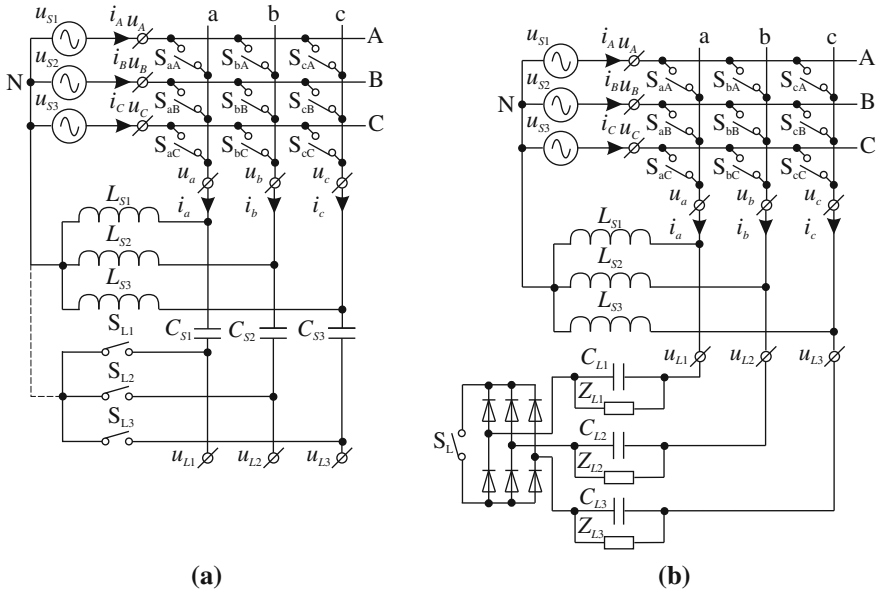


Fig. 2.62 Frequency converters with AC–AC buck-boost choppers and matrix converter proposed: **a** in [8–10], **b** in [104, 153, 154]

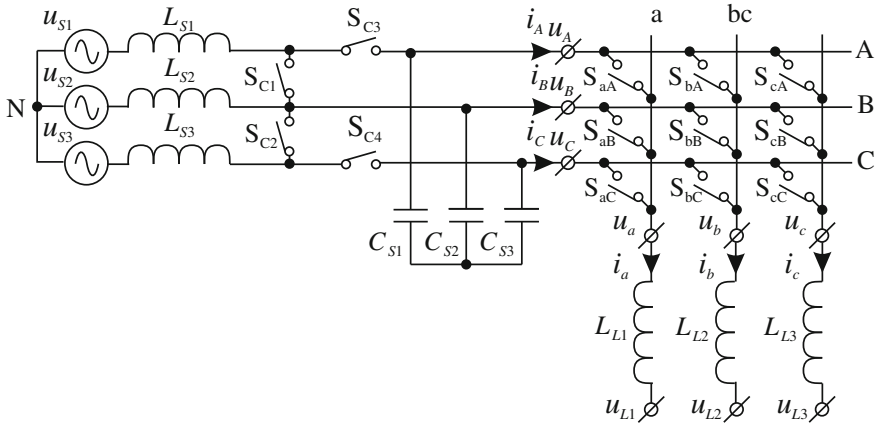


Fig. 2.63 Frequency converters with cascade connected AC–AC boost choppers and matrix converter

In recent times, another topology based on MRC has been presented, consisting of cascade connected boost MRC and MC as shown in Fig. 2.63 [66, 79, 80]. The operation of a boost chopper is only necessary when a voltage gain factor greater than 0.866 is required. If the required voltage gain is less than 0.866, then the topology is similar to the MC. The switches S_{C1} and S_{C2} are turned-off and the switches

S_{C3} and S_{C4} are turned-on. The increase of conduction losses in the case when the voltage gain is less than 0.866, is a drawback of this solution. Then, two bidirectional switches are turned-on all the time.

All frequency converters based on AC–AC matrix-reactance choppers offer a voltage transfer ratio greater than one.

2.4 Hybrid AC–AC Frequency Converters

The last group of frequency converters (Fig. 2.2) includes the hybrid solution. In order to obtain a voltage gain greater than one, the combination of AC–AC frequency converters (without DC energy storage) and one small or several small local DC energy storage elements or DC–DC buck-boost (boost) choppers are proposed. All hybrid frequency converters include a DC energy storage element, but with small dimensions. The topologies are more complex and modulation and commutation strategies are also elaborate.

In paper [35] the authors have proposed the first hybrid topology. Figure 2.64 shows a proposed circuit, which was named a modular matrix converter (MMC) [7]. The MMC is obtained by replacing each switch in the classical direct MC [135] by single-phase H bridge inverters. Unfortunately, the number of active devices increases, but in this topology has not a main DC energy storage elements. The main DC energy storage element is divided into several local and small DC energy storage elements. This approach has the advantages of reduced switching loss and elimination of clamp circuit. The peak voltages applied to the semiconductor devices are clamped to local capacitors. The output performance is also better than the classical solution. The main disadvantage is the number of semiconductors and passive elements. Major difficulties in achieving the required control is related to monitoring of DC voltages across the capacitors. Each DC voltage in the capacitors has to be controlled via feedback. Then the control strategies are very complex. Furthermore, this converter can provide the buck-boost control of output voltage amplitude and can operate with arbitrary power factors.

The next means of achieving converter hybridisation is by using an additional small-scale DC circuit in the MC topologies. There are two types of matrix converter configurations, the single-stage (classical MC) and the two-stage (IMC); therefore, two ways to implant a hybrid MC are possible with MC and IMC.

The first solution is to connect an H-bridge inverter in series with each of the MC outputs as suggested in Fig. 2.65 [77]. The topology of the hybrid converter from Fig. 2.65 enables step-up or step-down voltage control. This solution has a serious disadvantage related to the high number of power semiconductors and DC link capacitors, which have to smooth down the power ripple (twice the output frequency) that is characteristic of a single-phase inverter [77]. Moreover, these converter topologies again have energy storage elements (e.g., electrolytic capacitor) which reduce their life time.

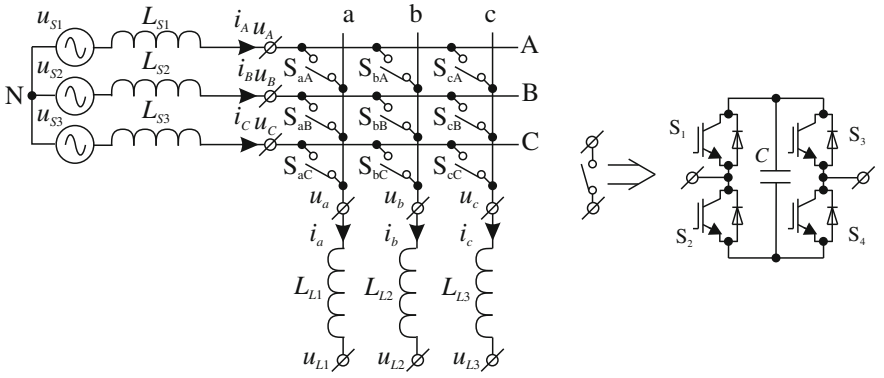


Fig. 2.64 Modular matrix converter (MMC) [7]

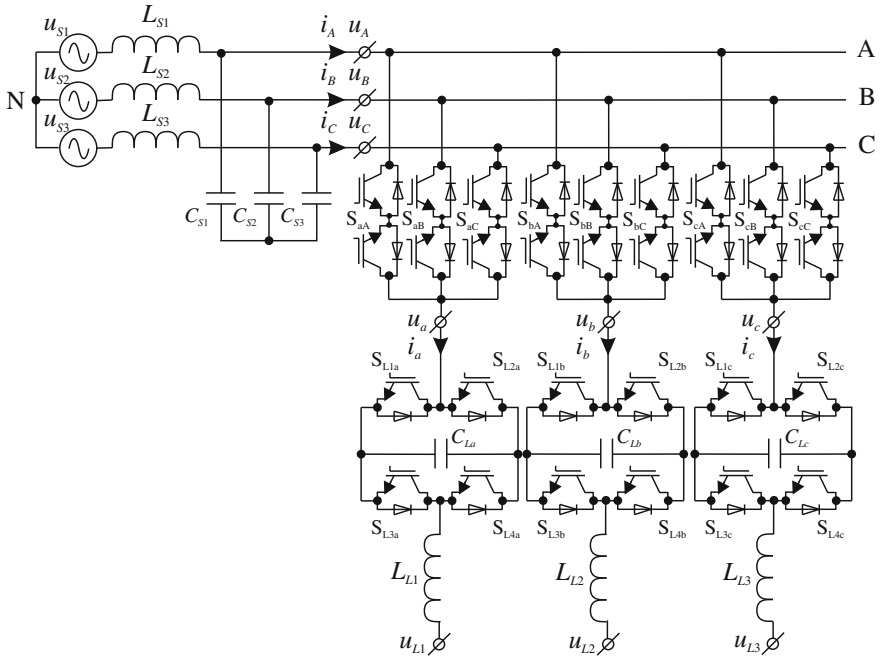


Fig. 2.65 Hybrid frequency converter with series connected MC and small scale H-bridge inverter on each output phase

The second solution is related to IMCs and solves the two most important drawbacks of the IMC—voltage transfer ratio equal to 0.866. It consists in introducing an auxiliary voltage supply in the form of an H-bridge inverter in the intermediary link of the IMC, with the purpose of compensating the voltage deficit. In this way, an increase of output voltage is obtained. The structure of an hybrid IMC with H-bridge

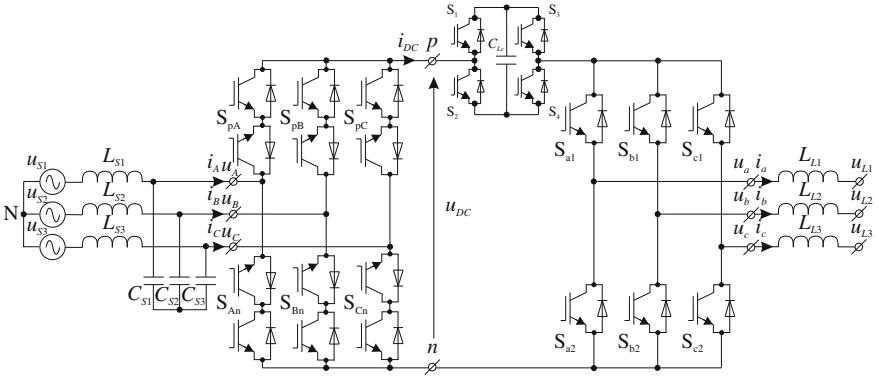


Fig. 2.66 Hybrid IMC with small scale H-bridge inverter in the intermediary link

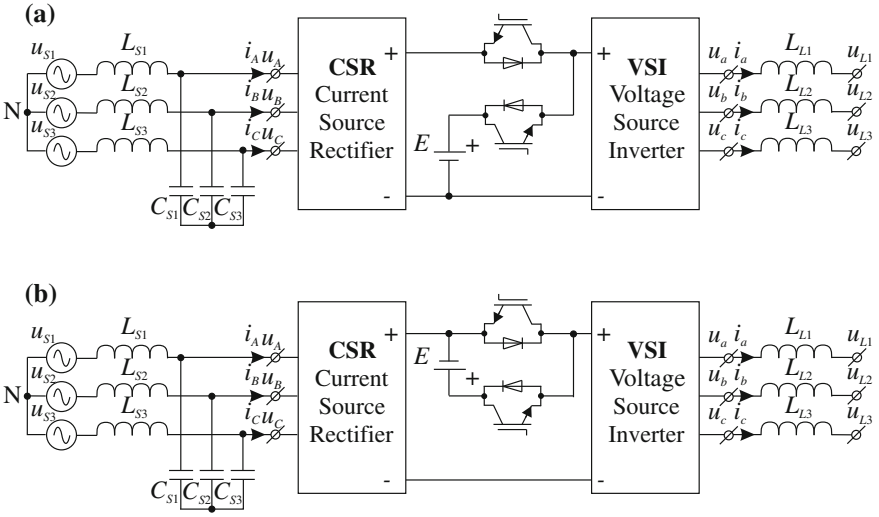


Fig. 2.67 Categories of hybrid IMC topologies employing: **a** an auxiliary high-voltage DC source; **b** low-voltage DC source

inverter is shown in Fig. 2.66 [73, 77, 78, 81, 144]. However, these converter topologies also have energy storage elements and their construction requires considerable work.

Another concept of hybrid IMC is proposed in [73], where hybrid structures are based on combined auxiliary voltage source in the intermediate DC link of the IMC. These converter topologies may be classified into two main groups depending on DC voltage level, as shown in Fig. 2.67. In the topology with an auxiliary high-voltage DC source, this source is used in parallel connection with a DC link, whereas in the topology with an auxiliary low-voltage DC source, in series connection with a DC

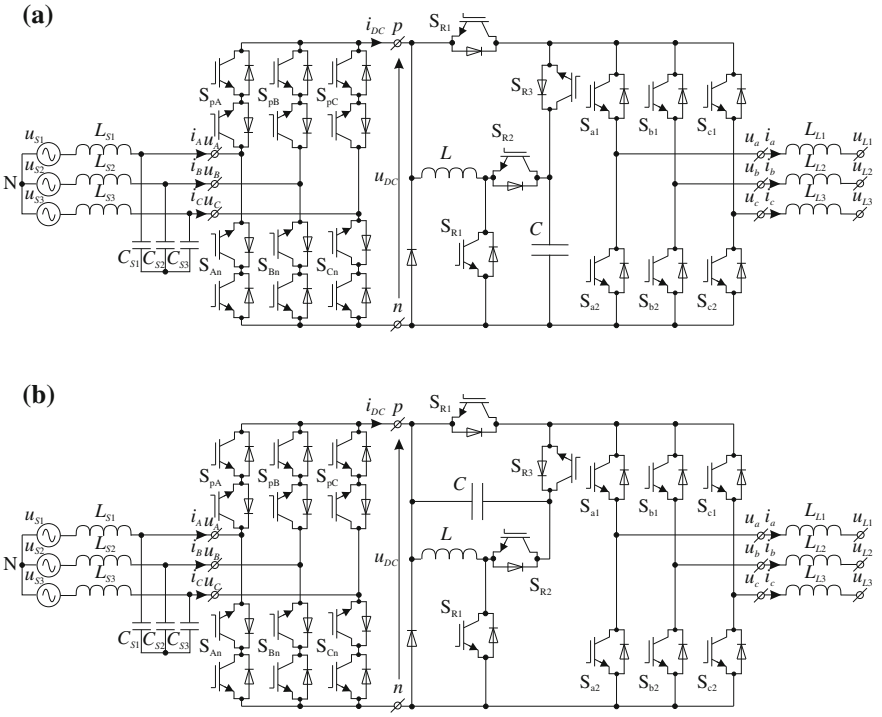


Fig. 2.68 Hybrid IMC structures: **a** with high-voltage auxiliary voltage source and reversible boost converter; **b** with low-voltage auxiliary voltage source and reversible flyback converter

link. The practical realisation of these concepts from Fig. 2.67, is shown in Fig. 2.68 [73, 144]. Unity voltage transfer is also obtained in these solutions.

In summary, hybrid concepts enable the enlargement of the voltage control range. To obtain these advantages, however, there is a higher complexity in the power stages and in their control. Furthermore, the DC energy storage element is still needed.

2.5 Summary of Topology Review

This section has dealt with a comprehensive review of AC–AC frequency converter topologies. This chapter has focused on inverter technologies with special attention to AC–AC conversion without DC energy storage elements. The potential converter topologies may be classified into three main groups depending AC–AC conversion (Fig. 2.2). Various inverter topologies have been presented, compared and evaluated against demands, lifetime, component ratings and voltage gain control capabilities.

Table 2.8 Summary of comparing frequency converter topologies

Name of converter	Modulation strategy	Voltage gain
With DC energy storage element		
Frequency converter with VSI	Space vector modulation (SVM)	>1
Frequency converter with CSI	Space vector modulation (SVM)	>1
Without DC energy storage element		
Voltage source matrix converter	Classical Venturini	0.5
	Improvement Venturini	0.866
	Scalar	0.866
	Indirect with fictitious DC link	1.05
	Space vector modulation (SVM)	0.866
	Duty-cycle SVM	1.155
Current source matrix converter	Classical Venturini	>1
	Space vector modulation (SVM)	>1
Indirect matrix converter (IMC)	Space vector modulation (SVM)	0.866
Sparse matrix converter (SMC)	Space vector modulation (SVM)	0.866
Very sparse matrix converter (VSMC)	Space vector modulation (SVM)	0.866
Ultra sparse matrix converter (USMC)	Space vector modulation (SVM)	0.866
Matrix-reactance frequency converters	Classical Venturini	>1
Cascaded connected MRC and MC	Space vector modulation (SVM)	>1
Multilevel indirect matrix converter	Space vector modulation (SVM)	>0.866
Multilevel direct matrix converter	Space vector modulation (SVM)	>0.8
Hybrid with small DC energy storage element		
Modular matrix converter	Space vector modulation (SVM)	>1
Hybrid direct MC with H bridge in output	Space vector modulation (SVM)	>1
Hybrid IMC with H bridge in DC link	Space vector modulation (SVM)	>1
Hybrid IMC with high-voltage auxiliary voltage source	Space vector modulation (SVM)	>1
Hybrid IMC with low-voltage auxiliary voltage source	Space vector modulation (SVM)	>1

The continual development of power electronic converters, for a range of applications, is characterised by the requirements for higher efficiency, lower volume, lower weight and lower production costs [82]. Frequency converters with DC energy storage have these desirable properties, but the voltage gain ratio is less than the one in most topologies and modulation strategies. For the topologies with modulation strategies with voltage gain ratio greater than one, there is low frequency deformation of output/input waveforms. Only on a few topologies without DC energy storage is buck-boost regulation of output voltages possible [8–10, 45, 46, 66, 79, 80, 87, 104, 153, 154]. Such topologies are not widely discussed in the literature. More interesting are topologies of matrix-reactance frequency converters, which will be analysed in detail in the following chapters. Finally, to complete this chapter, it is presented in Table 2.8, a summary comparison of the voltage gain ratio of frequency converter topologies.

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