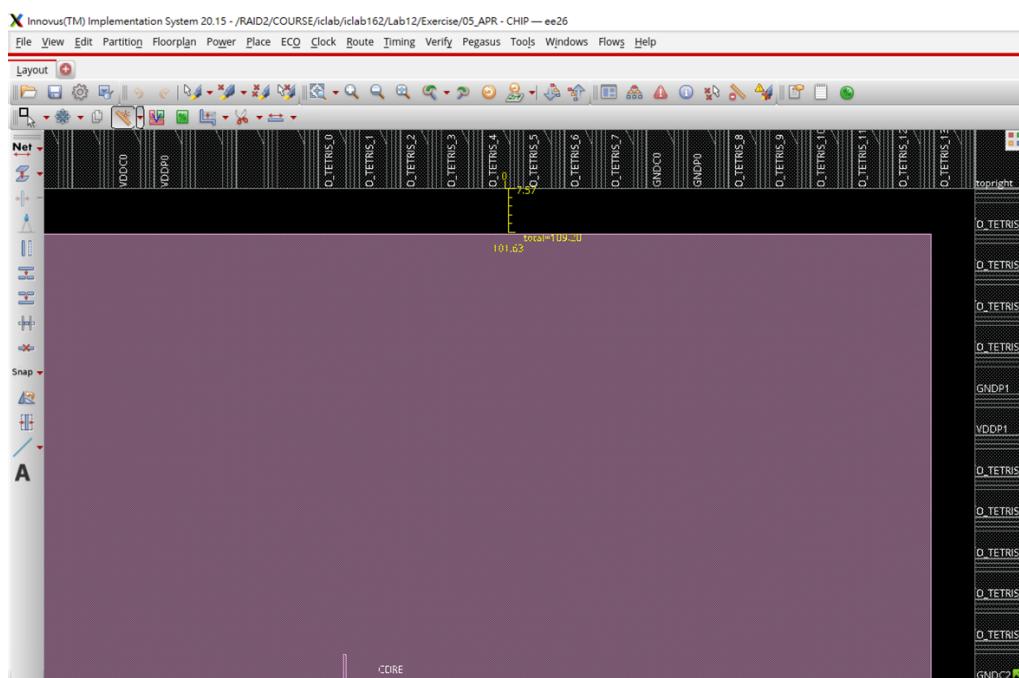
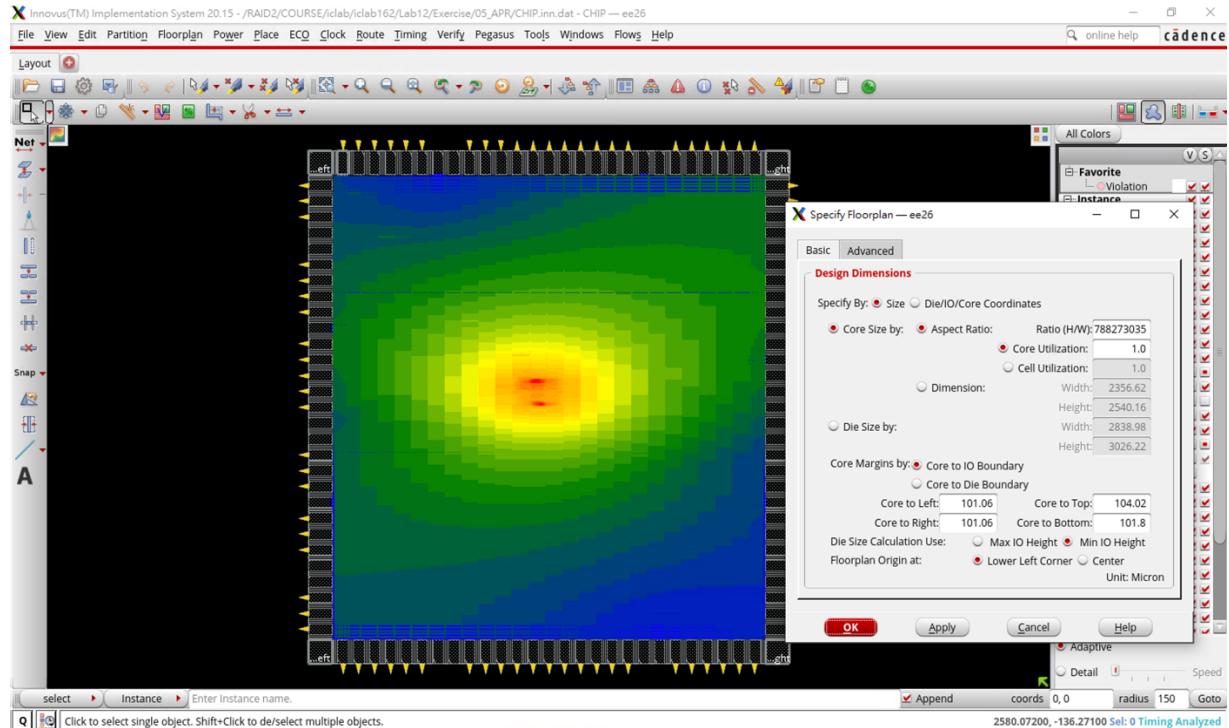
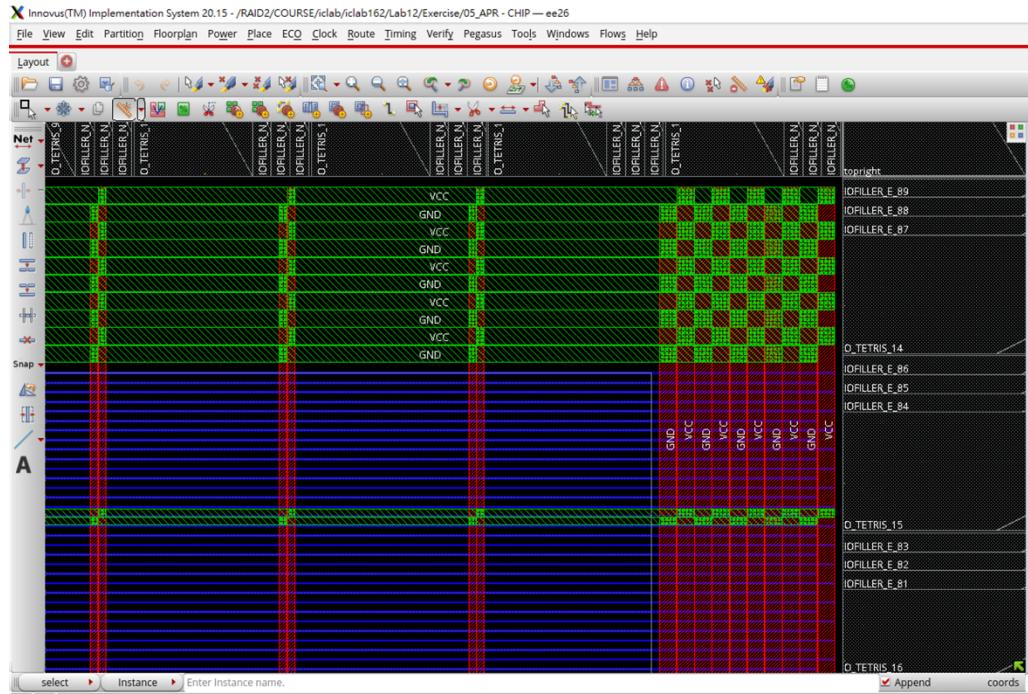


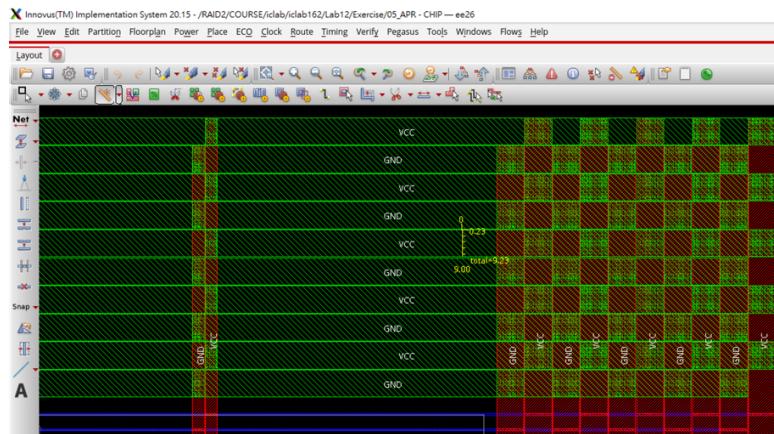
1. Core to IO boundary:



2. Core Ring :



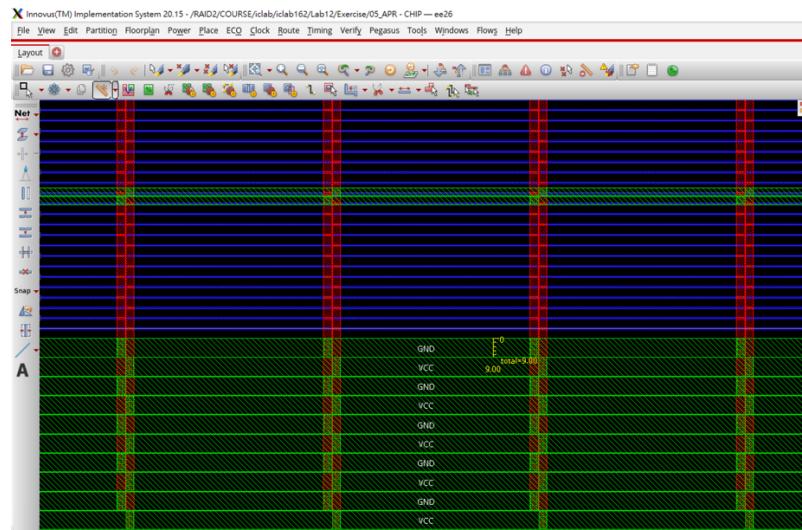
top :



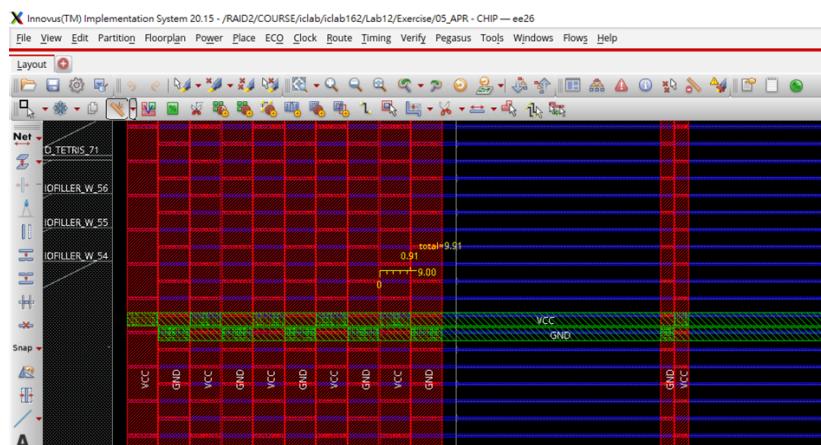
right :



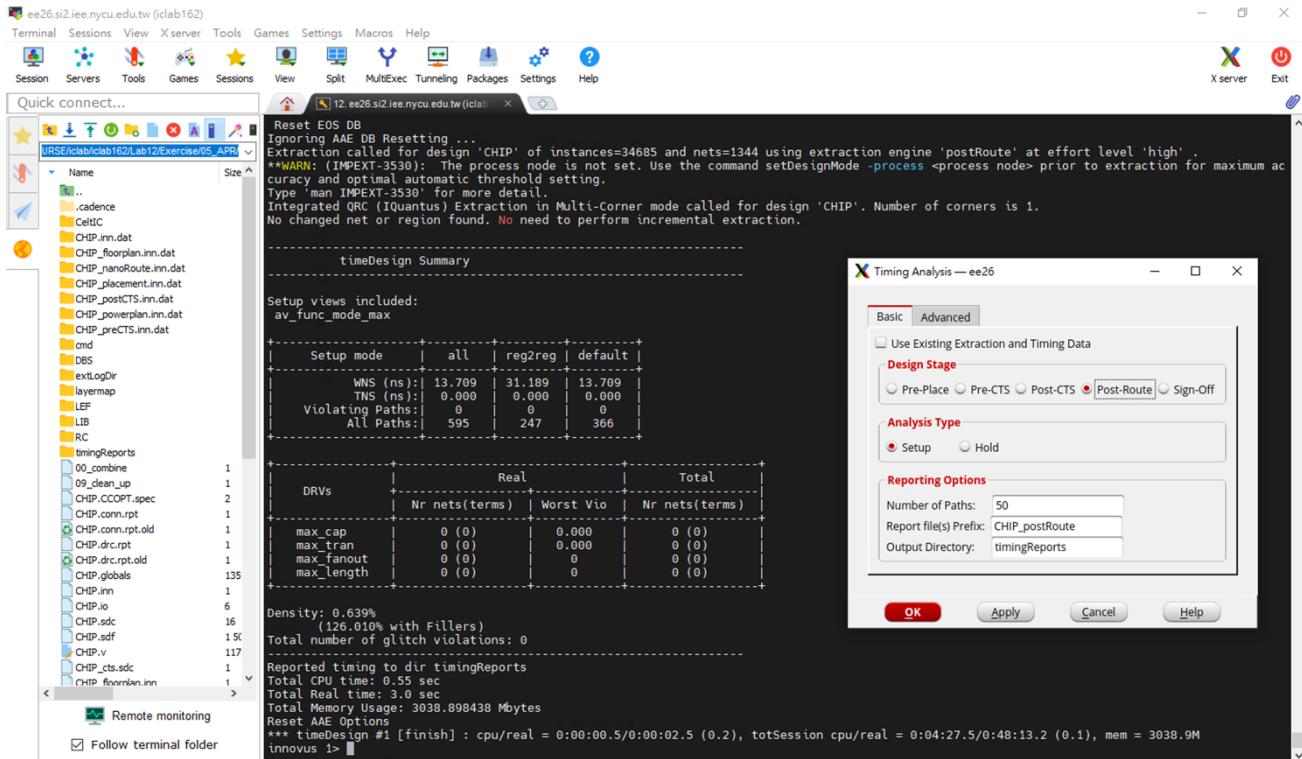
bottom :



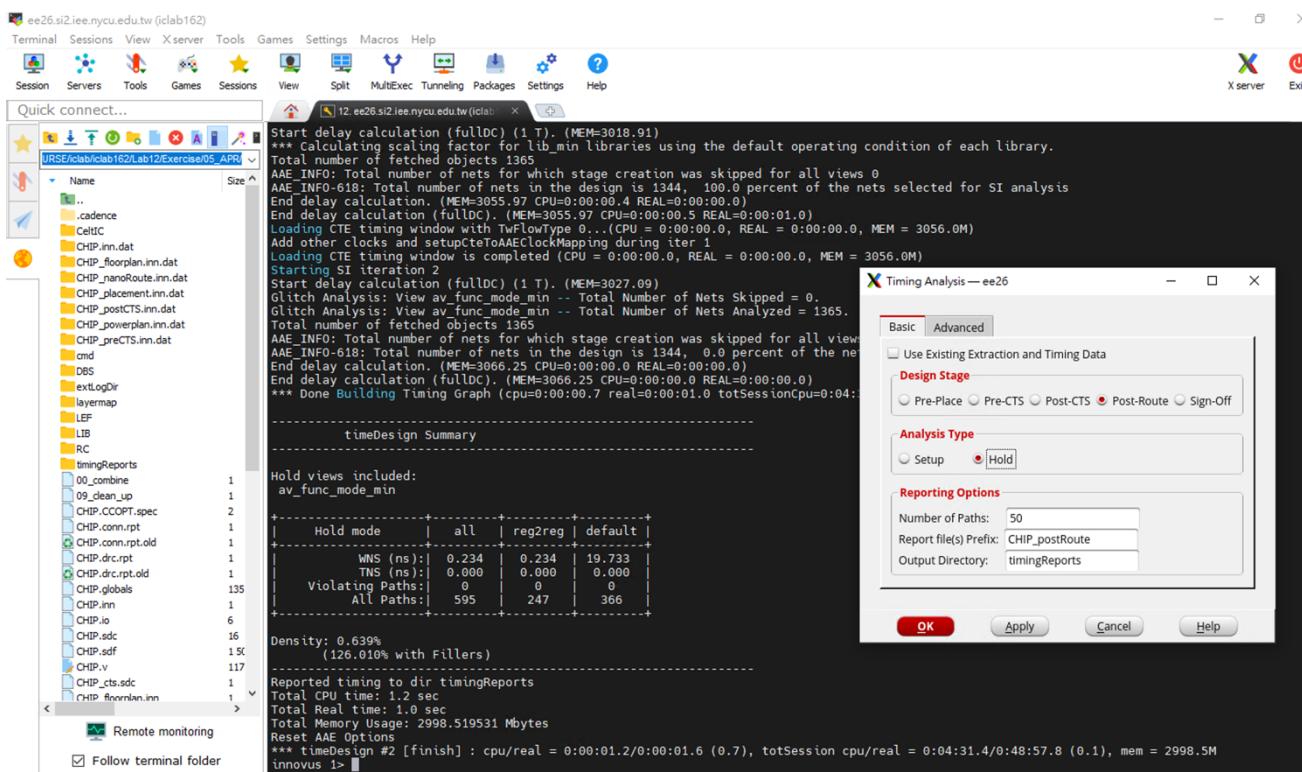
left :



3. Post-Route setup time analysis :



4. Post-Route hold time analysis :



5. DRC result :

```

ee26.si2.iee.nycu.edu.tw (iclab162)
Terminal Sessions View Xserver Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect...
12. ee26.si2.iee.nycu.edu.tw (iclab162) [idle] X server Exit
URSE/iclab162/Lab12/Exercise05_APR
Name
VERIFY DRC ..... Sub-Area : 112 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {522_240_2534_400_783_360_2787_840} 113 of 132
VERIFY DRC ..... Sub-Area : 113 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {783_360_2534_400_1044_480_2787_840} 114 of 132
VERIFY DRC ..... Sub-Area : 114 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {1044_480_2534_400_1305_600_2787_840} 115 of 132
VERIFY DRC ..... Sub-Area : 115 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {1305_600_2534_400_1566_720_2787_840} 116 of 132
VERIFY DRC ..... Sub-Area : 116 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {1566_720_2534_400_1827_840_2787_840} 117 of 132
VERIFY DRC ..... Sub-Area : 117 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {1827_840_2534_400_2088_960_2787_840} 118 of 132
VERIFY DRC ..... Sub-Area : 118 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {2088_960_2534_400_2350_080_2787_840} 119 of 132
VERIFY DRC ..... Sub-Area : 119 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {2350_080_2534_400_2611_200_2787_840} 120 of 132
VERIFY DRC ..... Sub-Area : 120 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {2611_200_2534_400_2838_980_2787_840} 121 of 132
VERIFY DRC ..... Sub-Area : 121 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {0_000_2787_840_261_120_3026_220} 122 of 132
VERIFY DRC ..... Sub-Area : 122 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {261_120_2787_840_522_240_3026_220} 123 of 132
VERIFY DRC ..... Sub-Area : 123 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {522_240_2787_840_783_360_3026_220} 124 of 132
VERIFY DRC ..... Sub-Area : 124 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {783_360_2787_840_1044_480_3026_220} 125 of 132
VERIFY DRC ..... Sub-Area : 125 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {1044_480_2787_840_1305_600_3026_220} 126 of 132
VERIFY DRC ..... Sub-Area : 126 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {1305_600_2787_840_1566_720_3026_220} 127 of 132
VERIFY DRC ..... Sub-Area : 127 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {1566_720_2787_840_1827_840_3026_220} 128 of 132
VERIFY DRC ..... Sub-Area : 128 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {1827_840_2787_840_2088_960_3026_220} 129 of 132
VERIFY DRC ..... Sub-Area : 129 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {2088_960_2787_840_2350_080_3026_220} 130 of 132
VERIFY DRC ..... Sub-Area : 130 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {2350_080_2787_840_2611_200_3026_220} 131 of 132
VERIFY DRC ..... Sub-Area : 131 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {2611_200_2787_840_2838_980_3026_220} 132 of 132
VERIFY DRC ..... Sub-Area : 132 complete 0 Viol.

Verification Complete : 0 Viol.

*** End Verify DRC (CPU: 0:00:00.6 ELAPSED TIME: 1.00 MEM: 20.0M) ***
innovus 1>

```

6. LVS result :

```

ee26.si2.iee.nycu.edu.tw (iclab162)
Terminal Sessions View Xserver Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect...
12. ee26.si2.iee.nycu.edu.tw (iclab162) [idle] X server Exit
URSE/iclab162/Lab12/Exercise05_APR
Name
VERIFY DRC ..... Sub-Area : 123 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {522_240_2787_840_783_360_3026_220} 124 of 132
VERIFY DRC ..... Sub-Area : 124 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {783_360_2787_840_1044_480_3026_220} 125 of 132
VERIFY DRC ..... Sub-Area : 125 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {1044_480_2787_840_1305_600_3026_220} 126 of 132
VERIFY DRC ..... Sub-Area : 126 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {1305_600_2787_840_1566_720_3026_220} 127 of 132
VERIFY DRC ..... Sub-Area : 127 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {1566_720_2787_840_1827_840_3026_220} 128 of 132
VERIFY DRC ..... Sub-Area : 128 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {1827_840_2787_840_2088_960_3026_220} 129 of 132
VERIFY DRC ..... Sub-Area : 129 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {2088_960_2787_840_2350_080_3026_220} 130 of 132
VERIFY DRC ..... Sub-Area : 130 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {2350_080_2787_840_2611_200_3026_220} 131 of 132
VERIFY DRC ..... Sub-Area : 131 complete 0 Viol.
VERIFY DRC ..... Sub-Area : {2611_200_2787_840_2838_980_3026_220} 132 of 132
VERIFY DRC ..... Sub-Area : 132 complete 0 Viol.

Verification Complete : 0 Viol.

*** End Verify DRC (CPU: 0:00:00.6 ELAPSED TIME: 1.00 MEM: 20.0M) ***
innovus 1> VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY_CONNECTIVITY *****
Start Time: Fri Dec 6 23:09:50 2024
Design Name: CHIP
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (2838.9800, 3026.2200)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
Found no problems or warnings.
End Summary

End Time: Fri Dec 6 23:09:50 2024
Time Elapsed: 0:00:00

***** End: VERIFY_CONNECTIVITY *****
Verification Complete : 0 Viol. 0 Wrngs.
(CPU Time: 0:00:00.1 MEM: 9.000M)
innovus 1>

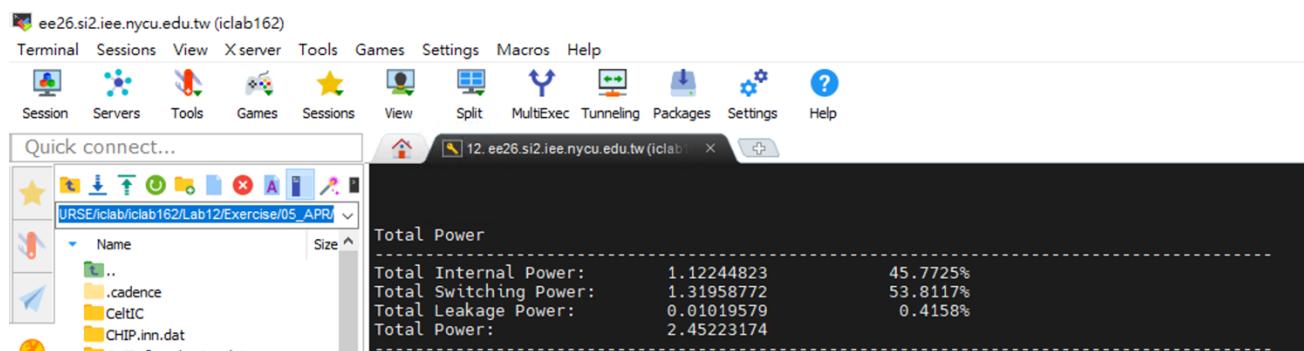
```

7. Post Layout simulation result :

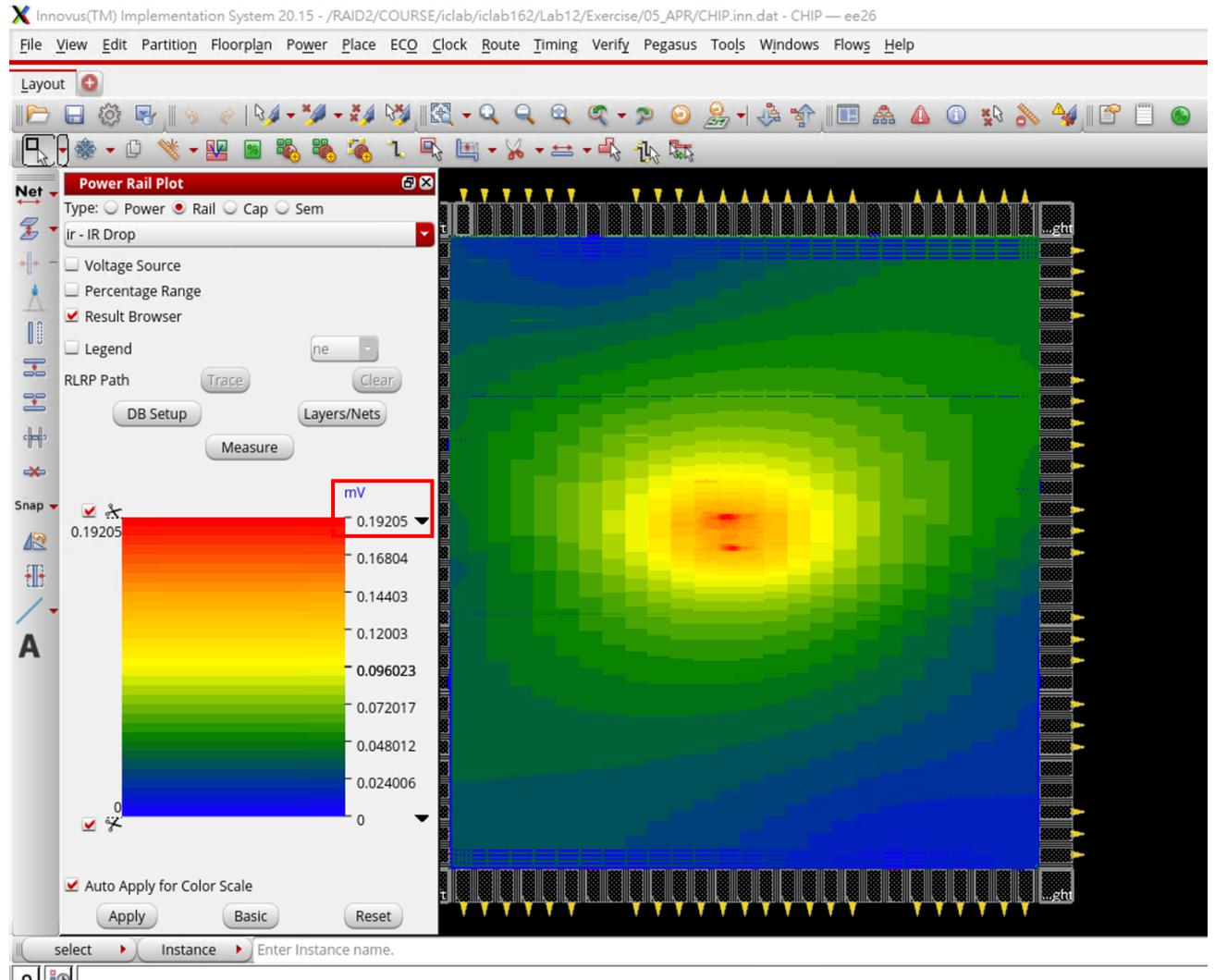
```
OUTPUT PORTS PROBLEMS SERIAL MONITOR TERMINAL DEBUG CONSOLE

No.      997 PASS
No.      998 PASS
No.      999 PASS
*****
    Congratulations!
        execution cycles = 84824
        clock period = 40.000000ns
*****
$finish called from file "PATTERN.v", line 26.
$finish at simulation time      4461420000
V C S   S i m u l a t i o n   R e p o r t
Time: 4461420000 ps
CPU Time: 7.230 seconds;      Data structure size: 0.6Mb
Fri Dec 6 22:13:49 2024
CPU time: 1.040 seconds to compile + .388 seconds to elab + .612 seconds to link + 7.291 seconds in simulation
22:13 iclab162@ee26[~/Lab12/Exercise/06_POST]$
```

8. Power result :



9. IR Drop Results :



我把 Core Utilization 設為 0.1 且 Core to IO boundary 都設為 101，開了 4 組的 Core power pads，平均的放在每一個邊上的對稱位置，為了控制 core 裡的每個點到 Core power pads 的距離都不會太遠，最終的 IR Drop 小於 0.2mV