Roll No.	2	0	2	1	1	0	2	3	8	

NIST INSTITUTE OF SCIENCE & TECHNOLOGY
(Autonomous)

B. Tech 3rd Semester (2021 Batch)				Branch(s)	CSE / IT
Subject Code	19CS3ES03T /19IT3ES03T	Subject Name		Digital Electronics Circuits	
Time	90 min	Exam	Mid Semester	Max. Marks	50
Examination Superintendent		Dr. Manabendra Patra			
Name of the Instructor(s)		*Prof. M. Suresh, Prof. Mitu Barala, Prof. Durga Prasad Dash*			
Date of Examination		*23/11/2022*	Sitting	1ST	

Answer Question No.1 from PART-I *which is compulsory, any four from PART-*II *and any one from* PART-III.

The figures in the right hand margin indicate marks.

PART-I

(Answer all the questions)

Q1.		CO	Level	Level-1: Knowledge Level-2: Comprehension Level-3: Application Level-4: Analysis Level-5: Synthesis Level -6: Evaluation	2 X 5
	(a)	1	2	What is the 16's complement of "EB2FC".	
	(b)	2	2	Write the Boolean expression of the outputs of a combinational circuit that does the subtraction of 2-bits serially.	
	(c)	1	2	Find the binary number representation of Gray code 110011111.	
	(d)	1	3	Show that Excess-3 code is a self complementing code.	
	(e)	2	3	If the Sum of the Full Adder will be implemented using only basic logic gates, find out the no. of gates required.	

PART-II

(Answer Any Four questions out of six)

Q2.		CO	Level	Level-1: Knowledge Level-2: Comprehension Level-3: Application Level-4: Analysis Level-5: Synthesis Level -6: Evaluation	4 X 6
	(a)	2	4	Represent the following function F = A'B(D' + C'D) + B(A + A'CD) using OR- AND-INVERT logic.	
	(b)	2	3	Prove that the Carry of a Full adder = XY+YZ+XZ, where X, Y, Z are the inputs.	
	(c)	1	3	F= B'CD'+A'B'C'+A'BCD'+AB'C' d(A,B,C,D)=∑(0,12,14,15) Simplify the function and also mention the prime implicants and essential prime implicants.	
	(d)	2	4	Design a 2-bit square circuit using only NAND gates.	
	(e)	2	3	Design a 16-bit Binary Parallel Adder (BPA) using four 4-bit BPAs. Use Block diagrams only to represent the 4-bit BPA. Describe the working principle of the circuit.	
	(f)	1	3	F=p'q+q'r'+pqr' Covert the function into PoS form and simplify it using Boolean laws.	

PART-III

(Answer Any One question out of two)

		CO	Level	Level-1: Knowledge Level-2: Comprehension Level-3: Application Level-4: Analysis Level-5: Synthesis Level -6: Evaluation	1 X 16
Q3.	(a)	2	3	Describe the Principle of "Carry" Look-ahead technique and its advantage. Write the Boolean functions and draw the logic diagram of a 4-bit carry look-ahead generator.	8
	(b)	2	3	Design a 4-bit parallel adder using carry look ahead generator. Write the Boolean expression for all the outputs.	8
Q4.	(a)	2	4	Design a Half Subtractor. Calculate the delay of the circuit if each of the following gates consumes the specified delays. AND =20 ns, OR = 12 ns, NOT =8 ns. EX-OR=42 ns, EX-NOR=36 ns	6
	(b)	2	4	Prove that a Full Subtractor can be designed using 2 half Subtractors with supportive Boolean expressions and draw the complete circuit. Also calculate the delay of the circuit by considering the gate delays mentioned in the above problem.	10