Registration No: -

2	2	0	1	2	0	2	4	5	5

Total Number of Pages: 03

B.Tech / 22IT3ES02T

3rd Semester Regular Examination: 2023-24

DIGITAL LOGIC DESIGN

BRANCH: IT

Time: 3 Hours

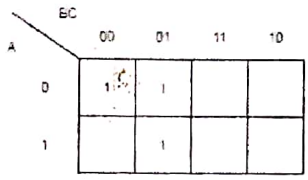
Max Marks: 100

Q Code: P132

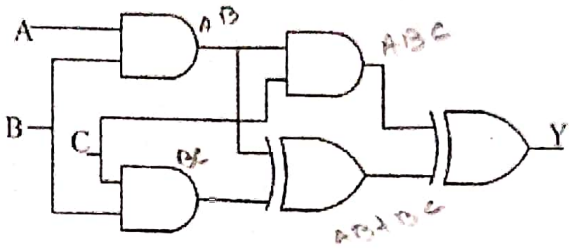
Answer Question No.1 (Part-1) which is compulsory, any EIGHT from Part-II and any TWO from Part-III.

The figures in the right hand margin indicate marks.

Part-I

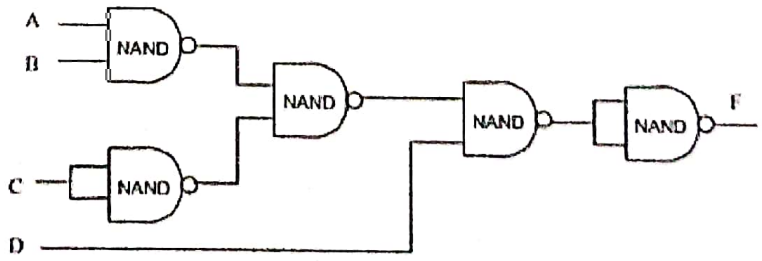
Q No.		CO	Level		
Q1				**Short Answer Type Questions (Answer All-10)**	(02x10)
	a)	1	1	Which logic gate is called universal logic gate and why it is called universal logic gate?	2
	b)	1	1	Which logic gate is said to be equivalence gate? Write its truth table.	2
	c)	2	3	Prove that: **AB + A'C + BC = AB + A'C** using Boolean algebra theorems and postulates	2
	d)	2	3	 Find the simplified SOP from above K-Map.	2
	e)	2	3	Design 4x1 MUX using 2X1 MUXes [use block diagram of 2x1 MUX]	2
	f)	2	3	Let a Gray code is: 10011010 Find the Binary equivalent of the above Gray code.	2
	g)	3	2	State the characteristic equation of T flip-flop.	2
	h)	3	2	What is the difference between SR flip-flop and JK flip-flop?	2
	i)	4	2	What is race-around condition?	2
	j)	4	3	How many address lines required to design a 512KB memory?	2

Part-II

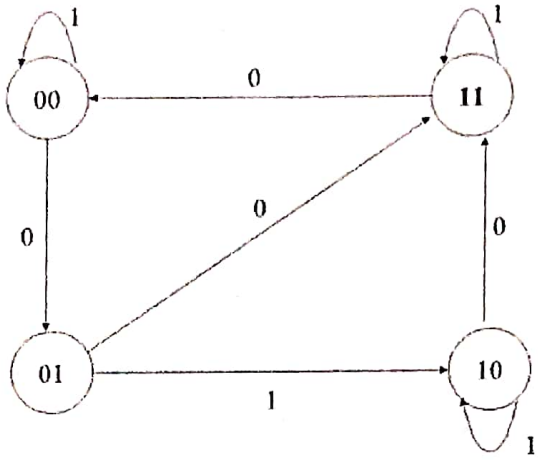
Q No.		CO	Level		
Q2				**Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)**	(06x08
	a)	1	3	Perform (23_{10}) - (-14_{10}) **using 2's complement** method.	6
	b)	1	3	For the circuit shown below, find the truth table and write the Boolean function of Y.	6
	c)	1			6
	d)	2	3	Simply the following function [in the form of SOP] using 4 variable K-Map $\mathbf{F(w,x,y,z)= \pi M(0,2,3,8,9,10,11,15)}$	6
	e)	2	3	Construct Full Adder using two Half Adders and with an additional logic gate.	6
	f)	2	3	Design 3 bit Binary to Gray code converter	6
	g)	2	3	Implement the given function using 8X1 MUX $\mathbf{F(A,B,C,D)= \sum m(1,4,5,7,9,12,13)}$	6
	h)	3	3	Derive Characteristic Table and Characteristic Equation of SR flip-flop	6
	i)	3	2	Draw and explain the operation of positive edge triggered D flip-flop	6
	j)	3	4	Show that a JK flip-flop can be converted to T flip-flop. Design it with the help of necessary tables and diagrams	6
	k)	4	2	Draw the diagram of 1-bit SRAM cell and explain its operation.	6
	l)	4	2	Differentiate between SRAM and DRAM	6

Part-III

Q No.		CO	Level		
Q3				**Long Answer Type Questions (Answer Any Two out of Four)**	(02x16
	a)	1	3	Reduce the following expressions to indicated number of literals: *i.* $(A' + C)(A' + C')(A + B + C'D)$ to four literals. *ii.* $(A'B(D' + C'D) + B(A + A'CD)$ to one literal.	8
	b)	1	3	Verify algebraically that the circuit shown in the below figure implements the following Boolean function, $F = \overline{C}(\overline{A} + \overline{B}) + \overline{D}$. Also represent F in canonical SOP form.	8



Q4	a)	2	3	A multiplier is a combinational logic circuit which multiplies two numbers in binary form. Design a 2-bit multiplier that multiplies two 2-bit numbers.	8
	b)	2	3	Design 4-bit Binary Parallel Adder using Full Adders.	8
Q5	a)	3	4	Design 3-bit synchronous DOWN counter. Draw the neat diagram of the counter.	8
	b)	3	4	Design the sequential logic circuit using T flip-flops which is described by the following state diagram	8



Q6	a)	3	3	Draw and explain the operation of SISO shift register. Find sequence of states of a Johnson Counter if the initial state is $(1000)_2$.	4+4
	b)	4	3	A decoder is used in memory decoding. Explain with the help of suitable example.	8