Roll No.	2	0	2	2	2	0	4	9	7	

NIST INSTITUTE OF SCIENCE & TECHNOLOGY
(Autonomous)

B. Tech 3rd Semester (2022Batch)				Branch(s)	CSE, IT, CST
Subject Code	22CS3ES02T	Subject Name		*Digital Logic Design*	
Time	*90 min*	Exam	Mid Semester	Max. Marks	50
Examination Superintendent		Prof. Chittaranjan Biswal			
Name of the Instructor(s)		Durga Prasad Dash, Mitu Baral, Malabika Pattnaik and Manoj K. Senapati			
Date of Examination		*25-11-23*	Sitting	1ST	

***Answer Question No.1from* PART-I *which is compulsory, any four from PART-II and any one from* PART-III.**

The figures in the right hand margin indicate marks.

PART-I

(Answer all the questions)

Q1.		CO	Level	**Level-1:** Knowledge **Level-2:** Comprehension **Level-3:** Application **Level-4:** Analysis **Level-5:** Synthesis **Level -6:** Evaluation	2 X 5
	(a)	1	3	Do the following operation (-15-12) in binary using 2's complement method.	
	(b)	1	3	A Max-term is represented by (P' + Q + R'+S'+T). What will be the Min-term for the corresponding inputs?	
	(c)	2	1	What is the application of Gray code?	
	(d)	2	3	A Multiplexer is having 10,000 data input lines. How many control signals are required to design it?	
	(e)	1	2	What do you mean by Negative logic in Digital circuit design?	

PART-II

(Answer Any Four questions out of six)

Q2.		CO	Level	Level-1: Knowledge Level-2: Comprehension Level-3: Application Level-4: Analysis Level-5: Synthesis Level -6: Evaluation	4 X 6
	(a)	1	3	Simplify the following function in SOP and POS forms $f(a,b,c,d) = \sum m(2,3,5,13,14) + d(8,9,10,11)$	
	(b)	2	2	Design the Borrow of a Full Subtractor using only 2-Level NOR gates.	
	(c)	2	2	Design a 3-bit Multiplier circuit.	
	(d)	2	3	Design a 3-bit Magnitude Comparator circuit	
	(e)	2	2	Specify the name of the arithmetic circuit that produces the output W= xy + yz +zx. Also draw it's truth table.	
	(f)	1	3	A 4-variable function is represented by F(p,q,r,s)=p'q' + rs' + qs. Represent the above function in canonical POS form and simplify it to POS form. Design the simplified expression using only NOR gates.	

PART-III

(Answer Any One question out of two)

		CO	Level	Level-1: Knowledge Level-2: Comprehension Level-3: Application Level-4: Analysis Level-5: Synthesis Level -6: Evaluation	1 X 16
Q3.	(a)	2	4	Design the following function using 4 to 1 MUX, where (a and d) should be used as the selection lines. $f(a,b,c,d) = \sum m(0,1,3,6,9,11,13,14)$	8
	(b)	2	3	Prove that a Full Adder can be designed using 2-Half Adders.	8
Q4.		2	4	Explain the disadvantages of Binary parallel adder and how to overcome it. Design the adder circuit that resolves the above issues. Also specifying the output logic expressions.	16