Roll No.	2	0	2	2	2	4	4	8	7	

NIST INSTITUTE OF SCIENCE & TECHNOLOGY
(Autonomous)

B. Tech 4th Semester (2022 Batch)				Branch(s)	CSE/IT/CST
Subject Code	22CS4PC01T/ 22IT4PCO1T/ 22CST4PC01T	Subject Name		*Computer Organization and Architecture*	
Time	*90 min*	Exam	Mid Semester	Max. Marks	50
Examination Superintendent		Prof. Chittaranjan Biswal			
Name of the Instructor(s)		*RabindraKumar Shial,Nibedita P.Mohapatra,Manoj Sahoo,Dr.P.Rajesh Kumar,Dr.Satya Sopan Mahato*			
Date of Examination		*16/04/2024*	Sitting	2nd	

***Answer Question No.1from* PART-I *which is compulsory, any four from PART-II*and *any one from* PART-III.**
The figures in the right hand margin indicate marks.

PART-I

(Answer all the questions)

Q1.		CO	Level	**Level-1:** Knowledge **Level-2:** Comprehension **Level-3**: Application **Level-4**: Analysis **Level-5:** Synthesis **Level -6:** Evaluation	2 X 5
	(a)	1	2	What are the different steps of instruction cycle?	2
	(b)	1	2	What are the different buses in a system?	2
	(c)	2	3	Find out the delay in 4-bit ripple carry adder and 4-bit carry lookahead adder.	2
	(d)	1	2	Differentiate between byte and word addressibility.	2
	(e)	2	2	What are the three essential elements of a number in float point notation?	2

PART-II

(Answer Any Four questions out of six)

Q2.		CO	Level	Level-1: Knowledge Level-2: Comprehension Level-3: Application Level-4: Analysis Level-5: Synthesis Level -6: Evaluation	4 X 6
	(a)	1	2	Discuss Von-Neumann architecture.	6
	(b)	1	2	Compare between RISC and CISC with suitable example.	6
	(c)	1	3	Write assembly programs that can evaluate the expression R=(P*Q)+(U-V) in a machine that supports (i) Two-address instruction format and (ii) one-address instruction format.	6
	(d)	1	2	An instruction is stored at location 600 with its address field at location 601. The address field has value 200. The content of R1 processor register is 400. Evaluate the effective address of the addressing mode of the instruction is (i) Direct (ii) Immediate (iii) Relative (iv) Register indirect (v) Index with R1 as a index register.	6
	(e)	2	3	Perform Booth multiplication on the following numbers: (-8) x (5).Show all the steps while performing the multiplication.	6
	(f)	2	3	Design 8-bit Ripple Carry Adder using 4-bit Ripple Carry Adder and calculate propagation delay for sum and carry.	6

PART-III

(Answer Any One question out of two)

		CO	Level	Level-1: Knowledge Level-2: Comprehension Level-3: Application Level-4: Analysis Level-5: Synthesis Level -6: Evaluation	1 X 16
Q3.	(a)	1	2	Explain basic operation of a system and Draw the internal architecture of a processor.	8
	(b)	2	3	Represent the number 94.125 in IEEE 754 Single precision and double precision floating point number.	8
Q4.	(a)	1	2	Explain about the types of addressing modes with example for each of them.	8
	(b)	2	3	Describe Booth algorithm using flow chat and multiply (-3) x (-5) using recording bit procedure..	8