Registration No: - | 2 | 2 | 0 | 1 | 2 | 0 | 2 | 4 | 5 | 5 |

Total Number of Pages: 02

B.Tech / 22IT4PC01T

4th Semester Regular Examination: 2023-24

COMPUTER ORGANIZATION AND ARCHITECTURE

BRANCH: IT

Time: 3 Hours

Max Marks: 100

Q Code: Q104

Answer Question No.1 (Part-1) which is compulsory, any EIGHT from Part-II and any TWO from Part-III.

The figures in the right hand margin indicate marks.

Part-I

Q No.		CO	Level		
Q1				**Short Answer Type Questions (Answer All-10)**	(02x10)
	a)	4	1	What are the different hazards in pipeline?	2
	b)	2	3	Design a 4-bit ripple carry adder.	2
	c)	1	3	An address field in an instruction contains the decimal value 16. Where is the corresponding operand located in the register addressing mode?	2
	d)	1	4	If an instruction contains four addresses, what might be the purpose of each address?	2
	e)	2	4	Consider a 6-bit floating-point format (Mantissa=3 bits, Exponent=3 bits). The 3-bit mantissa is signed-magnitude fraction and floating point number is normalized with an excess-K biased exponent. What is the suitable value of K?	2
	f)	3	2	What are the differences among EPROM, EEPROM, and flash memory?	2
	g)	2	2	What are the four essential elements of a number in floating-point notations?	2
	h)	1	2	Differentiate between computer organization and computer architecture.	2
	i)	3	3	What is memory hierarchy? With neat diagram mention the different types of memories in the memory hierarchy.	2
	j)	4	1	What are the different I/O data transfer modes?	2

Part-II

Q No.		CO	Level		
Q2				**Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)**	(06x08)
	a)	2	4	Multiply X (Multiplicand) with Y(Multiplier) using Booth's algorithm. X = 01111, Y = 11010.	6
	b)	1	2	With suitable diagram explain the difference between Harvard and Von-Neumann architecture.	6
	c)	3	2	Write short note on Set-Associative Mapping.	6
	d)	2	3	Divide −16 by 3 using two's complement division technique.	6
	e)	3	2	What are the differences among direct mapping, associative mapping, and set-associative mapping?	6

	f)	3	3	Draw the architecture for single-bus organization of data path inside a processor. Write the sequence of control steps required to execute the instruction "Add the contents of memory location NUM to register R1" in this architecture. Assume that each instruction consists of two words. The first word specifies the operation and the addressing mode, and the second word contains the number NUM ?	6
	g)	3	2	What is the difference between DRAM and SRAM in terms of characteristics such as speed, size, and cost?	6
	h)	3	2	What do you understand by semiconductor memory technology? How does it enhances the storage efficiency?	6
	i)	4	2	Differentiate between memory- mapped I/O and I/O mapped I/O.	6
	j)	3	3	Consider a single-level cache with an access time of 2.5 ns, a block size of 64 bytes, and a hit ratio of 0.95. Main memory uses a block transfer capability that has a first-word (4 bytes) access time of 50 ns and an access time of 5 ns for each word thereafter. What is the access time when there is a cache miss? Assume that the cache waits until the block has been fetched from main memory and then re-executes for a hit.	6
	k)	2	4	Design a half adder as two-level AND-OR circuit. Compute gate delay for sum and carry.	6
	l)	2	3	Convert 94.125 to IEEE 754 single and double precision floating point number.	6

Part-III

Q No.		CO	Level	**Long Answer Type Questions (Answer Any Two out of Four)**	(02x16)
Q3	a)	2	3	Carry-save Addition (CSA) is a technique to speed up multiplication process. Multiply X = 111110 with Y = 111111 using CSA technique.	8
	b)	3	2	What is the general relationship among access time, memory cost, and capacity?	8
Q4	a)	1	2	Draw block diagram of computer system. Describe the function of each component of computer system.	8
	b)	1	3	Write a program to evaluate the arithmetic statement: X = (A – B + C * (D * E – F) / (G + H * K) in a computer with a two-address instruction set. Your program should retain the content of the original variables.	8
Q5	a)	3	4	Design a 64kx8 memory module using 16kx1 memory chips.	8
	b)	4	3	The following sequences of instructions to be executed in a 5-stage pipeline. I1: Load R8, (R3) I2: Add R3, R3, 4 I3: Load R9, (R3) (i) Show the pipeline execution of the above instructions, without data forwarding. Find the number of clock cycles needed to execute the instruction. (ii) Show the pipeline execution of the above instructions, with data forwarding. Find the number of clock cycles needed to execute the instruction.	8
Q6	a)	3	2	What are the differences between write-back and write-through cache, and what are the implications for system performance?	8
	b)	3	4	A cache has a 95% hit ratio, an access time of 200ns on a cache hit and an access time of 800ns on a cache misses. Compute the effective access time.	8