AMBA-APB Verification key Scenarios: (Sequences/Testcases needs to be created)

1. **Basic read/write transactions: -**
   - Verify basic read and write operations to different address locations with specific data values.
   - Verify basic read and write operations to different address locations with random data values.
   - Single byte, half-word, and word reads/writes to different address locations.
   - Verify correct data transfer for valid addresses within the peripheral's address space.
   - Check proper assertion of PREADY signal during data transfer.
   - Generate random data with specific patterns through constraints and check for the write/read operation in different address locations
   - Stress test : Create and send 100 random APB read/write transaction and send to driver
2. **Address range checks: -**
   - Test access attempts outside the defined address range to ensure proper error handling.
   - Accessing addresses outside the defined peripheral address range
   - Verify appropriate error handling (e.g., protocol violation detection) on invalid addresses
3. **Error handling checks: -**
   - Slave Error Response: Verify that the slave signals a proper error response (like PSLVERR) when encountering invalid accesses.
   - Invalid Address Detection: Test scenarios where invalid addresses are used and the slave reports an error.
   - Data Parity Errors: Injecting parity errors in data transfers. (If applicable) Simulate data parity errors and check the error detection mechanism.
4. **Multiple Concurrent Accesses checks: -**
   - Simulate multiple masters accessing the same slave simultaneously.
   - Verify correct arbitration and data transfer behavior in a multi-master environment .
5. **Mixed Read/Write Operations: -**
   - Interleave read and write transactions to different addresses.
   - Check for proper data consistency and timing relationships.
6. **Access to Reserved Addresses: -**
   - Attempting to access reserved address ranges within the peripheral space .
   - Verify that the slave device handles reserved addresses appropriately.
7. **Edge Case Scenarios: -**
   - Invalid data widths (e.g., attempting to transfer data wider than the bus allows) .
   - Boundary conditions (accessing the first and last addresses in the address range) .
   - Data width check-Verify data transfers with different data widths supported by the APB interface .
   - Clock Domain Crossing- If applicable, test scenarios where data crosses between different clock domains.
   - Power Gating- Verify proper behavior when the APB slave is power-gated and then reactivated.
   - Corner Cases- Explore extreme values for address and data, and test for unexpected behaviour.

8. **Timing and wait states checks:-**
   - Normal Access with No Wait States: Test standard data transfers without any wait states.
   - Wait State Insertion: Verify correct behavior when the slave asserts "PREADY" signal, indicating the need for wait states.
   - Random Wait State Patterns: Introduce random wait state sequences to check for proper handling.
9. **Advanced Scenarios: -**
   - Burst Transfers: If supported, test burst mode transfers with different burst lengths.
   - Multiple Slave Accesses: Simulate scenarios where multiple slaves on the APB bus are accessed concurrently.
   - Access Permissions: Verify proper handling of read/write permissions on specific registers based on security settings.
10. **Randomization and Coverage:**
    - Random Address Generation: Generate random addresses within the valid address range to cover a wide range of access patterns.
    - Random Data Patterns: Randomize data values to test different data combinations.
    - Random Access Sequence: Create randomized sequences of read and write operations to improve coverage.