Jie Liu

471B Frank H. T. Rhodes Hall, Ithaca, NY 14850
Email: jl3952@cornell.edu • Phone: +1 (607) 216-7193
Website: https://sibylau.github.io • Github: Sibylau • LinkedIn: jl3952

EDUCATION

Cornell University, Ithaca, NY, USA

- Ph.D. student in Computer Systems Lab, ECE — Aug 2019 – Present
  - Advisor: Prof. Zhiru Zhang
  - Courses: Computer Architecture (A), Complex Digital ASIC Design (A), Advanced Compilers (A)

Tsinghua University, Beijing, China

- B.Eng in Microelectronic Science and Engineering — Sep 2015 – Jul 2019
  - Overall GPA: 3.62/4.0; Rank: 5/24

PROFESSIONAL EXPERIENCE

Xilinx, Inc., San Jose, CA, USA

- Compiler Intern at Xilinx Research Labs — May 2021 – Aug 2021
  - Hiring manager: Dr. Stephen Neuendorffer

University of California, Los Angeles (UCLA), Los Angeles, CA, USA

- Undergraduate Research Intern at the VAST Laboratory — Jun 2018 – Sep 2018
  - Advisor: Prof. Jason Cong
  - Mentor: Dr. Jie Wang

RESEARCH PROJECTS

Unified Abstraction of Sparse Formats for Compilers on Heterogeneous Platforms
Ph.D. student, With Prof. Zhiru Zhang, Cornell University — Sep 2021 – Present

- Proposed a unified tensor format abstraction to express both classic and custom hardware-friendly sparse formats.
- Implemented a compiler flow based on the MLIR framework that automatically converts tensor formats and generates sparse processing kernels.

Automatic Loop Scheduling for Spatial Architectures
Compiler Intern, With Dr. Stephen Neuendorffer, Xilinx, Inc. — May 2021 – Aug 2021

- Proposed an ILP model to solve for optimal mapping solutions from algorithmic loops to spatial architectures under given resource constraints.
- Implemented an automatic loop scheduling flow configured by results of the ILP solver as part of the MLIR AIEngine toolchain.

Backend Optimization for HeteroCL
Ph.D. student, With Prof. Zhiru Zhang, Cornell University — Sep 2020 – May 2021

- Implemented a loop unroll pass based on LLVM IR rewriting for HeteroCL.
- Implemented a Mentor Graphics Catapult High-Level Synthesis (HLS) backend for HeteroCL.

A Row-Wise Product Based Sparse-Sparse Matrix Multiplication Accelerator
Ph.D. student, With Prof. Zhiru Zhang, Cornell University — Nov 2019 – Sep 2020

- Involved in the design of a hardware friendly sparse format and a row-wise product based specialized accelerator architecture for sparse-sparse matrix multiplication (SpGEMM).
- Implemented the accelerator using PyMTL and Mentor Graphics Catapult HLS tool.

Systolic Array Design Implementation for Matrix Decomposition Algorithms
Undergraduate Research Intern, with Prof. Jason Cong, UCLA — Jul 2018 – Oct 2018

- Designed 1D and 2D highly-optimized systolic array architectures based on polyhedral analysis theory using Xilinx Vivado HLS tools.
- Achieved up to 50.13x and 4.58x better throughput compared with the Xilinx HLS linear algebra library and the LAPACK library on single-thread CPUs.

IMU-based System for Real-Time Pelvis Plane Measurement
Undergraduate Research Assistant, with Prof. Hong Chen, Tsinghua University — Oct 2017 – Apr 2018

- Built a pelvis position measurement system with IMU sensor modules, and optimized the position estimation algorithm for better accuracy and stability.

PUBLICATIONS

CONFERENCES

[1] N. Srivastava, H. Jin, J. Liu, D. Albonesi, and Z. Zhang, **MatRaptor: A Sparse-Sparse Matrix Multiplication Accelerator Based on Row-Wise Product**, 2020 53rd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), pp. 766-780. IEEE, 2020.

JOURNALS

[1] H. Chen, Z. Cao, S. Su, J. Liu and Z. Wang, **Measurement System for Attitude of Anterior Pelvic Plane and Implantation of Prothesis in THR Surgery**, *IEEE Transactions on Instrumentation and Measurement*,vol. 67, no. 8, pp. 1913-1921, Aug 2018.

POSTERS

[1] Jie Liu, Jason Cong, **Dataflow Systolic Array Implementations of Matrix Decomposition using High Level Synthesis**, *27th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2019)*, February 24-26, 2019, Monterey Bay Seaside, California, USA.

[2] Jie Liu, Hong Chen, Zhihua Wang, **IMU-based Real-Time Acetabular Prosthesis Implant Angles Measurement in Total Hip Replacement Surgeries**, *IEEE Biomedical Circuits and Systems Conference (BioCAS 2018)*, October 17-19, 2018, Cleveland, Ohio, USA.

SKILLS

Programming Languages: C/C++, Python, Matlab, Verilog / PyMTL, LaTeX, HSpice, SQL.
Frameworks: MLIR / LLVM
CAD Tools: Mentor Catapult HLS, Cadence Stratus HLS, Xilinx Vitis HLS

HONORS

Jacobs Scholar Fellowship, Cornell University 2019
Excellent SRT (Student Research Training) Project Award, Tsinghua University 2019
Summer Overseas Research Training Scholarship, Tsinghua University 2018