VCS

Industry's highest performance simulation solution

Overview

The Synopsys VCS® simulation solution (Figure 1) is the primary verification solution used by the majority of the world's top 20 semiconductor companies. VCS provides the industry's highest performance simulation and constraint solver engines. In addition, the comprehensive VCS solution offers Native Testbench (NTB) support, broad SystemVerilog support, verification planning, coverage analysis and closure, and native integration with Verdi® automated debug, the industry's de-facto debug standard. VCS is uniquely positioned to meet designers' and verification engineers' needs to address the challenges and complexity of today's SoCs.

Key Benefits

Industry-Leading Performance and Capacity

- Fine-grained parallelism: Support for multicore and many-core X86 processors
- Compile time: Partition compile, Dynamic Reconfiguration, Dynamic Test Loading (DTL)
- Runtime: Save/Restore, Constraint Solver optimization, Multicore

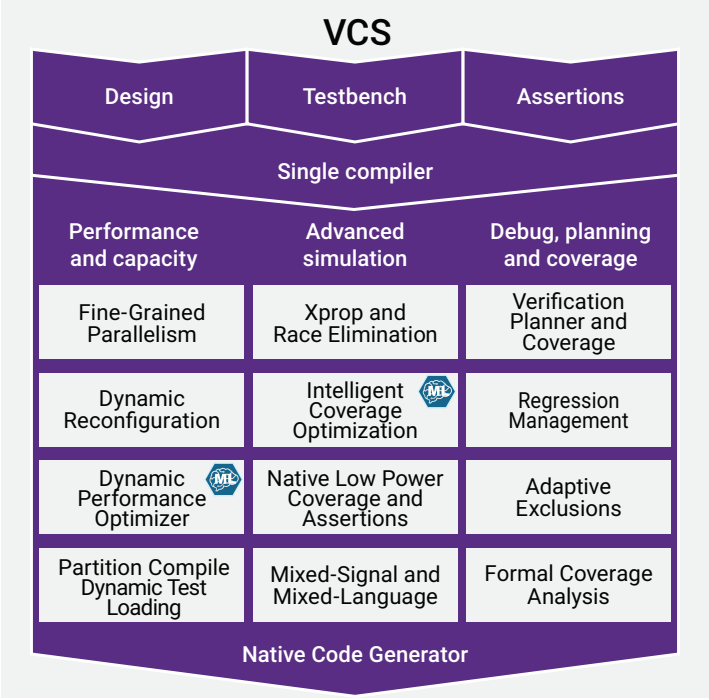

Figure 1: VCS simulation solution

Advanced Simulation Technologies

- Native low power, Xpropagation, SystemC and AMS co-simulation

Comprehensive and Natively-Integrated Planning, Coverage, Debug and Execution Management

- VCS provides key turnaround time and ease-of-use benefits via native integration with Verdi debug, VC Formal™ formal verification and VC VIP

Language Compliance

VCS supports all popular design and verification languages, including SystemVerilog, Verilog, VHDL, OpenVera™, SystemC™, and the Accellera® UVM™, VMM, and OVM methodologies (Figure 2). VCS' support for Accellera UVM also includes access to the VMM/UVM interoperability kit, which enables the use of VMM with UVM and vice versa. Besides supporting digital circuit design, VCS also supports analog and mixed-analog designs through Verilog-AMS, SPICE and SPF. This comprehensive support for advanced flows and methodologies enables VCS to help users develop the highest-quality mixed language functional verification environments in the shortest amount of time.

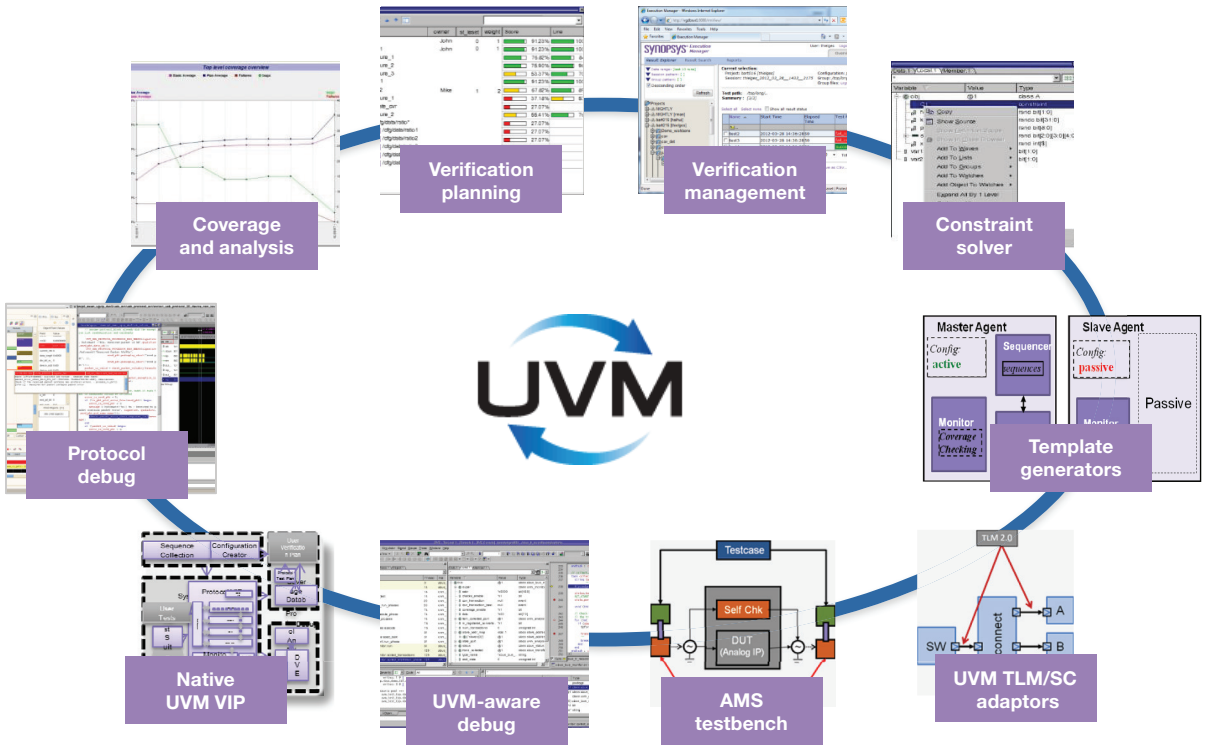

Figure 2: Complete SystemVerilog ecosystem

Verification Continuum Platform

VCS is the center of the most comprehensive and natively-integrated functional verification ecosystem in the industry. Complementing simulation, the VCS functional verification ecosystem provides formal verification with VC Formal, emulation with ZeBu® Server, testbench quality analysis with Certitude® functional qualification system and comprehensive coverage closure. The VCS ecosystem is a core element of the Synopsys Verification Continuum® Platform (Figure 3).

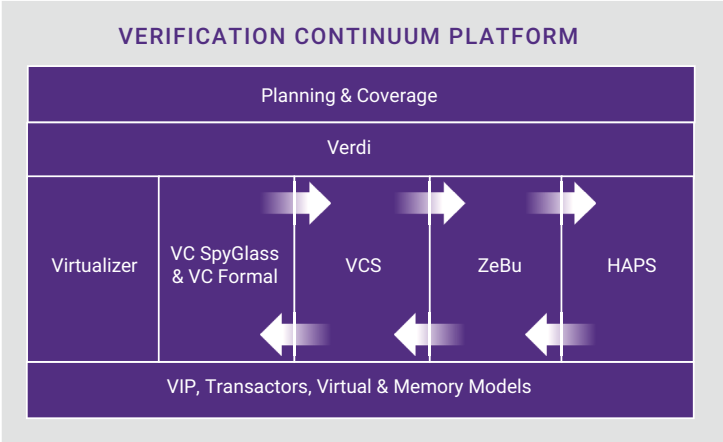

Figure 3: Synopsys Verification Continuum Platform

Performance

VCS is the industry's highest performance simulation solution. VCS offers industry-leading compile time and run time performance improvement technologies, and advanced fine-grained parallelism for simulation runtime reduction.

Compile Time Reduction for SoC Designs

VCS provides advanced tools for reducing compile turnaround time for complex SoC designs, including Precompiled IP support targeted at IP integration flows, Partition Compile to isolate portions of the testbench that are not changing during development cycles, and Dynamic Reconfiguration to compile for a target and select which model is used at runtime (Figure 4). Combined, these tools offer the most comprehensive set of solutions to maximize compile efficiency and reduce turnaround time for SoC verification flows.

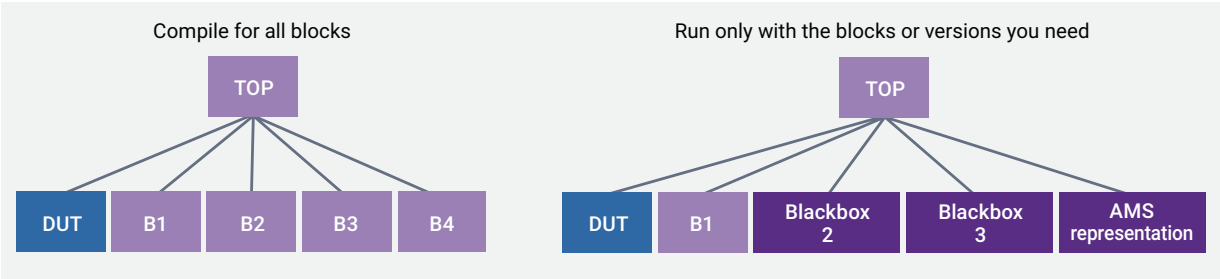

Figure 4: Dynamic reconfiguration

Partition Compile

VCS' Partition Compile technology allow users to achieve up to 10x faster compile time by only recompiling code that has changed and reusing the libraries for the unchanged modules already compiled earlier.

Dynamic Reconfiguration

VCS' Dynamic Reconfiguration (Figure 4) feature enables turnaround time reduction over entire regressions by allowing users to compile once and run different configurations/testbenches without need for recompiles. All debug and coverage features work seamlessly regardless of configuration.

Dynamic Test Loading (DTL)

VCS' DTL enables users to load or switch test sequences dynamically at run time. In addition, the simulator executable (simv) is not required to be generated for any new test, reducing re-compile time significantly. It also restores the simulation from a stored timestamp and saves run time by not repeating the common routines like reset and initialization sequences for the dynamically loaded test. DTL enhances performance by saving both compile and run time significantly.

Simulation Runtime Reduction

VCS' high performance simulation engine is continuously improved with state-of-the-art performance and memory optimization technologies, including advanced fined-grained parallelism support. These technologies provide best-in-class out of the box performance, and also support tuning simulator performance to a wide variety of user environments.

Fine-Grained Parallelism (FGP)

VCS' revolutionary FGP simulation technology enables far better performance compared to previous technologies by optimally aligning the size and requirements of the simulation tasks and the hardware resources available (either mainstream multicore processors, many-core processors, or both) — allowing far greater effective parallelization of the overall simulation, reducing simulation runtime by up to 2X for RTL and 5X for gate-level simulation, and enabling far better utilization of available hardware (Figure 5).

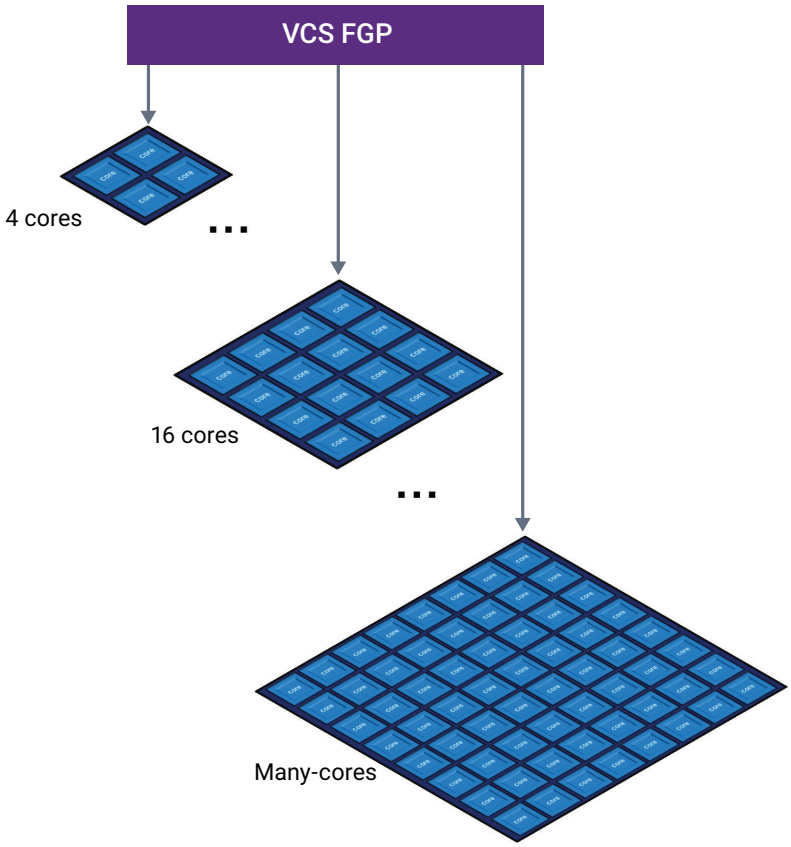

Figure 5: Supports available X86 cores

Because VCS FGP is a native feature, serial performance gains and parallel performance gains multiply, and all simulation technologies are supported, including Xprop, Native Low Power, SDF support, and parallelized FSDB dumping.

Save/Restore

Save/Restore feature (Figure 5) lets the user save the state of simulation in a file for it to be restored at another time or on a different machine. Designs that have a long design initialization simulation can benefit from this feature by saving the initial state and restoring the simulation to after initialization in subsequent runs thereby reducing simulation time.

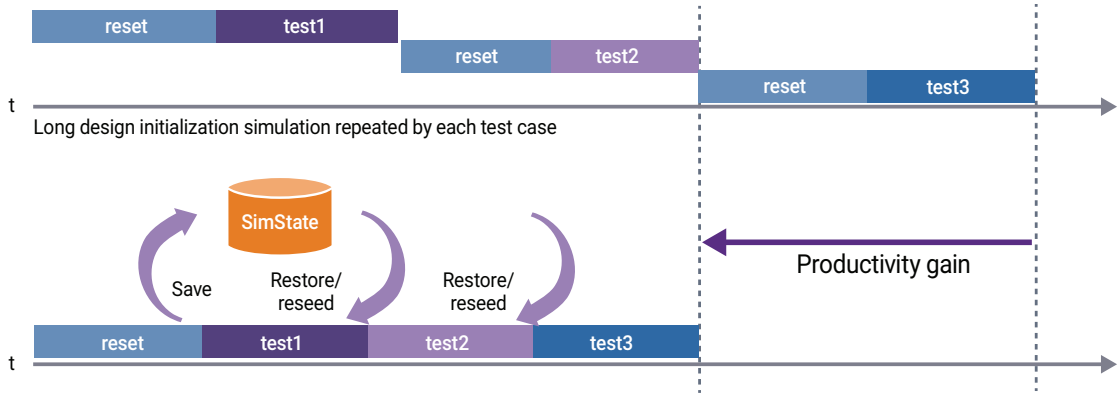

Figure 6: Save/restore benefit

Constraint Solver

VCS' industry-leading, high-performance constraint solver technology is powered by multiple solver engines that simultaneously analyze all user specified constraints to rapidly generate high-quality random stimulus that verifies corner case behavior. The constraint solver engines will find a solution to user constraints if one exists, minimizing constraint conflicts and maximizing verification productivity. This feature is essential for directing the randomized testing strategy towards a meaningful space and speeds up bug finding.

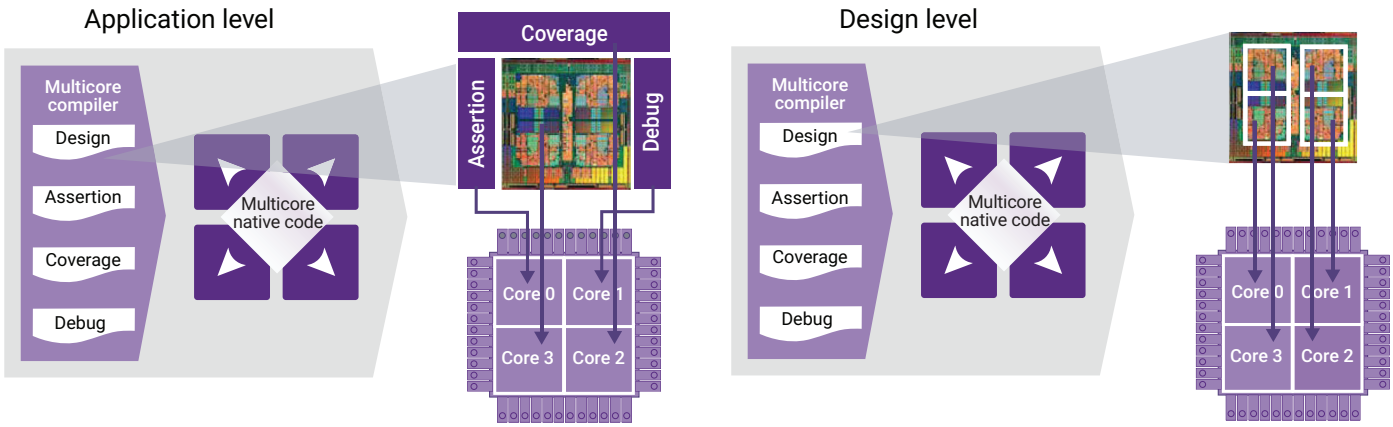

Figure 7: Verdi design and testbench debug

Advanced Simulation Technologies

Beyond simulation performance, VCS provides the broadest support for advanced simulation technologies needed to accurately and completely verify today's advanced designs.

Dynamic Performance Optimizer (DPO)

Dynamic Performance Optimizer (DPO) is an intelligent automated approach leveraging ML that enables necessary diagnostics during VCS compile and simulation to recommend optimizations for enabling maximum performance without manual intervention. DPO can achieve up to 2X performance gain over default settings depending on the design topology.

Intelligent Coverage Optimization (ICO)

VCS' ML-driven ICO technology allows adaptive stimulus input biasing to efficiently diversify the constraint random stimuli creation. It improves the stimulus quality, diversity scores, coverage and increases the likelihood of exposing new bugs. It also provides visibility to stimuli distribution, over-constraining and skewed distribution.

ICO accelerates coverage closure by 2X by improving the regression turnaround time (TAT), resulting in better time-to-market and first pass silicon success

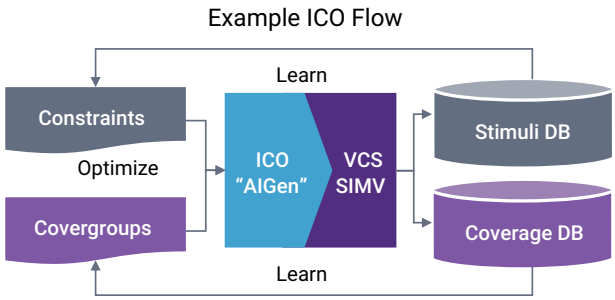

Figure 8: Intelligent Coverage Optimization (ICO)

Native Low Power

VCS' Native Low Power (NLP) simulation technology provides VCS with comprehensive low power verification and debug capabilities. NLP integration with Verdi also enables easy LP debug with advanced LP features, and provides excellent support for LP assertions and coverage for coverage-driven verification flows. VCS' native low power solution allows user to perform multi-voltage simulations so that they can feel the freedom to implement several techniques for power management.

Xpropagation

Certain RTL semantics, such as using x-value to denote indeterminate state, may not model actual hardware behavior accurately. Instead of having to rely on increasingly costly gate level simulation, VCS provides a way to simulate Xpropagation in multiple modes to model x-value in either more, less or equally optimistic modelling as compared to the regular gate-level simulation.

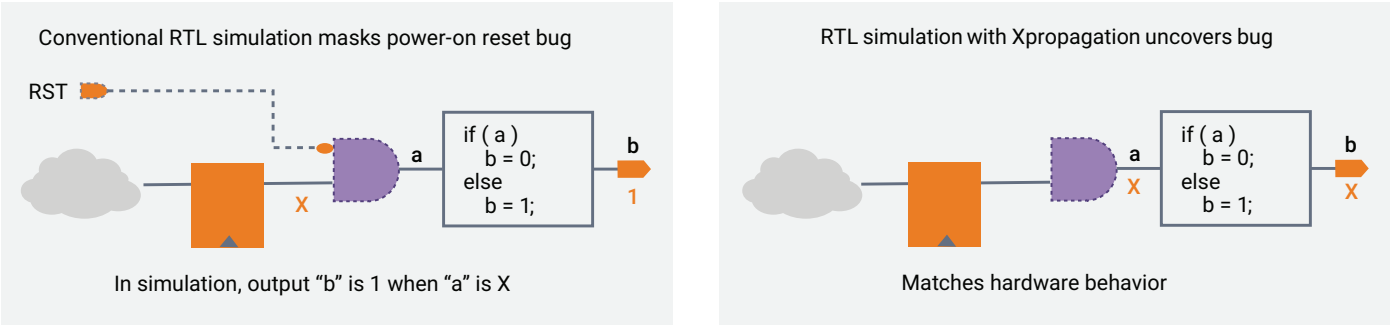

Figure 9: VCS Xpropagation support

Dynamic SDC Verification

VCS' SDC (Synopsys Design Constraints) Verification includes native capabilities to shift left Clock Domain Crossing (CDC) signoff and MCP (Multi Cycle Path) verification early from gate-level to RTL simulation. Users can inject metastability (jitter) at RTL to improve confidence for CDC signoff and verify the correctness of MCP at RTL level by providing SDC to VCS. In-addition, Verdi can be used for effective debug and analysis, including X-injection. The solution enables users to unmask critical design bugs early in the design cycle resulting in faster time-to-market.

SystemC Simulation and Co-simulation support

VCS SystemC support is fully compliant with IEEE 1666 SystemC versions and provides both direct simulation and cosimulation support. Direct variable access from/to SystemVerilog is supported, as are function calls across languages. VCS Profiler supports native SystemC profiling, and advanced debug is supported in Verdi CBug feature.

Component		Percentage
HSIM		0.00%
SystemC		10.07%
KERNEL		0.5%
VERILOG	Module	89.88%
	Total	89.88%
TOTAL		100%

SystemC profile data

Table 1: VCS

AMS Co-simulation

VCS provides many benefits for AMS designers namely—real number modeling, native low power and advanced methodology with AMS testbench. In addition, all analog and mixed signal data can be viewed in Verdi's advanced AMS debug environment, which is natively integrated with VCS to enable fastest analysis and finding root cause.

Planning and Coverage

A verification cycle is dominated by the time meeting coverage goals and spent in debug. VCS is natively integrated with Verdi Coverage (Figure 10) to support advanced coverage driven verification methodologies. VCS includes multiple integrated technologies—assertions, assertion checkers, interactive debug and Unified Report Generator (URG) for coverage data—to help define, measure and report coverage goals, and find coverage holes. VCS natively supports not only the complete SVA syntax from Verilog LRM, PSL and OVL, but also provides useful controls to manage the assertion output and performance of simulation. VCS' regression execution management capabilities provides powerful configuration, regression results database, and compute farm management features.

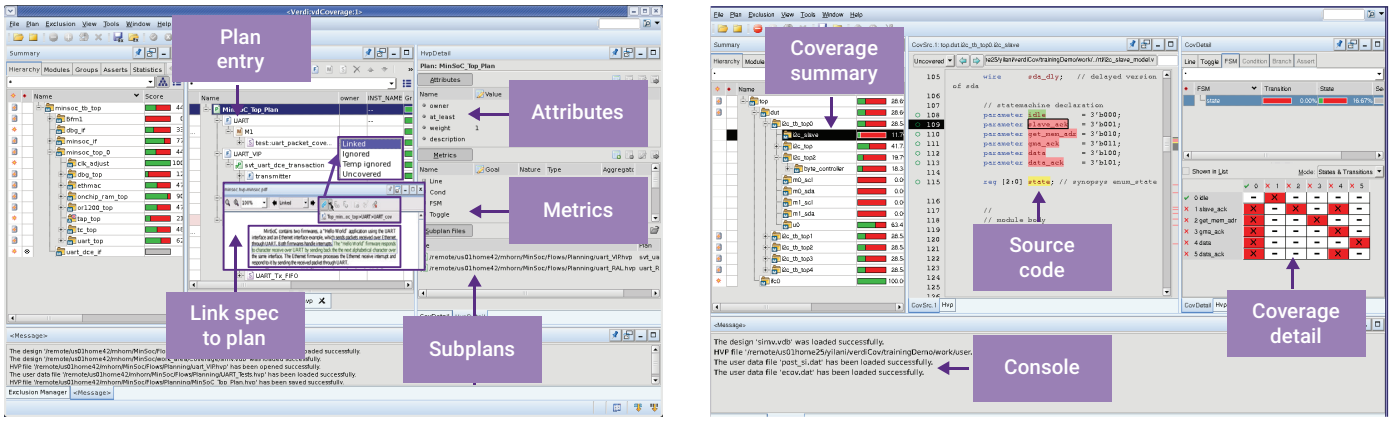

Figure 10: Verdi Verification Planner and Coverage Analyzer windows

Native Integrations

Native integrations between the high-performance VCS simulation engine and the other advanced engines in the Synopsys Verification Continuum Platform (Figure 3) enables improvements in time-to-market by up to months.

The Verification Continuum Platform's unified verification architecture eliminates these discontinuities with VCS Unified Compile, Verdi Unified Debug, and key native integrations such as the following:

- Verdi—Verdi Reverse Interactive Debug exemplifies the power of VCS engines and technologies natively integrated in the Verdi debug environment, and vice versa (Figure 11)

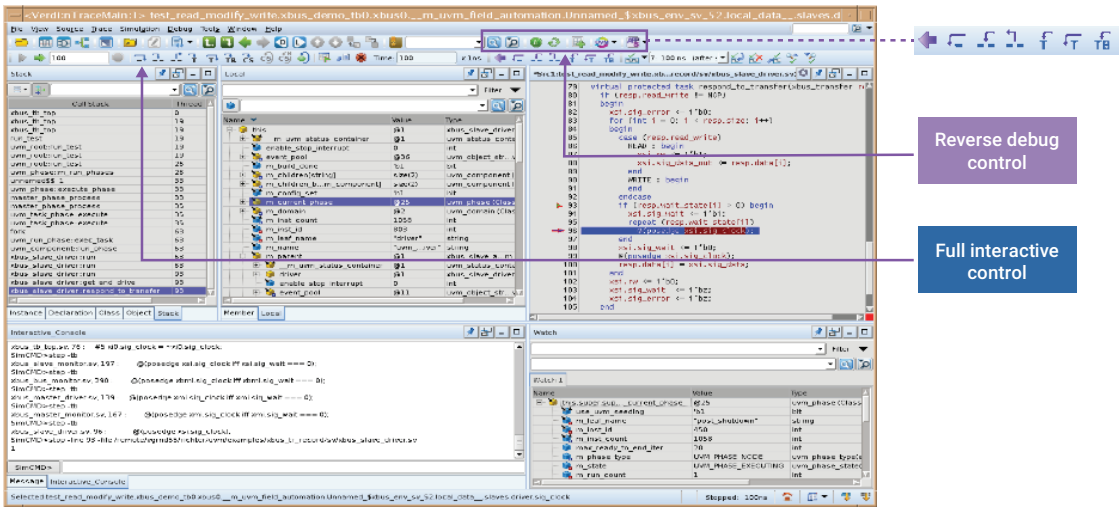

Figure 11: Verdi/VCS Reverse Interactive Debug—go back in time without setting check points

- Static and Formal—VC LP, VC SpyGlass, and VC Formal fully support Unified Compile with VCS and Unified Debug with Verdi
- Emulation—VCS congruent mode enables simulation to match actual hardware and facilitates emulation-simulation interoperability
- VIP—VC Verification IP solution offers native integration with VCS planning, coverage and constraint solver technologies, and provides native Verdi-based debug and Protocol Analyzer capabilities

Conclusion

VCS leads the industry in simulation performance and capacity and provides the most comprehensive fully integrated suite of technologies and tools to support the broadest range of verification strategies. VCS' technology roadmap is driven by continuous collaboration with industry leaders and is targeted at verification for today's and tomorrow's largest and most complex designs. In addition, VCS is complemented by the best support in the industry, all targeted at keeping verification schedules on track.

For more information about Synopsys products, support services or training, visit us on the web at: synopsys.com, contact your local sales representative or call 650.584.5000.