Started on	Thursday, 8 April 2021, 9:05 AM
State	Finished
Completed on	Thursday, 8 April 2021, 10:00 AM
Time taken	54 mins 42 secs
Marks	30.00/50.00
Grade	**6.00** out of 10.00 (**60**%)

Question **1**

Correct

Mark 1.00 out of 1.00

The use of which of the following in a computer is justified by the principle of locality?

- a. DMA
- b. Virtual memory
- c. Software interrupt
- d. Cache memory ✔

Your answer is correct.

The correct answer is:
Cache memory

Question **2**

Correct

Mark 1.00 out of 1.00

What is the two times shift right of the binary stream 0 1 0 1 1 1 1 0 1?

- a. 0 1 0 1 1 1 1 0 0
- b. 0 0 0 1 0 1 1 1 1 ✔
- c. None of the mentioned
- d. 0 1 0 1 1 1 1 0 1

Your answer is correct.

The correct answer is:
0 0 0 1 0 1 1 1 1

Question **3**

Incorrect

Mark 0.00 out of 1.00

In the MIPS pipeline architecture forwarding/bypassing is ----

- a. DMA based approach ✖
- b. Software based approach
- c. Combination of both hardware & software based approach
- d. Hardware based approach

Your answer is incorrect.

The correct answer is:
Hardware based approach

Question **4**

Correct

Mark 1.00 out of 1.00

For Von Neumann's architecture implementation. Select the correct option.

- a. I/O are required
- b. Memory is required
- c. All of the mentioned ✔
- d. CPU is required

Your answer is correct.

The correct answer is:
All of the mentioned

Question **5**

Incorrect

Mark 0.00 out of 1.00

Which one of the following is not a characteristic of loosely coupled computers?

- a. Efficient execution of programs and fine grained parallelism
- b. Shared memory ✖
- c. Message passing communication
- d. No shared memory

Your answer is incorrect.

The correct answer is:
Efficient execution of programs and fine grained parallelism

Question **6**

Correct

Mark 1.00 out of 1.00

The numbers of NAND and NOR gates required to implement full subtractor are?

- a. 10 and 9
- b. 9 and 9 ✔
- c. 11 and 11
- d. 9 and 10

Your answer is correct.

The correct answer is:
9 and 9

Question **7**

Incorrect

Mark 0.00 out of 1.00

A purely sequential program was observed to take 1000 seconds to complete execution on a certain four-processor MIMD computer. It was rewritten threads so that 76 % of the original code could run ideally parallel. Under the assumption that there is no other bottleneck, how long would this program take to complete execution on the four-processor MIMD computer?

- a. 430 sec.
- b. 340 sec.
- c. 476 sec. ✖
- d. 571 sec.

Your answer is incorrect.

The correct answer is:
430 sec.

Question **8**

Correct

Mark 1.00 out of 1.00

For 4-bit ripple carry adder design. Select the right option in terms of low cost and low power.

- a. 4 half adders
- b. 4 full adders
- c. 3 full adders and 1 half adder ✔
- d. 3 half adders and 1 full adder

Your answer is correct.

The correct answer is:
3 full adders and 1 half adder

Question **9**

Correct

Mark 1.00 out of 1.00

For Page replacement which approach is good?

- a. Segmentation
- b. Write back ✔
- c. Paging
- d. Write through

Your answer is correct.

The correct answer is:
Write back

Question **10**

Incorrect

Mark 0.00 out of 1.00

Instruction pipeline improves the CPU performance due to which one of the following reasons?

- a. Use of additional functional units
- b. Efficient utilization of the processor hardware
- c. Use a larger Cache
- d. Reduced memory access time ✖

Your answer is incorrect.

The correct answer is:
Efficient utilization of the processor hardware

Question **11**

Correct

Mark 1.00 out of 1.00

The IR store which one of the following?

- a. An instruction that has been fetched from the memory ✔
- b. An instruction that has been decoded
- c. An instruction that has been executed
- d. The address of the next instruction to be executed

Your answer is correct.

The correct answer is:
An instruction that has been fetched from the memory

Question **12**

Correct

Mark 1.00 out of 1.00

The shortfall of registers created by aggressive unrolling and scheduling is also known as --

- a. Forwarding
- b. Register pressure ✔
- c. Aggressive scaling
- d. Miss rate

Your answer is correct.

The correct answer is:

Register pressure

Question **13**

Correct

Mark 1.00 out of 1.00

ISA serves as an interface between ---

- a. Processor and DMA
- b. Processor and memory
- c. Processor and I/O
- d. Processor and operating system ✔

Your answer is correct.

The correct answer is:
Processor and operating system

Question **14**

Correct

Mark 1.00 out of 1.00

In the J-type instructions of MIPS --

- a. One operand is provided as a part of the instruction and other operand need to be fetched from memory ✔
- b. Both operands are not available in the register bank
- c. Both the operands are available in the register bank
- d. One operand is provided as a part of the instruction and other operand need to be get from accumulator

Your answer is correct.

The correct answers are:
Both the operands are available in the register bank,

One operand is provided as a part of the instruction and other operand need to be fetched from memory

Question **15**

Correct

Mark 1.00 out of 1.00

For the program given below the number of stalls required after the code transformed by the smart compiler are

MIPS Code:

1. LW R2, 0(R4)

2. LW R5, 4(R4)

3. ADD R1, R2, R3

- a. No stall is required ✔
- b. Two
- c. One
- d. Three

Your answer is correct.

The correct answer is:
No stall is required

Question **16**

Correct

Mark 1.00 out of 1.00

During 1 clock cycle, the pipeline (5-stage) can process --

- a. 6 different instructions
- b. 5 different instructions ✔
- c. 4 different instructions
- d. None of the mentioned

Your answer is correct.

The correct answer is:
5 different instructions

Question **17**

Correct

Mark 1.00 out of 1.00

A software interrupt is caused in which one of the following situations?

a. A page transfer from the hard disk to the main memory is complete

b. A system call ✔

c. Divide by zero encountered while running a program

d. A DMA call

Your answer is correct.

The correct answer is:
A system call

Question **18**

Correct

Mark 1.00 out of 1.00

Consider a pipeline having 4 phases with the duration of 60, 50, 90, and 80 ns. Given latch delay is 10 ns. What is the pipeline cycle time?

a. 60 ns

b. 70 ns

c. 90 ns

d. 100 ns ✔

Your answer is correct.

The correct answer is:
100 ns

Question **19**

Correct

Mark 1.00 out of 1.00

Which one of the following means is deployed flash memory to store data?

- a. Charge retained in a floating gate in each memory cell to indicate a logical 1 ✔
- b. Charge retained in a diode in each memory cell to indicate a logical 1
- c. Use of programmable fuse in each memory cell
- d. A six-transistor flip flop circuitry is used in each memory cell

Your answer is correct.

The correct answer is:
Charge retained in a floating gate in each memory cell to indicate a logical 1

Question **20**

Correct

Mark 1.00 out of 1.00

Which one of them is not a pipeline parameter?

- a. Throughput
- b. Pipeline cycle time
- c. Speed up ratio
- d. Ripple ratio ✔

Your answer is correct.

The correct answer is:
Ripple ratio

Question **21**

Incorrect

Mark 0.00 out of 1.00

Assume that the following types of computers, all hazards are handled through stalling. Which one of the following consumption would suffer from the least drag from the ideal performance due to hazards while running a typical program.

- a. A computer with a 5 stage pipelined and four issue superscalar processor
- b. A computer with a 5 stage pipelined processor ✖
- c. A computer with a 16 stage pipelined processor
- d. A computer with a 16 stage pipelined and four issue superscalar processor

Your answer is incorrect.

The correct answer is:
A computer with a 5 stage pipelined and four issue superscalar processor

Question **22**

Correct

Mark 1.00 out of 1.00

Von Neumann computers helping to which one of the following classes of computers?

- a. MIMD
- b. SISD ✔
- c. SIMD
- d. MISD

Your answer is correct.

The correct answer is:
SISD

Question **23**

Correct

Mark 1.00 out of 1.00

When an instruction is required to be brought from memory to CPU, on which one of the following busses is it fetched?

- a. Address bus
- b. Data bus ✔
- c. Control bus
- d. Peripheral bus

Your answer is correct.

The correct answer is:
Data bus

Question **24**

Incorrect

Mark 0.00 out of 1.00

For the load and store operation ---

- a. Effective address is calculated between 4th and 5th stage of the pipeline ✖
- b. Effective address is calculated at 3rd stage of the pipeline
- c. Effective address is calculated at 4th stage of the pipeline
- d. Effective address is calculated between 3rd and 4th stage of the pipeline

Your answer is incorrect.

The correct answer is:
Effective address is calculated at 3rd stage of the pipeline

Question **25**

Incorrect

Mark 0.00 out of 1.00

Which one of the following characteristics is associated with shared memory multiprocessors?

- a. Loosely coupled and coarse grained parallelism
- b. Tightly coupled and coarse grained parallelism
- c. Tightly coupled and fine grained parallelism
- d. Loosely coupled and fine grained parallelism ✖

Your answer is incorrect.

The correct answer is:
Tightly coupled and fine grained parallelism

Question **26**

Incorrect

Mark 0.00 out of 1.00

Which one of the following most accurately characterizes the primary reason for the use of translation lookaside buffer in a processor?

- a. TLB allows multiple processes to share the L1 Cache
- b. None of the mentioned ✖
- c. TLB ensures that a process does not access memory outside of its address space
- d. TLB makes translation of virtual addresses to physical addresses faster

Your answer is incorrect.

The correct answer is:
TLB makes translation of virtual addresses to physical addresses faster

Question **27**

Incorrect

Mark 0.00 out of 1.00

Which one of the following is true for a typical RISC architecture?

- a. Make use of multiprogrammed control unit ✖
- b. Makes use of hardwired control unit
- c. Supports may addressing modes
- d. Has much smaller Cache than CISC processors

Your answer is incorrect.

The correct answer is:
Makes use of hardwired control unit

Question **28**

Correct

Mark 1.00 out of 1.00

Which one of the following types of semiconductor memory is used as the main memory in a computer?

- a. Flash
- b. SRAM
- c. PROM
- d. DRAM ✔

Your answer is correct.

The correct answer is:
DRAM

Question **29**

Correct

Mark 1.00 out of 1.00

Which of the common cache?

- a. DRAM
- b. SRAM
- c. TLB ✔
- d. Taps

Your answer is correct.

The correct answer is:
TLB

Question **30**

Correct

Mark 1.00 out of 1.00

Which one of the following addressing modes are used in an instruction of the form ADD X, Y is?

- a. Immediate
- b. Absolute ✔
- c. Relative
- d. Indirect

Your answer is correct.

The correct answer is:
Absolute

Question **31**

Incorrect

Mark 0.00 out of 1.00

Which one of the following can be said about the speed of a multiplier capable of multiplying two 16-bit numbers?

- a. Booth's and array multiplier would be equally fastest
- b. Sign magnitude multiplier would be the fastest
- c. Array multiplier would be the fastest
- d. Booth's multiplier would be the fastest ✖

Your answer is incorrect.

The correct answer is:
Array multiplier would be the fastest

Question **32**

Correct

Mark 1.00 out of 1.00

Which one of the following is a major benefit of the Harvard architecture over the von Neumann architecture?

- a. Program written using single world instruction execute more quickly than multiword instructions
- b. None of the mentioned
- c. Code and data can be loaded into the CPU simultaneously on separate buses ✔
- d. Code and data share memory and increase program execution efficiency

Your answer is correct.

The correct answer is:
Code and data can be loaded into the CPU simultaneously on separate buses

Question **33**

Correct

Mark 1.00 out of 1.00

Which one of the following types of Interrupts can be caused by an executing program?

- a. Internal
- b. Hardware
- c. Software ✔
- d. External

Your answer is correct.

The correct answer is:
Software

Question **34**

Incorrect

Mark 0.00 out of 1.00

Shared memory multiprocessor fit best into which one of the following Flynn's classification of computers?

- a. Multiple instruction, single data stream ✖
- b. Single instruction, multiple data stream
- c. Multiple instruction, multiple data stream
- d. Single instruction, single data stream

Your answer is incorrect.

The correct answer is:
Multiple instruction, multiple data stream

Question **35**

Incorrect

Mark 0.00 out of 1.00

Distributed computers belong to which one of the following classes of computers?

- a. MIMD
- b. SISD
- c. MISD ✖
- d. SIMD

Your answer is incorrect.

The correct answer is:
MIMD

Question **36**

Correct

Mark 1.00 out of 1.00

The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Writeback (WB), The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each, and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards. What is the number of clock cycles required for the completion of the execution of the sequence of instruction?

- a. 229 cycles
- b. 219 cycles ✔
- c. 221 cycles
- d. 220 cycles

Your answer is correct.

The correct answer is:
219 cycles

Question **37**

Incorrect

Mark 0.00 out of 1.00

Vector processors are best classified into which one of the following Flynn's classifications of computers?

- a. Multiple instruction, single data stream ✖
- b. Multiple instruction, multiple data stream
- c. Single instruction, single data stream
- d. Single instruction, multiple data stream

Your answer is incorrect.

The correct answer is:
Single instruction, multiple data stream

Question **38**

Incorrect

Mark 0.00 out of 1.00

A computer, whose average memory access time is 20 ns has a page fault service time of 10 ms. For every 100 memory accesses, the one-page fault is generated. The effective access time for the memory in which one of the following?

- a. 30 ns ✖
- b. 20 ns
- c. 45 ns
- d. None of the mentioned

Your answer is incorrect.

The correct answer is:
20 ns

Question **39**

Correct

Mark 1.00 out of 1.00

Cache memory is?

- a. Interface between processor and main memory ✔
- b. Interface between processor and SRAM
- c. Interface between processor and virtual memory
- d. Interface between processor and DMA

Your answer is correct.

The correct answer is:
Interface between processor and main memory

Question **40**

Correct

Mark 1.00 out of 1.00

Consider the unpipelined machine with 10ns clock cycles. It uses four cycles for ALU operations and branches where as five cycles for memory operations. Assume that the relative frequencies of these operations are 40%,20%, and 40% respectively. Let due to clock skew and set up pipelining, the machine adds 1 ns of overhead to the clock. How much speed in instruction execution rate will we gain from the pipeline?

- a. 2X
- b. 1X
- c. 3X
- d. 4X ✔

Your answer is correct.

The correct answer is:
4X

Question **41**

Incorrect

Mark 0.00 out of 1.00

Which one of the following would cause the Page fault frequency in an operating system to reduce?

- a. Cache memory size is increased
- b. Executing processes exhibit high locality of reference ✖
- c. Size of the page reduced
- d. Executing processes remain CPU-bound

Your answer is incorrect.

The correct answer is:
Executing processes remain CPU-bound

Question **42**

Incorrect

Mark 0.00 out of 1.00

Which one of the following multiplexers would have a 4-bit data select input?

- a. 8:1
- b. 4:1 ✖
- c. 16:1
- d. 2:1

Your answer is incorrect.

The correct answer is:
16:1

Question **43**

Incorrect

Mark 0.00 out of 1.00

Pipelined processors are the best classified into which one of the following Flynn's classifications of computers?

- a. Single instruction, multiple data stream
- b. Multiple instruction, multiple data stream ✖
- c. Single instruction, single data stream
- d. Multiple instruction, single data stream

Your answer is incorrect.

The correct answer is:
Single instruction, single data stream

Question **44**

Correct

Mark 1.00 out of 1.00

in loop Unrolling with Scheduling---. Select the right option.

- a. Use different registers to avoid unnecessary constraints
- b. Identify that loop iterations are independent
- c. Determine the loads and stores that can be interchanged in the unrolled loop
- d. All of the mentioned ✔

Your answer is correct.

The correct answer is:
All of the mentioned

Question **45**

Correct

Mark 1.00 out of 1.00

Virtual memory is also known as?

- a. Interface between main memory and secondary memory
- b. All of the mentioned ✔
- c. Cache between main memory and secondary
- d. Buffer between main memory and secondary memory

Your answer is correct.

The correct answer is:
All of the mentioned

Question **46**

Incorrect

Mark 0.00 out of 1.00

Which of the following statement most accurately characterizes the responsibility of the memory management unit in the processor?

- a. Managing the interface between the processor and the main memory
- b. Managing the interfacing between main memory and hard disk
- c. Managing the physical memory of the machine
- d. Managing the translation of the virtual into physical address ✖

Your answer is incorrect.

The correct answer is:
Managing the physical memory of the machine

Question **47**

Correct

Mark 1.00 out of 1.00

Which one of the following addressing modes cannot be meaningfully used for the destination operand of an ADD instruction?

- a. Indexed ✔
- b. Direct
- c. Indirect
- d. Immediate

Your answer is correct.

The correct answer is:
Indexed

Question **48**

Incorrect

Mark 0.00 out of 1.00

When a processor fetches an instruction of the executing program, the binary code of the instruction gets stored in which one of the following?

- a. Program counter
- b. Instruction register
- c. General purpose register
- d. Accumulator ✖

Your answer is incorrect.

The correct answer is:
Program counter

Question **49**

Correct

Mark 1.00 out of 1.00

Which one of the following sentences best justifies the need for using a virtual memory operating system?

- a. It help to run multiple programs whose combined size is much larger than the size of the physical memory available on the machine ✔
- b. It help to extend the amount of physical memory that is being used
- c. It allows machines to communicate over a local area network
- d. It help to improve the performance of the hard disk

Your answer is correct.

The correct answer is:
It help to run multiple programs whose combined size is much larger than the size of the physical memory available on the machine

Question **50**

Incorrect

Mark 0.00 out of 1.00

What is true for virtual memory?

- a. Processor sends physical address for page table
- b. Processor sends virtual address for main memory ✖
- c. Processor sends physical address for main memory
- d. Processor sends virtual address for page table

Your answer is incorrect.

The correct answer is:
Processor sends virtual address for page table

◄ Online Test

Jump to...

Assignment-II ►

Started on	Thursday, 22 April 2021, 1:00 PM
State	Finished
Completed on	Thursday, 22 April 2021, 1:07 PM
Time taken	6 mins 54 secs
Marks	4.00/7.00
Grade	**5.71** out of 10.00 (**57**%)

Question **1**

Correct

Mark 1.00 out of 1.00

Cache memory is?

- a. Interface between processor and main memory ✔
- b. Interface between processor and virtual memory
- c. Interface between processor and SRAM
- d. Interface between processor and DMA

Your answer is correct.

The correct answer is:
Interface between processor and main memory

Question **2**

Incorrect

Mark 0.00 out of 1.00

The zero flag register of the MIPS pipeline architecture--

- a. Calculate the effective address by using the program counter register content ✖
- b. Calculate the effective address by adding the register content of the ALU
- c. Calculate the effective address by subtracting the register content of the ALU
- d. Calculate the effective address by using the instruction register content

Your answer is incorrect.

The correct answer is:
Calculate the effective address by subtracting the register content of the ALU

Question **3**

Incorrect

Mark 0.00 out of 1.00

Which one of the following about the MIPS rating of a computer is FALSE?

- a. MIPS rating of computer depends on the computer being used
- b. MIPS rating of a computer can very based on which instruction of a processor are being considered
- c. None of the mentioned ✖
- d. MIPS rating of a processor is independent of the program is being executed.

Your answer is incorrect.

The correct answer is:
MIPS rating of a processor is independent of the program is being executed.

Question **4**

Incorrect

Mark 0.00 out of 1.00

For the load and store operation ---

- a. Effective address is calculated at 4th stage of the pipeline
- b. Effective address is calculated between 4th and 5th stage of the pipeline ✖
- c. Effective address is calculated at 3rd stage of the pipeline
- d. Effective address is calculated between 3rd and 4th stage of the pipeline

Your answer is incorrect.

The correct answer is:
Effective address is calculated at 3rd stage of the pipeline

Question **5**

Correct

Mark 1.00 out of 1.00

Which one of the following options most correctly lists the important parts of a Von Neumann computer?

- a. Hard disks, buses, and CPU
- b. Memory, CPU, buses, and printers
- c. Memory, input/output units, and CPU ✔
- d. Buses, memory, and input/output controllers

Your answer is correct.

The correct answer is:
Memory, input/output units, and CPU

Question **6**

Correct

Mark 1.00 out of 1.00

The von Neumann bottleneck can be attributed to which one of the following?

- a. Slow speed of input/output devices
- b. Mismatch between the speed of the secondary and primary storages
- c. Low clock speeds
- d. Mismatch between the speed of the CPU and primary storages ✔

Your answer is correct.

The correct answer is:
Mismatch between the speed of the CPU and primary storages

Question **7**

Correct

Mark 1.00 out of 1.00

In MIPS architecture, the program counter send the address multiple of 4 due to --

- a. Word addressability of memory
- b. Bit addressability of memory
- c. Nibble addressability of memory
- d. Byte addressability of memory ✔

Your answer is correct.

The correct answer is:
Byte addressability of memory

◄ CS-208: Pre-End-Sem Online Test

Jump to...

Started on	Friday, 26 March 2021, 1:35 PM
State	Finished
Completed on	Friday, 26 March 2021, 1:50 PM
Time taken	14 mins 57 secs
Marks	8.00/20.00
Grade	**4.00** out of 10.00 (**40**%)

Question **1**

Incorrect

Mark 0.00 out of 1.00

In which one of the following addressing modes, the content of the program counter is added to the address part of the instruction in order to obtain the effective address.

- a. Register addressing mode
- b. Indexed addressing mode ✖
- c. Absolute addressing mode
- d. Register indirect addressing mode

Your answer is incorrect.

The correct answer is:
Register indirect addressing mode

Question **2**

Correct

Mark 1.00 out of 1.00

An instruction cycle refers to which one of the following?

- a. Decoding the instruction and calculation of effective address
- b. Executing an instruction
- c. Fetching an instruction
- d. All of the mentioned ✔

Your answer is correct.

The correct answer is:
All of the mentioned

Question **3**

Correct

Mark 1.00 out of 1.00

Which one of the following most profoundly describes the functionality of the control unit in CPU?

- a. To perform the arithmetic operations based on decoded program instruction
- b. To store program instruction
- c. To generate the control signals based on decoded program instructions ✔
- d. To perform logic operations based on decoded program instructions

Your answer is correct.

The correct answer is:
To generate the control signals based on decoded program instructions

Question **4**

Incorrect

Mark 0.00 out of 1.00

Which one of the following statements about a computer supporting unaligned data access is most accurate regarding the storage of data items having sizes that may not be multiples of the word size.

- a. Data transfer is inefficient and data also storage in memory would not be efficient
- b. Data transfer is efficient and also data can be stored efficiently in memory
- c. Data transfer is inefficient but data can be stored efficiently in memory
- d. Data transfer is efficient but data storage in memory would not efficient. ✖

Your answer is incorrect.

The correct answer is:
Data transfer is inefficient but data can be stored efficiently in memory

Question **5**

Incorrect

Mark 0.00 out of 1.00

The content of the multiplicand register and the multiplier register of a hardware circuit implementing Booth's algorithm is the binary numbers 111001 and 111100 what would be the result produced by the multiplier circuitry (Decimal)

- a. -1828
- b. 1812
- c. 28 ✖
- d. -28

Your answer is incorrect.

The correct answer is:
1812

Question **6**

Incorrect

Mark 0.00 out of 1.00

A booth's multiplier circuit needs to inspect at most how many LSB bits to determine whether to add the multiplier, subtract the multiplier or leave the partial result unchanged during any step in the sequence of multiplication steps?

- a. Two bits ✖
- b. All bits of the multipicand
- c. All bits of the multiplier
- d. One bit

Your answer is incorrect.

The correct answer is:
One bit

Question **7**

Incorrect

Mark 0.00 out of 1.00

Divide overflow is easiest to handle in which one of the following circuits implementing division?

- a. Fixed point 2's complement division
- b. Floating point division
- c. Fixed point 1's complement division
- d. Fixed point sign magnitude division ✖

Your answer is incorrect.

The correct answer is:
Floating point division

Question **8**

Correct

Mark 1.00 out of 1.00

In order to realize an adder that can add two 16-bit numbers, how many full adders and half adders would be required?

- a. One half adder and 15 full adders ✔
- b. 17 half adders and 0 full adder
- c. 15 half adders and one full adder
- d. 10 half adders and 11 full adders

Your answer is correct.

The correct answer is:
One half adder and 15 full adders

Question **9**

Incorrect

Mark 0.00 out of 1.00

Which one of the following can be said about the speed of a multiplier capable of multiplying two 16-bit numbers?

- a. Booth's and array multiplier would be equally fastest
- b. Sign magnitude multiplier would be the fastest
- c. Array multiplier would be the fastest
- d. Booth's multiplier would be the fastest ✖

Your answer is incorrect.

The correct answer is:
Array multiplier would be the fastest

Question **10**

Correct

Mark 1.00 out of 1.00

In the implementation of a binary multiplier circuit, which one of the following set of logic gates is used?

- a. 2 input AND gates only
- b. XOR gates and shift registers
- c. 2 input X-or gates and 2-input AND gates ✔
- d. 2-input NOR gates and 1 XOR gate

Your answer is correct.

The correct answer is:
2 input X-or gates and 2-input AND gates

Question **11**

Incorrect

Mark 0.00 out of 1.00

A computer has a word size of 16-bit and has 16 programmer visible registers. each instruction has two sources and one destination operands and uses only register direct addressing mode. what is the maximum number of op-codes that this processor can have?

- a. 64
- b. 32 ✖
- c. 16
- d. 8

Your answer is incorrect.

The correct answer is:
16

Question **12**

Incorrect

Mark 0.00 out of 1.00

After fetching an instruction from memory, the binary code of the instruction is stored in which one of the following?

- a. Accumulator ✖
- b. Program counter
- c. Instruction pointer
- d. Instruction register

Your answer is incorrect.

The correct answer is:
Instruction register

Question **13**

Incorrect

Mark 0.00 out of 1.00

The IR store which one of the following?

- a. An instruction that has been executed
- b. An instruction that has been fetched from the memory
- c. The address of the next instruction to be executed
- d. An instruction that has been decoded ✖

Your answer is incorrect.

The correct answer is:
An instruction that has been fetched from the memory

Question **14**

Correct

Mark 1.00 out of 1.00

Cache memory is?

- a. Interface between processor and DMA
- b. Interface between processor and SRAM
- c. Interface between processor and main memory ✔
- d. Interface between processor and virtual memory

Your answer is correct.

The correct answer is:
Interface between processor and main memory

Question **15**

Correct

Mark 1.00 out of 1.00

Which of the common cache?

- a. Taps
- b. DRAM
- c. TLB ✔
- d. SRAM

Your answer is correct.

The correct answer is:
TLB

Question **16**

Correct

Mark 1.00 out of 1.00

------is the concept in which a process is copied into the main memory from the secondary memory according to the requirement.

- a. Pagging
- b. None of the mentioned
- c. Demand pagging ✔
- d. Segmentation

Your answer is correct.

The correct answer is:
Demand pagging

Question **17**

Incorrect

Mark 0.00 out of 1.00

When an instruction is required to be brought from memory to CPU, on which one of the following busses is it fetched?

- a. Peripheral bus
- b. Control bus
- c. Data bus
- d. Address bus ✖

Your answer is incorrect.

The correct answer is:
Data bus

Question **18**

Incorrect

Mark 0.00 out of 1.00

Consider a three address RISC processor ISA. Which one of the following correctly characterizes an effect of doubling the number of registers in the processor?

- a. Instruction size would be increase by 2-bit
- b. Instruction size would be increase by 1-bit
- c. Instruction size would be increase by 3-bit
- d. Instruction size would be unaffected ✖

Your answer is incorrect.

The correct answer is:
Instruction size would be increase by 3-bit

Question **19**

Correct

Mark 1.00 out of 1.00

Swap space exists in _____

- a. DRAM
- b. Primary memory
- c. Secondary memory ✔
- d. None of the mentioned

Your answer is correct.

The correct answer is:
Secondary memory

Question **20**

Incorrect

Mark 0.00 out of 1.00

If the page hit is there in the page table then?

- a. Data can be dire accessed from main memory without address translation ✖
- b. Data can be directly accessed from disc
- c. Data can be dire accessed from main memory after the address translation
- d. None of the mentioned

Your answer is incorrect.

The correct answer is:
Data can be dire accessed from main memory after the address translation

◄ CS-208: Mid-Sem Online Test

Jump to...

CS-208: Pre-End-Sem Online Test ►

Started on	Tuesday, 2 February 2021, 10:20 AM
State	Finished
Completed on	Tuesday, 2 February 2021, 10:59 AM
Time taken	39 mins 34 secs
Marks	24.00/35.00
Grade	**6.86** out of 10.00 (**69**%)

Question **1**

Correct

Mark 1.00 out of 1.00

In the J-type instructions of MIPS --

- a. One operand is provided as a part of the instruction and other operand need to be fetched from memory
- b. Both operands are not available in the register bank
- c. Both the operands are available in the register bank ✔
- d. One operand is provided as a part of the instruction and other operand need to be get from accumulator

Your answer is correct.

The correct answers are:
Both the operands are available in the register bank,

One operand is provided as a part of the instruction and other operand need to be fetched from memory

Question **2**

Incorrect

Mark 0.00 out of 1.00

Forwarding can be implemented in 5-stage and 6-stage MIPS pipeline --

- a. Using three multiplexers ✖
- b. Using two multiplexers with extra latch
- c. Using two multiplexers
- d. Using one multiplexer

Your answer is incorrect.

The correct answer is:
Using two multiplexers

Question **3**

Correct

Mark 1.00 out of 1.00

The features of the RISC processor --

- a. Instruction execute in one or two clock cycle
- b. Small number of addressing modes
- c. Small number of the instructions
- d. All of the mentioned ✔

Your answer is correct.

The correct answer is:
All of the mentioned

Question **4**

Correct

Mark 1.00 out of 1.00

The shortfall of registers created by aggressive unrolling and scheduling is also known as --

- a. Register pressure
- b. Aggressive scaling
- c. Forwarding ✖
- d. Miss rate

Your answer is correct.

The correct answer is:

Register pressure

Question **5**

Correct

Mark 1.00 out of 1.00

Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 5 ns. What is the Pipeline cycle time?

- a. 105 ns
- b. 75 ns
- c. 100 ns
- d. 95 ns ✔

Your answer is correct.

The correct answer is:
95 ns

Question **6**

Incorrect

Mark 0.00 out of 1.00

In MIPS architecture, increasing the number of stages --

- a. Will always improve the performance after the optimal value of the stages
- b. Will always decrease the performance.
- c. Will always improve the performance. ✖
- d. Will improve the performance up to optimal value of the stages and beyond the optimal value it will decrease

Your answer is incorrect.

The correct answers are:
Will always decrease the performance.,

Will improve the performance up to optimal value of the stages and beyond the optimal value it will decrease

Question **7**

Correct

Mark 1.00 out of 1.00

For calculating the effective address, the upper 6 bits and concatenation done between---

- a. Program counter and constant value which was the part of the instruction ✔
- b. Program counter and constant value which was not the part of the instruction
- c. Address register and constant value which was the part of the instruction
- d. Address register and constant value which was not the part of the instruction

Your answer is correct.

The correct answer is:
Program counter and constant value which was the part of the instruction

Question **8**

Correct

Mark 1.00 out of 1.00

Using booth's algorithms multiply 7 with 3 and assume register AC is 4 bit. The value of AC after 3rd and 4th cycles are

- a. 0 1 1 1 0 and 1 0 1 0 0
- b. 0 0 1 1 and 1 0 1 1
- c. 0 0 1 0 and 1 0 1 0 ✔
- d. 1 0 1 0 and 1 0 1 0

Your answer is correct.

The correct answer is:
0 0 1 0 and 1 0 1 0

Question **9**

Correct

Mark 1.00 out of 1.00

What is the two times shift right of the binary stream 0 1 0 1 1 1 1 0 1?

a. 0 1 0 1 1 1 1 0 0

b. 0 1 0 1 1 1 1 0 1

c. 0 0 0 1 0 1 1 1 1 ✔

d. None of the mentioned

Your answer is correct.

The correct answer is:
0 0 0 1 0 1 1 1 1

Question **10**

Incorrect

Mark 0.00 out of 1.00

The following assembly program is run over the MIPS pipeline architecture. Choose the wrong option.

Assembly code:

i1. pp1: L.D F0,0(R1);

i2. ADD.D F4,F0,F2;

i3. S.D F4,0(R1);

i4. DADDUI R1,R1,#-8;

i5. BNE R1,R2,pp1

a. i2 is used for adding scalar value ✖

b. i4 is used as an increment pointer

c. i3 is used to store the results

d. i1 is used for array element

Your answer is incorrect.

The correct answers are:
i1 is used for array element,

i4 is used as an increment pointer

Question **11**

Incorrect

Mark 0.00 out of 1.00

A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The number of and gates required to design full adders are?

- a. Nine
- b. Twelve ✖
- c. Eight
- d. Ten

Your answer is incorrect.

The correct answer is:
Nine

Question **12**

Incorrect

Mark 0.00 out of 1.00

A pipelined processor has seven stages, namely, IF1, IF2, ID, EX, MEM1, MEM2, WB. Assuming all the stages require the same amount of time and the time period of the non- pipelined processors is 14 ns, find out the clock frequency and speedup of the pipelined processor. Assume the delay of the latches is 1 ns.

- a. 1Khz and 50
- b. 1.2 Khz and 30 ✖
- c. 1 Khz and 3
- d. None of the mentioned

Your answer is incorrect.

The correct answer is:
None of the mentioned

Question **13**

Correct

Mark 1.00 out of 1.00

For the code given below, select the wrong answer.

MIPS Code:
1. add r1, r2, r3
2. sub r4, r1, r5

- a. Data hazard is present
- b. One stalls is required to remove the data hazard ✔
- c. For the second instruction, operands are required at 3rd stage of the pipeline
- d. There will be no hazard for the first instruction

Your answer is correct.

The correct answer is:
One stalls is required to remove the data hazard

Question **14**

Correct

Mark 1.00 out of 1.00

The instruction ADD Rd,Rs, Rt is ---

- a. R-type instruction of MIPS
- b. I-type instruction of MIPS
- c. P-type instruction of MIPS
- d. J-type instruction of MIPS ✖

Your answer is correct.

The correct answer is:
R-type instruction of MIPS

Question **15**

Incorrect

Mark 0.00 out of 1.00

Consider the following instruction sequence five-stage pipeline,

ADD R1, R2, R1 --- I1

LW R2,0(R1) --- I2

LW R1,4(R1) -- I3

OR R3, R1, R2 -- I4

Select the correct option.

- a. RAW hazards is present in instructions I1-I2
- b. All of the mentioned
- c. RAW hazards is present in instructions I2-I3 ✖
- d. RAW hazards is present in instructions I3-I4

Your answer is incorrect.

The correct answer is:
All of the mentioned

Question **16**

Incorrect

Mark 0.00 out of 1.00

In MIPS architecture, the program counter send the address multiple of 4 due to --

- a. Bit addressability of memory ✖
- b. Byte addressability of memory
- c. Nibble addressability of memory
- d. Word addressability of memory

Your answer is incorrect.

The correct answer is:
Byte addressability of memory

Question **17**

Incorrect

Mark 0.00 out of 1.00

For the code given below choose the wrong answer.

MIPS Code:

1. ADD r1, r2, r3
2. SUB r4, r1, r5
3. AND r6, r1, r7
4. OR r8, r1, r9
5. XOR r10, r1, r11

- a. Using split phase of the clock, data hazard can be eliminated from instruction no. fifth
- b. Using split phase of the clock, data hazard can be eliminated from instruction no. fourth
- c. Using split phase of the clock, data hazard can be eliminated from instruction no. second
- d. Direct data dependence is there ✖

Your answer is incorrect.

The correct answer is:
Using split phase of the clock, data hazard can be eliminated from instruction no. second

Question **18**

Correct

Mark 1.00 out of 1.00

If multiplicand (M) is 0111, the AC register is initialized with zero. What will be the content of the AC register after operation AC= AC-M?

- a. 1100
- b. 1111
- c. 1010
- d. 1001 ✔

Your answer is correct.

The correct answer is:
1001

Question **19**

Incorrect

Mark 0.00 out of 1.00

Pipelining of a MIPS-like Processor, select the right option

- a. All ALU operations are performed on register operands
- b. All of the mentioned ✔
- c. Separate Instruction and data memory is required
- d. Only instructions which access memory are load and store instructions

Your answer is incorrect.

The correct answer is:
All of the mentioned

Question **20**

Correct

Mark 1.00 out of 1.00

For the code given below. Select the right option.

```
if p1 {
S1;
};
if p2 {
S2;
};
```

- a. S1 cannot be moved before the branch ✔
- b. S1 is control dependent on p1, but S2 is not control dependent on p1
- c. S2 cannot be moved after the branch
- d. All of the mentioned

Your answer is correct.

The correct answers are: S1 is control dependent on p1, but S2 is not control dependent on p1, S1 cannot be moved before the branch, All of the mentioned

Question **21**

Correct

Mark 1.00 out of 1.00

In the MIPS architecture, data transfer takes place between --

- a. Register to memory
- b. Register to register
- c. Memory to register
- d. All of the mentioned ✔

Your answer is correct.

The correct answer is:
All of the mentioned

Question **22**

Correct

Mark 1.00 out of 1.00

In the MIPS architecture, the meaning of the instruction can be found from --

- a. Accumulator register
- b. Instruction register ✔
- c. Program counter register
- d. Address register

Your answer is correct.

The correct answer is:
Instruction register

Question **23**

Correct

Mark 1.00 out of 1.00

The zero flag register of the MIPS pipeline architecture--

- a. Calculate the effective address by adding the register content of the ALU
- b. Calculate the effective address by subtracting the register content of the ALU ✔
- c. Calculate the effective address by using the instruction register content
- d. Calculate the effective address by using the program counter register content

Your answer is correct.

The correct answer is:
Calculate the effective address by subtracting the register content of the ALU

Question **24**

Correct

Mark 1.00 out of 1.00

During 1 clock cycle, the pipeline (5-stage) can process --

- a. 4 different instructions
- b. 6 different instructions
- c. 5 different instructions ✔
- d. None of the mentioned

Your answer is correct.

The correct answer is:
5 different instructions

Question **25**

Correct

Mark 1.00 out of 1.00

What is the arithmetic shift right operation after the 1st cycle for the following binary stream 1 0 0 1 0 0 1 1 0 ?

- a. 1 0 0 1 0 0 1 1 0
- b. 1 1 0 0 1 0 0 1 1
- c. 0 1 1 0 0 1 0 0 1
- d. 1 1 1 0 0 1 0 0 1 ✖

Your answer is correct.

The correct answer is:
1 1 0 0 1 0 0 1 1

Question **26**

Incorrect

Mark 0.00 out of 1.00

CACHE memory act as an interface between---

- a. Processor hardware and main memory
- b. Processor hardware and I/O ✖

Your answer is incorrect.

The correct answer is:
Processor hardware and main memory

Question **27**

Correct

Mark 1.00 out of 1.00

in loop Unrolling with Scheduling---. Select the right option.

- a. Identify that loop iterations are independent ✖
- b. Use different registers to avoid unnecessary constraints
- c. Determine the loads and stores that can be interchanged in the unrolled loop
- d. All of the mentioned

Your answer is correct.

The correct answer is:
All of the mentioned

Question **28**

Correct

Mark 1.00 out of 1.00

A four-stage pipeline has stage delays of 150, 120, 160, and 140 ns respectively. Registers are used between the stages and have a delay of 10 ns each. What is the cycle time?

- a. 140 ns
- b. 170 ns ✔
- c. 165 ns
- d. 155 ns

Your answer is correct.

The correct answer is:
170 ns

Question **29**

Incorrect

Mark 0.00 out of 1.00

Which unit is responsible for directing the operations of computer arithmetic and logical unit?

- a. I/O interface
- b. ALU itself
- c. Control unit
- d. Program ✖

Your answer is incorrect.

The correct answer is:
Control unit

Question **30**

Correct

Mark 1.00 out of 1.00

What is the shift right of the binary stream 0 1 0 1 1 1 1 0 1?

- a. 0 0 1 0 1 1 1 0 1
- b. 0 0 1 0 1 1 1 1 1
- c. 0 0 1 0 1 1 1 1 0 ✔
- d. 1 0 1 0 1 1 1 1 0

Your answer is correct.

The correct answer is:
0 0 1 0 1 1 1 1 0

Question **31**

Correct

Mark 1.00 out of 1.00

In the MIPS pipeline architecture forwarding/bypassing is ----

- a. Software based approach
- b. Hardware based approach ✔
- c. Combination of both hardware & software based approach
- d. DMA based approach

Your answer is correct.

The correct answer is:
Hardware based approach

Question **32**

Correct

Mark 1.00 out of 1.00

For the program given below the number of stalls required after the code transformed by the smart compiler are

MIPS Code:

1. LW R2, 0(R4)

2. LW R5, 4(R4)

3. ADD R1, R2, R3

- a. One ✖
- b. Three
- c. Two
- d. No stall is required

Your answer is correct.

The correct answer is:
No stall is required

Question **33**

Correct

Mark 1.00 out of 1.00

For the load and store operation ---

- a. Effective address is calculated at 3rd stage of the pipeline
- b. Effective address is calculated between 4th and 5th stage of the pipeline
- c. Effective address is calculated at 4th stage of the pipeline
- d. Effective address is calculated between 3rd and 4th stage of the pipeline ✖

Your answer is correct.

The correct answer is:
Effective address is calculated at 3rd stage of the pipeline

Question **34**

Correct

Mark 1.00 out of 1.00

Addressing modes are used to calculate the effective address by using the --

- a. Control Unit ✖
- b. DMA
- c. ALU unit only
- d. ALU + control unit

Your answer is correct.

The correct answer is:
ALU + control unit

Question **35**

Correct

Mark 1.00 out of 1.00

For the code given below identifies the data hazard.

Code:

add r1, r2, r3

sub r1, r4, r5

- a. None of the mentioned
- b. WAW ✔
- c. RAW
- d. WAR

Your answer is correct.

The correct answer is:
WAW

◄ Announcements

Jump to...

CS-208: Mid-Sem Online Test ►

Started on	Thursday, 15 April 2021, 1:00 PM
State	Finished
Completed on	Thursday, 15 April 2021, 1:30 PM
Time taken	29 mins 56 secs
Marks	15.00/25.00
Grade	**6.00** out of 10.00 (**60**%)

Question **1**

Complete

Mark 0.00 out of 1.00

Assumed that pipeline is optimized for branches when the branch is taken in program,

How many pipelines bubble on a taken branch in the ALP.

```
26 sub $11, $5, $9
30 beq $2, $4, 8
34 and $13, $3, $6
38 or $14, $3, $7
42 add $15, $5, $3
46 slt $16, $7, $8
. . .
52 lw $5, 51($8)
```

- a. 2
- b. 4
- c. 1
- d. 0

Question **2**

Complete

Mark 1.00 out of 1.00

MBR ← PC

MAR ← X

PC ← Y

Memory ← MBR

Which one of the following is a possible operation performed by this sequence?

a. Operand fetch

b. Conditional branch

c. Instruction fetch

d. Initiation of interrupt service

Question **3**

Complete

Mark 1.00 out of 1.00

When executing this program using Tomasulo's algorithm, Find out last clock cycle

LD F2, 8(R3)

LD F4, 8(R3)

MULTD F10, F2, F4

LD F6, 10(R3)

LD F8, 12(R3)

MULTD F12, F6, F8

ADDD F12, F10, F12

a. 25

b. 22

c. 24

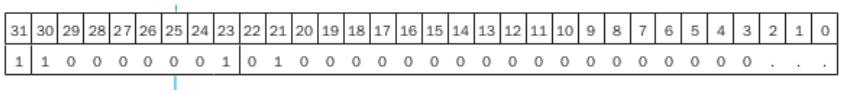
d. 19

Question **4**

Complete

Mark 0.00 out of 1.00

Which decimal number is used by this single-precision float?



- a. -5.0
- b. -7.0
- c. -4.0
- d. -6.0

Question **5**

Complete

Mark 1.00 out of 1.00

Out of order execution is used in?

- a. **Scoreboard algorithm**
- b. **None of the mentioned**
- c. **Scoreboard and Tomasulo algorithm**
- d. **Tomasulo algorithm**

Question **6**

Complete

Mark 0.00 out of 1.00

How many data hazards are available in between “SUB” and “SW” in the following assemble program.

sub $3, $2, $4

and $13, $3, $6

or $14, $7, $3

add $15,$3,$3

sw $16, 100($3)

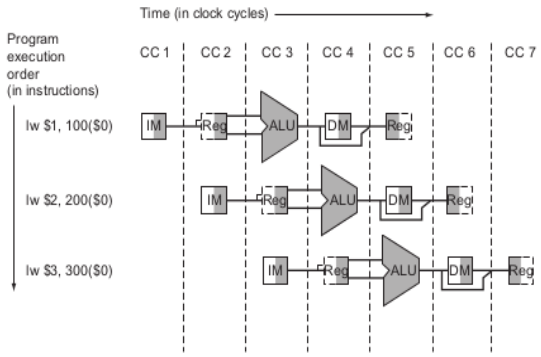
- a. 2
- b. 4
- c. 1
- d. 0

Question **7**

Complete

Mark 1.00 out of 1.00

Which memory is used during one of the five stages of instruction?



- a. Data
- b. Register
- c. None of the mentioned
- d. Instruction

Question **8**

Complete

Mark 0.00 out of 1.00

Consider three-branch prediction schemes: predict not taken, predict taken, and dynamic prediction. Assume that they all have zero penalties when they predict correctly and two cycles when they are wrong. Assume that the average predicted accuracy of the dynamic predictor is 90%. Which predictor is the best choice for the following branches?

- a. None of the mentioned
- b. A branch that is taken with 5% frequency
- c. A branch that is taken with 95% frequency
- d. A branch that is taken with 70% frequency

Question **9**

Complete

Mark 1.00 out of 1.00

The principle of pipelining is?

- a. Parallelism
- b. None of the mentioned
- c. Overlapping
- d. Serial

Question **10**

Complete

Mark 0.00 out of 1.00

For the load and store operation ---

- a. Effective address is calculated at 3rd stage of the pipeline
- b. Effective address is calculated between 4th and 5th stage of the pipeline
- c. Effective address is calculated at 4th stage of the pipeline
- d. Effective address is calculated between 3rd and 4th stage of the pipeline

Question **11**

Complete

Mark 1.00 out of 1.00

Which one of the following addressing modes cannot be meaningfully used for the destination operand of an ADD instruction?

- a. Indexed
- b. Immediate
- c. Indirect
- d. Direct

Question **12**

Complete

Mark 1.00 out of 1.00

In the J-type instructions of MIPS --

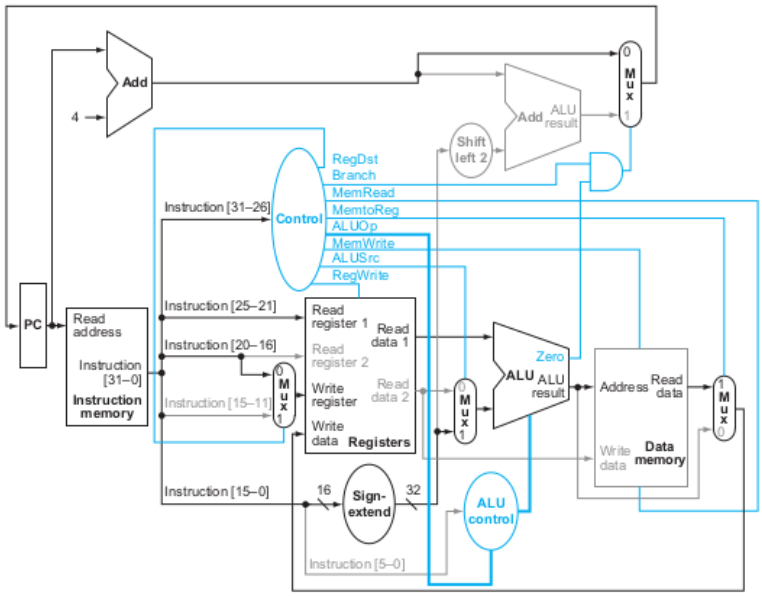
- a. Both operands are not available in the register bank
- b. One operand is provided as a part of the instruction and other operand need to be fetched from memory
- c. Both the operands are available in the register bank
- d. One operand is provided as a part of the instruction and other operand need to be get from accumulator

Question **13**

Complete

Mark 0.00 out of 1.00

Which type of datapath architecture is given in the following



a. With Load instruction

b. I-type of instruction

c. None of the mentioned

d. R-type of instruction

Question **14**

Complete

Mark 0.00 out of 1.00

Consider the following code segment:

Load R1,Loc1; Load R1 from memory location Loc1

Load R2, Loc2; Load R2 from memory location Loc2

Add R1, R2, R1; Add R1 and R2 and save the result in R1

Dec R2; Decrement R2

Dec R1; Decrement R1

Mpy R1,R2, R3; Multiply R1 and R2 and store in R3

Store R3, Loc3; Store r3 in Memory Location Loc3

What is the number of cycles needed to execute the above code segment assuming each instruction takes one cycle to execute?

- a. 14
- b. 7
- c. 10
- d. 13

Question **15**

Complete

Mark 1.00 out of 1.00

What is ISA?

- a. Interface between hardware and sensors
- b. Interface between hardware and RAM
- c. Interface between hardware and software
- d. Interface between hardware and DMA

Question **16**

Complete

Mark 1.00 out of 1.00

How many binary digits are required to show the IEEE 754 binary representation of the number -0.75 base 10 in single precision?

- a. 28
- b. 30
- c. 32
- d. 31

Question **17**

Complete

Mark 1.00 out of 1.00

Pipeline performance is measured by?

- a. Ripple factor
- b. K-Factor
- c. Speed up factor
- d. QE factor

Question **18**

Complete

Mark 0.00 out of 1.00

When executing this program using Tomasulo's algorithm, Find out the last clock cycle

LD F1, 7(R2)
LD F3, 7(R2)
MULTD F9, F1, F3
LD F5, 9(R2)
LD F7, 11(R2)
MULTD F11, F5, F7
ADDD F11, F9, F11
LD F9, 11(R2)
ADDD F11, F11, F9

- a. 22
- b. 23
- c. None of the mentioned
- d. 21

Question **19**

Complete

Mark 1.00 out of 1.00

Consider a 6-stage instruction pipeline, where all stages are perfectly balanced. Assume that there is no cycle-time overhead of pipelining. When an application is executing on this 6-stage pipeline, the speedup achieved with respect to non-pipelined execution if 50% of the instructions incur 2 pipeline stall cycles is?

- a. 6
- b. 4
- c. 3
- d. 7

Question **20**

Complete

Mark 0.00 out of 1.00

Register renaming is used in?

- a. Pipeline Forwarding technique
- b. DRAM memory
- c. Loop unrolling
- d. Virtual memory

Question **21**

Complete

Mark 1.00 out of 1.00

For computers based on three-address instruction formats, each address field can be used to specify which of the following:

S1: A memory operand

S2: A processor register

S3: An implied accumulator register

a. **Only S2 and S3**

b. **Either S2 or S3**

c. **S1, S2 and S3**

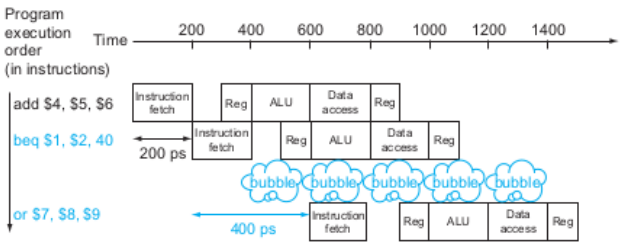
d. **Either S1 or S2**

Question **22**

Complete

Mark 1.00 out of 1.00

Which type of hazards represents the given figure given below?



a. Data hazard

b. Structural

c. None of the mentioned

d. Control

Question **23**
Complete
Mark 1.00 out of 1.00

Booth's algorithm is used for?

- a. Octal multipication
- b. Decimal multipication
- c. Binary multipication
- d. String multipication

Question **24**
Complete
Mark 0.00 out of 1.00

Match the following

X. Indirect Addressing **I. Array implementation**

Y. Indexed Addressing **II. Writing re-locatable code**

Z. Base Register Addressing **III. Passing array as parameter**

- a. **(X, I) (Y, III) (Z, II)**
- b. **(X, III) (Y, II) (Z, I)**
- c. **(X, III) (Y, I) (Z, II)**
- d. **(X, II) (Y, III) (Z, I)**

Question **25**
Complete
Mark 1.00 out of 1.00

When an instruction is required to be brought from memory to CPU, on which one of the following busses is it fetched?

- a. Control bus
- b. Address bus
- c. Peripheral bus
- d. Data bus

◄ Lab-9 and Lab-10 Evaluation

Jump to...

Started on	Wednesday, 7 April 2021, 1:35 PM
State	Finished
Completed on	Wednesday, 7 April 2021, 1:50 PM
Time taken	14 mins 53 secs
Marks	20.00/25.00
Grade	**8.00** out of 10.00 (**80**%)

Question **1**
Complete
Mark 1.00 out of 1.00

The contention for the usage of a hardware device is called _____

- a. Stalk
- b. Optimized compilers
- c. Deadlock
- d. Structural hazard

Question **2**
Complete
Mark 0.00 out of 1.00

_____ occurs when an instruction depends on the result of a previous instruction. But it's result is not yet available.

- a. Data Hazards
- b. None of the mentioned
- c. Structural Hazards
- d. Control Hazards

Question **3**
Complete
Mark 1.00 out of 1.00

The pipelining process is also known as ____

- a. Assembly line operation
- b. Superscalar operation
- c. Dependency
- d. Von Neumann cycle

Question **4**

Complete

Mark 1.00 out of 1.00

Which of the following is not a pipeline conflict?

- a. Data Dependency
- b. Timing variation
- c. Load balancing
- d. Branching

Question **5**

Complete

Mark 1.00 out of 1.00

The periods of time when the unit is idle is called as _____

- a. Hazards
- b. Bubbles
- c. Both Stalls and Bubbles
- d. Stalls

Question **6**

Complete

Mark 0.00 out of 1.00

The control signals to read instruction memory and to write the PC are always asserted, so there is nothing special to control in this pipeline stage.

- a. Instruction fetch
- b. Memory access

  Memory access

  Memory access
- c. Write back
- d. decoding

Question **7**

Complete

Mark 0.00 out of 1.00

The error in the following code is:

Code:

```
main()
{
cycles = 0;
for (i = 1 to the number of instructions);
{
for (j = 1 to instructions[i]);
{
cycles = cycles - 1;
}
}
output results (cycles * cycle length);
}
```

a. cycles = cycles - 1;

b. for (i = 1 to the number of instructions);

c. for (j = 1 to instructions[i]);

d. output results (cycles * cycle length);

Question **8**

Complete

Mark 1.00 out of 1.00

An important compiler technique to get more performance from loops is _____

a. Data transfer instruction

b. latency

c. CPI

d. loop unrolling

Question **9**

Complete

Mark 1.00 out of 1.00

Pipelining is a technique that exploits ____among the instructions in a sequential instruction stream.

- a. Dynamic branch prediction
- b. single instruction
- c. multiple instruction
- d. Parallelism

Question **10**

Complete

Mark 1.00 out of 1.00

The stalling of the processor due to the unavailability of the instructions is called as _____

- a. Control hazard
- b. Structural hazard
- c. None of the mentioned
- d. Input hazard

Question **11**

Complete

Mark 1.00 out of 1.00

The time lost due to the branch instruction is often referred to as _____

- a. Branch penalty
- b. Delay
- c. Deadlock
- d. Latency

Question **12**

Complete

Mark 1.00 out of 1.00

Number of clock cycles between a load instruction and an instruction that can use the result of the load without stalling the pipeline

- a. latency
- b. Efficiency
- c. Gain of instruction
- d. Throughput

Question **13**

Complete

Mark 1.00 out of 1.00

The __ stage, which places the result back into the register file in the middle of the datapath

- a. decoding
- b. Instruction fetch
- c. Memory access
- d. Write back

Question **14**

Complete

Mark 0.00 out of 1.00

_____ hazards caused by access of memory (resources) by two segments at the same time.

- a. None of the mentioned
- b. Data hazards
- c. Structural hazards
- d. Control hazards

Question **15**
Complete
Mark 1.00 out of 1.00

A ____ is a small memory indexed by the lower portion of the address of the branch instruction.

- a. Branch prediction buffer
- b. **Dynamic branch prediction**
- c. **prediction branch**
- d. **Dynamic branch**

Question **16**
Complete
Mark 1.00 out of 1.00

How many types of pipelining exist?

- a. 2
- b. 5
- c. 3
- d. 4

Question **17**
Complete
Mark 1.00 out of 1.00

in loop Unrolling with Scheduling---. Select the right option.

- a. All of the mentioned
- b. Determine the loads and stores that can be interchanged in the unrolled loop
- c. Use different registers to avoid unnecessary constraints
- d. Identify that loop iterations are independent

Question **18**
Complete
Mark 1.00 out of 1.00

For software pipeline. Select the right option.

- a. Less memory space is required
- b. Speed is high
- c. All of the mentioned
- d. Independent instructions can be part of pipeline loop body

Question **19**
Complete
Mark 1.00 out of 1.00

The situation wherein the data of operands are not available is called _____

- a. Stock
- b. Deadlock
- c. Structural hazard
- d. Data hazard

Question **20**
Complete
Mark 1.00 out of 1.00

Which of the following is an advantage of pipelining?

- a. Pipelining increases the overall performance of CPU
- b. Faster ALU can be designed with pipelining
- c. Instruction throughput increases
- d. All of the mentioned

Question **21**
Complete
Mark 1.00 out of 1.00

_____ have been developed specifically for pipelined systems.

- a. None of the mentioned
- b. Speed up utilities
- c. Utility software
- d. Optimizing compilers

Question **22**
Complete
Mark 1.00 out of 1.00

A ____ is a cycle in the pipeline without new input.

- a. CPI
- b. latency
- c. stall
- d. forwarding

Question **23**
Complete
Mark 1.00 out of 1.00

Any condition that causes a processor to stall is called as _____

- a. System error
- b. Hazard
- c. None of the mentioned
- d. Page fault

Question **24**

Complete

Mark 1.00 out of 1.00

In the Arithmetic pipeline, the floating-point addition and subtraction are done in ___ parts.

- a. 4
- b. 2
- c. 5
- d. 3

Question **25**

Complete

Mark 0.00 out of 1.00

For the program given below the number of stalls required after the code transformed by the smart compiler are

MIPS Code:

1. LW R2, 0(R4)
2. LW R5, 4(R4)
3. ADD R1, R2, R3

- a. One
- b. Two
- c. Three
- d. Zero

◄ Lab-5 and Lab-6 Evaluation

Jump to...

Lab-9 and Lab-10 Evaluation ►

Started on	Wednesday, 10 March 2021, 1:40 PM
State	Finished
Completed on	Wednesday, 10 March 2021, 1:50 PM
Time taken	9 mins 58 secs

Question **1**
Complete
Marked out of 1.00

Ratio of CPU clock cycles for a program to the clock time is

- a. **CPU time**
- b. UPI
- c. CPI
- d. **Instruction count**

Question **2**
Complete
Marked out of 1.00

How many bits are in the (1,3) branch predictor with 2K entries?

- a. 4K
- b. 5K
- c. 12K
- d. 1K

Question **3**

Complete

Marked out of 1.00

What is the decimal value of this 32-bit two's complement number? (1111 1111 1111 1111 1111 1111 1111 1100)base2

- a. **(-9)base10**
- b. **(-8)base10**
- c. **(-6)base10**
- d. **(-4)base10**

Question **4**

Complete

Marked out of 1.00

Consider two instructions m and n, with m preceding n in program order. The possible data hazards are ___ , n tries to read a source before m writes it, so n incorrectly gets the old value.

- a. WAR
- b. RAR
- c. RAW
- d. WAW

Question **5**

Complete

Marked out of 1.00

A non pipelined processor has a clock rate of 2.5 GHz and an average CPI (Cycle per instruction) of 4. AN upgrade to the processor introduces a five-stage pipeline. However, due to internal pipeline delays, such as latency delay the clock rate of the new processor has to be reduced to 2 GHz. What is the speedup achieved for a typical program?

- a. 4
- b. 3
- c. 4.8
- d. 3.8

Question **6**

Complete

Marked out of 1.00

A micro control unit is required to generate a total of 25 control signals. Assume that during any microinstruction at most two control signals are active minimum no of bits required in the control word to generate the control signal will be

- a. 12
- b. 10
- c. 2.5
- d. 2

Question **7**

Complete

Marked out of 1.00

Which of the following is not a valid segment of four-stage instruction pipeline?

- a. **DA**
- b. **DO**
- c. **EX**
- d. **FI**

Question **8**

Complete

Marked out of 1.00

___ hazards are present only in pipelines that write in more than one pipe stage or allow instruction to proceed even when a previous instruction is stalled.

- a. **RAW**
- b. **WAR**
- c. **WAW**
- d. **RAR**

Question **9**

Complete

Marked out of 1.00

A computer architect is designing the memory system for the next version of a processor. IF the current version of the processor spends 40 percent of its time processing memory references, by how much must the architect speed up the memory system to achieve an overall speedup of 1.2?

- a. 1.07
- b. 1.01
- c. 1.71
- d. 1.51

Question **10**

Complete

Marked out of 1.00

Which of the following is an advantage of pipelining?

- a. **Pipelining increases the overall performance of the CPU.**
- b. **All of the mentioned**
- c. **Instruction throughput increases.**
- d. **Faster ALU can be designed when pipelining is used.**

Question **11**

Complete

Marked out of 1.00

How many branch-selected entries are in a (3,3) predictor that has a total of 24K bits in the prediction buffer?

- a. 3K
- b. 4K
- c. 2K
- d. 1K

Question **12**

Complete

Marked out of 1.00

All processors use pipelining to overlap the execution of instructions and improve performance. This potential overlap among instructions is called

- a. **All of the above**
- b. **Loop-Level Parallelism**
- c. **instruction-level parallelism**
- d. **Data-Level Parallelism**

Question **13**

Complete

Marked out of 1.00

A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speedup ratio of the pipeline for 100 tasks.

a. **100/21**

b. **4/21**

c. **21/4**

d. **21/100**

Question **14**

Complete

Marked out of 1.00

Consider two instructions m and n, with m preceding n in program order. The possible data hazards are _____, n tries to write a destination before it is read by m, so m incorrectly gets the new value.

a. **RAW**

b. **WAR**

c. **WAW**

d. **RAR**

Question **15**

Complete

Marked out of 1.00

Computer A has an Instruction count of 20 billion, a Clock rate of 8 GHz, and CPI of 1 then what is MIPS.

- a. 3K
- b. 2K
- c. 7K
- d. 8K

Question **16**

Complete

Marked out of 1.00

A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. What is the maximum speedup that can be achieved for 100 tasks?

- a. 10
- b. 6
- c. 5
- d. 7

Question **17**

Complete

Marked out of 1.00

Suppose we have two implementations of the same instruction set architecture. Computer A has a clock cycle time of 500 ps and a CPI of 1.2 for some programs, and computer B has a clock cycle time of 250 ps and a CPI of 2.0 for the same program. Which computer is faster for this program and by how much?

- a. **Computer B is 1.2 times as fast as computer A**
- b. **Computer A is 2 times as fast as computer B**
- c. **Computer A is 1.2 times as fast as computer B**
- d. **Computer B is 2 times as fast as computer A**

Question **18**

Complete

Marked out of 1.00

Find the correct sequence to perform any instruction in four-stage pipelining.

a. **DA, FI, EX, FO**

b. **FI, DA, EX, FO**

c. **FI, DA, FO, EX**

d. **FI, FO, DA, EX**

Question **19**

Complete

Marked out of 1.00

Each stage in pipelining should be completed within _____ cycle.

a. 1

b. 2

c. 1.5

d. 3

Question **20**

Complete

Marked out of 1.00

In the arithmetic pipeline, consider the first number's exponent is 4 and the second number's exponent is 6. Which exponent will be selected after comparing both?

- a. 2
- b. 4
- c. 6
- d. 10

◄ Lab 3 and Lab 4 online test

Jump to...

Lab-7 and Lab-8 Evaluation ►

Started on	Wednesday, 10 February 2021, 1:40 PM
State	Finished
Completed on	Wednesday, 10 February 2021, 1:48 PM
Time taken	7 mins 59 secs
Grade	**6.00** out of 10.00 (**60**%)

Question **1**
Complete
Mark 1.00 out of 1.00

What will be the right shift of 01111111 after 8 cycles?

- a. 01111111
- b. 0000001
- c. 11111111
- d. None of the mentioned

Question **2**
Complete
Mark 1.00 out of 1.00

If LSB bit of Q and Q_{-1} are equal then the operation performed by the Booth's algorithm is

- a. AC =AC +M
- b. None of the mentioned
- c. Shift right
- d. AC =AC - M

Question **3**
Complete
Mark 1.00 out of 1.00

What is the three times shift right of the binary stream 0 1 0 1 1 1 1 0 1?

- a. 0 0 1 0 1 1 1 1 0 1
- b. 0 1 0 1 1 1 1 0 1
- c. 1 1 0 1 1 1 1 0 1
- d. None of the mentioned

Question **4**

Complete

Mark 1.00 out of 1.00

A 16-bit ripple carry adder is realized using 16 identical full adders. The carry propagation delay of each full adder is 12 ns and the sum propagation delay of each full adder is 15 ns. The worst case delay of this 16 bit adder will be _____?

- a. 192 ns
- b. 190 ns
- c. None of the mentioned
- d. 193 ns

Question **5**

Complete

Mark 0.00 out of 1.00

Ripple carry adder is ?

- a. Parallel adder
- b. Sum and carry are parallel available
- c. None of the mentioned
- d. Serial adder

Question **6**

Complete

Mark 1.00 out of 1.00

The Ripple carry adder is designed and fabricated based on

- a. None of the mentioned
- b. V Technology
- c. R technology
- d. L Technology

Question **7**

Complete

Mark 0.00 out of 1.00

The parallel multipliers like radix 2 and radix 4 modified booth multiplier does the computations using

- a. More adders and lesser iterative steps
- b. lesser adders and more iterative steps
- c. lesser adders and lesser iterative steps
- d. more adders and more iterative steps

Question **8**

Complete

Mark 0.00 out of 1.00

```
The program given below
```

```
Begin
   Condition:
   1. If Qn and Qn+1 are same i.e. 00 or 11 perform arithmetic shift by 1 bit.
   2. If Qn Qn+1 = 10 do A= A + BR and perform arithmetic shift by 1 bit.
   3. If Qn Qn+1 = 01 do A= A – BR and perform arithmetic shift by 2 bit.
```

```
End
```

- a. Condition 1 not true
- b. None of the mentioned
- c. Condition 2 not true
- d. Condition 3 is True

Question **9**

Complete

Mark 1.00 out of 1.00

What is the arithmetic shift right operation after the 3nd cycle for the following binary stream 1 0 0 1 0 0 1 1 0 ?

- a. 1 1 0 1 0 0 1 1 0
- b. 1 0 0 1 0 0 1 1 0
- c. None of the mentioned
- d. 0 0 0 0 1 0 0 1 1 0

Question **10**

Complete

Mark 0.00 out of 1.00

Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N- bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit in which the carry-out of each full adder is

- a. N-1 Adder output
- b. N-2 Adder output
- c. N-3 Adder output
- d. None of the mentioned

◄ Announcements

Jump to...

Lab-5 and Lab-6 Evaluation ►