Started on	Friday, 11 March 2022, 10:00 AM
State	Finished
Completed on	Friday, 11 March 2022, 11:05 AM
Time taken	1 hour 4 mins
Marks	40.0/45.0
Grade	**17.8** out of 20.0 (**89**%)

Question **1**

Correct

Mark 1.0 out of 1.0

A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The number of and gates required to design full adders are?

- a. Nine ✔
- b. Twelve
- c. Eight
- d. Ten

Your answer is correct.

The correct answer is:
Nine

Question **2**

Correct

Mark 1.0 out of 1.0

Consider the following instruction sequence five-stage pipeline,

ADD R1, R2, R1 --- I1

LW R2,0(R1) --- I2

LW R1,4(R1) -- I3

OR R3, R1, R2 -- I4

Select the correct option.

- a. RAW hazards is present in instructions I1-I2
- b. RAW hazards is present in instructions I2-I3
- c. RAW hazards is present in instructions I3-I4
- d. All of the mentioned ✔

Your answer is correct.

The correct answer is:
All of the mentioned

Question **3**

Correct

Mark 1.0 out of 1.0

Pipelining of a MIPS-like Processor, select the right option

- a. Only instructions which access memory are load and store instructions
- b. All of the mentioned ✔
- c. All ALU operations are performed on register operands
- d. Separate Instruction and data memory is required

Your answer is correct.

The correct answer is:
All of the mentioned

Question **4**

Correct

Mark 1.0 out of 1.0

In pipelining, which of the following operation is used to enhance the memory access speed?

- a. Cache ✔
- b. Registers
- c. Stack
- d. Queue

Your answer is correct.

The correct answer is:
Cache

Question **5**

Correct

Mark 1.0 out of 1.0

Forwarding can be implemented in 5-stage and 6-stage MIPS pipeline --

- a. Using one multiplexer
- b. Using three multiplexers
- c. Using two multiplexers ✔
- d. Using two multiplexers with extra latch

Your answer is correct.

The correct answer is:
Using two multiplexers

Question **6**

Correct

Mark 1.0 out of 1.0

If multiplicand (M) is 0111, the AC register is initialized with zero. What will be the content of the AC register after operation AC= AC-M?

- a. 1111
- b. 1010
- c. 1001 ✔
- d. 1100

Your answer is correct.

The correct answer is:
1001

Question **7**

Correct

Mark 1.0 out of 1.0

Instruction pipeline improves the CPU performance due to which one of the following reasons?

- a. Efficient utilization of the processor hardware ✔
- b. Use of additional functional units
- c. Reduced memory access time
- d. Use a larger Cache

Your answer is correct.

The correct answer is:
Efficient utilization of the processor hardware

Question **8**

Incorrect

Mark 0.0 out of 1.0

Overcoming control dependence is done by ____ on the outcome of branches?

- a. None of the mentioned ✖
- b. speculating
- c. Out of order scheme
- d. Scoreboard

Your answer is incorrect.

The correct answer is:
speculating

Question **9**

Correct

Mark 1.0 out of 1.0

A computer has a word size of 16-bit and has 16 programmer visible registers. each instruction has two sources and one destination operands and uses only register direct addressing mode. what is the maximum number of op-codes that this processor can have?

- a. 32
- b. 64
- c. 8
- d. 16 ✔

Your answer is correct.

The correct answer is:
16

Question **10**

Correct

Mark 1.0 out of 1.0

Little Endian byte order puts the byte having address

- a. Most Significant Position
- b. Least Significant Position ✔
- c. Middle Significant Position

Your answer is correct.

The correct answer is:
Least Significant Position

Question **11**

Correct

Mark 1.0 out of 1.0

For the load and store operation ---

- a. Effective address is calculated between 3rd and 4th stage of the pipeline
- b. Effective address is calculated at 4th stage of the pipeline
- c. Effective address is calculated between 4th and 5th stage of the pipeline
- d. Effective address is calculated at 3rd stage of the pipeline ✔

Your answer is correct.

The correct answer is:
Effective address is calculated at 3rd stage of the pipeline

Question **12**

Incorrect

Mark 0.0 out of 1.0

The instruction Z=X+Y; needs to be run on accumulator-based architecture. Choose the current option.

- a. One operand is available in DMA
- b. Both operands are available in the register bank ✖
- c. One operand is available in the accumulator and other need to be fetched from memory
- d. Both operands are available in the accumulator

Your answer is incorrect.

The correct answer is:
One operand is available in the accumulator and other need to be fetched from memory

Question **13**

Correct

Mark 1.0 out of 1.0

A four-stage pipeline has stage delays of 150, 120, 160, and 140 ns respectively. Registers are used between the stages and have a delay of 10 ns each. What is the cycle time?

- a. 140 ns
- b. 170 ns ✔
- c. 155 ns
- d. 165 ns

Your answer is correct.

The correct answer is:
170 ns

Question **14**

Correct

Mark 1.0 out of 1.0

A pipelined processor has seven stages, namely, IF1, IF2, ID, EX, MEM1, MEM2, WB. Assuming all the stages require the same amount of time and the time period of the non- pipelined processors is 14 ns, find out the clock frequency and speedup of the pipelined processor. Assume the delay of the latches is 1 ns.

- a. 1 Khz and 3
- b. None of the mentioned ✔
- c. 1Khz and 50
- d. 1.2 Khz and 30

Your answer is correct.

The correct answer is:
None of the mentioned

Question **15**

Correct

Mark 1.0 out of 1.0

ARM processors are available in the form of -------- pipelining?

- a. Both 3 and 5 stages ✔
- b. 3 stage
- c. 5 stage
- d. None of them

Your answer is correct.

The correct answer is:
Both 3 and 5 stages

Question **16**

Incorrect

Mark 0.0 out of 1.0

Parallelism can be achieved by----------technique.

- a. Hardware
- b. Compiler
- c. Software
- d. All of the above ✖

Your answer is incorrect.

The correct answer is:
Hardware

Question **17**

Correct

Mark 1.0 out of 1.0

The stages of 3 stage pipelining are----?

- a. Address generation, Fetch, Execute.
- b. Decode, Fetch, Execute
- c. Execute, Fetch, Decode
- d. Fetch, Decode, Execute ✔

Your answer is correct.

The correct answer is:
Fetch, Decode, Execute

Question **18**

Correct

Mark 1.0 out of 1.0

Branch predictors, that use the behavior of other branches to make a prediction is called?

- a. one-level predictor
- b. Branch predictors that use the behavior of other branches to make a predic- correlating predictors ✔
- c. non-correlation predictors
- d. multi-level predictors

Your answer is correct.

The correct answer is:
Branch predictors that use the behavior of other branches to make a predic- correlating predictors

Question **19**

Correct

Mark 1.0 out of 1.0

Forwarding can be implemented in 5-stage and 6-stage MIPS pipeline --

- a. Using three multiplexers
- b. Using one multiplexer
- c. Using two multiplexers with extra latch
- d. Using two multiplexers ✔

Your answer is correct.

The correct answer is:
Using two multiplexers

Question **20**

Correct

Mark 1.0 out of 1.0

In which one of the following addressing modes, the content of the program counter is added to the address part of the instruction in order to obtain the effective address.

- a. Indexed addressing mode
- b. Absolute addressing mode
- c. Register addressing mode
- d. Register indirect addressing mode ✔

Your answer is correct.

The correct answer is:
Register indirect addressing mode

Question **21**

Correct

Mark 1.0 out of 1.0

The zero flag register of the MIPS pipeline architecture--

- a. Calculate the effective address by using the instruction register content
- b. Calculate the effective address by adding the register content of the ALU
- c. Calculate the effective address by subtracting the register content of the ALU ✔
- d. Calculate the effective address by using the program counter register content

Your answer is correct.

The correct answer is:
Calculate the effective address by subtracting the register content of the ALU

Question **22**

Correct

Mark 1.0 out of 1.0

When the data operands are not available then it is called----?

- a. Pop
- b. Data hazard ✔
- c. Deadlock
- d. Push

Your answer is correct.

The correct answer is:
Data hazard

Question **23**

Correct

Mark 1.0 out of 1.0

Using booth's algorithms multiply 7 with 3 and assume register AC is 4 bit. The value of AC after 3rd and 4th cycles are

- a. 1 0 1 0 and 1 0 1 0
- b. 0 0 1 0 and 1 0 1 0 ✔
- c. 0 1 1 1 0 and 1 0 1 0 0
- d. 0 0 1 1 and 1 0 1 1

Your answer is correct.

The correct answer is:
0 0 1 0 and 1 0 1 0

Question **24**

Correct

Mark 1.0 out of 1.0

The features of the RISC processor --

- a. Small number of addressing modes
- b. Instruction execute in one or two clock cycle
- c. All of the mentioned ✔
- d. Small number of the instructions

Your answer is correct.

The correct answer is:
All of the mentioned

Question **25**

Correct

Mark 1.0 out of 1.0

Consider a three address RISC processor ISA. Which one of the following correctly characterizes an effect of doubling the number of registers in the processor?

- a. Instruction size would be increase by 3-bit ✔
- b. Instruction size would be increase by 1-bit
- c. Instruction size would be unaffected
- d. Instruction size would be increase by 2-bit

Your answer is correct.

The correct answer is:
Instruction size would be increase by 3-bit

Question **26**

Incorrect

Mark 0.0 out of 1.0

Throughput is calculated as

- a. Speed of the processor/ Number of instructions
- b. The number of instructions/ Total time to complete the instructions ✖
- c. Total time to complete the instructions/number of instructions
- d. The number of instructions/speed of the processor

Your answer is incorrect.

The correct answer is:
Total time to complete the instructions/number of instructions

Question **27**

Correct

Mark 1.0 out of 1.0

In pipelined processor, the WB stage in instruction execution is ....stage?

- a. Fifth ✔
- b. Seventh
- c. First
- d. Third

Your answer is correct.

The correct answer is:
Fifth

Question **28**

Correct

Mark 1.0 out of 1.0

An instruction cycle refers to which one of the following?

- a. Executing an instruction
- b. Fetching an instruction
- c. All of the mentioned ✔
- d. Decoding the instruction and calculation of effective address

Your answer is correct.

The correct answer is:
All of the mentioned

Question **29**

Correct

Mark 1.0 out of 1.0

For calculating the effective address, the upper 6 bits and concatenation done between---

- a. Program counter and constant value which was not the part of the instruction
- b. Address register and constant value which was not the part of the instruction
- c. Program counter and constant value which was the part of the instruction ✔
- d. Address register and constant value which was the part of the instruction

Your answer is correct.

The correct answer is:
Program counter and constant value which was the part of the instruction

Question **30**

Correct

Mark 1.0 out of 1.0

DIV.D F0,F2,F4

ADD.D F6,F0,F8

S.D F6,0(R1)

SUB.D F8,F10,F14

MUL.D F6,F10,F8

Which types of hazards are available in the above-given code?

a. WAR and RAR

b. WAR and RAW

c. WAW and WAR ✔

d. RAW and WAR

Your answer is correct.

The correct answer is:
WAW and WAR

Question **31**

Correct

Mark 1.0 out of 1.0

In a pipelined processor, the processing units for integers and floating point is-------?

a. Same unit.

b. Separate unit. ✔

c. No unit.

d. Within each other.

Your answer is correct.

The correct answer is:
Separate unit.

Question **32**

Correct

Mark 1.0 out of 1.0

Addressing modes are used to calculate the effective address by using the --

- a. Control Unit
- b. ALU + control unit ✔
- c. DMA
- d. ALU unit only

Your answer is correct.

The correct answer is:
ALU + control unit

Question **33**

Correct

Mark 1.0 out of 1.0

What is the arithmetic shift right operation after the 1st cycle for the following binary stream 1 0 0 1 0 0 1 1 0 ?

- a. 1 1 1 0 0 1 0 0 1
- b. 0 1 1 0 0 1 0 0 1
- c. 1 1 0 0 1 0 0 1 1 ✔
- d. 1 0 0 1 0 0 1 1 0

Your answer is correct.

The correct answer is:
1 1 0 0 1 0 0 1 1

Question **34**

Incorrect

Mark 0.0 out of 1.0

Pipelining is a ----------technique?

- a. Superscalar operation ✖
- b. Parallel operation
- c. Serial operation
- d. Scalar operation

Your answer is incorrect.

The correct answer is:
Serial operation

Question **35**

Correct

Mark 1.0 out of 1.0

Out-of-order execution introduces the possibility of ____ hazards.

- a. WAR and WAW ✔
- b. RAR and WAR
- c. WAR and RAW
- d. RAW and RAR

Your answer is correct.

The correct answer is:
WAR and WAW

Question **36**

Correct

Mark 1.0 out of 1.0

A booth's multiplier circuit needs to inspect at most how many LSB bits to determine whether to add the multiplier, subtract the multiplier or leave the partial result unchanged during any step in the sequence of multiplication steps?

- a. One bit ✔
- b. All bits of the multiplier
- c. All bits of the multipicand
- d. Two bits

Your answer is correct.

The correct answer is:
One bit

Question **37**

Correct

Mark 1.0 out of 1.0

Which of the following instruction is not used for changing state....?

- a. no
- b. nop ✔
- c. nope
- d. no-op

Your answer is correct.

The correct answer is:
nop

Question **38**

Correct

Mark 1.0 out of 1.0

In the MIPS architecture, data transfer takes place between --

- a. Register to register
- b. All of the mentioned ✔
- c. Register to memory
- d. Memory to register

Your answer is correct.

The correct answer is:
All of the mentioned

Question **39**

Correct

Mark 1.0 out of 1.0

Von Neumann computers helping to which one of the following classes of computers?

- a. MIMD
- b. MISD
- c. SISD ✔
- d. SIMD

Your answer is correct.

The correct answer is:
SISD

Question **40**

Correct

Mark 1.0 out of 1.0

Which of the addressing mode refer the memory two times in accessing the data?

- a. indirect addressing mode ✔
- b. Direct addressing mode
- c. Immediate addressing mode
- d. Relative addressing mode

Your answer is correct.

The correct answer is:
indirect addressing mode

Question **41**

Correct

Mark 1.0 out of 1.0

In the MIPS instruction fields, the shamt field is of

- a. 4 bits
- b. 6 bits
- c. 7 bits
- d. 5 bits ✔

Your answer is correct.

The correct answer is:
5 bits

Question **42**

Correct

Mark 1.0 out of 1.0

The following assembly program is run over the MIPS pipeline architecture. Choose the wrong option.

Assembly code:

i1. pp1: L.D F0,0(R1);

i2. ADD.D F4,F0,F2;

i3. S.D F4,0(R1);

i4. DADDUI R1,R1,#-8;

i5. BNE R1,R2,pp1

- a. i1 is used for array element ✔
- b. i4 is used as an increment pointer
- c. i3 is used to store the results
- d. i2 is used for adding scalar value

Your answer is correct.

The correct answers are:
i1 is used for array element,

i4 is used as an increment pointer

Question **43**

Correct

Mark 1.0 out of 1.0

Which one of the following most profoundly describes the functionality of the control unit in CPU?

- a. To store program instruction
- b. To perform logic operations based on decoded program instructions
- c. To generate the control signals based on decoded program instructions ✔
- d. To perform the arithmetic operations based on decoded program instruction

Your answer is correct.

The correct answer is:
To generate the control signals based on decoded program instructions

Question **44**

Correct

Mark 1.0 out of 1.0

By using pipelining, the latency of the instructions---?

- a. Increases
- b. Decreases ✔
- c. Remains the same
- d. It is unity

Your answer is correct.

The correct answer is:
Decreases

Question **45**

Correct

Mark 1.0 out of 1.0

The following lines of code IR <= Memory[PC]; PC <= PC + 4; explains the

- a. None of them
- b. Instruction Decode Step
- c. Instruction Fetch Step ✔
- d. Instruction Excute Step

Your answer is correct.

The correct answer is:
Instruction Fetch Step

◄ CS-208-Assignment-2_02-03-2022

Jump to...

CS-208-Assignment-3_06-04-2022 ►