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|---|---|
| **Started on** | Saturday, 9 April 2022, 11:00 AM |
| **State** | Finished |
| **Completed on** | Saturday, 9 April 2022, 11:48 AM |
| **Time taken** | 48 mins 9 secs |
| **Marks** | 26.00/35.00 |
| **Grade** | **7.43** out of 10.00 (**74**%) |

Question **1**

Complete

Mark 0.00 out of 1.00

**In 2 bit ripple carry adder, used XOR, AND, and OR gates propagation delay are 15ns, 10ns and 5ns, respectively. What is the required time for a valid answer?**

- a. **60ns**
- b. **50ns**
- c. **70ns**
- d. **30ns**

Question **2**

Complete

Mark 1.00 out of 1.00

For the Stages of Datapath and control( Execution sequence) for instruction MOV 20(R1),R2. Select the correct option?

- a. Add 20 to value in register R1
- b. All of the mentioned
- c. Decode to find that it is an MOV instruction, then read registers R1 and R2
- d. Fetch the instruction, and increment PC

Question **3**

Complete

Mark 1.00 out of 1.00

Consider a ideal pipeline having 5 phases with duration 30, 10, 40, 10 and 30 ns. Given latch delay is 5 ns. What is the Non-pipeline execution time in ns?

- a. 110
- b. 120
- c. 130
- d. 100

Question **4**

Complete

Mark 1.00 out of 1.00

**Among ripple carry adder and carry look ahead, in which time delay is independent of a number of bits of operand.**

- a. **None**
- b. **Both**
- c. **Ripple carry adder**
- d. **carry look ahead**

Question **5**

Complete

Mark 1.00 out of 1.00

What is the two times arithmetic shift right (ASR) of the binary stream 0 1 0 1 1 1 1 0 1?

- a. 0 0 0 1 0 1 1 1 1
- b. 0 1 0 1 1 1 1 0 1
- c. 1 0 0 1 0 1 1 1 0
- d. 0 1 0 1 1 1 1 0 0

Question **6**

Complete

Mark 0.00 out of 1.00

The role of sign extension hardware in data path architechture?

- a. All of the mentioned
- b. To convert the 8 bit to 32 bit binary number
- c. To convert the 16 bit to 32 bit binary number
- d. To convert the 12 bit to 32 bit binary number

Question **7**

Complete

Mark 1.00 out of 1.00

**Code:**

**DIV.D F0,F2,F4**

**ADD.D F6,F0,F8**

**S.D F6,0(R1)**

**SUB.D F8,F10,F14**

**MUL.D F6,F10,F8**

**How many possible hazards are available in the given code?**

- a. 4
- b. 5
- c. 2
- d. 3

Question **8**

Complete

Mark 1.00 out of 1.00

**In 4 bit ripple carry adder, carry propagation delay is 10ns, and sum propagation delay is 20ns. What is the required time for a valid answer?**

- a. **50ns**
- b. **40ns**
- c. **30ns**
- d. **20ns**

Question **9**

Complete

Mark 1.00 out of 1.00

A four stage pipeline has the stage delays as 150, 120, 160 and 140 ns respectively. Registers are used between the stages and have a delay of 5 ns each. Assuming constant clocking rate, what is the total time (micro second) taken to process 1000 data items on the pipeline?

- a. 165.1
- b. 165.3
- c. 165.4
- d. 165.5

Question **10**

Complete

Mark 0.00 out of 1.00

**The 2bits ripple carry adder is made by 3 input XOR, OR and 2 input AND gate. All 3 input gates have a propagation delay of 5ns, and 2 input gates have a propagation delay of 1ns. What is the required time for a valid answer?**

- a. **13ns**
- b. **11ns**
- c. **10ns**
- d. **16ns**

Question **11**

Complete

Mark 1.00 out of 1.00

The first and second address sent by the PC to the memory and their corresponding content will be stored into

- a. Instruction register and PC register
- b. Both into instruction register
- c. Instruction register and data register
- d. None of the mentioned

Question **12**

Complete

Mark 1.00 out of 1.00

**Any condition that causes a processor to stall is called as _____**

- a. **Page fault**
- b. Pipeline error
- c. **Hazard**
- d. **System error**

Question **13**

Complete

Mark 1.00 out of 1.00

Pipelining of a MIPS-like Processor, select the right option

- a. All ALU operations are performed on register operands
- b. Only instructions which access memory are load and store instructions
- c. All of the mentioned
- d. Separate Instruction and data memory is required

Question **14**

Complete

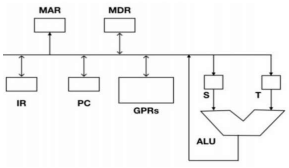
Mark 1.00 out of 1.00

Consider the following data path of a CPU. The ALU, the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU. Two clock cycles are needed for memory read operation – the first one for loading address in the MAR and the next one for loading data from the memory bus into the MDR. The instruction "call Rn, sub" is a two word instruction. Assuming that PC is incremented during the fetch cycle of the first word of the instruction, its register transfer interpretation is

Rn←PC+1Rn←PC+1;

PC←M[PC]PC←M[PC];

How many minimum number of CPU clock cycles needed during the execution cycle of this instruction?




- a. 2 cycle
- b. 7 cycle
- c. 3 cycle
- d. 5 cycle

Question **15**

Complete

Mark 1.00 out of 1.00

In the MIPS architecture, data transfer takes place between ?

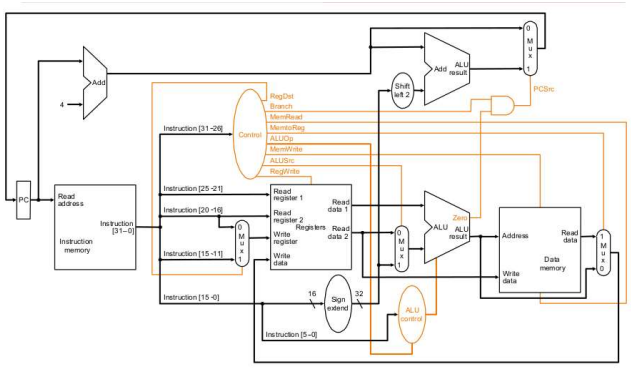
- a. All of the mentioned
- b. Register to memory
- c. Memory to register
- d. Register to register

Question **16**

Complete

Mark 1.00 out of 1.00

For the figure given below, select the correct option ?




- a. I-type instruction can not be executed
- b. R-type instruction can not be executed
- c. None of the mentioned
- d. J-type instruction can not be executed

Question **17**

Complete

Mark 0.00 out of 1.00

**Which one is not the pipeline performance parameter?**

- a. Speed up ratio
- b. Pipeline cycle time
- c. Throughput
- d. Pipeline overlapping factor

Question **18**

Complete

Mark 0.00 out of 1.00

Consider a pipeline having 4 phases with duration 10, 20, 30 and 40 ns. Given latch delay is 10 ns. The pipeline may produce wrong output data if the minimum clock cycle time (ns) is less than

- a. 40
- b. 30
- c. 20
- d. 10

Question **19**

Complete

Mark 1.00 out of 1.00

How many types of pipelining exist?

- a. 2
- b. 3
- c. 4
- d. 1

Question **20**

Complete

Mark 1.00 out of 1.00

**The contention for the usage of a hardware device is called _____**

- a. Control hazard
- b. None of the Mentioned
- c. **Structural hazard**
- d. **Data hazard**

Question **21**

Complete

Mark 0.00 out of 1.00

The features of the RISC processor ?

- a. Small number of addressing modes
- b. Small number of the instructions
- c. Instruction execute in one or two clock cycle
- d. All of the mentioned

Question **22**

Complete

Mark 1.00 out of 1.00

Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 20 ns. What is Pipeline cycle time in ns.

- a. 110
- b. None of the mentioned
- c. 90
- d. 100

Question **23**

Complete

Mark 1.00 out of 1.00

Consider the unpipelined machine with 10ns clock cycles. It uses four cycles for ALU operations and branches where as five cycles for memory operations. Assume that the relative frequencies of these operations are 40%,20% and 40% respectively. Let due to clock skew and set up pipelining, the machine adds 1 ns of overhead to the clock. What is the average instruction execution time(ns)?

- a. 32
- b. 42
- c. None of the mentioned
- d. 40

Question **24**

Complete

Mark 1.00 out of 1.00

Which of the following is not a pipeline conflict?

- a. Timing variation
- b. Load balancing
- c. Data Dependency
- d. Branching

Question **25**

Complete

Mark 0.00 out of 1.00

The full 32 bit target address is computed by concatenating?

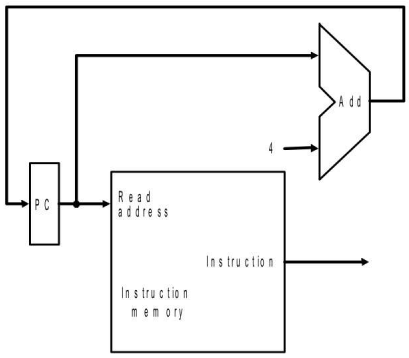
- a. 26 bit immediate field of the jump instruction
- b. All of the mentioned
- c. Bits 00 in the lowest positions
- d. Upper 4 bits of PC+4

Question **26**

Complete

Mark 0.00 out of 1.00

For the figure given below, select the correct option




- a. PC = PC+0 for the first address
- b. All of the mentioned
- c. PC = PC+4 for the second address
- d. Address will be the multiple fo 4

Question **27**

Complete

Mark 1.00 out of 1.00

In which one of the following addressing modes, the content of the program counter is added to the address part of the instruction in order to obtain the effective address?

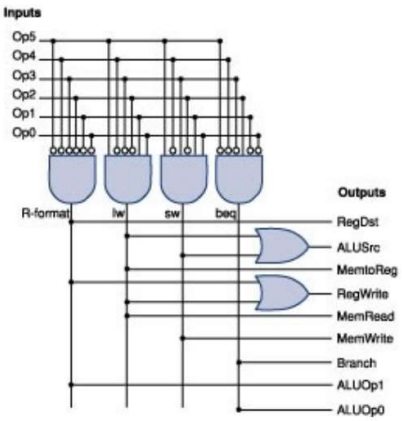
- a. Indexed addressing mode
- b. Absolute addressing mode
- c. Register indirect addressing mode
- d. Register addressing mode

Question **28**

Complete

Mark 1.00 out of 1.00

The figure given below is the example of ?




- a. Branch control unit
- b. ALU control unit
- c. RAW hazard control unit
- d. CPU Main control unit

Question **29**

Complete

Mark 1.00 out of 1.00

Which one of the following about the MIPS rating of a computer is FALSE?

- a. MIPS rating of a processor is independent of the program is being executed.
- b. MIPS rating of computer depends on the computer being used
- c. None of the mentioned
- d. MIPS rating of a computer can very based on which instruction of a processor are being considered

Question **30**

Complete

Mark 1.00 out of 1.00

**Out-of-order execution introduces the possibility of ____ hazards**

a. **RAW and RAR**

b. **WAR and RAW**

c. **WAR and WAW**

d. **RAR and WAR**

Question **31**

Complete

Mark 1.00 out of 1.00

The processor speed has been increased over the last five decades due the ?

a. None of the mentioned

b. Charl's law

c. Moore's Law

d. Krammar's Law

Question **32**

Complete

Mark 1.00 out of 1.00

The two numbers given below are multiplied using Booth's algorithm.

Multiplicand : 0101 1010 1110 1110

Multiplier: 0111 0111 1011 1101

How many additions/Subtractions are required for the multiplication of the above two numbers?

- a. 9 additions/Subtractions are required
- b. 5 additions/Subtractions are required
- c. 8 additions/Subtractions are required
- d. None of the mentioned

Question **33**

Complete

Mark 0.00 out of 1.00

**Carry look adder is better than ripple carry adder because of_____**

- a. **Both**
- b. **Complex architecture**
- c. **Less propagation delay**
- d. **None**

Question **34**

Complete

Mark 1.00 out of 1.00

A booth's multiplier circuit needs to inspect at most how many LSB bits to determine whether to add the multiplier, subtract the multiplier or leave the partial result unchanged during any step in the sequence of multiplication steps?

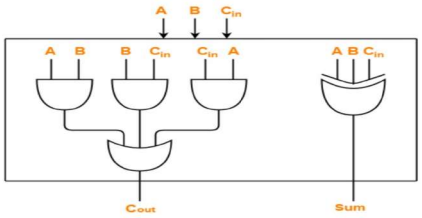
- a. 3 bits
- b. 2 bits
- c. 1 bit
- d. None of the mentioned

Question **35**

Complete

Mark 1.00 out of 1.00

Following figure shows the implementation of full adders in a 16-bit ripple carry adder realized using 16 identical full adders. The propagation delay of the XOR, AND and OR gates are 20 ns, 15 ns and 10 ns respectively. The worst case delay (ns) of this 16 bit adder will be?




a. 396

b. 394

c. 393

d. 395

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