

Started on Friday, 11 March 2022, 10:00 AM

State Finished

Completed on Friday, 11 March 2022, 11:08 AM

Time taken 1 hour 8 mins

Marks 39.00/45.00

Grade **8.67** out of 10.00 (**87%**)

Question **1**

Correct

Mark 1.00 out of 1.00

Which of the addressing mode refer the memory two times in accessing the data?

- a. Direct addressing mode
- b. indirect addressing mode
- c. Immediate addressing mode
- d. Relative addressing mode



Your answer is correct.

The correct answer is:

indirect addressing mode

Question **2**

Correct

Mark 1.00 out of 1.00

Using booth's algorithms multiply 7 with 3 and assume register AC is 4 bit. The value of AC after 3rd and 4th cycles are

- a. 1 0 1 0 and 1 0 1 0
- b. 0 0 1 1 and 1 0 1 1
- c. 0 0 1 0 and 1 0 1 0
- d. 0 1 1 1 0 and 1 0 1 0 0



Your answer is correct.

The correct answer is:

0 0 1 0 and 1 0 1 0

Question **3**

Incorrect

Mark 0.00 out of 1.00

DIV.D F0,F2,F4

ADD.D F6,F0,F8

S.D F6,0(R1)

SUB.D F8,F10,F14

MUL.D F6,F10,F8

Which types of hazards are available in the above-given code?

- a. WAR and RAR
- b. RAW and WAR ✗
- c. WAW and WAR
- d. WAR and RAW

Your answer is incorrect.

The correct answer is:

WAW and WAR

Question **4**

Correct

Mark 1.00 out of 1.00

Little Endian byte order puts the byte having address

- a. Least Significant Position ✓
- b. Middle Significant Position
- c. Most Significant Position

Your answer is correct.

The correct answer is:

Least Significant Position

Question 5

Correct

Mark 1.00 out of 1.00

In the MIPS instruction fields, the shamt field is of

- a. 7 bits
- b. 6 bits
- c. 5 bits
- d. 4 bits



Your answer is correct.

The correct answer is:

5 bits

Question 6

Correct

Mark 1.00 out of 1.00

Branch predictors, that use the behavior of other branches to make a prediction is called?

- a. multi-level predictors
- b. non-correlation predictors
- c. Branch predictors that use the behavior of other branches to make a predicting correlating predictors
- d. one-level predictor



Your answer is correct.

The correct answer is:

Branch predictors that use the behavior of other branches to make a predicting correlating predictors

Question **7**

Correct

Mark 1.00 out of 1.00

The zero flag register of the MIPS pipeline architecture--

- a. Calculate the effective address by adding the register content of the ALU
- b. Calculate the effective address by using the instruction register content
- c. Calculate the effective address by subtracting the register content of the ALU
- d. Calculate the effective address by using the program counter register content



Your answer is correct.

The correct answer is:

Calculate the effective address by subtracting the register content of the ALU

Question **8**

Correct

Mark 1.00 out of 1.00

Which one of the following most profoundly describes the functionality of the control unit in CPU?

- a. To generate the control signals based on decoded program instructions
- b. To store program instruction
- c. To perform the arithmetic operations based on decoded program instruction
- d. To perform logic operations based on decoded program instructions



Your answer is correct.

The correct answer is:

To generate the control signals based on decoded program instructions

Question **9**

Correct

Mark 1.00 out of 1.00

An instruction cycle refers to which one of the following?

- a. Fetching an instruction
- b. Executing an instruction
- c. All of the mentioned
- d. Decoding the instruction and calculation of effective address



Your answer is correct.

The correct answer is:

All of the mentioned

Question **10**

Correct

Mark 1.00 out of 1.00

A booth's multiplier circuit needs to inspect at most how many LSB bits to determine whether to add the multiplier, subtract the multiplier or leave the partial result unchanged during any step in the sequence of multiplication steps?

- a. All bits of the multiplier
- b. All bits of the multipicand
- c. One bit
- d. Two bits



Your answer is correct.

The correct answer is:

One bit

Question 11

Incorrect

Mark 0.00 out of 1.00

Throughput is calculated as

- a. Total time to complete the instructions/number of instructions
- b. Speed of the processor/ Number of instructions ✗
- c. The number of instructions/ Total time to complete the instructions
- d. The number of instructions/speed of the processor

Your answer is incorrect.

The correct answer is:

Total time to complete the instructions/number of instructions

Question 12

Incorrect

Mark 0.00 out of 1.00

Parallelism can be achieved by-----technique.

- a. Compiler
- b. Software
- c. All of the above ✗
- d. Hardware

Your answer is incorrect.

The correct answer is:

Hardware

Question **13**

Correct

Mark 1.00 out of 1.00

The features of the RISC processor --

- a. Small number of addressing modes
- b. Small number of the instructions
- c. Instruction execute in one or two clock cycle
- d. All of the mentioned



Your answer is correct.

The correct answer is:

All of the mentioned

Question **14**

Correct

Mark 1.00 out of 1.00

If multiplicand (M) is 0111, the AC register is initialized with zero. What will be the content of the AC register after operation $AC = AC - M$?

- a. 1001
- b. 1100
- c. 1010
- d. 1111



Your answer is correct.

The correct answer is:

1001

Question 15

Correct

Mark 1.00 out of 1.00

Addressing modes are used to calculate the effective address by using the --

- a. ALU unit only
- b. ALU + control unit ✓
- c. Control Unit
- d. DMA

Your answer is correct.

The correct answer is:

ALU + control unit

Question 16

Incorrect

Mark 0.00 out of 1.00

Pipelining is a -----technique?

- a. Superscalar operation ✗
- b. Parallel operation
- c. Scalar operation
- d. Serial operation

Your answer is incorrect.

The correct answer is:

Serial operation

Question **17**

Correct

Mark 1.00 out of 1.00

In the MIPS architecture, data transfer takes place between --

- a. Register to register
- b. All of the mentioned
- c. Register to memory
- d. Memory to register



Your answer is correct.

The correct answer is:

All the mentioned

Question **18**

Correct

Mark 1.00 out of 1.00

In which one of the following addressing modes, the content of the program counter is added to the address part of the instruction in order to obtain the effective address.

- a. Indexed addressing mode
- b. Register addressing mode
- c. Register indirect addressing mode
- d. Absolute addressing mode



Your answer is correct.

The correct answer is:

Register indirect addressing mode

Question **19**

Correct

Mark 1.00 out of 1.00

Forwarding can be implemented in 5-stage and 6-stage MIPS pipeline --

- a. Using one multiplexer
- b. Using three multiplexers
- c. Using two multiplexers with extra latch
- d. Using two multiplexers



Your answer is correct.

The correct answer is:

Using two multiplexers

Question **20**

Correct

Mark 1.00 out of 1.00

Von Neumann computers helping to which one of the following classes of computers?

- a. SISD
- b. MIMD
- c. MISD
- d. SIMD



Your answer is correct.

The correct answer is:

SISD

Question 21

Correct

Mark 1.00 out of 1.00

The stages of 3 stage pipelining are----?

- a. Fetch, Decode, Execute
- b. Execute, Fetch, Decode
- c. Address generation, Fetch, Execute.
- d. Decode, Fetch, Execute



Your answer is correct.

The correct answer is:

Fetch, Decode, Execute

Question 22

Correct

Mark 1.00 out of 1.00

When the data operands are not available then it is called----?

- a. Deadlock
- b. Data hazard
- c. Pop
- d. Push



Your answer is correct.

The correct answer is:

Data hazard

Question **23**

Correct

Mark 1.00 out of 1.00

Instruction pipeline improves the CPU performance due to which one of the following reasons?

- a. Use a larger Cache
- b. Use of additional functional units
- c. Efficient utilization of the processor hardware ✓
- d. Reduced memory access time

Your answer is correct.

The correct answer is:

Efficient utilization of the processor hardware

Question **24**

Correct

Mark 1.00 out of 1.00

A pipelined processor has seven stages, namely, IF1, IF2, ID, EX, MEM1, MEM2, WB. Assuming all the stages require the same amount of time and the time period of the non- pipelined processors is 14 ns, find out the clock frequency and speedup of the pipelined processor. Assume the delay of the latches is 1 ns.

- a. 1 KHz and 3
- b. None of the mentioned ✓
- c. 1Khz and 50
- d. 1.2 KHz and 30

Your answer is correct.

The correct answer is:

None of the mentioned

Question **25**

Correct

Mark 1.00 out of 1.00

In pipelining, which of the following operation is used to enhance the memory access speed?

- a. Queue
- b. Cache
- c. Registers
- d. Stack



Your answer is correct.

The correct answer is:

Cache

Question **26**

Correct

Mark 1.00 out of 1.00

The following lines of code $IR \leq \text{Memory}[PC]$; $PC \leq PC + 4$; explains the

- a. None of them
- b. Instruction Decode Step
- c. Instruction Fetch Step
- d. Instruction Execute Step



Your answer is correct.

The correct answer is:

Instruction Fetch Step

Question **27**

Correct

Mark 1.00 out of 1.00

A four-stage pipeline has stage delays of 150, 120, 160, and 140 ns respectively. Registers are used between the stages and have a delay of 10 ns each. What is the cycle time?

- a. 155 ns
- b. 140 ns
- c. 165 ns
- d. 170 ns



Your answer is correct.

The correct answer is:

170 ns

Question **28**

Incorrect

Mark 0.00 out of 1.00

Overcoming control dependence is done by ____ on the outcome of branches?

- a. None of the mentioned
- b. speculating
- c. Out of order scheme
- d. Scoreboard



Your answer is incorrect.

The correct answer is:

speculating

Question **29**

Correct

Mark 1.00 out of 1.00

Consider a three address RISC processor ISA. Which one of the following correctly characterizes an effect of doubling the number of registers in the processor?

- a. Instruction size would be increase by 1-bit
- b. Instruction size would be increase by 2-bit
- c. Instruction size would be unaffected
- d. Instruction size would be increase by 3-bit



Your answer is correct.

The correct answer is:

Instruction size would be increase by 3-bit

Question **30**

Correct

Mark 1.00 out of 1.00

A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The number of and gates required to design full adders are?

- a. Eight
- b. Nine
- c. Twelve
- d. Ten



Your answer is correct.

The correct answer is:

Nine

Question **31**

Correct

Mark 1.00 out of 1.00

For calculating the effective address, the upper 6 bits and concatenation done between---

- a. Program counter and constant value which was the part of the instruction
- b. Address register and constant value which was not the part of the instruction
- c. Program counter and constant value which was not the part of the instruction
- d. Address register and constant value which was the part of the instruction



Your answer is correct.

The correct answer is:

Program counter and constant value which was the part of the instruction

Question **32**

Correct

Mark 1.00 out of 1.00

The instruction $Z=X+Y$; needs to be run on accumulator-based architecture. Choose the current option.

- a. One operand is available in DMA
- b. Both operands are available in the register bank
- c. One operand is available in the accumulator and other need to be fetched from memory
- d. Both operands are available in the accumulator



Your answer is correct.

The correct answer is:

One operand is available in the accumulator and other need to be fetched from memory

Question **33**

Incorrect

Mark 0.00 out of 1.00

ARM processors are available in the form of ----- pipelining?

- a. None of them
- b. 3 stage ✗
- c. Both 3 and 5 stages
- d. 5 stage

Your answer is incorrect.

The correct answer is:

Both 3 and 5 stages

Question **34**

Correct

Mark 1.00 out of 1.00

In a pipelined processor, the processing units for integers and floating point is-----?

- a. Separate unit. ✓
- b. Within each other.
- c. Same unit.
- d. No unit.

Your answer is correct.

The correct answer is:

Separate unit.

Question **35**

Correct

Mark 1.00 out of 1.00

Forwarding can be implemented in 5-stage and 6-stage MIPS pipeline --

- a. Using two multiplexers ✓
- b. Using one multiplexer
- c. Using three multiplexers
- d. Using two multiplexers with extra latch

Your answer is correct.

The correct answer is:

Using two multiplexers

Question **36**

Correct

Mark 1.00 out of 1.00

What is the arithmetic shift right operation after the 1st cycle for the following binary stream 1 0 0 1 0 0 1 1 0 ?

- a. 1 1 0 0 1 0 0 1 1 ✓
- b. 1 0 0 1 0 0 1 1 0
- c. 1 1 1 0 0 1 0 0 1
- d. 0 1 1 0 0 1 0 0 1

Your answer is correct.

The correct answer is:

1 1 0 0 1 0 0 1 1

Question **37**

Correct

Mark 1.00 out of 1.00

Out-of-order execution introduces the possibility of ____ hazards.

- a. RAR and WAR
- b. WAR and WAW ✓
- c. WAR and RAW
- d. RAW and RAR

Your answer is correct.

The correct answer is:

WAR and WAW

Question **38**

Correct

Mark 1.00 out of 1.00

Consider the following instruction sequence five-stage pipeline,

ADD R1, R2, R1 --- I1

LW R2,0(R1) --- I2

LW R1,4(R1) -- I3

OR R3, R1, R2 -- I4

Select the correct option.

- a. RAW hazards is present in instructions I3-I4
- b. All of the mentioned ✓
- c. RAW hazards is present in instructions I1-I2
- d. RAW hazards is present in instructions I2-I3

Your answer is correct.

The correct answer is:

All of the mentioned

Question **39**

Correct

Mark 1.00 out of 1.00

A computer has a word size of 16-bit and has 16 programmer visible registers. each instruction has two sources and one destination operands and uses only register direct addressing mode. what is the maximum number of op-codes that this processor can have?

- a. 8
- b. 16 ✓
- c. 64
- d. 32

Your answer is correct.

The correct answer is:

16

Question **40**

Correct

Mark 1.00 out of 1.00

Which of the following instruction is not used for changing state....?

- a. nop ✓
- b. nope
- c. no-op
- d. no

Your answer is correct.

The correct answer is:

nop

Question 41

Correct

Mark 1.00 out of 1.00

For the load and store operation ---

- a. Effective address is calculated at 4th stage of the pipeline
- b. Effective address is calculated between 4th and 5th stage of the pipeline
- c. Effective address is calculated between 3rd and 4th stage of the pipeline
- d. Effective address is calculated at 3rd stage of the pipeline



Your answer is correct.

The correct answer is:

Effective address is calculated at 3rd stage of the pipeline

Question 42

Correct

Mark 1.00 out of 1.00

The following assembly program is run over the MIPS pipeline architecture. Choose the wrong option.

Assembly code:

```
i1. pp1: LD F0,0(R1);  
i2. ADD.D F4,F0,F2;  
i3. S.D F4,0(R1);  
i4. DADDUI R1,R1,#-8;  
i5. BNE R1,R2,pp1
```

- a. i1 is used for array element
- b. i3 is used to store the results
- c. i2 is used for adding scalar value
- d. i4 is used as an increment pointer



Your answer is correct.

The correct answers are:

i1 is used for array element,

i4 is used as an increment pointer

Question **43**

Correct

Mark 1.00 out of 1.00

By using pipelining, the latency of the instructions---?

- a. It is unity
- b. Increases
- c. Decreases
- d. Remains the same



Your answer is correct.

The correct answer is:

Decreases

Question **44**

Correct

Mark 1.00 out of 1.00

In pipelined processor, the WB stage in instruction execution isstage?

- a. Seventh
- b. Fifth
- c. First
- d. Third



Your answer is correct.

The correct answer is:

Fifth

Question **45**

Correct

Mark 1.00 out of 1.00

Pipelining of a MIPS-like Processor, select the right option

- a. All of the mentioned ✓
- b. All ALU operations are performed on register operands
- c. Only instructions which access memory are load and store instructions
- d. Separate Instruction and data memory is required

Your answer is correct.

The correct answer is:

All of the mentioned

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[CS-208-Assignment-3_06-04-2022 ►](#)

Started on Wednesday, 23 February 2022, 12:10 PM

State Finished

Completed on Wednesday, 23 February 2022, 12:15 PM

Time taken 4 mins 56 secs

Marks 2.00/5.00

Grade 4.00 out of 10.00 (40%)

Question 1

Incorrect

Mark 0.00 out of 1.00

For the given code select the correct option.

Code:

Load R1, A

Load R2, B

Add R3, R1, R2

Store C, R3

- a. Register to register based MIPS processor
- b. Accumulator based MIPS Processor
- c. Memory to register based MIPS processor
- d. Register to Memory based MIPS processor



Your answer is incorrect.

The correct answer is:

Register to register based MIPS processor

Question 2

Correct

Mark 1.00 out of 1.00

For the instructions Load R1, 0(R2). Choose the correct option.

- a. All of the mentioned
- b. Effective address will be the addition of 0 and content of R2
- c. Effective address is calculated by the ALU
- d. From the memory 0+R2's location content will loaded into the destination register



Your answer is correct.

The correct answer is:

All of the mentioned

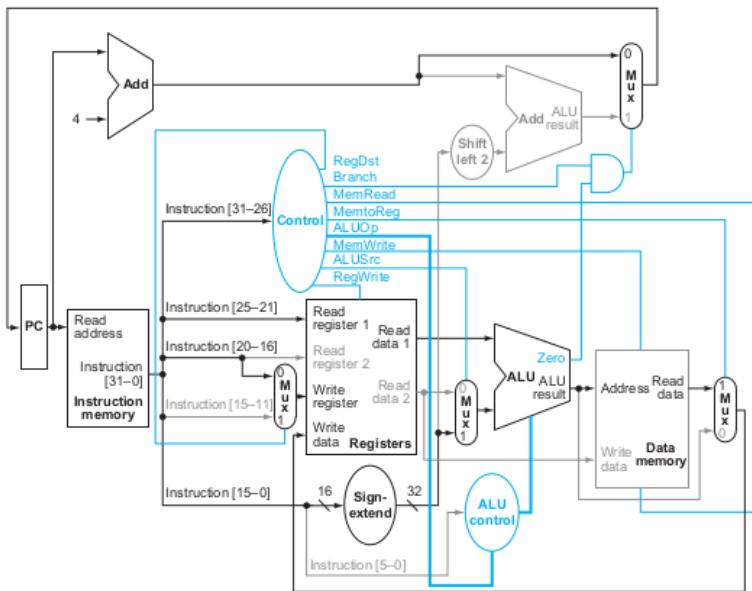


Question 3

Incorrect

Mark 0.00 out of 1.00

Which type of datapath architecture is given in the following ?



- a. R-type of instruction
- b. J-type instruction
- c. With Load instruction
- d. Branch on equal instruction ✖

Your answer is incorrect.

The correct answer is:

With Load instruction

Question 4

Correct

Mark 1.00 out of 1.00

ALU to support the MIPS instruction should have ?

- a. All of the mentioned ✓
- b. Subtraction using two's complement
- c. Replica of 1-bit ALU to produce a 32-bit ALU
- d. Multiplexor to select the output we want

Your answer is correct.

The correct answer is:

All of the mentioned



Question 5

Incorrect

Mark 0.00 out of 1.00

for Pseudo-direct Addressing. Select the correct option.

- a. Address is 26 bits of constant within instruction concatenated with lower 6 bits of PC
- b. Address is 26 bits of constant within instruction concatenated with upper 6 bits of PC
- c. Address is 26 bits of constant within instruction concatenated with upper 6 bits of Instruction register ✖
- d. Address is 26 bits of constant within instruction concatenated with lower 6 bits of Instruction register

Your answer is incorrect.

The correct answer is:

Address is 26 bits of constant within instruction concatenated with upper 6 bits of PC

[◀ CS-208-Assignment-2_02-03-2022](#)

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[CS-208 MidSem Online Test-11-03-2022 ►](#)



Started on Wednesday, 2 March 2022, 12:10 PM

State Finished

Completed on Wednesday, 2 March 2022, 12:15 PM

Time taken 4 mins 58 secs

Marks 4.00/7.00

Grade 5.71 out of 10.00 (57%)

Question 1

Correct

Mark 1.00 out of 1.00

Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 5 ns. What is the Pipeline cycle time?

- a. 100 ns
- b. 105 ns
- c. 75 ns
- d. 95 ns



Your answer is correct.

The correct answer is:

95 ns

Question 2

Incorrect

Mark 0.00 out of 1.00

In MIPS architecture, increasing the number of stages --

- a. Will always decrease the performance.
- b. Will always improve the performance after the optimal value of the stages
- c. Will improve the performance up to optimal value of the stages and beyond the optimal value it will decrease
- d. Will always improve the performance.



Your answer is incorrect.

The correct answers are:

Will always decrease the performance.,

Will improve the performance up to optimal value of the stages and beyond the optimal value it will decrease

Question 3

Incorrect

Mark 0.00 out of 1.00

For the code given below choose the wrong answer.

MIPS Code:

1. ADD r1, r2, r3
2. SUB r4, r1, r5
3. AND r6, r1, r7
4. OR r8, r1, r9
5. XOR r10, r1, r11

- a. Using split phase of the clock, data hazard can be eliminated from instruction no. fourth
- b. Using split phase of the clock, data hazard can be eliminated from instruction no. fifth ✗
- c. Using split phase of the clock, data hazard can be eliminated from instruction no. second
- d. Direct data dependence is there

Your answer is incorrect.

The correct answer is:

Using split phase of the clock, data hazard can be eliminated from instruction no. second

Question 4

Correct

Mark 1.00 out of 1.00

For the code given below. Select the right option.

```
if p1 {  
    S1;  
}  
if p2 {  
    S2;  
}
```

- a. S1 is control dependent on p1, but S2 is not control dependent on p1
- b. All of the mentioned ✓
- c. S2 cannot be moved after the branch
- d. S1 cannot be moved before the branch

Your answer is correct.

The correct answers are: S1 is control dependent on p1, but S2 is not control dependent on p1, S1 cannot be moved before the branch, All of the mentioned

Question 5

Incorrect

Mark 0.00 out of 1.00

DIV.D F0,F2,F4
ADD.D F6,F0,F8
S.D F6,0(R1)
SUB.D F8,F10,F14
MUL.D F6,F10,F8

How many possible hazards are available in the above-given code?

- a. 2
- b. 5
- c. 4
- d. 3



Your answer is incorrect.

The correct answer is:

3

Question 6

Correct

Mark 1.00 out of 1.00

Which one of the following about the MIPS rating of a computer is FALSE?

- a. None of the mentioned
- b. MIPS rating of a processor is independent of the program is being executed.
- c. MIPS rating of computer depends on the computer being used
- d. MIPS rating of a computer can very based on which instruction of a processor are being considered



Your answer is correct.

The correct answer is:

MIPS rating of a processor is independent of the program is being executed.

Question **7**

Correct

Mark 1.00 out of 1.00

The processor speed has been increased over the last five decades due the --

- a. Krammar's Law
- b. Moore's Law ✓
- c. Charl's law
- d. Newton's law

Your answer is correct.

The correct answer is: Moore's Law

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[CS-208-Assignment-1_23-02-2022 ►](#)

Started on Wednesday, 6 April 2022, 12:10 PM

State Finished

Completed on Wednesday, 6 April 2022, 12:15 PM

Time taken 4 mins 52 secs

Marks 1.00/4.00

Grade **2.50** out of 10.00 (**25%**)

Question **1**

Complete

Mark 1.00 out of 1.00

For the Software Pipelining, select the correct option.

- a. unroll loop body with an unroll factor of n
- b. All of the mentioned
- c. select order of instructions from different iterations to pipeline
- d. "paste" instructions from different iterations into the new pipelined loop body

Question **2**

Complete

Mark 0.00 out of 1.00

Dynamic pipeline scheduling chooses which instructions to execute next, possibly reordering them to avoid stalls?

- a. **Dynamic branch prediction**
- b. **Dynamic pipeline**
- c. **Prediction branch**
- d. **Branch prediction**

Question 3

Complete

Mark 0.00 out of 1.00

Consider the following code:

CODE:

Load R1,Loc1; Load R1 from memory location Loc1

Load R2,Loc2; Load R2 from memory location Loc2

Add R1,R2,R1; Add R1 and R2 and save result in R1

Dec R2; Decrement R2

Dec R1; Decrement R1

Mpy R1,R2,R3; Multiply R1 and R2 and store in R3

Store R3, Loc3; Store r3 in Memory Location Loc3

What is the number of cycles needed to execute the above code assuming each instruction takes one cycle to execute?

- a. 5
- b. 9
- c. 7
- d. 10

Question 4

Complete

Mark 0.00 out of 1.00

For Dynamic Scheduling, select the correct option.

- a. The software determines the order in which instructions execute
- b. The DMA determines the order in which instructions execute
- c. None of the mentioned
- d. The hardware determines the order in which instructions execute

[◀ CS-208 MidSem Online Test-11-03-2022](#)

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[CS-208-Assignment-4_13-04-2022 ►](#)

Started on Wednesday, 13 April 2022, 12:10 PM

State Finished

Completed on Wednesday, 13 April 2022, 12:15 PM

Time taken 4 mins 45 secs

Marks 2.00/4.00

Grade 5.00 out of 10.00 (50%)

Question 1

Correct

Mark 1.00 out of 1.00

Which of the following processor uses primarily static in nature?

- a. Superscalar(speculative)
- b. Superscalar(static)
- c. EPIC
- d. Superscalar(dynamic)



Your answer is correct.

The correct answer is:

EPIC

Question 2

Incorrect

Mark 0.00 out of 1.00

Which of the following processor uses static in nature?

- a. Superscalar(dynamic)
- b. Superscalar(static)
- c. VLIW/LIW
- d. Superscalar(speculative)



Your answer is incorrect.

The correct answer is:

VLIW/LIW

Question 3

Incorrect

Mark 0.00 out of 1.00

Which of the following processor uses Dynamic in nature

- a. Superscalar(dynamic) ✗
- b. Superscalar(speculative)
- c. Superscalar(static)
- d. All of the mentioned

Your answer is incorrect.

The correct answer is:

All of the mentioned

Question 4

Correct

Mark 1.00 out of 1.00

The tightly coupled set of thread execution working on a single task is as?

- a. Multithread
- b. Multiprocess
- c. Parallel Processing ✓
- d. Serial Processing

Your answer is correct.

The correct answer is:

Parallel Processing

◀ CS-208-Assignment-3_06-04-2022

Jump to...

CS-208-Assignment-5_20-04-2022 ►

Started on Wednesday, 20 April 2022, 12:10 PM

State Finished

Completed on Wednesday, 20 April 2022, 12:15 PM

Time taken 4 mins 34 secs

Marks 4.00/5.00

Grade 8.00 out of 10.00 (80%)

Question 1

Correct

Mark 1.00 out of 1.00

Making Address Translation Faster, Choose the correct option.

- a. Each memory access requires two memory reads
- b. The page tables are stored in the main memory
- c. A special address translation cache called Translation Lookaside is required
- d. All of the mentioned



Your answer is correct.

The correct answer is:

All of the mentioned

Question 2

Correct

Mark 1.00 out of 1.00

For virtual memory address translation, select the correct option.

- a. Hardware converts virtual addresses to virtual addresses and OS-managed lookup table
- b. Hardware converts physical addresses to virtual addresses and OS-managed lookup table
- c. Hardware converts virtual addresses to physical addresses and OS-managed lookup table
- d. None of the mentioned



Your answer is correct.

The correct answer is:

Hardware converts virtual addresses to physical addresses and OS-managed lookup table

Question **3**

Incorrect

Mark 0.00 out of 1.00

What is miss penalty for the parameters given below.

1. One clock to send the address.
2. 10 clocks for each DRAM access.
3. 1 clock for send the memory word to CACHE from DRAM.
4. CACHE width is 4W and DRAM width is 1W

- a. 45 Clock Cycles
- b. 44 Clock Cycles
- c. None of the mentioned
- d. 46 Clock Cycles ✗

Your answer is incorrect.

The correct answer is:

45 Clock Cycles

Question **4**

Correct

Mark 1.00 out of 1.00

For 32 bit data/4 blocks, 32 bit address is given for the CACHE of 32 KB(data part only). Calculate the size of the CACHE?

- a. 316 KB
- b. 314 KB ✓
- c. 314 B
- d. None of the mentioned

Your answer is correct.

The correct answer is:

314 KB

Question 5

Correct

Mark 1.00 out of 1.00

For the Virtual Memory Design Issues, select the right option.

- a. All of the mentioned ✓
- b. Write through approach cannot be used
- c. Page size should be large enough to try to amortize the high access time
- d. Page faults need not be handled by hardware

Your answer is correct.

The correct answer is:

All of the mentioned

[◀ CS-208-Assignment-4_13-04-2022](#)

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Started on	Tuesday, 2 February 2021, 10:20 AM
State	Finished
Completed on	Tuesday, 2 February 2021, 11:00 AM
Time taken	40 mins 35 secs
Marks	24.00/35.00
Grade	6.86 out of 10.00 (69%)

Question 1

Incorrect

Mark 0.00 out of 1.00

A four-stage pipeline has stage delays of 150, 120, 160, and 140 ns respectively. Registers are used between the stages and have a delay of 10 ns each. What is the cycle time?

- a. 155 ns
- b. 140 ns
- c. 170 ns
- d. 165 ns



Your answer is incorrect.

The correct answer is:

170 ns

Question **2**

Correct

Mark 1.00 out of 1.00

In MIPS architecture, the program counter send the address multiple of 4 due to --

- a. Nibble addressability of memory
- b. Bit addressability of memory
- c. Word addressability of memory
- d. Byte addressability of memory



Your answer is correct.

The correct answer is:

Byte addressability of memory

Question **3**

Incorrect

Mark 0.00 out of 1.00

Addressing modes are used to calculate the effective address by using the --

- a. ALU + control unit
- b. Control Unit
- c. DMA
- d. ALU unit only



Your answer is incorrect.

The correct answer is:

ALU + control unit

Question **4**

Correct

Mark 1.00 out of 1.00

Pipelining of a MIPS-like Processor, select the right option

- a. Separate Instruction and data memory is required ✖
- b. All ALU operations are performed on register operands
- c. All of the mentioned
- d. Only instructions which access memory are load and store instructions

Your answer is correct.

The correct answer is:

All of the mentioned

Question 5

Correct

Mark 1.00 out of 1.00

For the code given below. Select the right option.

```
if p1 {  
    S1;  
}  
if p2 {  
    S2;  
}
```

- a. All of the mentioned
- b. S2 cannot be moved after the branch
- c. S1 cannot be moved before the branch
- d. S1 is control dependent on p1, but S2 is not control dependent on p1



Your answer is correct.

The correct answers are: S1 is control dependent on p1, but S2 is not control dependent on p1, S1 cannot be moved before the branch,
All of the mentioned

Question **6**

Correct

Mark 1.00 out of 1.00

What is the two times shift right of the binary stream 0 1 0 1 1 1 1 0 1?

- a. None of the mentioned
- b. 0 1 0 1 1 1 1 0 0
- c. 0 0 0 1 0 1 1 1 1
- d. 0 1 0 1 1 1 1 0 1



Your answer is correct.

The correct answer is:

0 0 0 1 0 1 1 1 1

Question **7**

Correct

Mark 1.00 out of 1.00

CACHE memory act as an interface between---

- a. Processor hardware and main memory
- b. Processor hardware and I/O



Your answer is correct.

The correct answer is:

Processor hardware and main memory

Question 8

Correct

Mark 1.00 out of 1.00

In the MIPS architecture, data transfer takes place between --

- a. Register to register
- b. Memory to register
- c. Register to memory
- d. All of the mentioned



Your answer is correct.

The correct answer is:

All of the mentioned

Question **9**

Correct

Mark 1.00 out of 1.00

In the MIPS pipeline architecture forwarding/bypassing is ----

- a. Hardware based approach
- b. DMA based approach
- c. Software based approach
- d. Combination of both hardware & software based approach



Your answer is correct.

The correct answer is:

Hardware based approach

Question 10

Incorrect

Mark 0.00 out of 1.00

The zero flag register of the MIPS pipeline architecture--

- a. Calculate the effective address by subtracting the register content of the ALU
- b. Calculate the effective address by using the instruction register content
- c. Calculate the effective address by adding the register content of the ALU ✖
- d. Calculate the effective address by using the program counter register content

Your answer is incorrect.

The correct answer is:

Calculate the effective address by subtracting the register content of the ALU

Question **11**

Correct

Mark 1.00 out of 1.00

For the code given below, select the wrong answer.

MIPS Code:

1. add r1, r2, r3
2. sub r4, r1, r5

- a. Data hazard is present
- b. For the second instruction, operands are required at 3rd stage of the pipeline
- c. There will be no hazard for the first instruction
- d. One stalls is required to remove the data hazard



Your answer is correct.

The correct answer is:

One stalls is required to remove the data hazard

Question **12**

Correct

Mark 1.00 out of 1.00

Using booth's algorithms multiply 7 with 3 and assume register AC is 4 bit. The value of AC after 3rd and 4th cycles are

- a. 1 0 1 0 and 1 0 1 0
- b. 0 0 1 0 and 1 0 1 0
- c. 0 0 1 1 and 1 0 1 1
- d. 0 1 1 1 0 and 1 0 1 0 0



Your answer is correct.

The correct answer is:

0 0 1 0 and 1 0 1 0

Question 13

Incorrect

Mark 0.00 out of 1.00

For the program given below the number of stalls required after the code transformed by the smart compiler are

MIPS Code:

1. LW R2, 0(R4)
2. LW R5, 4(R4)
3. ADD R1, R2, R3

- a. One
- b. Two
- c. Three
- d. No stall is required



Your answer is incorrect.

The correct answer is:

No stall is required

Question **14**

Correct

Mark 1.00 out of 1.00

The shortfall of registers created by aggressive unrolling and scheduling is also known as --

- a. Miss rate
- b. Forwarding ✖
- c. Aggressive scaling
- d. Register pressure

Your answer is correct.

The correct answer is:

Register pressure

Question **15**

Incorrect

Mark 0.00 out of 1.00

During 1 clock cycle, the pipeline (5-stage) can process --

- a. 4 different instructions
- b. 5 different instructions
- c. None of the mentioned
- d. 6 different instructions

✖

Your answer is incorrect.

The correct answer is:

5 different instructions

Question **16**

Correct

Mark 1.00 out of 1.00

Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 5 ns. What is the Pipeline cycle time?

- a. 95 ns
- b. 105 ns
- c. 75 ns
- d. 100 ns



Your answer is correct.

The correct answer is:

95 ns

Question **17**

Correct

Mark 1.00 out of 1.00

For the code given below choose the wrong answer.

MIPS Code:

1. ADD r1, r2, r3
2. SUB r4, r1, r5
3. AND r6, r1, r7
4. OR r8, r1, r9
5. XOR r10, r1, r11

- a. Using split phase of the clock, data hazard can be eliminated from instruction no. fifth
- b. Using split phase of the clock, data hazard can be eliminated from instruction no. fourth
- c. Direct data dependence is there
- d. Using split phase of the clock, data hazard can be eliminated from instruction no. second



Your answer is correct.

The correct answer is:

Using split phase of the clock, data hazard can be eliminated from instruction no. second

Question **18**

Incorrect

Mark 0.00 out of 1.00

What is the arithmetic shift right operation after the 1st cycle for the following binary stream 1 0 0 1 0 0 1 1 0 ?

- a. 0 1 1 0 0 1 0 0 1
- b. 1 1 0 0 1 0 0 1 1
- c. 1 0 0 1 0 0 1 1 0
- d. 1 1 1 0 0 1 0 0 1

✖

Your answer is incorrect.

The correct answer is:

1 1 0 0 1 0 0 1 1

Question **19**

Correct

Mark 1.00 out of 1.00

What is the shift right of the binary stream 0 1 0 1 1 1 1 0 1?

- a. 0 0 1 0 1 1 0 1
- b. 0 0 1 0 1 1 1 1
- c. 1 0 1 0 1 1 1 0
- d. 0 0 1 0 1 1 1 1 0



Your answer is correct.

The correct answer is:

0 0 1 0 1 1 1 0

Question 20

Incorrect

Mark 0.00 out of 1.00

In MIPS architecture, increasing the number of stages --

- a. Will improve the performance up to optimal value of the stages and beyond the optimal value it will decrease ✓
- b. Will always improve the performance.
- c. Will always decrease the performance.
- d. Will always improve the performance after the optimal value of the stages

Your answer is incorrect.

The correct answers are:

Will always decrease the performance.,

Will improve the performance up to optimal value of the stages and beyond the optimal value it will decrease

Question **21**

Incorrect

Mark 0.00 out of 1.00

A pipelined processor has seven stages, namely, IF1, IF2, ID, EX, MEM1, MEM2, WB. Assuming all the stages require the same amount of time and the time period of the non- pipelined processors is 14 ns, find out the clock frequency and speedup of the pipelined processor. Assume the delay of the latches is 1 ns.

- a. 1Khz and 50
- b. 1 Khz and 3
- c. None of the mentioned
- d. 1.2 Khz and 30

✖

Your answer is incorrect.

The correct answer is:

None of the mentioned

Question **22**

Correct

Mark 1.00 out of 1.00

In the J-type instructions of MIPS --

- a. One operand is provided as a part of the instruction and other operand need to be get from accumulator
- b. Both the operands are available in the register bank ✓
- c. Both operands are not available in the register bank
- d. One operand is provided as a part of the instruction and other operand need to be fetched from memory

Your answer is correct.

The correct answers are:

Both the operands are available in the register bank,

One operand is provided as a part of the instruction and other operand need to be fetched from memory

Question **23**

Incorrect

Mark 0.00 out of 1.00

The features of the RISC processor --

- a. All of the mentioned
- b. Instruction execute in one or two clock cycle
- c. Small number of the instructions
- d. Small number of addressing modes

✗

Your answer is incorrect.

The correct answer is:

All of the mentioned

Question **24**

Correct

Mark 1.00 out of 1.00

Which unit is responsible for directing the operations of computer arithmetic and logical unit?

- a. I/O interface
- b. ALU itself ✖
- c. Control unit
- d. Program

Your answer is correct.

The correct answer is:

Control unit

Question **25**

Correct

Mark 1.00 out of 1.00

For the code given below identifies the data hazard.

Code:

add r1, r2, r3
sub r1, r4, r5

- a. WAR
- b. RAW
- c. None of the mentioned
- d. WAW



Your answer is correct.

The correct answer is:

WAW

Question **26**

Correct

Mark 1.00 out of 1.00

For the load and store operation ---

- a. Effective address is calculated at 4th stage of the pipeline
- b. Effective address is calculated between 4th and 5th stage of the pipeline
- c. Effective address is calculated at 3rd stage of the pipeline
- d. Effective address is calculated between 3rd and 4th stage of the pipeline

✗

Your answer is correct.

The correct answer is:

Effective address is calculated at 3rd stage of the pipeline

Question **27**

Incorrect

Mark 0.00 out of 1.00

Consider the following instruction sequence five-stage pipeline,

ADD R1, R2, R1 --- I1

LW R2,0(R1) --- I2

LW R1,4(R1) -- I3

OR R3, R1, R2 -- I4

Select the correct option.

- a. RAW hazards is present in instructions I1-I2
- b. All of the mentioned
- c. RAW hazards is present in instructions I2-I3
- d. RAW hazards is present in instructions I3-I4

✖

Your answer is incorrect.

The correct answer is:

All of the mentioned

Question **28**

Correct

Mark 1.00 out of 1.00

In the MIPS architecture, the meaning of the instruction can be found from --

- a. Accumulator register
- b. Address register
- c. Instruction register
- d. Program counter register



Your answer is correct.

The correct answer is:

Instruction register

Question **29**

Correct

Mark 1.00 out of 1.00

If multiplicand (M) is 0111, the AC register is initialized with zero. What will be the content of the AC register after operation $AC = AC - M$?

- a. 1100
- b. 1111
- c. 1010
- d. 1001



Your answer is correct.

The correct answer is:

1001

Question **30**

Correct

Mark 1.00 out of 1.00

Forwarding can be implemented in 5-stage and 6-stage MIPS pipeline --

- a. Using two multiplexers with extra latch
- b. Using one multiplexer
- c. Using two multiplexers
- d. Using three multiplexers



Your answer is correct.

The correct answer is:

Using two multiplexers

Question 31

Incorrect

Mark 0.00 out of 1.00

The instruction ADD Rd,Rs, Rt is ---

- a. I-type instruction of MIPS
- b. P-type instruction of MIPS
- c. J-type instruction of MIPS
- d. R-type instruction of MIPS



Your answer is incorrect.

The correct answer is:

R-type instruction of MIPS

Question **32**

Correct

Mark 1.00 out of 1.00

The following assembly program is run over the MIPS pipeline architecture. Choose the wrong option.

Assembly code:

i1. `pp1: L.D F0,0(R1);`
i2. `ADD.D F4,F0,F2;`
i3. `S.D F4,0(R1);`
i4. `DADDUI R1,R1,#-8;`
i5. `BNE R1,R2,pp1`

- a. i4 is used as an increment pointer
- b. i3 is used to store the results
- c. i1 is used for array element
- d. i2 is used for adding scalar value



Your answer is correct.

The correct answers are:

i1 is used for array element,

i4 is used as an increment pointer

Question **33**

Correct

Mark 1.00 out of 1.00

in loop Unrolling with Scheduling---. Select the right option.

- a. All of the mentioned
- b. Determine the loads and stores that can be interchanged in the unrolled loop
- c. Use different registers to avoid unnecessary constraints
- d. Identify that loop iterations are independent

✗

Your answer is correct.

The correct answer is:

All of the mentioned

Question **34**

Correct

Mark 1.00 out of 1.00

For calculating the effective address, the upper 6 bits and concatenation done between---

- a. Address register and constant value which was not the part of the instruction
- b. Program counter and constant value which was not the part of the instruction
- c. Program counter and constant value which was the part of the instruction
- d. Address register and constant value which was the part of the instruction



Your answer is correct.

The correct answer is:

Program counter and constant value which was the part of the instruction

Question **35**

Correct

Mark 1.00 out of 1.00

A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The number of and gates required to design full adders are?

- a. Nine
- b. Twelve
- c. Eight
- d. Ten



Your answer is correct.

The correct answer is:

Nine

[◀ Announcements](#)

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[CS-208: Mid-Sem Online Test ▶](#)

Started on	Thursday, 22 April 2021, 1:00 PM
State	Finished
Completed on	Thursday, 22 April 2021, 1:07 PM
Time taken	6 mins 56 secs
Marks	5.00/7.00
Grade	7.14 out of 10.00 (71%)

Question 1

Correct

Mark 1.00 out of 1.00

The von Neumann bottleneck can be attributed to which one of the following?

- a. Mismatch between the speed of the secondary and primary storages
- b. Slow speed of input/output devices
- c. Low clock speeds
- d. Mismatch between the speed of the CPU and primary storages



Your answer is correct.

The correct answer is:

Mismatch between the speed of the CPU and primary storages

Question **2**

Correct

Mark 1.00 out of 1.00

In MIPS architecture, the program counter send the address multiple of 4 due to --

- a. Byte addressability of memory
- b. Word addressability of memory
- c. Bit addressability of memory
- d. Nibble addressability of memory



Your answer is correct.

The correct answer is:

Byte addressability of memory

Question 3

Correct

Mark 1.00 out of 1.00

Cache memory is?

- a. Interface between processor and main memory
- b. Interface between processor and DMA
- c. Interface between processor and virtual memory
- d. Interface between processor and SRAM



Your answer is correct.

The correct answer is:

Interface between processor and main memory

Question **4**

Correct

Mark 1.00 out of 1.00

For the load and store operation ---

- a. Effective address is calculated between 4th and 5th stage of the pipeline
- b. Effective address is calculated at 3rd stage of the pipeline
- c. Effective address is calculated at 4th stage of the pipeline
- d. Effective address is calculated between 3rd and 4th stage of the pipeline



Your answer is correct.

The correct answer is:

Effective address is calculated at 3rd stage of the pipeline

Question 5

Correct

Mark 1.00 out of 1.00

Which one of the following options most correctly lists the important parts of a Von Neumann computer?

- a. Memory, input/output units, and CPU
- b. Buses, memory, and input/output controllers
- c. Memory, CPU, buses, and printers
- d. Hard disks, buses, and CPU



Your answer is correct.

The correct answer is:

Memory, input/output units, and CPU

Question **6**

Incorrect

Mark 0.00 out of 1.00

Which one of the following about the MIPS rating of a computer is FALSE?

- a. MIPS rating of a computer can very based on which instruction of a processor are being considered
- b. MIPS rating of a processor is independent of the program is being executed.
- c. MIPS rating of computer depends on the computer being used
- d. None of the mentioned

✗

Your answer is incorrect.

The correct answer is:

MIPS rating of a processor is independent of the program is being executed.

Question **7**

Incorrect

Mark 0.00 out of 1.00

The zero flag register of the MIPS pipeline architecture--

- a. Calculate the effective address by adding the register content of the ALU ✖
- b. Calculate the effective address by using the program counter register content
- c. Calculate the effective address by using the instruction register content
- d. Calculate the effective address by subtracting the register content of the ALU

Your answer is incorrect.

The correct answer is:

Calculate the effective address by subtracting the register content of the ALU

◀ CS-208: Pre-End-Sem Online Test

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End Sem Exam (06-May-2021) ►

Started on	Friday, 26 March 2021, 1:35 PM
State	Finished
Completed on	Friday, 26 March 2021, 1:50 PM
Time taken	14 mins 54 secs
Marks	12.00/20.00
Grade	6.00 out of 10.00 (60%)

Question 1

Incorrect

Mark 0.00 out of 1.00

In which one of the following addressing modes, the content of the program counter is added to the address part of the instruction in order to obtain the effective address.

- a. Register indirect addressing mode
- b. Register addressing mode
- c. Absolute addressing mode
- d. Indexed addressing mode

✗

Your answer is incorrect.

The correct answer is:

Register indirect addressing mode

Question **2**

Correct

Mark 1.00 out of 1.00

An instruction cycle refers to which one of the following?

- a. Executing an instruction
- b. Fetching an instruction
- c. Decoding the instruction and calculation of effective address
- d. All of the mentioned



Your answer is correct.

The correct answer is:

All of the mentioned

Question **3**

Correct

Mark 1.00 out of 1.00

Which one of the following most profoundly describes the functionality of the control unit in CPU?

- a. To store program instruction
- b. To perform the arithmetic operations based on decoded program instruction
- c. To generate the control signals based on decoded program instructions
- d. To perform logic operations based on decoded program instructions



Your answer is correct.

The correct answer is:

To generate the control signals based on decoded program instructions

Question **4**

Incorrect

Mark 0.00 out of 1.00

Which one of the following statements about a computer supporting unaligned data access is most accurate regarding the storage of data items having sizes that may not be multiples of the word size.

- a. Data transfer is inefficient but data can be stored efficiently in memory
- b. Data transfer is efficient and also data can be stored efficiently in memory
- c. Data transfer is efficient but data storage in memory would not be efficient. ✖
- d. Data transfer is inefficient and data storage in memory would not be efficient

Your answer is incorrect.

The correct answer is:

Data transfer is inefficient but data can be stored efficiently in memory

Question 5

Incorrect

Mark 0.00 out of 1.00

The content of the multiplicand register and the multiplier register of a hardware circuit implementing Booth's algorithm is the binary numbers 111001 and 111100 what would be the result produced by the multiplier circuitry (Decimal)

- a. -28
- b. 1812
- c. 28 ✖
- d. -1828

Your answer is incorrect.

The correct answer is:

1812

Question **6**

Incorrect

Mark 0.00 out of 1.00

A booth's multiplier circuit needs to inspect at most how many LSB bits to determine whether to add the multiplier, subtract the multiplier or leave the partial result unchanged during any step in the sequence of multiplication steps?

- a. One bit
- b. All bits of the multiplier
- c. All bits of the multiplicand
- d. Two bits

✗

Your answer is incorrect.

The correct answer is:

One bit

Question **7**

Incorrect

Mark 0.00 out of 1.00

Divide overflow is easiest to handle in which one of the following circuits implementing division?

- a. Fixed point sign magnitude division
- b. Floating point division
- c. Fixed point 1's complement division
- d. Fixed point 2's complement division

✗

Your answer is incorrect.

The correct answer is:

Floating point division

Question 8

Correct

Mark 1.00 out of 1.00

In order to realize an adder that can add two 16-bit numbers, how many full adders and half adders would be required?

- a. One half adder and 15 full adders
- b. 15 half adders and one full adder
- c. 10 half adders and 11 full adders
- d. 17 half adders and 0 full adder



Your answer is correct.

The correct answer is:

One half adder and 15 full adders

Question **9**

Incorrect

Mark 0.00 out of 1.00

Which one of the following can be said about the speed of a multiplier capable of multiplying two 16-bit numbers?

- a. Booth's and array multiplier would be equally fastest
- b. Array multiplier would be the fastest
- c. Booth's multiplier would be the fastest
- d. Sign magnitude multiplier would be the fastest



Your answer is incorrect.

The correct answer is:

Array multiplier would be the fastest

Question **10**

Correct

Mark 1.00 out of 1.00

In the implementation of a binary multiplier circuit, which one of the following set of logic gates is used?

- a. XOR gates and shift registers
- b. 2 input X-or gates and 2-input AND gates
- c. 2 input AND gates only
- d. 2-input NOR gates and 1 XOR gate



Your answer is correct.

The correct answer is:

2 input X-or gates and 2-input AND gates

Question **11**

Incorrect

Mark 0.00 out of 1.00

A computer has a word size of 16-bit and has 16 programmer visible registers. each instruction has two sources and one destination operands and uses only register direct addressing mode. what is the maximum number of op-codes that this processor can have?

- a. 16
- b. 8
- c. 64
- d. 32

✗

Your answer is incorrect.

The correct answer is:

16

Question **12**

Correct

Mark 1.00 out of 1.00

After fetching an instruction from memory, the binary code of the instruction is stored in which one of the following?

- a. Accumulator
- b. Program counter
- c. Instruction register
- d. Instruction pointer



Your answer is correct.

The correct answer is:

Instruction register

Question **13**

Correct

Mark 1.00 out of 1.00

The IR store which one of the following?

- a. An instruction that has been fetched from the memory
- b. An instruction that has been executed
- c. An instruction that has been decoded
- d. The address of the next instruction to be executed



Your answer is correct.

The correct answer is:

An instruction that has been fetched from the memory

Question **14**

Correct

Mark 1.00 out of 1.00

Cache memory is?

- a. Interface between processor and SRAM
- b. Interface between processor and virtual memory
- c. Interface between processor and main memory
- d. Interface between processor and DMA



Your answer is correct.

The correct answer is:

Interface between processor and main memory

Question **15**

Correct

Mark 1.00 out of 1.00

Which of the common cache?

- a. DRAM
- b. SRAM
- c. TLB
- d. Taps



Your answer is correct.

The correct answer is:

TLB

Question 16

Correct

Mark 1.00 out of 1.00

-----is the concept in which a process is copied into the main memory from the secondary memory according to the requirement.

- a. Segmentation
- b. Pagging
- c. Demand pagging
- d. None of the mentioned



Your answer is correct.

The correct answer is:

Demand pagging

Question **17**

Correct

Mark 1.00 out of 1.00

When an instruction is required to be brought from memory to CPU, on which one of the following busses is it fetched?

- a. Peripheral bus
- b. Data bus
- c. Address bus
- d. Control bus



Your answer is correct.

The correct answer is:

Data bus

Question **18**

Incorrect

Mark 0.00 out of 1.00

Consider a three address RISC processor ISA. Which one of the following correctly characterizes an effect of doubling the number of registers in the processor?

- a. Instruction size would be increase by 3-bit
- b. Instruction size would be increase by 1-bit
- c. Instruction size would be increase by 2-bit
- d. Instruction size would be unaffected

✖

Your answer is incorrect.

The correct answer is:

Instruction size would be increase by 3-bit

Question **19**

Correct

Mark 1.00 out of 1.00

Swap space exists in _____

- a. Secondary memory
- b. Primary memory
- c. DRAM
- d. None of the mentioned



Your answer is correct.

The correct answer is:

Secondary memory

Question **20**

Correct

Mark 1.00 out of 1.00

If the page hit is there in the page table then?

- a. None of the mentioned
- b. Data can be dire accessed from main memory without address translation
- c. Data can be dire accessed from main memory after the address translation
- d. Data can be directly accessed from disc



Your answer is correct.

The correct answer is:

Data can be dire accessed from main memory after the address translation

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Started on	Thursday, 4 March 2021, 10:00 AM
State	Finished
Completed on	Thursday, 4 March 2021, 10:40 AM
Time taken	40 mins 1 sec
Marks	38.00/40.00
Grade	9.50 out of 10.00 (95%)

Question 1

Complete

Mark 1.00 out of 1.00

What is the arithmetic shift right operation after the 1st cycle for the following binary stream 1 0 0 1 0 0 1 1 0 ?

- a. 1 1 1 0 0 1 0 0 1
- b. 0 1 1 0 0 1 0 0 1
- c. 1 1 0 0 1 0 0 1 1
- d. 1 0 0 1 0 0 1 1 0

Your answer is correct.

The correct answer is:

1 1 0 0 1 0 0 1 1

Question **2**

Complete

Mark 1.00 out of 1.00

The shortfall of registers created by aggressive unrolling and scheduling is also known as --

- a. Miss rate
- b. Forwarding
- c. Register pressure
- d. Aggressive scaling

Your answer is correct.

The correct answer is:

Register pressure

Question **3**

Complete

Mark 1.00 out of 1.00

Consider the following instruction sequence five-stage pipeline,

ADD R1, R2, R1 --- I1

LW R2,0(R1) --- I2

LW R1,4(R1) -- I3

OR R3, R1, R2 -- I4

Select the correct option.

- a. RAW hazards is present in instructions I1-I2
- b. RAW hazards is present in instructions I3-I4
- c. All of the mentioned
- d. RAW hazards is present in instructions I2-I3

Your answer is correct.

The correct answer is:

All of the mentioned

Question **4**

Complete

Mark 1.00 out of 1.00

Pipelining of a MIPS-like Processor, select the right option

- a. All of the mentioned
- b. All ALU operations are performed on register operands
- c. Separate Instruction and data memory is required
- d. Only instructions which access memory are load and store instructions

Your answer is correct.

The correct answer is:

All of the mentioned

Question **5**

Complete

Mark 1.00 out of 1.00

in loop Unrolling with Scheduling---. Select the right option.

- a. All of the mentioned
- b. Use different registers to avoid unnecessary constraints
- c. Identify that loop iterations are independent
- d. Determine the loads and stores that can be interchanged in the unrolled loop

Your answer is correct.

The correct answer is:

All of the mentioned

Question **6**

Complete

Mark 1.00 out of 1.00

For the code given below. Select the right option.

```
if p1 {  
S1;  
};  
if p2 {  
S2;  
};
```

- a. S1 is control dependent on p1, but S2 is not control dependent on p1
- b. All of the mentioned
- c. S2 cannot be moved after the branch
- d. S1 cannot be moved before the branch

Your answer is correct.

The correct answers are: S1 is control dependent on p1, but S2 is not control dependent on p1, S1 cannot be moved before the branch,
All of the mentioned

Question **7**

Complete

Mark 1.00 out of 1.00

Which unit is responsible for directing the operations of computer arithmetic and logical unit?

- a. I/O interface
- b. ALU itself
- c. Program
- d. Control unit

Your answer is correct.

The correct answer is:

Control unit

Question **8**

Complete

Mark 1.00 out of 1.00

Forwarding can be implemented in 5-stage and 6-stage MIPS pipeline --

- a. Using three multiplexers
- b. Using two multiplexers
- c. Using one multiplexer
- d. Using two multiplexers with extra latch

Your answer is correct.

The correct answer is:

Using two multiplexers

Question **9**

Complete

Mark 1.00 out of 1.00

For the program given below the number of stalls required after the code transformed by the smart compiler are

MIPS Code:

1. LW R2, 0(R4)
2. LW R5, 4(R4)
3. ADD R1, R2, R3

- a. One
- b. Three
- c. Two
- d. No stall is required

Your answer is correct.

The correct answer is:

No stall is required

Question 10

Complete

Mark 1.00 out of 1.00

For the load and store operation ---

- a. Effective address is calculated between 4th and 5th stage of the pipeline
- b. Effective address is calculated at 3rd stage of the pipeline
- c. Effective address is calculated between 3rd and 4th stage of the pipeline
- d. Effective address is calculated at 4th stage of the pipeline

Your answer is correct.

The correct answer is:

Effective address is calculated at 3rd stage of the pipeline

Question **11**

Complete

Mark 1.00 out of 1.00

In the MIPS architecture, the meaning of the instruction can be found from --

- a. Accumulator register
- b. Program counter register
- c. Address register
- d. Instruction register

Your answer is correct.

The correct answer is:

Instruction register

Question **12**

Complete

Mark 1.00 out of 1.00

During 1 clock cycle, the pipeline (5-stage) can process --

- a. 5 different instructions
- b. 6 different instructions
- c. None of the mentioned
- d. 4 different instructions

Your answer is correct.

The correct answer is:

5 different instructions

Question **13**

Complete

Mark 1.00 out of 1.00

What is the two times shift right of the binary stream 0 1 0 1 1 1 1 0 1?

- a. 0 1 0 1 1 1 1 0 1
- b. 0 1 0 1 1 1 1 0 0
- c. None of the mentioned
- d. 0 0 0 1 0 1 1 1 1

Your answer is correct.

The correct answer is:

0 0 0 1 0 1 1 1 1

Question **14**

Complete

Mark 1.00 out of 1.00

The processor speed has been increased over the last five decades due the --

- a. Newton's law
- b. Moore's Law
- c. Charl's law
- d. Krammar's Law

Your answer is correct.

The correct answer is: Moore's Law

Question 15

Complete

Mark 1.00 out of 1.00

CACHE memory act as an interface between---

- a. Processor hardware and virtual memory
- b. Processor hardware and main memory
- c. Processor hardware and control unit
- d. Processor hardware and I/O

Your answer is correct.

The correct answer is:

Processor hardware and main memory

Question 16

Complete

Mark 1.00 out of 1.00

A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The number of and gates required to design full adders are?

- a. Ten
- b. Nine
- c. Eight
- d. Twelve

Your answer is correct.

The correct answer is:

Nine

Question **17**

Complete

Mark 1.00 out of 1.00

The features of the RISC processor --

- a. Small number of the instructions
- b. Instruction execute in one or two clock cycle
- c. Small number of addressing modes
- d. All of the mentioned

Your answer is correct.

The correct answer is:

All of the mentioned

Question 18

Complete

Mark 1.00 out of 1.00

Using booth's algorithms multiply 7 with 3 and assume register AC is 4 bit. The value of AC after 3rd and 4th cycles are

- a. 1 0 1 0 and 1 0 1 0
- b. 0 0 1 0 and 1 0 1 0
- c. 0 1 1 1 0 and 1 0 1 0 0
- d. 0 0 1 1 and 1 0 1 1

Your answer is correct.

The correct answer is:

0 0 1 0 and 1 0 1 0

Question 19

Complete

Mark 1.00 out of 1.00

For the code given below, select the wrong answer.

MIPS Code:

1. add r1, r2, r3
2. sub r4, r1, r5

- a. For the second instruction, operands are required at 3rd stage of the pipeline
- b. There will be no hazard for the first instruction
- c. Data hazard is present
- d. One stalls is required to remove the data hazard

Your answer is correct.

The correct answer is:

One stalls is required to remove the data hazard

Question **20**

Complete

Mark 1.00 out of 1.00

In the MIPS architecture, data transfer takes place between --

- a. Register to register
- b. All of the mentioned
- c. Register to memory
- d. Memory to register

Your answer is correct.

The correct answer is:

All of the mentioned

Question **21**

Complete

Mark 0.00 out of 1.00

Mico-architecture are also known as --

- a. Micro programmed control unit
- b. Computer organization
- c. Computer architecture
- d. Macro programmed control unit

Your answer is incorrect.

The correct answer is:

Computer organization

Question **22**

Complete

Mark 1.00 out of 1.00

Addressing modes are used to calculate the effective address by using the --

- a. DMA
- b. ALU + control unit
- c. Control Unit
- d. ALU unit only

Your answer is correct.

The correct answer is:

ALU + control unit

Question 23

Complete

Mark 1.00 out of 1.00

The instruction $Z=X+Y$; needs to be run on accumulator-based architecture. Choose the current option.

- a. One operand is available in DMA
- b. Both operands are available in the accumulator
- c. Both operands are available in the register bank
- d. One operand is available in the accumulator and other need to be fetched from memory

Your answer is correct.

The correct answer is:

One operand is available in the accumulator and other need to be fetched from memory

Question **24**

Complete

Mark 1.00 out of 1.00

What is the shift right of the binary stream 0 1 0 1 1 1 1 0 1?

- a. 0 0 1 0 1 1 1 1
- b. 0 0 1 0 1 1 1 0 1
- c. 1 0 1 0 1 1 1 1 0
- d. 0 0 1 0 1 1 1 1 0

Your answer is correct.

The correct answer is:

0 0 1 0 1 1 1 1 0

Question **25**

Complete

Mark 1.00 out of 1.00

In MIPS architecture, the program counter send the address multiple of 4 due to --

- a. Byte addressability of memory
- b. Word addressability of memory
- c. Bit addressability of memory
- d. Nibble addressability of memory

Your answer is correct.

The correct answer is:

Byte addressability of memory

Question 26

Complete

Mark 1.00 out of 1.00

The zero flag register of the MIPS pipeline architecture--

- a. Calculate the effective address by adding the register content of the ALU
- b. Calculate the effective address by using the instruction register content
- c. Calculate the effective address by subtracting the register content of the ALU
- d. Calculate the effective address by using the program counter register content

Your answer is correct.

The correct answer is:

Calculate the effective address by subtracting the register content of the ALU

Question **27**

Complete

Mark 1.00 out of 1.00

A four-stage pipeline has stage delays of 150, 120, 160, and 140 ns respectively. Registers are used between the stages and have a delay of 10 ns each. What is the cycle time?

- a. 170 ns
- b. 140 ns
- c. 155 ns
- d. 165 ns

Your answer is correct.

The correct answer is:

170 ns

Question **28**

Complete

Mark 1.00 out of 1.00

For the code given below choose the wrong answer.

MIPS Code:

1. ADD r1, r2, r3
2. SUB r4, r1, r5
3. AND r6, r1, r7
4. OR r8, r1, r9
5. XOR r10, r1, r11

- a. Using split phase of the clock, data hazard can be eliminated from instruction no. fourth
- b. Using split phase of the clock, data hazard can be eliminated from instruction no. second
- c. Using split phase of the clock, data hazard can be eliminated from instruction no. fifth
- d. Direct data dependence is there

Your answer is correct.

The correct answer is:

Using split phase of the clock, data hazard can be eliminated from instruction no. second

Question **29**

Complete

Mark 1.00 out of 1.00

In the MIPS pipeline architecture forwarding/bypassing is ----

- a. DMA based approach
- b. Combination of both hardware & software based approach
- c. Hardware based approach
- d. Software based approach

Your answer is correct.

The correct answer is:

Hardware based approach

Question **30**

Complete

Mark 1.00 out of 1.00

A pipelined processor has seven stages, namely, IF1, IF2, ID, EX, MEM1, MEM2, WB. Assuming all the stages require the same amount of time and the time period of the non- pipelined processors is 14 ns, find out the clock frequency and speedup of the pipelined processor. Assume the delay of the latches is 1 ns.

- a. 1Khz and 50
- b. None of the mentioned
- c. 1 Khz and 3
- d. 1.2 Khz and 30

Your answer is correct.

The correct answer is:

None of the mentioned

Question **31**

Complete

Mark 1.00 out of 1.00

If multiplicand (M) is 0111, the AC register is initialized with zero. What will be the content of the AC register after operation $AC = AC - M$?

- a. 1100
- b. 1111
- c. 1001
- d. 1010

Your answer is correct.

The correct answer is:

1001

Question **32**

Complete

Mark 1.00 out of 1.00

For calculating the effective address, the upper 6 bits and concatenation done between---

- a. Program counter and constant value which was the part of the instruction
- b. Address register and constant value which was not the part of the instruction
- c. Address register and constant value which was the part of the instruction
- d. Program counter and constant value which was not the part of the instruction

Your answer is correct.

The correct answer is:

Program counter and constant value which was the part of the instruction

Question **33**

Complete

Mark 1.00 out of 1.00

The instruction ADD Rd,Rs, Rt is ---

- a. P-type instruction of MIPS
- b. R-type instruction of MIPS
- c. J-type instruction of MIPS
- d. I-type instruction of MIPS

Your answer is correct.

The correct answer is:

R-type instruction of MIPS

Question **34**

Complete

Mark 1.00 out of 1.00

In the J-type instructions of MIPS --

- a. One operand is provided as a part of the instruction and other operand need to be get from accumulator
- b. One operand is provided as a part of the instruction and other operand need to be fetched from memory
- c. Both operands are not available in the register bank
- d. Both the operands are available in the register bank

Your answer is correct.

The correct answers are:

Both the operands are available in the register bank,

One operand is provided as a part of the instruction and other operand need to be fetched from memory

Question **35**

Complete

Mark 1.00 out of 1.00

The following assembly program is run over the MIPS pipeline architecture. Choose the wrong option.

Assembly code:

i1. `pp1: L.D F0,0(R1);`
i2. `ADD.D F4,F0,F2;`
i3. `S.D F4,0(R1);`
i4. `DADDUI R1,R1,#-8;`
i5. `BNE R1,R2,pp1`

- a. i4 is used as an increment pointer
- b. i3 is used to store the results
- c. i1 is used for array element
- d. i2 is used for adding scalar value

Your answer is correct.

The correct answers are:

i1 is used for array element,

i4 is used as an increment pointer

Question **36**

Complete

Mark 0.00 out of 1.00

ISA serves as an interface between ---

- a. Processor and DMA
- b. Processor and memory
- c. Processor and operating system
- d. Processor and I/O

Your answer is incorrect.

The correct answer is:

Processor and operating system

Question **37**

Complete

Mark 1.00 out of 1.00

For the code given below identifies the data hazard.

Code:

add r1, r2, r3
sub r1, r4, r5

- a. RAW
- b. None of the mentioned
- c. WAR
- d. WAW

Your answer is correct.

The correct answer is:

WAW

Question 38

Complete

Mark 1.00 out of 1.00

In MIPS architecture, increasing the number of stages --

- a. Will always decrease the performance.
- b. Will always improve the performance.
- c. Will always improve the performance after the optimal value of the stages
- d. Will improve the performance up to optimal value of the stages and beyond the optimal value it will decrease

Your answer is correct.

The correct answers are:

Will always decrease the performance.,

Will improve the performance up to optimal value of the stages and beyond the optimal value it will decrease

Question **39**

Complete

Mark 1.00 out of 1.00

Programmer visible part of the machine hardware--

- a. All of the mentioned
- b. Instruction set
- c. Registers and instructions format
- d. Addressing modes

Your answer is correct.

The correct answer is:

All of the mentioned

Question **40**

Complete

Mark 1.00 out of 1.00

Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 5 ns. What is the Pipeline cycle time?

- a. 100 ns
- b. 95 ns
- c. 105 ns
- d. 75 ns

Your answer is correct.

The correct answer is:

95 ns

◀ 10 % online test (fifth week)

Jump to...



Online Test ►

Started on	Thursday, 8 April 2021, 9:05 AM
State	Finished
Completed on	Thursday, 8 April 2021, 10:00 AM
Time taken	54 mins 51 secs
Marks	34.00/50.00
Grade	6.80 out of 10.00 (68%)

Question 1

Correct

Mark 1.00 out of 1.00

For the load and store operation ---

- a. Effective address is calculated at 4th stage of the pipeline
- b. Effective address is calculated between 3rd and 4th stage of the pipeline
- c. Effective address is calculated at 3rd stage of the pipeline
- d. Effective address is calculated between 4th and 5th stage of the pipeline



Your answer is correct.

The correct answer is:

Effective address is calculated at 3rd stage of the pipeline

Question **2**

Correct

Mark 1.00 out of 1.00

Which one of the following addressing modes cannot be meaningfully used for the destination operand of an ADD instruction?

- a. Immediate
- b. Indirect
- c. Direct
- d. Indexed



Your answer is correct.

The correct answer is:

Indexed

Question **3**

Correct

Mark 1.00 out of 1.00

Which one of the following types of Interrupts can be caused by an executing program?

- a. Hardware
- b. External
- c. Internal
- d. Software



Your answer is correct.

The correct answer is:

Software

Question **4**

Correct

Mark 1.00 out of 1.00

Cache memory is?

- a. Interface between processor and DMA
- b. Interface between processor and virtual memory
- c. Interface between processor and SRAM
- d. Interface between processor and main memory



Your answer is correct.

The correct answer is:

Interface between processor and main memory

Question 5

Incorrect

Mark 0.00 out of 1.00

For Page replacement which approach is good?

- a. Write back
- b. Segmentation
- c. Paging
- d. Write through

✗

Your answer is incorrect.

The correct answer is:

Write back

Question **6**

Incorrect

Mark 0.00 out of 1.00

When a processor fetches an instruction of the executing program, the binary code of the instruction gets stored in which one of the following?

- a. Program counter
- b. General purpose register
- c. Instruction register
- d. Accumulator

✗

Your answer is incorrect.

The correct answer is:

Program counter

Question **7**

Correct

Mark 1.00 out of 1.00

Which of the following statement most accurately characterizes the responsibility of the memory management unit in the processor?

- a. Managing the interfacing between main memory and hard disk
- b. Managing the physical memory of the machine
- c. Managing the translation of the virtual into physical address
- d. Managing the interface between the processor and the main memory



Your answer is correct.

The correct answer is:

Managing the physical memory of the machine

Question 8

Correct

Mark 1.00 out of 1.00

Which one of the following is a major benefit of the Harvard architecture over the von Neumann architecture?

- a. Code and data share memory and increase program execution efficiency
- b. Code and data can be loaded into the CPU simultaneously on separate buses ✓
- c. None of the mentioned
- d. Program written using single word instruction execute more quickly than multiword instructions

Your answer is correct.

The correct answer is:

Code and data can be loaded into the CPU simultaneously on separate buses

Question **9**

Incorrect

Mark 0.00 out of 1.00

Which one of the following can be said about the speed of a multiplier capable of multiplying two 16-bit numbers?

- a. Sign magnitude multiplier would be the fastest
- b. Booth's and array multiplier would be equally fastest ✖
- c. Booth's multiplier would be the fastest
- d. Array multiplier would be the fastest

Your answer is incorrect.

The correct answer is:

Array multiplier would be the fastest

Question **10**

Correct

Mark 1.00 out of 1.00

Which one of the following types of semiconductor memory is used as the main memory in a computer?

- a. SRAM
- b. Flash
- c. PROM
- d. DRAM



Your answer is correct.

The correct answer is:

DRAM

Question **11**

Incorrect

Mark 0.00 out of 1.00

Which one of the following would cause the Page fault frequency in an operating system to reduce?

- a. Executing processes remain CPU-bound
- b. Executing processes exhibit high locality of reference
- c. Cache memory size is increased
- d. Size of the page reduced



Your answer is incorrect.

The correct answer is:

Executing processes remain CPU-bound

Question **12**

Correct

Mark 1.00 out of 1.00

Which one of the following addressing modes are used in an instruction of the form ADD X, Y is?

- a. Immediate
- b. Indirect
- c. Relative
- d. Absolute



Your answer is correct.

The correct answer is:

Absolute

Question 13

Correct

Mark 1.00 out of 1.00

The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Writeback (WB). The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each, and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards. What is the number of clock cycles required for the completion of the execution of the sequence of instruction?

- a. 220 cycles
- b. 221 cycles
- c. 219 cycles
- d. 229 cycles



Your answer is correct.

The correct answer is:

219 cycles

Question **14**

Correct

Mark 1.00 out of 1.00

Consider a pipeline having 4 phases with the duration of 60, 50, 90, and 80 ns. Given latch delay is 10 ns. What is the pipeline cycle time?

- a. 60 ns
- b. 90 ns
- c. 100 ns
- d. 70 ns



Your answer is correct.

The correct answer is:

100 ns

Question **15**

Correct

Mark 1.00 out of 1.00

Vector processors are best classified into which one of the following Flynn's classifications of computers?

- a. Multiple instruction, multiple data stream
- b. Single instruction, multiple data stream
- c. Single instruction, single data stream
- d. Multiple instruction, single data stream



Your answer is correct.

The correct answer is:

Single instruction, multiple data stream

Question 16

Incorrect

Mark 0.00 out of 1.00

In the J-type instructions of MIPS --

- a. Both operands are not available in the register bank ✖
- b. One operand is provided as a part of the instruction and other operand need to be fetched from memory
- c. One operand is provided as a part of the instruction and other operand need to be get from accumulator
- d. Both the operands are available in the register bank

Your answer is incorrect.

The correct answers are:

Both the operands are available in the register bank,

One operand is provided as a part of the instruction and other operand need to be fetched from memory

Question 17

Correct

Mark 1.00 out of 1.00

Which one of the following sentences best justifies the need for using a virtual memory operating system?

- a. It help to extend the amount of physical memory that is being used
- b. It help to improve the performance of the hard disk
- c. It help to run multiple programs whose combined size is much larger than the size of the physical memory available on the machine ✓
- d. It allows machines to communicate over a local area network

Your answer is correct.

The correct answer is:

It help to run multiple programs whose combined size is much larger than the size of the physical memory available on the machine

Question 18

Incorrect

Mark 0.00 out of 1.00

Which one of the following means is deployed flash memory to store data?

- a. A six-transistor flip flop circuitry is used in each memory cell ✖
- b. Charge retained in a diode in each memory cell to indicate a logical 1
- c. Use of programmable fuse in each memory cell
- d. Charge retained in a floating gate in each memory cell to indicate a logical 1

Your answer is incorrect.

The correct answer is:

Charge retained in a floating gate in each memory cell to indicate a logical 1

Question **19**

Incorrect

Mark 0.00 out of 1.00

A computer, whose average memory access time is 20 ns has a page fault service time of 10 ms. For every 100 memory accesses, the one-page fault is generated. The effective access time for the memory in which one of the following?

- a. 20 ns
- b. 30 ns
- c. 45 ns
- d. None of the mentioned



Your answer is incorrect.

The correct answer is:

20 ns

Question **20**

Correct

Mark 1.00 out of 1.00

Which of the common cache?

- a. SRAM
- b. Taps
- c. DRAM
- d. TLB



Your answer is correct.

The correct answer is:

TLB

Question **21**

Correct

Mark 1.00 out of 1.00

When an instruction is required to be brought from memory to CPU, on which one of the following busses is it fetched?

- a. Control bus
- b. Address bus
- c. Peripheral bus
- d. Data bus



Your answer is correct.

The correct answer is:

Data bus

Question **22**

Correct

Mark 1.00 out of 1.00

Pipelined processors are the best classified into which one of the following Flynn's classifications of computers?

- a. Single instruction, multiple data stream
- b. Multiple instruction, multiple data stream
- c. Single instruction, single data stream
- d. Multiple instruction, single data stream



Your answer is correct.

The correct answer is:

Single instruction, single data stream

Question **23**

Correct

Mark 1.00 out of 1.00

Which one of them is not a pipeline parameter?

- a. Pipeline cycle time
- b. Speed up ratio
- c. Throughput
- d. Ripple ratio



Your answer is correct.

The correct answer is:

Ripple ratio

Question **24**

Incorrect

Mark 0.00 out of 1.00

Assume that the following types of computers, all hazards are handled through stalling. Which one of the following consumption would suffer from the least drag from the ideal performance due to hazards while running a typical program.

- a. A computer with a 5 stage pipelined processor
- b. A computer with a 16 stage pipelined and four issue superscalar processor
- c. A computer with a 16 stage pipelined processor
- d. A computer with a 5 stage pipelined and four issue superscalar processor

✗

Your answer is incorrect.

The correct answer is:

A computer with a 5 stage pipelined and four issue superscalar processor

Question **25**

Correct

Mark 1.00 out of 1.00

The shortfall of registers created by aggressive unrolling and scheduling is also known as --

- a. Forwarding
- b. Register pressure
- c. Aggressive scaling
- d. Miss rate



Your answer is correct.

The correct answer is:

Register pressure

Question **26**

Correct

Mark 1.00 out of 1.00

The numbers of NAND and NOR gates required to implement full subtractor are?

- a. 11 and 11
- b. 9 and 10
- c. 10 and 9
- d. 9 and 9



Your answer is correct.

The correct answer is:

9 and 9

Question **27**

Correct

Mark 1.00 out of 1.00

For Von Neumann's architecture implementation. Select the correct option.

- a. I/O are required
- b. All of the mentioned
- c. Memory is required
- d. CPU is required



Your answer is correct.

The correct answer is:

All of the mentioned

Question **28**

Correct

Mark 1.00 out of 1.00

Von Neumann computers belong to which one of the following classes of computers?

- a. SIMD
- b. MIMD
- c. MISD
- d. SISD



Your answer is correct.

The correct answer is:

SISD

Question **29**

Correct

Mark 1.00 out of 1.00

Distributed computers belong to which one of the following classes of computers?

- a. SISD
- b. SIMD
- c. MISD
- d. MIMD



Your answer is correct.

The correct answer is:

MIMD

Question **30**

Correct

Mark 1.00 out of 1.00

What is the two times shift right of the binary stream 0 1 0 1 1 1 1 0 1?

- a. 0 1 0 1 1 1 1 0 0
- b. 0 0 0 1 0 1 1 1 1
- c. None of the mentioned
- d. 0 1 0 1 1 1 1 0 1



Your answer is correct.

The correct answer is:

0 0 0 1 0 1 1 1 1

Question **31**

Correct

Mark 1.00 out of 1.00

Virtual memory is also known as?

- a. Interface between main memory and secondary memory
- b. All of the mentioned
- c. Cache between main memory and secondary
- d. Buffer between main memory and secondary memory



Your answer is correct.

The correct answer is:

All of the mentioned

Question **32**

Correct

Mark 1.00 out of 1.00

Instruction pipeline improves the CPU performance due to which one of the following reasons?

- a. Reduced memory access time
- b. Efficient utilization of the processor hardware
- c. Use of additional functional units
- d. Use a larger Cache



Your answer is correct.

The correct answer is:

Efficient utilization of the processor hardware

Question **33**

Incorrect

Mark 0.00 out of 1.00

Which one of the following is true for a typical RISC architecture?

- a. Makes use of hardwired control unit
- b. Has much smaller Cache than CISC processors
- c. Supports many addressing modes
- d. Make use of multiprogrammed control unit



Your answer is incorrect.

The correct answer is:

Makes use of hardwired control unit

Question **34**

Incorrect

Mark 0.00 out of 1.00

Which one of the following characteristics is associated with shared memory multiprocessors?

- a. Loosely coupled and coarse grained parallelism
- b. Tightly coupled and coarse grained parallelism
- c. Loosely coupled and fine grained parallelism
- d. Tightly coupled and fine grained parallelism

✗

Your answer is incorrect.

The correct answer is:

Tightly coupled and fine grained parallelism

Question 35

Incorrect

Mark 0.00 out of 1.00

In the MIPS pipeline architecture forwarding/bypassing is ----

- a. DMA based approach
- b. Hardware based approach
- c. Software based approach
- d. Combination of both hardware & software based approach



Your answer is incorrect.

The correct answer is:

Hardware based approach

Question **36**

Correct

Mark 1.00 out of 1.00

The IR store which one of the following?

- a. An instruction that has been decoded
- b. An instruction that has been fetched from the memory
- c. The address of the next instruction to be executed
- d. An instruction that has been executed



Your answer is correct.

The correct answer is:

An instruction that has been fetched from the memory

Question **37**

Correct

Mark 1.00 out of 1.00

For 4-bit ripple carry adder design. Select the right option in terms of low cost and low power.

- a. 3 full adders and 1 half adder
- b. 4 half adders
- c. 4 full adders
- d. 3 half adders and 1 full adder



Your answer is correct.

The correct answer is:

3 full adders and 1 half adder

Question **38**

Correct

Mark 1.00 out of 1.00

The use of which of the following in a computer is justified by the principle of locality?

- a. DMA
- b. Cache memory
- c. Virtual memory
- d. Software interrupt



Your answer is correct.

The correct answer is:

Cache memory

Question **39**

Correct

Mark 1.00 out of 1.00

Consider the unpipelined machine with 10ns clock cycles. It uses four cycles for ALU operations and branches where as five cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 20%, and 40% respectively. Let due to clock skew and set up pipelining, the machine adds 1 ns of overhead to the clock. How much speed in instruction execution rate will we gain from the pipeline?

- a. 3X
- b. 4X
- c. 2X
- d. 1X



Your answer is correct.

The correct answer is:

4X

Question **40**

Incorrect

Mark 0.00 out of 1.00

During 1 clock cycle, the pipeline (5-stage) can process --

- a. 4 different instructions
- b. 6 different instructions
- c. None of the mentioned
- d. 5 different instructions

✖

Your answer is incorrect.

The correct answer is:

5 different instructions

Question **41**

Correct

Mark 1.00 out of 1.00

ISA serves as an interface between ---

- a. Processor and operating system
- b. Processor and I/O
- c. Processor and memory
- d. Processor and DMA



Your answer is correct.

The correct answer is:

Processor and operating system

Question **42**

Correct

Mark 1.00 out of 1.00

Which one of the following multiplexers would have a 4-bit data select input?

- a. 4:1
- b. 16:1
- c. 2:1
- d. 8:1



Your answer is correct.

The correct answer is:

16:1

Question **43**

Incorrect

Mark 0.00 out of 1.00

Shared memory multiprocessor fit best into which one of the following Flynn's classification of computers?

- a. Multiple instruction, single data stream
- b. Single instruction, single data stream
- c. Single instruction, multiple data stream
- d. Multiple instruction, multiple data stream

✖

Your answer is incorrect.

The correct answer is:

Multiple instruction, multiple data stream

Question **44**

Incorrect

Mark 0.00 out of 1.00

Which one of the following is not a characteristic of loosely coupled computers?

- a. Efficient execution of programs and fine grained parallelism
- b. Shared memory ✖
- c. No shared memory
- d. Message passing communication

Your answer is incorrect.

The correct answer is:

Efficient execution of programs and fine grained parallelism

Question **45**

Correct

Mark 1.00 out of 1.00

What is true for virtual memory?

- a. Processor sends virtual address for main memory
- b. Processor sends virtual address for page table
- c. Processor sends physical address for main memory
- d. Processor sends physical address for page table



Your answer is correct.

The correct answer is:

Processor sends virtual address for page table

Question **46**

Incorrect

Mark 0.00 out of 1.00

Which one of the following most accurately characterizes the primary reason for the use of translation lookaside buffer in a processor?

- a. TLB makes translation of virtual addresses to physical addresses faster
- b. None of the mentioned
- c. TLB allows multiple processes to share the L1 Cache ✖
- d. TLB ensures that a process does not access memory outside of its address space

Your answer is incorrect.

The correct answer is:

TLB makes translation of virtual addresses to physical addresses faster

Question **47**

Correct

Mark 1.00 out of 1.00

A purely sequential program was observed to take 1000 seconds to complete execution on a certain four-processor MIMD computer. It was rewritten threads so that 76 % of the original code could run ideally parallel. Under the assumption that there is no other bottleneck, how long would this program take to complete execution on the four-processor MIMD computer?

- a. 430 sec.
- b. 476 sec.
- c. 571 sec.
- d. 340 sec.



Your answer is correct.

The correct answer is:

430 sec.

Question **48**

Correct

Mark 1.00 out of 1.00

in loop Unrolling with Scheduling---. Select the right option.

- a. Use different registers to avoid unnecessary constraints
- b. Determine the loads and stores that can be interchanged in the unrolled loop
- c. Identify that loop iterations are independent
- d. All of the mentioned



Your answer is correct.

The correct answer is:

All of the mentioned

Question **49**

Correct

Mark 1.00 out of 1.00

For the program given below the number of stalls required after the code transformed by the smart compiler are

MIPS Code:

1. LW R2, 0(R4)
2. LW R5, 4(R4)
3. ADD R1, R2, R3

- a. One
- b. Three
- c. No stall is required
- d. Two



Your answer is correct.

The correct answer is:

No stall is required

Question **50**

Incorrect

Mark 0.00 out of 1.00

A software interrupt is caused in which one of the following situations?

- a. Divide by zero encountered while running a program
- b. A page transfer from the hard disk to the main memory is complete
- c. A DMA call
- d. A system call

✖

Your answer is incorrect.

The correct answer is:

A system call

◀ Online Test

Jump to...



Assignment-II ►

Started on Friday, 18 February 2022, 1:40 PM

State Finished

Completed on Friday, 18 February 2022, 1:47 PM

Time taken 6 mins 58 secs

Marks 5.00/7.00

Grade **7.14** out of 10.00 (**71%**)

Question 1

Complete

Mark 1.00 out of 1.00

An instruction register is the part of a CPU's control unit that holds the _____ currently being executed

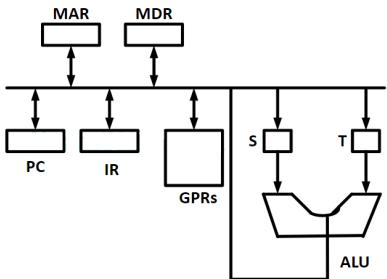
- a. data
- b. instruction
- c. None of the mentioned
- d. address

Question 2

Complete

Mark 1.00 out of 1.00

Consider the following data path of a cpu:



In the above data path size of bus, ALU and all registers are equal. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU.

Two clock cycles are needed for memory read operation- one is for loading address in MAR and one for loading data from memory but into MDR.

The instruction "call Rn,sub" is a two word instruction. Assume that program counter is incremented during the fetch cycle of the first word of the instruction, it's register transfer interpretation is

Rn <= PC + 1;

PC <= M[PC];

The no. of minimum number of CPU clock cycles required in the execution cycle of this instruction?

- a. 2
- b. 1
- c. 4
- d. 3

Question 3

Complete

Mark 0.00 out of 1.00

A machine (31-bit architecture, with 1-word long instructions) has 64 registers, each register is 32 bits long. It needs to support 45 instructions, which have an immediate operand in addition to two register operands. Assuming that the immediate operand is an unsigned integer, what is the maximum value of the immediate operand?

- a. 26383
- b. None of the mentioned
- c. 16333
- d. 16383

Question 4

Complete

Mark 1.00 out of 1.00

In a system, which has 32 registers the register id is _____ long?

- a. 16 bit
- b. 4 bit
- c. 5 bit
- d. 6 bit

Question 5

Complete

Mark 1.00 out of 1.00

_____ register specifically holds the _____ and provides it to instruction decoder circuit

- a. Memory and instruction
- b. data and instruction
- c. Instruction and instruction
- d. instruction and data

Question 6

Complete

Mark 0.00 out of 1.00

Which unit is responsible for directing the operations of computer arithmetic and logical unit?

- a. Multiplexer
- b. ALU by itself
- c. Control Unit
- d. Program Counter

Question **7**

Complete

Mark 1.00 out of 1.00

The components to design the data path architecture ?

- a. None of the mentioned
- b. Control unit and MUX
- c. ALU, Control unit, program counter
- d. ALU, MUX, Registres

[◀ Announcements](#)

Jump to...

[Assignment 2-18-02-2022 ►](#)

Started on Friday, 18 February 2022, 1:55 PM

State Finished

Completed on Friday, 18 February 2022, 2:02 PM

Time taken 7 mins 38 secs

Marks 5.00/5.00

Grade **10.00** out of 10.00 (**100%**)

Question **1**

Complete

Mark 1.00 out of 1.00

The two numbers given below are multiplied using Booth's algorithm.

Multiplicand : 0101 1010 1110 1110

Multiplier: 0111 0111 1011 1101

How many additions/Subtractions are required for ?

- a. **3 subtractions and 3 additions**
- b. **4 subtractions and 3 additions**
- c. **4 subtractions and 4 additions**
- d. **3 subtractions and 4 additions**

Question **2**

Complete

Mark 1.00 out of 1.00

for B= 0 0 0 1 1 1 0 0 0 1 1 what will be the arithmetic shift right ?

- a. **0 0 0 1 1 1 1 0 0 0 1**
- b. 0 0 0 0 1 1 1 0 0 0 1
- c. 1 0 0 0 1 1 1 0 0 0 1
- d. 0 0 0 0 1 1 1 0 0 0 0 0

Question **3**

Complete

Mark 1.00 out of 1.00

Using Booth's Algorithm for multiplication, the multiplier -57 will be recorded as?

a. **0 -1 0 0 1 1 1 -1**

b. **0 -1 0 0 1 0 0 -1**

c. **None of the mentioned**

d. **0 -1 0 0 1 0 1 -1**

Question **4**

Complete

Mark 1.00 out of 1.00

When both integer are +ve i.e. (+ve) x (+ve) = (+ve) and Multiply 7 with 3 and register size is 4 bit. Choose the correct option?

a. 4 Cycles are required to complete the multiplication

b. 7 Cycles are required to complete the multiplication

c. 5 Cycles are required to complete the multiplication

d. 3 Cycles are required to complete the multiplication

Question **5**

Complete

Mark 1.00 out of 1.00

For A= 0 0 1 0 1 0 1 0 0 what will be arithmetic shift right ?

a. A= 0 0 0 1 0 1 0 0 0

b. A= 1 1 1 1 0 1 0 1 1

c. A= 0 1 1 1 0 1 0 1 0

d. A= 0 0 0 1 0 1 0 1 0

[◀ Assignment 1-18-02-2022](#)

Jump to...

Started on Friday, 25 February 2022, 1:50 PM

State Finished

Completed on Friday, 25 February 2022, 1:55 PM

Time taken 5 mins 49 secs

Marks 4.00/4.00

Grade **10.00** out of 10.00 (**100%**)

Question **1**

Complete

Mark 1.00 out of 1.00

What is true for the look ahead carry adder?

- a. To reduce the computation time, there are faster ways to add two binary numbers by using carry lookahead adders
- b. They work by creating two signals P and G known to be Carry Propagator and Carry Generator.
- c. All of the mentioned
- d. The carry propagator is propagated to the next level whereas the carry generator is used to generate the output carry ,regardless of input carry.

Question **2**

Complete

Mark 1.00 out of 1.00

A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 microseconds. A 4-bit ripple-carry binary adder is implemented by using full adders.What is the total propagation time of this 4-bit binary adder in microseconds.

- a. **19.8 ms**
- b. **19.5 ms**
- c. **20 ms**
- d. **19.2 ms**



Question **3**

Complete

Mark 1.00 out of 1.00

Two 1's with a carry-in of 1 are added using a ripple carry adder. What are the outputs?

- a. 1,1
- b. 1,0
- c. 0,0
- d. 0,1

Question **4**

Complete

Mark 1.00 out of 1.00

For $X = (A \oplus B) C + (A \oplus B) C$ & $Y = AB + (A \oplus B) C$, choose the correct option.

- a. Are the expressions for the carry look ahead adder
- b. None of the mentioned
- c. Are the expressions for the Full subtractor
- d. Are the expressions for the ripple carry adder

◀ Assignment 2-18-02-2022

Jump to...

Assignment 4-04-03-2022 ►



Started on Friday, 4 March 2022, 1:50 PM

State Finished

Completed on Friday, 4 March 2022, 1:57 PM

Time taken 6 mins 58 secs

Marks 3.00/5.00

Grade **6.00** out of 10.00 (**60%**)

Question **1**

Complete

Mark 1.00 out of 1.00

For the RISC pipeline. Choose the correct option.

- a. The only operations that affect memory are loads and stores
- b. All operands are in registers
- c. all instructions are the same size
- d. All of the mentioned

Question **2**

Complete

Mark 0.00 out of 1.00

For the single instruction pipeline (code given below). The two stalls are provided as a part of the program. Choose the correct option?

Begin: add t0, t1, t2

nop

nop

.end Begin

- a. For the given program no stalls are required
- b. For the given program two more stalls are required
- c. For the given program three more stalls are required
- d. For the given program one more stall is required

Question 3

Complete

Mark 1.00 out of 1.00

For Implementing Instruction Pipeline ?

- a. Cycle time does not dependent on stages of the pipeline
- b. None of the mentioned
- c. Cycle time is determined by the smallest stage
- d. Cycle time is determined by the longest stage

Question 4

Complete

Mark 0.00 out of 1.00

A four stage pipeline has the stage delays as 150, 120, 170 and 140 ns respectively. Registers are used between the stages and have a delay of 5 ns each. Assuming constant clocking rate. The total time taken to process 1000 data items on the pipeline?

- a. 165.5 us
- b. 170.5 us
- c. 180.3 us
- d. 165.3 us

Question 5

Complete

Mark 1.00 out of 1.00

The Ideal RISC pipeline may have?

- a. Successive instructions are independent of one another
- b. Instructions are executed in sequence one after the other in the order in which they are written
- c. Instructions can be divided into independent parts, each taking nearly equal time
- d. All of the mentioned

[◀ Assignment 3-25-02-2022](#)

Jump to...

Started on Wednesday, 23 February 2022, 12:10 PM

State Finished

Completed on Wednesday, 23 February 2022, 12:15 PM

Time taken 4 mins 56 secs

Marks 2.00/5.00

Grade 4.00 out of 10.00 (40%)

Question 1

Incorrect

Mark 0.00 out of 1.00

For the given code select the correct option.

Code:

Load R1, A

Load R2, B

Add R3, R1, R2

Store C, R3

- a. Register to register based MIPS processor
- b. Accumulator based MIPS Processor
- c. Memory to register based MIPS processor
- d. Register to Memory based MIPS processor



Your answer is incorrect.

The correct answer is:

Register to register based MIPS processor

Question 2

Correct

Mark 1.00 out of 1.00

For the instructions Load R1, 0(R2). Choose the correct option.

- a. All of the mentioned
- b. Effective address will be the addition of 0 and content of R2
- c. Effective address is calculated by the ALU
- d. From the memory 0+R2's location content will loaded into the destination register



Your answer is correct.

The correct answer is:

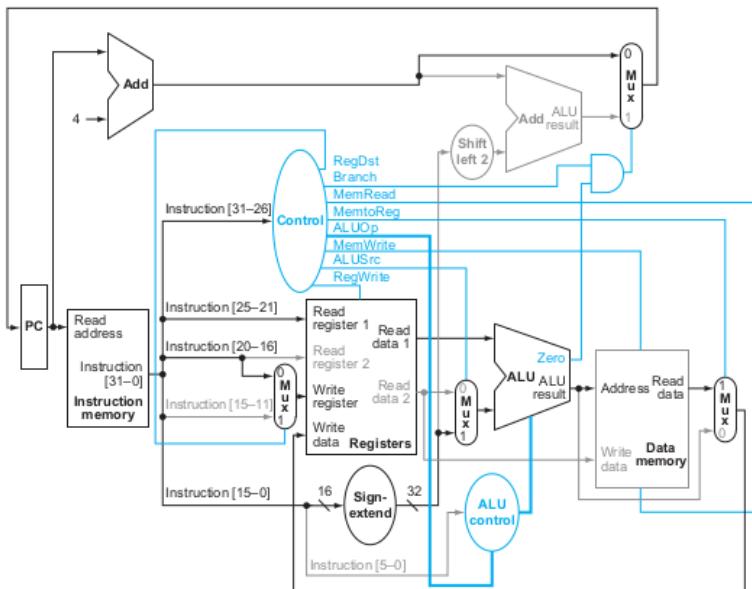
All of the mentioned

Question 3

Incorrect

Mark 0.00 out of 1.00

Which type of datapath architecture is given in the following ?



- a. R-type of instruction
- b. J-type instruction
- c. With Load instruction
- d. Branch on equal instruction ✗

Your answer is incorrect.

The correct answer is:

With Load instruction

Question 4

Correct

Mark 1.00 out of 1.00

ALU to support the MIPS instruction should have ?

- a. All of the mentioned ✓
- b. Subtraction using two's complement
- c. Replica of 1-bit ALU to produce a 32-bit ALU
- d. Multiplexor to select the output we want

Your answer is correct.

The correct answer is:

All of the mentioned

Question 5

Incorrect

Mark 0.00 out of 1.00

for Pseudo-direct Addressing. Select the correct option.

- a. Address is 26 bits of constant within instruction concatenated with lower 6 bits of PC
- b. Address is 26 bits of constant within instruction concatenated with upper 6 bits of PC
- c. Address is 26 bits of constant within instruction concatenated with upper 6 bits of Instruction register ✖
- d. Address is 26 bits of constant within instruction concatenated with lower 6 bits of Instruction register

Your answer is incorrect.

The correct answer is:

Address is 26 bits of constant within instruction concatenated with upper 6 bits of PC

[◀ Announcements](#)

Jump to...

[CS-208-Assignment-2_02-03-2022 ►](#)

Started on Wednesday, 2 March 2022, 12:10 PM

State Finished

Completed on Wednesday, 2 March 2022, 12:15 PM

Time taken 4 mins 58 secs

Marks 4.00/7.00

Grade 5.71 out of 10.00 (57%)

Question 1

Correct

Mark 1.00 out of 1.00

Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 5 ns. What is the Pipeline cycle time?

- a. 100 ns
- b. 105 ns
- c. 75 ns
- d. 95 ns



Your answer is correct.

The correct answer is:

95 ns

Question 2

Incorrect

Mark 0.00 out of 1.00

In MIPS architecture, increasing the number of stages --

- a. Will always decrease the performance.
- b. Will always improve the performance after the optimal value of the stages
- c. Will improve the performance up to optimal value of the stages and beyond the optimal value it will decrease
- d. Will always improve the performance.



Your answer is incorrect.

The correct answers are:

Will always decrease the performance.,

Will improve the performance up to optimal value of the stages and beyond the optimal value it will decrease

Question 3

Incorrect

Mark 0.00 out of 1.00

For the code given below choose the wrong answer.

MIPS Code:

1. ADD r1, r2, r3
2. SUB r4, r1, r5
3. AND r6, r1, r7
4. OR r8, r1, r9
5. XOR r10, r1, r11

- a. Using split phase of the clock, data hazard can be eliminated from instruction no. fourth
- b. Using split phase of the clock, data hazard can be eliminated from instruction no. fifth ✗
- c. Using split phase of the clock, data hazard can be eliminated from instruction no. second
- d. Direct data dependence is there

Your answer is incorrect.

The correct answer is:

Using split phase of the clock, data hazard can be eliminated from instruction no. second

Question 4

Correct

Mark 1.00 out of 1.00

For the code given below. Select the right option.

```
if p1 {  
    S1;  
}  
if p2 {  
    S2;  
}
```

- a. S1 is control dependent on p1, but S2 is not control dependent on p1
- b. All of the mentioned ✓
- c. S2 cannot be moved after the branch
- d. S1 cannot be moved before the branch

Your answer is correct.

The correct answers are: S1 is control dependent on p1, but S2 is not control dependent on p1, S1 cannot be moved before the branch, All of the mentioned

Question 5

Incorrect

Mark 0.00 out of 1.00

DIV.D F0,F2,F4

ADD.D F6,F0,F8

S.D F6,0(R1)

SUB.D F8,F10,F14

MUL.D F6,F10,F8

How many possible hazards are available in the above-given code?

- a. 2
- b. 5
- c. 4
- d. 3



Your answer is incorrect.

The correct answer is:

3

Question 6

Correct

Mark 1.00 out of 1.00

Which one of the following about the MIPS rating of a computer is FALSE?

- a. None of the mentioned
- b. MIPS rating of a processor is independent of the program is being executed.
- c. MIPS rating of computer depends on the computer being used
- d. MIPS rating of a computer can very based on which instruction of a processor are being considered



Your answer is correct.

The correct answer is:

MIPS rating of a processor is independent of the program is being executed.

Question 7

Correct

Mark 1.00 out of 1.00

The processor speed has been increased over the last five decades due the --

- a. Krammar's Law
- b. Moore's Law ✓
- c. Charl's law
- d. Newton's law

Your answer is correct.

The correct answer is: Moore's Law

[◀ CS-208-Assignment-1_23-02-2022](#)

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Started on Thursday, 8 April 2021, 9:05 AM

State Finished

Completed on Thursday, 8 April 2021, 10:00 AM

Time taken 54 mins 42 secs

Marks 30.00/50.00

Grade **6.00** out of 10.00 (**60%**)

Question **1**

Correct

Mark 1.00 out of 1.00

The use of which of the following in a computer is justified by the principle of locality?

- a. DMA
- b. Virtual memory
- c. Software interrupt
- d. Cache memory



Your answer is correct.

The correct answer is:

Cache memory

Question **2**

Correct

Mark 1.00 out of 1.00

What is the two times shift right of the binary stream 0 1 0 1 1 1 1 0 1?

- a. 0 1 0 1 1 1 1 0 0
- b. 0 0 0 1 0 1 1 1 1
- c. None of the mentioned
- d. 0 1 0 1 1 1 1 0 1



Your answer is correct.

The correct answer is:

0 0 0 1 0 1 1 1 1

Question 3

Incorrect

Mark 0.00 out of 1.00

In the MIPS pipeline architecture forwarding/bypassing is ----

- a. DMA based approach ✗
- b. Software based approach
- c. Combination of both hardware & software based approach
- d. Hardware based approach

Your answer is incorrect.

The correct answer is:

Hardware based approach

Question 4

Correct

Mark 1.00 out of 1.00

For Von Neumann's architecture implementation. Select the correct option.

- a. I/O are required
- b. Memory is required
- c. All of the mentioned ✓
- d. CPU is required

Your answer is correct.

The correct answer is:

All of the mentioned

Question 5

Incorrect

Mark 0.00 out of 1.00

Which one of the following is not a characteristic of loosely coupled computers?

- a. Efficient execution of programs and fine grained parallelism
- b. Shared memory ✗
- c. Message passing communication
- d. No shared memory

Your answer is incorrect.

The correct answer is:

Efficient execution of programs and fine grained parallelism

Question 6

Correct

Mark 1.00 out of 1.00

The numbers of NAND and NOR gates required to implement full subtractor are?

- a. 10 and 9
- b. 9 and 9 ✓
- c. 11 and 11
- d. 9 and 10

Your answer is correct.

The correct answer is:

9 and 9

Question 7

Incorrect

Mark 0.00 out of 1.00

A purely sequential program was observed to take 1000 seconds to complete execution on a certain four-processor MIMD computer. It was rewritten threads so that 76 % of the original code could run ideally parallel. Under the assumption that there is no other bottleneck, how long would this program take to complete execution on the four-processor MIMD computer?

- a. 430 sec.
- b. 340 sec.
- c. 476 sec. ✗
- d. 571 sec.

Your answer is incorrect.

The correct answer is:

430 sec.

Question 8

Correct

Mark 1.00 out of 1.00

For 4-bit ripple carry adder design. Select the right option in terms of low cost and low power.

- a. 4 half adders
- b. 4 full adders
- c. 3 full adders and 1 half adder ✓
- d. 3 half adders and 1 full adder

Your answer is correct.

The correct answer is:

3 full adders and 1 half adder

Question 9

Correct

Mark 1.00 out of 1.00

For Page replacement which approach is good?

- a. Segmentation
- b. Write back
- c. Paging
- d. Write through



Your answer is correct.

The correct answer is:

Write back

Question 10

Incorrect

Mark 0.00 out of 1.00

Instruction pipeline improves the CPU performance due to which one of the following reasons?

- a. Use of additional functional units
- b. Efficient utilization of the processor hardware
- c. Use a larger Cache
- d. Reduced memory access time



Your answer is incorrect.

The correct answer is:

Efficient utilization of the processor hardware

Question 11

Correct

Mark 1.00 out of 1.00

The IR store which one of the following?

- a. An instruction that has been fetched from the memory
- b. An instruction that has been decoded
- c. An instruction that has been executed
- d. The address of the next instruction to be executed



Your answer is correct.

The correct answer is:

An instruction that has been fetched from the memory

Question 12

Correct

Mark 1.00 out of 1.00

The shortfall of registers created by aggressive unrolling and scheduling is also known as --

- a. Forwarding
- b. Register pressure
- c. Aggressive scaling
- d. Miss rate



Your answer is correct.

The correct answer is:

Register pressure

Question 13

Correct

Mark 1.00 out of 1.00

ISA serves as an interface between ---

- a. Processor and DMA
- b. Processor and memory
- c. Processor and I/O
- d. Processor and operating system



Your answer is correct.

The correct answer is:

Processor and operating system

Question 14

Correct

Mark 1.00 out of 1.00

In the J-type instructions of MIPS --

- a. One operand is provided as a part of the instruction and other operand need to be fetched from memory
- b. Both operands are not available in the register bank
- c. Both the operands are available in the register bank
- d. One operand is provided as a part of the instruction and other operand need to be get from accumulator



Your answer is correct.

The correct answers are:

Both the operands are available in the register bank,

One operand is provided as a part of the instruction and other operand need to be fetched from memory

Question 15

Correct

Mark 1.00 out of 1.00

For the program given below the number of stalls required after the code transformed by the smart compiler are

MIPS Code:

1. LW R2, 0(R4)
2. LW R5, 4(R4)
3. ADD R1, R2, R3

- a. No stall is required ✓
- b. Two
- c. One
- d. Three

Your answer is correct.

The correct answer is:

No stall is required

Question 16

Correct

Mark 1.00 out of 1.00

During 1 clock cycle, the pipeline (5-stage) can process --

- a. 6 different instructions
- b. 5 different instructions ✓
- c. 4 different instructions
- d. None of the mentioned

Your answer is correct.

The correct answer is:

5 different instructions

Question 17

Correct

Mark 1.00 out of 1.00

A software interrupt is caused in which one of the following situations?

- a. A page transfer from the hard disk to the main memory is complete
- b. A system call ✓
- c. Divide by zero encountered while running a program
- d. A DMA call

Your answer is correct.

The correct answer is:

A system call

Question 18

Correct

Mark 1.00 out of 1.00

Consider a pipeline having 4 phases with the duration of 60, 50, 90, and 80 ns. Given latch delay is 10 ns. What is the pipeline cycle time?

- a. 60 ns
- b. 70 ns
- c. 90 ns
- d. 100 ns ✓

Your answer is correct.

The correct answer is:

100 ns

Question 19

Correct

Mark 1.00 out of 1.00

Which one of the following means is deployed flash memory to store data?

- a. Charge retained in a floating gate in each memory cell to indicate a logical 1
- b. Charge retained in a diode in each memory cell to indicate a logical 1
- c. Use of programmable fuse in each memory cell
- d. A six-transistor flip flop circuitry is used in each memory cell



Your answer is correct.

The correct answer is:

Charge retained in a floating gate in each memory cell to indicate a logical 1

Question 20

Correct

Mark 1.00 out of 1.00

Which one of them is not a pipeline parameter?

- a. Throughput
- b. Pipeline cycle time
- c. Speed up ratio
- d. Ripple ratio



Your answer is correct.

The correct answer is:

Ripple ratio

Question 21

Incorrect

Mark 0.00 out of 1.00

Assume that the following types of computers, all hazards are handled through stalling. Which one of the following consumption would suffer from the least drag from the ideal performance due to hazards while running a typical program.

- a. A computer with a 5 stage pipelined and four issue superscalar processor
- b. A computer with a 5 stage pipelined processor ✗
- c. A computer with a 16 stage pipelined processor
- d. A computer with a 16 stage pipelined and four issue superscalar processor

Your answer is incorrect.

The correct answer is:

A computer with a 5 stage pipelined and four issue superscalar processor

Question 22

Correct

Mark 1.00 out of 1.00

Von Neumann computers belong to which one of the following classes of computers?

- a. MIMD
- b. SISD ✓
- c. SIMD
- d. MISD

Your answer is correct.

The correct answer is:

SISD

Question 23

Correct

Mark 1.00 out of 1.00

When an instruction is required to be brought from memory to CPU, on which one of the following busses is it fetched?

- a. Address bus
- b. Data bus
- c. Control bus
- d. Peripheral bus



Your answer is correct.

The correct answer is:

Data bus

Question 24

Incorrect

Mark 0.00 out of 1.00

For the load and store operation ---

- a. Effective address is calculated between 4th and 5th stage of the pipeline
- b. Effective address is calculated at 3rd stage of the pipeline
- c. Effective address is calculated at 4th stage of the pipeline
- d. Effective address is calculated between 3rd and 4th stage of the pipeline



Your answer is incorrect.

The correct answer is:

Effective address is calculated at 3rd stage of the pipeline

Question 25

Incorrect

Mark 0.00 out of 1.00

Which one of the following characteristics is associated with shared memory multiprocessors?

- a. Loosely coupled and coarse grained parallelism
- b. Tightly coupled and coarse grained parallelism
- c. Tightly coupled and fine grained parallelism
- d. Loosely coupled and fine grained parallelism



Your answer is incorrect.

The correct answer is:

Tightly coupled and fine grained parallelism

Question 26

Incorrect

Mark 0.00 out of 1.00

Which one of the following most accurately characterizes the primary reason for the use of translation lookaside buffer in a processor?

- a. TLB allows multiple processes to share the L1 Cache
- b. None of the mentioned
- c. TLB ensures that a process does not access memory outside of its address space
- d. TLB makes translation of virtual addresses to physical addresses faster



Your answer is incorrect.

The correct answer is:

TLB makes translation of virtual addresses to physical addresses faster

Question 27

Incorrect

Mark 0.00 out of 1.00

Which one of the following is true for a typical RISC architecture?

- a. Make use of multiprogrammed control unit
- b. Makes use of hardwired control unit
- c. Supports many addressing modes
- d. Has much smaller Cache than CISC processors



Your answer is incorrect.

The correct answer is:

Makes use of hardwired control unit

Question 28

Correct

Mark 1.00 out of 1.00

Which one of the following types of semiconductor memory is used as the main memory in a computer?

- a. Flash
- b. SRAM
- c. PROM
- d. DRAM



Your answer is correct.

The correct answer is:

DRAM

Question 29

Correct

Mark 1.00 out of 1.00

Which of the common cache?

- a. DRAM
- b. SRAM
- c. TLB
- d. Taps



Your answer is correct.

The correct answer is:

TLB

Question 30

Correct

Mark 1.00 out of 1.00

Which one of the following addressing modes are used in an instruction of the form ADD X, Y is?

- a. Immediate
- b. Absolute
- c. Relative
- d. Indirect



Your answer is correct.

The correct answer is:

Absolute

Question 31

Incorrect

Mark 0.00 out of 1.00

Which one of the following can be said about the speed of a multiplier capable of multiplying two 16-bit numbers?

- a. Booth's and array multiplier would be equally fastest
- b. Sign magnitude multiplier would be the fastest
- c. Array multiplier would be the fastest
- d. Booth's multiplier would be the fastest ✖

Your answer is incorrect.

The correct answer is:

Array multiplier would be the fastest

Question 32

Correct

Mark 1.00 out of 1.00

Which one of the following is a major benefit of the Harvard architecture over the von Neumann architecture?

- a. Program written using single word instruction execute more quickly than multiword instructions
- b. None of the mentioned
- c. Code and data can be loaded into the CPU simultaneously on separate buses ✓
- d. Code and data share memory and increase program execution efficiency

Your answer is correct.

The correct answer is:

Code and data can be loaded into the CPU simultaneously on separate buses

Question 33

Correct

Mark 1.00 out of 1.00

Which one of the following types of Interrupts can be caused by an executing program?

- a. Internal
- b. Hardware
- c. Software
- d. External



Your answer is correct.

The correct answer is:

Software

Question 34

Incorrect

Mark 0.00 out of 1.00

Shared memory multiprocessor fit best into which one of the following Flynn's classification of computers?

- a. Multiple instruction, single data stream
- b. Single instruction, multiple data stream
- c. Multiple instruction, multiple data stream
- d. Single instruction, single data stream



Your answer is incorrect.

The correct answer is:

Multiple instruction, multiple data stream

Question 35

Incorrect

Mark 0.00 out of 1.00

Distributed computers belong to which one of the following classes of computers?

- a. MIMD
- b. SISD
- c. MISD ✗
- d. SIMD

Your answer is incorrect.

The correct answer is:

MIMD

Question 36

Correct

Mark 1.00 out of 1.00

The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Writeback (WB). The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each, and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards. What is the number of clock cycles required for the completion of the execution of the sequence of instruction?

- a. 229 cycles
- b. 219 cycles ✓
- c. 221 cycles
- d. 220 cycles

Your answer is correct.

The correct answer is:

219 cycles

Question 37

Incorrect

Mark 0.00 out of 1.00

Vector processors are best classified into which one of the following Flynn's classifications of computers?

- a. Multiple instruction, single data stream
- b. Multiple instruction, multiple data stream
- c. Single instruction, single data stream
- d. Single instruction, multiple data stream



Your answer is incorrect.

The correct answer is:

Single instruction, multiple data stream

Question 38

Incorrect

Mark 0.00 out of 1.00

A computer, whose average memory access time is 20 ns has a page fault service time of 10 ms. For every 100 memory accesses, the one-page fault is generated. The effective access time for the memory in which one of the following?

- a. 30 ns
- b. 20 ns
- c. 45 ns
- d. None of the mentioned



Your answer is incorrect.

The correct answer is:

20 ns

Question 39

Correct

Mark 1.00 out of 1.00

Cache memory is?

- a. Interface between processor and main memory
- b. Interface between processor and SRAM
- c. Interface between processor and virtual memory
- d. Interface between processor and DMA



Your answer is correct.

The correct answer is:

Interface between processor and main memory

Question 40

Correct

Mark 1.00 out of 1.00

Consider the unpipelined machine with 10ns clock cycles. It uses four cycles for ALU operations and branches where as five cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 20%, and 40% respectively. Let due to clock skew and set up pipelining, the machine adds 1 ns of overhead to the clock. How much speed in instruction execution rate will we gain from the pipeline?

- a. 2X
- b. 1X
- c. 3X
- d. 4X



Your answer is correct.

The correct answer is:

4X

Question 41

Incorrect

Mark 0.00 out of 1.00

Which one of the following would cause the Page fault frequency in an operating system to reduce?

- a. Cache memory size is increased
- b. Executing processes exhibit high locality of reference ✖
- c. Size of the page reduced
- d. Executing processes remain CPU-bound

Your answer is incorrect.

The correct answer is:

Executing processes remain CPU-bound

Question 42

Incorrect

Mark 0.00 out of 1.00

Which one of the following multiplexers would have a 4-bit data select input?

- a. 8:1
- b. 4:1 ✖
- c. 16:1
- d. 2:1

Your answer is incorrect.

The correct answer is:

16:1

Question 43

Incorrect

Mark 0.00 out of 1.00

Pipelined processors are the best classified into which one of the following Flynn's classifications of computers?

- a. Single instruction, multiple data stream
- b. Multiple instruction, multiple data stream
- c. Single instruction, single data stream
- d. Multiple instruction, single data stream



Your answer is incorrect.

The correct answer is:

Single instruction, single data stream

Question 44

Correct

Mark 1.00 out of 1.00

in loop Unrolling with Scheduling---. Select the right option.

- a. Use different registers to avoid unnecessary constraints
- b. Identify that loop iterations are independent
- c. Determine the loads and stores that can be interchanged in the unrolled loop
- d. All of the mentioned



Your answer is correct.

The correct answer is:

All of the mentioned

Question 45

Correct

Mark 1.00 out of 1.00

Virtual memory is also known as?

- a. Interface between main memory and secondary memory
- b. All of the mentioned ✓
- c. Cache between main memory and secondary
- d. Buffer between main memory and secondary memory

Your answer is correct.

The correct answer is:

All of the mentioned

Question 46

Incorrect

Mark 0.00 out of 1.00

Which of the following statement most accurately characterizes the responsibility of the memory management unit in the processor?

- a. Managing the interface between the processor and the main memory
- b. Managing the interfacing between main memory and hard disk
- c. Managing the physical memory of the machine
- d. Managing the translation of the virtual into physical address ✗

Your answer is incorrect.

The correct answer is:

Managing the physical memory of the machine

Question 47

Correct

Mark 1.00 out of 1.00

Which one of the following addressing modes cannot be meaningfully used for the destination operand of an ADD instruction?

- a. Indexed
- b. Direct
- c. Indirect
- d. Immediate



Your answer is correct.

The correct answer is:

Indexed

Question 48

Incorrect

Mark 0.00 out of 1.00

When a processor fetches an instruction of the executing program, the binary code of the instruction gets stored in which one of the following?

- a. Program counter
- b. Instruction register
- c. General purpose register
- d. Accumulator



Your answer is incorrect.

The correct answer is:

Program counter

Question 49

Correct

Mark 1.00 out of 1.00

Which one of the following sentences best justifies the need for using a virtual memory operating system?

- a. It help to run multiple programs whose combined size is much larger than the size of the physical memory available on the machine ✓
- b. It help to extend the amount of physical memory that is being used
- c. It allows machines to communicate over a local area network
- d. It help to improve the performance of the hard disk

Your answer is correct.

The correct answer is:

It help to run multiple programs whose combined size is much larger than the size of the physical memory available on the machine

Question 50

Incorrect

Mark 0.00 out of 1.00

What is true for virtual memory?

- a. Processor sends physical address for page table
- b. Processor sends virtual address for main memory ✗
- c. Processor sends physical address for main memory
- d. Processor sends virtual address for page table

Your answer is incorrect.

The correct answer is:

Processor sends virtual address for page table

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Started on Thursday, 22 April 2021, 1:00 PM

State Finished

Completed on Thursday, 22 April 2021, 1:07 PM

Time taken 6 mins 54 secs

Marks 4.00/7.00

Grade **5.71** out of 10.00 (**57%**)

Question **1**

Correct

Mark 1.00 out of 1.00

Cache memory is?

- a. Interface between processor and main memory
- b. Interface between processor and virtual memory
- c. Interface between processor and SRAM
- d. Interface between processor and DMA



Your answer is correct.

The correct answer is:

Interface between processor and main memory

Question **2**

Incorrect

Mark 0.00 out of 1.00

The zero flag register of the MIPS pipeline architecture--

- a. Calculate the effective address by using the program counter register content
- b. Calculate the effective address by adding the register content of the ALU
- c. Calculate the effective address by subtracting the register content of the ALU
- d. Calculate the effective address by using the instruction register content



Your answer is incorrect.

The correct answer is:

Calculate the effective address by subtracting the register content of the ALU

Question 3

Incorrect

Mark 0.00 out of 1.00

Which one of the following about the MIPS rating of a computer is FALSE?

- a. MIPS rating of computer depends on the computer being used
- b. MIPS rating of a computer can very based on which instruction of a processor are being considered
- c. None of the mentioned ✖
- d. MIPS rating of a processor is independent of the program is being executed.

Your answer is incorrect.

The correct answer is:

MIPS rating of a processor is independent of the program is being executed.

Question 4

Incorrect

Mark 0.00 out of 1.00

For the load and store operation ---

- a. Effective address is calculated at 4th stage of the pipeline
- b. Effective address is calculated between 4th and 5th stage of the pipeline ✖
- c. Effective address is calculated at 3rd stage of the pipeline
- d. Effective address is calculated between 3rd and 4th stage of the pipeline

Your answer is incorrect.

The correct answer is:

Effective address is calculated at 3rd stage of the pipeline

Question 5

Correct

Mark 1.00 out of 1.00

Which one of the following options most correctly lists the important parts of a Von Neumann computer?

- a. Hard disks, buses, and CPU
- b. Memory, CPU, buses, and printers
- c. Memory, input/output units, and CPU
- d. Buses, memory, and input/output controllers



Your answer is correct.

The correct answer is:

Memory, input/output units, and CPU

Question 6

Correct

Mark 1.00 out of 1.00

The von Neumann bottleneck can be attributed to which one of the following?

- a. Slow speed of input/output devices
- b. Mismatch between the speed of the secondary and primary storages
- c. Low clock speeds
- d. Mismatch between the speed of the CPU and primary storages



Your answer is correct.

The correct answer is:

Mismatch between the speed of the CPU and primary storages

Question 7

Correct

Mark 1.00 out of 1.00

In MIPS architecture, the program counter send the address multiple of 4 due to --

- a. Word addressability of memory
- b. Bit addressability of memory
- c. Nibble addressability of memory
- d. Byte addressability of memory



Your answer is correct.

The correct answer is:

Byte addressability of memory

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Started on Friday, 26 March 2021, 1:35 PM

State Finished

Completed on Friday, 26 March 2021, 1:50 PM

Time taken 14 mins 57 secs

Marks 8.00/20.00

Grade 4.00 out of 10.00 (40%)

Question 1

Incorrect

Mark 0.00 out of 1.00

In which one of the following addressing modes, the content of the program counter is added to the address part of the instruction in order to obtain the effective address.

- a. Register addressing mode
- b. Indexed addressing mode ✗
- c. Absolute addressing mode
- d. Register indirect addressing mode

Your answer is incorrect.

The correct answer is:

Register indirect addressing mode

Question 2

Correct

Mark 1.00 out of 1.00

An instruction cycle refers to which one of the following?

- a. Decoding the instruction and calculation of effective address
- b. Executing an instruction
- c. Fetching an instruction
- d. All of the mentioned ✓

Your answer is correct.

The correct answer is:

All of the mentioned

Question 3

Correct

Mark 1.00 out of 1.00

Which one of the following most profoundly describes the functionality of the control unit in CPU?

- a. To perform the arithmetic operations based on decoded program instruction
- b. To store program instruction
- c. To generate the control signals based on decoded program instructions
- d. To perform logic operations based on decoded program instructions



Your answer is correct.

The correct answer is:

To generate the control signals based on decoded program instructions

Question 4

Incorrect

Mark 0.00 out of 1.00

Which one of the following statements about a computer supporting unaligned data access is most accurate regarding the storage of data items having sizes that may not be multiples of the word size.

- a. Data transfer is inefficient and data also storage in memory would not be efficient
- b. Data transfer is efficient and also data can be stored efficiently in memory
- c. Data transfer is inefficient but data can be stored efficiently in memory
- d. Data transfer is efficient but data storage in memory would not efficient.



Your answer is incorrect.

The correct answer is:

Data transfer is inefficient but data can be stored efficiently in memory

Question 5

Incorrect

Mark 0.00 out of 1.00

The content of the multiplicand register and the multiplier register of a hardware circuit implementing Booth's algorithm is the binary numbers 111001 and 111100 what would be the result produced by the multiplier circuitry (Decimal)

- a. -1828
- b. 1812
- c. 28 ✗
- d. -28

Your answer is incorrect.

The correct answer is:

1812

Question 6

Incorrect

Mark 0.00 out of 1.00

A booth's multiplier circuit needs to inspect at most how many LSB bits to determine whether to add the multiplier, subtract the multiplier or leave the partial result unchanged during any step in the sequence of multiplication steps?

- a. Two bits ✗
- b. All bits of the multiplicand
- c. All bits of the multiplier
- d. One bit

Your answer is incorrect.

The correct answer is:

One bit

Question 7

Incorrect

Mark 0.00 out of 1.00

Divide overflow is easiest to handle in which one of the following circuits implementing division?

- a. Fixed point 2's complement division
- b. Floating point division
- c. Fixed point 1's complement division
- d. Fixed point sign magnitude division



Your answer is incorrect.

The correct answer is:

Floating point division

Question 8

Correct

Mark 1.00 out of 1.00

In order to realize an adder that can add two 16-bit numbers, how many full adders and half adders would be required?

- a. One half adder and 15 full adders
- b. 17 half adders and 0 full adder
- c. 15 half adders and one full adder
- d. 10 half adders and 11 full adders



Your answer is correct.

The correct answer is:

One half adder and 15 full adders

Question 9

Incorrect

Mark 0.00 out of 1.00

Which one of the following can be said about the speed of a multiplier capable of multiplying two 16-bit numbers?

- a. Booth's and array multiplier would be equally fastest
- b. Sign magnitude multiplier would be the fastest
- c. Array multiplier would be the fastest
- d. Booth's multiplier would be the fastest



Your answer is incorrect.

The correct answer is:

Array multiplier would be the fastest

Question 10

Correct

Mark 1.00 out of 1.00

In the implementation of a binary multiplier circuit, which one of the following set of logic gates is used?

- a. 2 input AND gates only
- b. XOR gates and shift registers
- c. 2 input X-or gates and 2-input AND gates
- d. 2-input NOR gates and 1 XOR gate



Your answer is correct.

The correct answer is:

2 input X-or gates and 2-input AND gates

Question 11

Incorrect

Mark 0.00 out of 1.00

A computer has a word size of 16-bit and has 16 programmer visible registers. each instruction has two sources and one destination operands and uses only register direct addressing mode. what is the maximum number of op-codes that this processor can have?

- a. 64
- b. 32 ✗
- c. 16
- d. 8

Your answer is incorrect.

The correct answer is:

16

Question 12

Incorrect

Mark 0.00 out of 1.00

After fetching an instruction from memory, the binary code of the instruction is stored in which one of the following?

- a. Accumulator ✗
- b. Program counter
- c. Instruction pointer
- d. Instruction register

Your answer is incorrect.

The correct answer is:

Instruction register

Question 13

Incorrect

Mark 0.00 out of 1.00

The IR store which one of the following?

- a. An instruction that has been executed
- b. An instruction that has been fetched from the memory
- c. The address of the next instruction to be executed
- d. An instruction that has been decoded



Your answer is incorrect.

The correct answer is:

An instruction that has been fetched from the memory

Question 14

Correct

Mark 1.00 out of 1.00

Cache memory is?

- a. Interface between processor and DMA
- b. Interface between processor and SRAM
- c. Interface between processor and main memory
- d. Interface between processor and virtual memory



Your answer is correct.

The correct answer is:

Interface between processor and main memory

Question 15

Correct

Mark 1.00 out of 1.00

Which of the common cache?

- a. Taps
- b. DRAM
- c. TLB
- d. SRAM



Your answer is correct.

The correct answer is:

TLB

Question 16

Correct

Mark 1.00 out of 1.00

-----is the concept in which a process is copied into the main memory from the secondary memory according to the requirement.

- a. Pagging
- b. None of the mentioned
- c. Demand pagging
- d. Segmentation



Your answer is correct.

The correct answer is:

Demand pagging

Question 17

Incorrect

Mark 0.00 out of 1.00

When an instruction is required to be brought from memory to CPU, on which one of the following busses is it fetched?

- a. Peripheral bus
- b. Control bus
- c. Data bus
- d. Address bus ✖

Your answer is incorrect.

The correct answer is:

Data bus

Question 18

Incorrect

Mark 0.00 out of 1.00

Consider a three address RISC processor ISA. Which one of the following correctly characterizes an effect of doubling the number of registers in the processor?

- a. Instruction size would be increase by 2-bit
- b. Instruction size would be increase by 1-bit
- c. Instruction size would be increase by 3-bit
- d. Instruction size would be unaffected ✖

Your answer is incorrect.

The correct answer is:

Instruction size would be increase by 3-bit

Question 19

Correct

Mark 1.00 out of 1.00

Swap space exists in _____

- a. DRAM
- b. Primary memory
- c. Secondary memory
- d. None of the mentioned



Your answer is correct.

The correct answer is:

Secondary memory

Question 20

Incorrect

Mark 0.00 out of 1.00

If the page hit is there in the page table then?

- a. Data can be directly accessed from main memory without address translation
- b. Data can be directly accessed from disc
- c. Data can be directly accessed from main memory after the address translation
- d. None of the mentioned



Your answer is incorrect.

The correct answer is:

Data can be directly accessed from main memory after the address translation

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Started on Tuesday, 2 February 2021, 10:20 AM

State Finished

Completed on Tuesday, 2 February 2021, 10:59 AM

Time taken 39 mins 34 secs

Marks 24.00/35.00

Grade **6.86** out of 10.00 (**69%**)

Question 1

Correct

Mark 1.00 out of 1.00

In the J-type instructions of MIPS --

- a. One operand is provided as a part of the instruction and other operand need to be fetched from memory
- b. Both operands are not available in the register bank
- c. Both the operands are available in the register bank
- d. One operand is provided as a part of the instruction and other operand need to be get from accumulator



Your answer is correct.

The correct answers are:

Both the operands are available in the register bank,

One operand is provided as a part of the instruction and other operand need to be fetched from memory

Question 2

Incorrect

Mark 0.00 out of 1.00

Forwarding can be implemented in 5-stage and 6-stage MIPS pipeline --

- a. Using three multiplexers
- b. Using two multiplexers with extra latch
- c. Using two multiplexers
- d. Using one multiplexer



Your answer is incorrect.

The correct answer is:

Using two multiplexers

Question 3

Correct

Mark 1.00 out of 1.00

The features of the RISC processor --

- a. Instruction execute in one or two clock cycle
- b. Small number of addressing modes
- c. Small number of the instructions
- d. All of the mentioned



Your answer is correct.

The correct answer is:

All of the mentioned

Question 4

Correct

Mark 1.00 out of 1.00

The shortfall of registers created by aggressive unrolling and scheduling is also known as --

- a. Register pressure
- b. Aggressive scaling
- c. Forwarding
- d. Miss rate



Your answer is correct.

The correct answer is:

Register pressure

Question 5

Correct

Mark 1.00 out of 1.00

Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 5 ns. What is the Pipeline cycle time?

- a. 105 ns
- b. 75 ns
- c. 100 ns
- d. 95 ns



Your answer is correct.

The correct answer is:

95 ns

Question 6

Incorrect

Mark 0.00 out of 1.00

In MIPS architecture, increasing the number of stages --

- a. Will always improve the performance after the optimal value of the stages
- b. Will always decrease the performance.
- c. Will always improve the performance.
- d. Will improve the performance up to optimal value of the stages and beyond the optimal value it will decrease



Your answer is incorrect.

The correct answers are:

Will always decrease the performance.,

Will improve the performance up to optimal value of the stages and beyond the optimal value it will decrease

Question 7

Correct

Mark 1.00 out of 1.00

For calculating the effective address, the upper 6 bits and concatenation done between---

- a. Program counter and constant value which was the part of the instruction
- b. Program counter and constant value which was not the part of the instruction
- c. Address register and constant value which was the part of the instruction
- d. Address register and constant value which was not the part of the instruction



Your answer is correct.

The correct answer is:

Program counter and constant value which was the part of the instruction

Question 8

Correct

Mark 1.00 out of 1.00

Using booth's algorithms multiply 7 with 3 and assume register AC is 4 bit. The value of AC after 3rd and 4th cycles are

- a. 0 1 1 1 0 and 1 0 1 0 0
- b. 0 0 1 1 and 1 0 1 1
- c. 0 0 1 0 and 1 0 1 0
- d. 1 0 1 0 and 1 0 1 0



Your answer is correct.

The correct answer is:

0 0 1 0 and 1 0 1 0

Question 9

Correct

Mark 1.00 out of 1.00

What is the two times shift right of the binary stream 0 1 0 1 1 1 1 0 1?

- a. 0 1 0 1 1 1 1 0 0
- b. 0 1 0 1 1 1 1 0 1
- c. 0 0 0 1 0 1 1 1 1
- d. None of the mentioned



Your answer is correct.

The correct answer is:

0 0 0 1 0 1 1 1 1

Question 10

Incorrect

Mark 0.00 out of 1.00

The following assembly program is run over the MIPS pipeline architecture. Choose the wrong option.

Assembly code:

- i1. pp1: L.D F0,0(R1);
- i2. ADD.D F4,F0,F2;
- i3. S.D F4,0(R1);
- i4. DADDUI R1,R1,#-8;
- i5. BNE R1,R2,pp1

- a. i2 is used for adding scalar value ✖
- b. i4 is used as an increment pointer
- c. i3 is used to store the results
- d. i1 is used for array element



Your answer is incorrect.

The correct answers are:

i1 is used for array element,

i4 is used as an increment pointer

Question 11

Incorrect

Mark 0.00 out of 1.00

A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The number of and gates required to design full adders are?

- a. Nine
- b. Twelve X
- c. Eight
- d. Ten

Your answer is incorrect.

The correct answer is:

Nine

Question 12

Incorrect

Mark 0.00 out of 1.00

A pipelined processor has seven stages, namely, IF1, IF2, ID, EX, MEM1, MEM2, WB. Assuming all the stages require the same amount of time and the time period of the non- pipelined processors is 14 ns, find out the clock frequency and speedup of the pipelined processor. Assume the delay of the latches is 1 ns.

- a. 1Khz and 50
- b. 1.2 Khz and 30 X
- c. 1 Khz and 3
- d. None of the mentioned

Your answer is incorrect.

The correct answer is:

None of the mentioned

Question 13

Correct

Mark 1.00 out of 1.00

For the code given below, select the wrong answer.

MIPS Code:

1. add r1, r2, r3
2. sub r4, r1, r5

- a. Data hazard is present
- b. One stalls is required to remove the data hazard ✓
- c. For the second instruction, operands are required at 3rd stage of the pipeline
- d. There will be no hazard for the first instruction

Your answer is correct.

The correct answer is:

One stalls is required to remove the data hazard

Question 14

Correct

Mark 1.00 out of 1.00

The instruction ADD Rd,Rs, Rt is ---

- a. R-type instruction of MIPS
- b. I-type instruction of MIPS
- c. P-type instruction of MIPS
- d. J-type instruction of MIPS ✗

Your answer is correct.

The correct answer is:

R-type instruction of MIPS

Question 15

Incorrect

Mark 0.00 out of 1.00

Consider the following instruction sequence five-stage pipeline,

ADD R1, R2, R1 --- I1

LW R2,0(R1) --- I2

LW R1,4(R1) -- I3

OR R3, R1, R2 -- I4

Select the correct option.

- a. RAW hazards is present in instructions I1-I2
- b. All of the mentioned
- c. RAW hazards is present in instructions I2-I3
- d. RAW hazards is present in instructions I3-I4



Your answer is incorrect.

The correct answer is:

All of the mentioned

Question 16

Incorrect

Mark 0.00 out of 1.00

In MIPS architecture, the program counter send the address multiple of 4 due to --

- a. Bit addressability of memory
- b. Byte addressability of memory
- c. Nibble addressability of memory
- d. Word addressability of memory



Your answer is incorrect.

The correct answer is:

Byte addressability of memory

Question 17

Incorrect

Mark 0.00 out of 1.00

For the code given below choose the wrong answer.

MIPS Code:

1. ADD r1, r2, r3
2. SUB r4, r1, r5
3. AND r6, r1, r7
4. OR r8, r1, r9
5. XOR r10, r1, r11

- a. Using split phase of the clock, data hazard can be eliminated from instruction no. fifth
- b. Using split phase of the clock, data hazard can be eliminated from instruction no. fourth
- c. Using split phase of the clock, data hazard can be eliminated from instruction no. second
- d. Direct data dependence is there



Your answer is incorrect.

The correct answer is:

Using split phase of the clock, data hazard can be eliminated from instruction no. second

Question 18

Correct

Mark 1.00 out of 1.00

If multiplicand (M) is 0111, the AC register is initialized with zero. What will be the content of the AC register after operation $AC = AC - M$?

- a. 1100
- b. 1111
- c. 1010
- d. 1001



Your answer is correct.

The correct answer is:

1001

Question 19

Incorrect

Mark 0.00 out of 1.00

Pipelining of a MIPS-like Processor, select the right option

- a. All ALU operations are performed on register operands
- b. All of the mentioned ✓
- c. Separate Instruction and data memory is required
- d. Only instructions which access memory are load and store instructions

Your answer is incorrect.

The correct answer is:

All of the mentioned

Question 20

Correct

Mark 1.00 out of 1.00

For the code given below. Select the right option.

```
if p1 {  
    S1;  
}  
if p2 {  
    S2;  
}
```

- a. S1 cannot be moved before the branch ✓
- b. S1 is control dependent on p1, but S2 is not control dependent on p1
- c. S2 cannot be moved after the branch
- d. All of the mentioned

Your answer is correct.

The correct answers are: S1 is control dependent on p1, but S2 is not control dependent on p1, S1 cannot be moved before the branch,
All of the mentioned

Question 21

Correct

Mark 1.00 out of 1.00

In the MIPS architecture, data transfer takes place between --

- a. Register to memory
- b. Register to register
- c. Memory to register
- d. All of the mentioned



Your answer is correct.

The correct answer is:

All of the mentioned

Question 22

Correct

Mark 1.00 out of 1.00

In the MIPS architecture, the meaning of the instruction can be found from --

- a. Accumulator register
- b. Instruction register
- c. Program counter register
- d. Address register



Your answer is correct.

The correct answer is:

Instruction register

Question 23

Correct

Mark 1.00 out of 1.00

The zero flag register of the MIPS pipeline architecture--

- a. Calculate the effective address by adding the register content of the ALU
- b. Calculate the effective address by subtracting the register content of the ALU
- c. Calculate the effective address by using the instruction register content
- d. Calculate the effective address by using the program counter register content



Your answer is correct.

The correct answer is:

Calculate the effective address by subtracting the register content of the ALU

Question 24

Correct

Mark 1.00 out of 1.00

During 1 clock cycle, the pipeline (5-stage) can process --

- a. 4 different instructions
- b. 6 different instructions
- c. 5 different instructions
- d. None of the mentioned



Your answer is correct.

The correct answer is:

5 different instructions

Question 25

Correct

Mark 1.00 out of 1.00

What is the arithmetic shift right operation after the 1st cycle for the following binary stream 1 0 0 1 0 0 1 1 0 ?

- a. 1 0 0 1 0 0 1 1 0
- b. 1 1 0 0 1 0 0 1 1
- c. 0 1 1 0 0 1 0 0 1
- d. 1 1 1 0 0 1 0 0 1



Your answer is correct.

The correct answer is:

1 1 0 0 1 0 0 1 1

Question 26

Incorrect

Mark 0.00 out of 1.00

CACHE memory act as an interface between---

- a. Processor hardware and main memory
- b. Processor hardware and I/O



Your answer is incorrect.

The correct answer is:

Processor hardware and main memory

Question 27

Correct

Mark 1.00 out of 1.00

in loop Unrolling with Scheduling---. Select the right option.

- a. Identify that loop iterations are independent
- b. Use different registers to avoid unnecessary constraints
- c. Determine the loads and stores that can be interchanged in the unrolled loop
- d. All of the mentioned



Your answer is correct.

The correct answer is:

All of the mentioned

Question 28

Correct

Mark 1.00 out of 1.00

A four-stage pipeline has stage delays of 150, 120, 160, and 140 ns respectively. Registers are used between the stages and have a delay of 10 ns each. What is the cycle time?

- a. 140 ns
- b. 170 ns
- c. 165 ns
- d. 155 ns



Your answer is correct.

The correct answer is:

170 ns

Question 29

Incorrect

Mark 0.00 out of 1.00

Which unit is responsible for directing the operations of computer arithmetic and logical unit?

- a. I/O interface
- b. ALU itself
- c. Control unit
- d. Program



Your answer is incorrect.

The correct answer is:

Control unit

Question 30

Correct

Mark 1.00 out of 1.00

What is the shift right of the binary stream 0 1 0 1 1 1 1 0 1?

- a. 0 0 1 0 1 1 1 0 1
- b. 0 0 1 0 1 1 1 1 1
- c. 0 0 1 0 1 1 1 1 0
- d. 1 0 1 0 1 1 1 1 0



Your answer is correct.

The correct answer is:

0 0 1 0 1 1 1 1 0

Question 31

Correct

Mark 1.00 out of 1.00

In the MIPS pipeline architecture forwarding/bypassing is ----

- a. Software based approach
- b. Hardware based approach
- c. Combination of both hardware & software based approach
- d. DMA based approach



Your answer is correct.

The correct answer is:

Hardware based approach

Question 32

Correct

Mark 1.00 out of 1.00

For the program given below the number of stalls required after the code transformed by the smart compiler are

MIPS Code:

1. LW R2, 0(R4)
2. LW R5, 4(R4)
3. ADD R1, R2, R3

- a. One
- b. Three
- c. Two
- d. No stall is required



Your answer is correct.

The correct answer is:

No stall is required

Question 33

Correct

Mark 1.00 out of 1.00

For the load and store operation ---

- a. Effective address is calculated at 3rd stage of the pipeline
- b. Effective address is calculated between 4th and 5th stage of the pipeline
- c. Effective address is calculated at 4th stage of the pipeline
- d. Effective address is calculated between 3rd and 4th stage of the pipeline



Your answer is correct.

The correct answer is:

Effective address is calculated at 3rd stage of the pipeline

Question 34

Correct

Mark 1.00 out of 1.00

Addressing modes are used to calculate the effective address by using the --

- a. Control Unit
- b. DMA
- c. ALU unit only
- d. ALU + control unit



Your answer is correct.

The correct answer is:

ALU + control unit

Question 35

Correct

Mark 1.00 out of 1.00

For the code given below identifies the data hazard.

Code:

```
add r1, r2, r3  
sub r1, r4, r5
```

- a. None of the mentioned
- b. WAW
- c. RAW
- d. WAR



Your answer is correct.

The correct answer is:

WAW

◀ Announcements

Jump to...

CS-208: Mid-Sem Online Test ►

Started on Thursday, 15 April 2021, 1:00 PM**State** Finished**Completed on** Thursday, 15 April 2021, 1:30 PM**Time taken** 29 mins 56 secs**Marks** 15.00/25.00**Grade** **6.00** out of 10.00 (**60%**)**Question 1**

Complete

Mark 0.00 out of 1.00

Assumed that pipeline is optimized for branches when the branch is taken in program,

How many pipelines bubble on a taken branch in the ALP.

26 sub \$11, \$5, \$9

30 beq \$2, \$4, 8

34 and \$13, \$3, \$6

38 or \$14, \$3, \$7

42 add \$15, \$5, \$3

46 slt \$16, \$7, \$8

...

52 lw \$5, 51(\$8)

 a. 2 b. 4 c. 1 d. 0

Question 2

Complete

Mark 1.00 out of 1.00

MBR \leftarrow PC

MAR \leftarrow X

PC \leftarrow Y

Memory \leftarrow MBR

Which one of the following is a possible operation performed by this sequence?

- a. Operand fetch
- b. Conditional branch
- c. Instruction fetch
- d. Initiation of interrupt service

Question 3

Complete

Mark 1.00 out of 1.00

When executing this program using Tomasulo's algorithm, Find out last clock cycle

LD F2, 8(R3)

LD F4, 8(R3)

MULTD F10, F2, F4

LD F6, 10(R3)

LD F8, 12(R3)

MULTD F12, F6, F8

ADDD F12, F10, F12

- a. 25
- b. 22
- c. 24
- d. 19

Question 4

Complete

Mark 0.00 out of 1.00

Which decimal number is used by this single-precision float?

- a. -5.0
 - b. -7.0
 - c. -4.0
 - d. -6.0

Question 5

Complete

Mark 1.00 out of 1.00

Out of order execution is used in?

- a. **Scoreboard algorithm**
 - b. **None of the mentioned**
 - c. **Scoreboard and Tomasulo algorithm**
 - d. **Tomasulo algorithm**

Question 6

Complete

Mark 0.00 out of 1.00

How many data hazards are available in between "SUB" and "SW" in the following assemble program.

sub \$3, \$2, \$4

and \$13, \$3, \$6

or \$14, \$7, \$3

add \$15 \$3 \$3

sw. \$16,100(\$3)

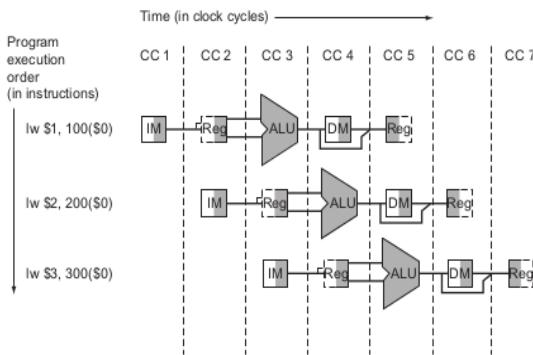
- a. 2
 - b. 4
 - c. 1
 - d. 0

Question 7

Complete

Mark 1.00 out of 1.00

Which memory is used during one of the five stages of instruction?



- a. Data
- b. Register
- c. None of the mentioned
- d. Instruction

Question 8

Complete

Mark 0.00 out of 1.00

Consider three-branch prediction schemes: predict not taken, predict taken, and dynamic prediction. Assume that they all have zero penalties when they predict correctly and two cycles when they are wrong. Assume that the average predicted accuracy of the dynamic predictor is 90%. Which predictor is the best choice for the following branches?

- a. None of the mentioned
- b. A branch that is taken with 5% frequency
- c. A branch that is taken with 95% frequency
- d. A branch that is taken with 70% frequency

Question 9

Complete

Mark 1.00 out of 1.00

The principle of pipelining is?

- a. Parallelism
- b. None of the mentioned
- c. Overlapping
- d. Serial

Question 10

Complete

Mark 0.00 out of 1.00

For the load and store operation ---

- a. Effective address is calculated at 3rd stage of the pipeline
- b. Effective address is calculated between 4th and 5th stage of the pipeline
- c. Effective address is calculated at 4th stage of the pipeline
- d. Effective address is calculated between 3rd and 4th stage of the pipeline

Question 11

Complete

Mark 1.00 out of 1.00

Which one of the following addressing modes cannot be meaningfully used for the destination operand of an ADD instruction?

- a. Indexed
- b. Immediate
- c. Indirect
- d. Direct

Question 12

Complete

Mark 1.00 out of 1.00

In the J-type instructions of MIPS --

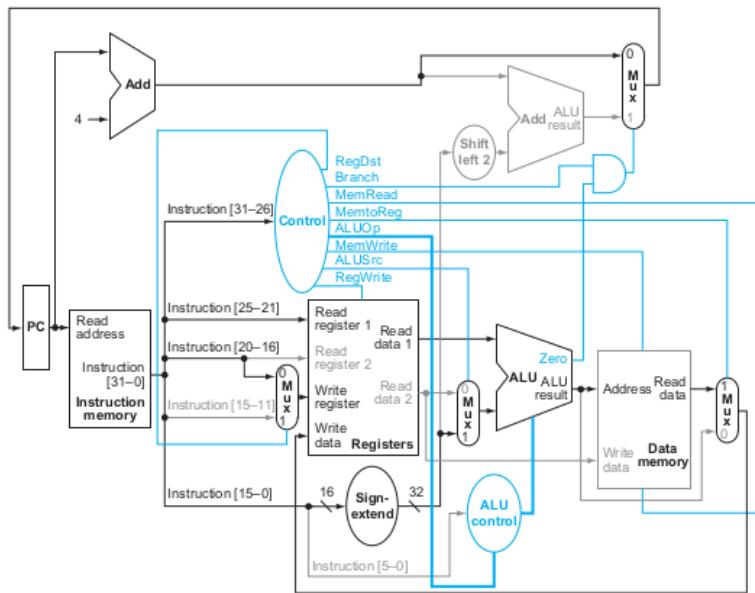
- a. Both operands are not available in the register bank
- b. One operand is provided as a part of the instruction and other operand need to be fetched from memory
- c. Both the operands are available in the register bank
- d. One operand is provided as a part of the instruction and other operand need to be get from accumulator

Question 13

Complete

Mark 0.00 out of 1.00

Which type of datapath architecture is given in the following



- a. With Load instruction
- b. I-type of instruction
- c. None of the mentioned
- d. R-type of instruction

Question 14

Complete

Mark 0.00 out of 1.00

Consider the following code segment:

Load R1,Loc1; Load R1 from memory location Loc1

Load R2, Loc2; Load R2 from memory location Loc2

Add R1, R2, R1; Add R1 and R2 and save the result in R1

Dec R2; Decrement R2

Dec R1; Decrement R1

Mpy R1,R2, R3; Multiply R1 and R2 and store in R3

Store R3, Loc3; Store r3 in Memory Location Loc3

What is the number of cycles needed to execute the above code segment assuming each instruction takes one cycle to execute?

- a. 14
- b. 7
- c. 10
- d. 13

Question 15

Complete

Mark 1.00 out of 1.00

What is ISA?

- a. Interface between hardware and sensors
- b. Interface between hardware and RAM
- c. Interface between hardware and software
- d. Interface between hardware and DMA

Question 16

Complete

Mark 1.00 out of 1.00

How many binary digits are required to show the IEEE 754 binary representation of the number -0.75 base 10 in single precision?

- a. 28
- b. 30
- c. 32
- d. 31

Question 17

Complete

Mark 1.00 out of 1.00

Pipeline performance is measured by?

- a. Ripple factor
- b. K-Factor
- c. Speed up factor
- d. QE factor

Question 18

Complete

Mark 0.00 out of 1.00

When executing this program using Tomasulo's algorithm, Find out the last clock cycle

LD F1, 7(R2)
LD F3, 7(R2)
MULTD F9, F1, F3
LD F5, 9(R2)
LD F7, 11(R2)
MULTD F11, F5, F7
ADDD F11, F9, F11
LD F9, 11(R2)
ADDD F11, F11, F9

- a. 22
- b. 23
- c. None of the mentioned
- d. 21

Question 19

Complete

Mark 1.00 out of 1.00

Consider a 6-stage instruction pipeline, where all stages are perfectly balanced. Assume that there is no cycle-time overhead of pipelining. When an application is executing on this 6-stage pipeline, the speedup achieved with respect to non-pipelined execution if 50% of the instructions incur 2 pipeline stall cycles is?

- a. 6
- b. 4
- c. 3
- d. 7

Question 20

Complete

Mark 0.00 out of 1.00

Register renaming is used in?

- a. Pipeline Forwarding technique
- b. DRAM memory
- c. Loop unrolling
- d. Virtual memory

Question 21

Complete

Mark 1.00 out of 1.00

For computers based on three-address instruction formats, each address field can be used to specify which of the following:

- S1: A memory operand
- S2: A processor register
- S3: An implied accumulator register

a. **Only S2 and S3**

b. **Either S2 or S3**

c. **S1, S2 and S3**

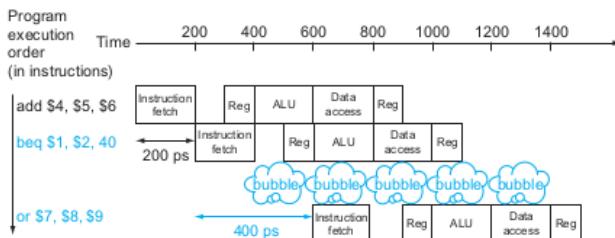
d. **Either S1 or S2**

Question 22

Complete

Mark 1.00 out of 1.00

Which type of hazards represents the given figure given below?



a. Data hazard

b. Structural

c. None of the mentioned

d. Control

Question 23

Complete

Mark 1.00 out of 1.00

Booth's algorithm is used for?

- a. Octal multiplication
- b. Decimal multiplication
- c. Binary multiplication
- d. String multiplication

Question 24

Complete

Mark 0.00 out of 1.00

Match the following

- | | |
|------------------------------------|--|
| X. Indirect Addressing | I. Array implementation |
| Y. Indexed Addressing | II. Writing re-locatable code |
| Z. Base Register Addressing | III. Passing array as parameter |

- a. (X, I) (Y, III) (Z, II)
- b. (X, III) (Y, II) (Z, I)
- c. (X, III) (Y, I) (Z, II)
- d. (X, II) (Y, III) (Z, I)

Question 25

Complete

Mark 1.00 out of 1.00

When an instruction is required to be brought from memory to CPU, on which one of the following busses is it fetched?

- a. Control bus
- b. Address bus
- c. Peripheral bus
- d. Data bus

[◀ Lab-9 and Lab-10 Evaluation](#)[Jump to...](#)

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Started on Wednesday, 7 April 2021, 1:35 PM

State Finished

Completed on Wednesday, 7 April 2021, 1:50 PM

Time taken 14 mins 53 secs

Marks 20.00/25.00

Grade **8.00** out of 10.00 (**80%**)

Question **1**

Complete

Mark 1.00 out of 1.00

The contention for the usage of a hardware device is called _____

- a. Stalk
- b. Optimized compilers
- c. Deadlock
- d. Structural hazard

Question **2**

Complete

Mark 0.00 out of 1.00

_____ occurs when an instruction depends on the result of a previous instruction. But its result is not yet available.

- a. Data Hazards
- b. None of the mentioned
- c. Structural Hazards
- d. Control Hazards

Question **3**

Complete

Mark 1.00 out of 1.00

The pipelining process is also known as _____

- a. Assembly line operation
- b. Superscalar operation
- c. Dependency
- d. Von Neumann cycle

Question 4

Complete

Mark 1.00 out of 1.00

Which of the following is not a pipeline conflict?

- a. Data Dependency
- b. Timing variation
- c. Load balancing
- d. Branching

Question 5

Complete

Mark 1.00 out of 1.00

The periods of time when the unit is idle is called as _____

- a. Hazards
- b. Bubbles
- c. Both Stalls and Bubbles
- d. Stalls

Question 6

Complete

Mark 0.00 out of 1.00

The control signals to read instruction memory and to write the PC are always asserted, so there is nothing special to control in this pipeline stage.

- a. Instruction fetch
- b. Memory access
Memory access
Memory access
- c. Write back
- d. decoding

Question 7

Complete

Mark 0.00 out of 1.00

The error in the following code is:

Code:

```
main()
{
    cycles = 0;
    for (i = 1 to the number of instructions);
    {
        for (j = 1 to instructions[i]);
        {
            cycles = cycles - 1;
        }
    }
    output results (cycles * cycle length);
}
```

- a. cycles = cycles - 1;
- b. for (i = 1 to the number of instructions);
- c. for (j = 1 to instructions[i]);
- d. output results (cycles * cycle length);

Question 8

Complete

Mark 1.00 out of 1.00

An important compiler technique to get more performance from loops is _____

- a. Data transfer instruction
- b. latency
- c. CPI
- d. loop unrolling

Question 9

Complete

Mark 1.00 out of 1.00

Pipelining is a technique that exploits ___ among the instructions in a sequential instruction stream.

- a. Dynamic branch prediction
- b. single instruction
- c. multiple instruction
- d. Parallelism

Question 10

Complete

Mark 1.00 out of 1.00

The stalling of the processor due to the unavailability of the instructions is called as _____

- a. Control hazard
- b. Structural hazard
- c. None of the mentioned
- d. Input hazard

Question 11

Complete

Mark 1.00 out of 1.00

The time lost due to the branch instruction is often referred to as _____

- a. Branch penalty
- b. Delay
- c. Deadlock
- d. Latency

Question 12

Complete

Mark 1.00 out of 1.00

Number of clock cycles between a load instruction and an instruction that can use the result of the load without stalling the pipeline

- a. latency
- b. Efficiency
- c. Gain of instruction
- d. Throughput

Question 13

Complete

Mark 1.00 out of 1.00

The stage, which places the result back into the register file in the middle of the datapath

- a. decoding
- b. Instruction fetch
- c. Memory access
- d. Write back

Question 14

Complete

Mark 0.00 out of 1.00

 hazards caused by access of memory (resources) by two segments at the same time.

- a. None of the mentioned
- b. Data hazards
- c. Structural hazards
- d. Control hazards

Question 15

Complete

Mark 1.00 out of 1.00

A ___ is a small memory indexed by the lower portion of the address of the branch instruction.

- a. Branch prediction buffer
- b. **Dynamic branch prediction**
- c. **prediction branch**
- d. **Dynamic branch**

Question 16

Complete

Mark 1.00 out of 1.00

How many types of pipelining exist?

- a. 2
- b. 5
- c. 3
- d. 4

Question 17

Complete

Mark 1.00 out of 1.00

in loop Unrolling with Scheduling---. Select the right option.

- a. All of the mentioned
- b. Determine the loads and stores that can be interchanged in the unrolled loop
- c. Use different registers to avoid unnecessary constraints
- d. Identify that loop iterations are independent

Question 18

Complete

Mark 1.00 out of 1.00

For software pipeline. Select the right option.

- a. Less memory space is required
- b. Speed is high
- c. All of the mentioned
- d. Independent instructions can be part of pipeline loop body

Question 19

Complete

Mark 1.00 out of 1.00

The situation wherein the data of operands are not available is called _____

- a. Stock
- b. Deadlock
- c. Structural hazard
- d. Data hazard

Question 20

Complete

Mark 1.00 out of 1.00

Which of the following is an advantage of pipelining?

- a. Pipelining increases the overall performance of CPU
- b. Faster ALU can be designed with pipelining
- c. Instruction throughput increases
- d. All of the mentioned

Question 21

Complete

Mark 1.00 out of 1.00

_____ have been developed specifically for pipelined systems.

- a. None of the mentioned
- b. Speed up utilities
- c. Utility software
- d. Optimizing compilers

Question 22

Complete

Mark 1.00 out of 1.00

A _____ is a cycle in the pipeline without new input.

- a. CPI
- b. latency
- c. stall
- d. forwarding

Question 23

Complete

Mark 1.00 out of 1.00

Any condition that causes a processor to stall is called as _____

- a. System error
- b. Hazard
- c. None of the mentioned
- d. Page fault

Question 24

Complete

Mark 1.00 out of 1.00

In the Arithmetic pipeline, the floating-point addition and subtraction are done in ___ parts.

- a. 4
- b. 2
- c. 5
- d. 3

Question 25

Complete

Mark 0.00 out of 1.00

For the program given below the number of stalls required after the code transformed by the smart compiler are

MIPS Code:

1. LW R2, 0(R4)
2. LW R5, 4(R4)
3. ADD R1, R2, R3

- a. One
- b. Two
- c. Three
- d. Zero

[◀ Lab-5 and Lab-6 Evaluation](#)

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Started on Wednesday, 10 March 2021, 1:40 PM

State Finished

Completed on Wednesday, 10 March 2021, 1:50 PM

Time taken 9 mins 58 secs

Question 1

Complete

Marked out of 1.00

Ratio of CPU clock cycles for a program to the clock time is

- a. CPU time
- b. UPI
- c. CPI
- d. Instruction count

Question 2

Complete

Marked out of 1.00

How many bits are in the (1,3) branch predictor with 2K entries?

- a. 4K
- b. 5K
- c. 12K
- d. 1K

Question 3

Complete

Marked out of 1.00

What is the decimal value of this 32-bit two's complement number? (1111 1111 1111 1111 1111 1111 1100**)_{base2}**

a. (-9)_{base10}

b. (-8)_{base10}

c. (-6)_{base10}

d. (-4)_{base10}

Question 4

Complete

Marked out of 1.00

Consider two instructions m and n, with m preceding n in program order. The possible data hazards are ___, n tries to read a source before m writes it, so n incorrectly gets the old value.

a. WAR

b. RAR

c. RAW

d. WAW

Question 5

Complete

Marked out of 1.00

A non pipelined processor has a clock rate of 2.5 GHz and an average CPI (Cycle per instruction) of 4. An upgrade to the processor introduces a five-stage pipeline. However, due to internal pipeline delays, such as latency delay the clock rate of the new processor has to be reduced to 2 GHz. What is the speedup achieved for a typical program?

a. 4

b. 3

c. 4.8

d. 3.8

Question 6

Complete

Marked out of 1.00

A micro control unit is required to generate a total of 25 control signals. Assume that during any microinstruction at most two control signals are active minimum no of bits required in the control word to generate the control signal will be

- a. 12
- b. 10
- c. 2.5
- d. 2

Question 7

Complete

Marked out of 1.00

Which of the following is not a valid segment of four-stage instruction pipeline?

- a. DA
- b. DO
- c. EX
- d. FI

Question 8

Complete

Marked out of 1.00

___ hazards are present only in pipelines that write in more than one pipe stage or allow instruction to proceed even when a previous instruction is stalled.

- a. RAW
- b. WAR
- c. WAW
- d. RAR

Question 9

Complete

Marked out of 1.00

A computer architect is designing the memory system for the next version of a processor. IF the current version of the processor spends 40 percent of its time processing memory references, by how much must the architect speed up the memory system to achieve an overall speedup of 1.2?

- a. 1.07
- b. 1.01
- c. 1.71
- d. 1.51

Question 10

Complete

Marked out of 1.00

Which of the following is an advantage of pipelining?

- a. Pipelining increases the overall performance of the CPU.
- b. All of the mentioned
- c. Instruction throughput increases.
- d. Faster ALU can be designed when pipelining is used.

Question 11

Complete

Marked out of 1.00

How many branch-selected entries are in a (3,3) predictor that has a total of 24K bits in the prediction buffer?

- a. 3K
- b. 4K
- c. 2K
- d. 1K

Question 12

Complete

Marked out of 1.00

All processors use pipelining to overlap the execution of instructions and improve performance. This potential overlap among instructions is called

- a. All of the above
- b. Loop-Level Parallelism
- c. instruction-level parallelism
- d. Data-Level Parallelism

Question 13

Complete

Marked out of 1.00

A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speedup ratio of the pipeline for 100 tasks.

 a. **100/21** b. **4/21** c. **21/4** d. **21/100**

Question 14

Complete

Marked out of 1.00

Consider two instructions m and n, with m preceding n in program order. The possible data hazards are _____, n tries to write a destination before it is read by m, so m incorrectly gets the new value.

 a. **RAW** b. **WAR** c. **WAW** d. **RAR**

Question 15

Complete

Marked out of 1.00

Computer A has an Instruction count of 20 billion, a Clock rate of 8 GHz, and CPI of 1 then what is MIPS.

- a. 3K
- b. 2K
- c. 7K
- d. 8K

Question 16

Complete

Marked out of 1.00

A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. What is the maximum speedup that can be achieved for 100 tasks?

- a. 10
- b. 6
- c. 5
- d. 7

Question 17

Complete

Marked out of 1.00

Suppose we have two implementations of the same instruction set architecture. Computer A has a clock cycle time of 500 ps and a CPI of 1.2 for some programs, and computer B has a clock cycle time of 250 ps and a CPI of 2.0 for the same program. Which computer is faster for this program and by how much?

- a. Computer B is 1.2 times as fast as computer A
- b. Computer A is 2 times as fast as computer B
- c. Computer A is 1.2 times as fast as computer B
- d. Computer B is 2 times as fast as computer A

Question 18

Complete

Marked out of 1.00

Find the correct sequence to perform any instruction in four-stage pipelining. a. DA, FI, EX, FO b. FI, DA, EX, FO c. FI, DA, FO, EX d. FI, FO, DA, EX**Question 19**

Complete

Marked out of 1.00

Each stage in pipelining should be completed within _____ cycle. a. 1 b. 2 c. 1.5 d. 3

Question 20

Complete

Marked out of 1.00

In the arithmetic pipeline, consider the first number's exponent is 4 and the second number's exponent is 6. Which exponent will be selected after comparing both?

- a. 2
- b. 4
- c. 6
- d. 10

[◀ Lab 3 and Lab 4 online test](#)

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[Lab-7 and Lab-8 Evaluation ►](#)

Started on Wednesday, 10 February 2021, 1:40 PM

State Finished

Completed on Wednesday, 10 February 2021, 1:48 PM

Time taken 7 mins 59 secs

Grade 6.00 out of 10.00 (60%)

Question 1

Complete

Mark 1.00 out of 1.00

What will be the right shift of 01111111 after 8 cycles?

- a. 01111111
- b. 0000001
- c. 11111111
- d. None of the mentioned

Question 2

Complete

Mark 1.00 out of 1.00

If LSB bit of Q and Q₋₁ are equal then the operation performed by the Booth's algorithm is

- a. AC =AC +M
- b. None of the mentioned
- c. Shift right
- d. AC =AC - M

Question 3

Complete

Mark 1.00 out of 1.00

What is the three times shift right of the binary stream 0 1 0 1 1 1 1 0 1?

- a. 0 0 1 0 1 1 1 1 0 1
- b. 0 1 0 1 1 1 1 0 1
- c. 1 1 0 1 1 1 1 0 1
- d. None of the mentioned

Question 4

Complete

Mark 1.00 out of 1.00

A 16-bit ripple carry adder is realized using 16 identical full adders. The carry propagation delay of each full adder is 12 ns and the sum propagation delay of each full adder is 15 ns. The worst case delay of this 16 bit adder will be ____?

- a. 192 ns
- b. 190 ns
- c. None of the mentioned
- d. 193 ns

Question 5

Complete

Mark 0.00 out of 1.00

Ripple carry adder is ?

- a. Parallel adder
- b. Sum and carry are parallel available
- c. None of the mentioned
- d. Serial adder

Question 6

Complete

Mark 1.00 out of 1.00

The Ripple carry adder is designed and fabricated based on

- a. None of the mentioned
- b. V Technology
- c. R technology
- d. L Technology

Question 7

Complete

Mark 0.00 out of 1.00

The parallel multipliers like radix 2 and radix 4 modified booth multiplier does the computations using

- a. More adders and lesser iterative steps
- b. lesser adders and more iterative steps
- c. lesser adders and lesser iterative steps
- d. more adders and more iterative steps

Question 8

Complete

Mark 0.00 out of 1.00

The program given below

```
Begin
    Condition:
    1. If Qn and Qn+1 are same i.e. 00 or 11 perform arithmetic shift by 1 bit.
    2. If Qn Qn+1 = 10 do A= A + BR and perform arithmetic shift by 1 bit.
    3. If Qn Qn+1 = 01 do A= A - BR and perform arithmetic shift by 2 bit.
```

End

- a. Condition 1 not true
- b. None of the mentioned
- c. Condition 2 not true
- d. Condition 3 is True

Question 9

Complete

Mark 1.00 out of 1.00

What is the arithmetic shift right operation after the 3nd cycle for the following binary stream 1 0 0 1 0 0 1 1 0 ?

- a. 1 1 0 1 0 0 1 1 0
- b. 1 0 0 1 0 0 1 1 0
- c. None of the mentioned
- d. 0 0 0 0 1 0 0 1 1 0

Question 10

Complete

Mark 0.00 out of 1.00

Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N-bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit in which the carry-out of each full adder is

- a. N-1 Adder output
- b. N-2 Adder output
- c. N-3 Adder output
- d. None of the mentioned

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[Lab-5 and Lab-6 Evaluation ►](#)