Started on	Friday, 18 February 2022, 1:40 PM
State	Finished
Completed on	Friday, 18 February 2022, 1:47 PM
Time taken	6 mins 36 secs
Marks	5.00/7.00
Grade	**7.14** out of 10.00 (**71**%)

Question **1**

Complete

Mark 0.00 out of 1.00

A machine (31-bit architecture, with 1-word long instructions) has 64 registers, each register is 32 bits long. It needs to support 45 instructions, which have an immediate operand in addition to two register operands. Assuming that the immediate operand is an unsigned integer, what is the maximum value of the immediate operand?

- a. 26383
- b. 16383
- c. 16333
- d. None of the mentioned

Question **2**

Complete

Mark 1.00 out of 1.00

_____ register specifically holds the _____ and provides it to instruction decoder circuit

- a. **Memory and instruction**
- b. **Instruction and instruction**
- c. **data and instruction**
- d. **instruction and data**

Question **3**

Complete

Mark 1.00 out of 1.00

The components to design the data path architecture ?

- a. Control unit and MUX
- b. ALU, MUX, Registres
- c. None of the mentioned
- d. ALU, Control unit, program counter

Question **4**

Complete

Mark 0.00 out of 1.00

Which unit is responsible for directing the operations of computer arithmetic and logical unit?

- a. Control Unit
- b. Multiplexer
- c. ALU by itself
- d. Program Counter

Question **5**

Complete

Mark 1.00 out of 1.00

An instruction register is the part of a CPU's control unit that holds the _____ currently being executed

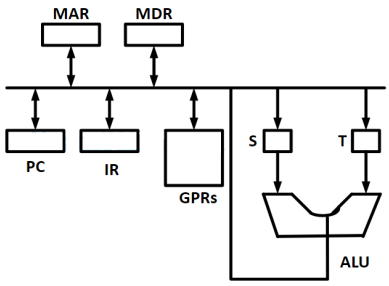
- a. **instruction**
- b. **address**
- c. **data**
- d. None of the mentioned

Question **6**

Complete

Mark 1.00 out of 1.00

Consider the following data path of a cpu:



In the above data path size of bus, ALU and all registers are equal. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU.

Two clock cycles are needed for memory read operation- one is for loading address in MAR and one for loading data from memory but into MDR.

The instruction "call Rn,sub" is a two word instruction. Assume that program counter is incremented during the fetch cycle of the first word of the instruction, it's register transfer interpretation is

Rn <= PC + 1;

PC <= M[PC];

The no. of minimum number of CPU clock cycles required in the execution cycle of this instruction?

- a. 3
- b. 1
- c. 4
- d. 2

Question **7**

Complete

Mark 1.00 out of 1.00

In a system, which has 32 registers the register id is _____ long?

- a. 4 bit
- b. 5 bit
- c. 6 bit
- d. 16 bit

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