Design Assignment #1

(Deadline: 11:59PM PDT, April 28, 2017)

Name (Last, First):

Student Id #:

INSTRUCTIONS

NOTE: This design assignment is to be done individually using EDA Playground. https://www.edaplayground.com. You should have already gone through the startup guide.

SUBMISSION PROCEDURE: You need to submit your solution online via Gradescope. https://www.gradescope.com/courses/4278 (code: MDZ4EM). The website will automatically grade your submission.

DESIGN PROCEDURE: Note that for each Verilog design task a dassignX_X.v and optionally dassignX_X.tb are provided. The .v file contains the module you are to design. This file may contain the testbench. You are to fill in these modules for each design task. The .tb file is an explicit testbench that tests your design. You should use the testbench to exhaustively test your designs for all possible input combinations where possible. Note that these files have module names and interface signal names already defined. These MUST NOT be changed (deleted from or added to) in any way - doing so will in all likelihood result in a design that will not comply with the grading program and thus result in a zero score. Similarly, you cannot change the filename.

Design Task #1

File provided: *dassign1_1.v*

Write the Verilog modules for the following logic gates: 2-input NAND, 3-input NAND, 2-input NOR, 3-input NOR, 2-input XOR, INV, and MUX. The code for the wrappers is shown. Then write the structural Verilog that matches the design in Problem #1 in Homework #1. Compare the results of the structural design with the logical expression you derived in the Homework to show that the structural results match.

Design Task #2

File provided: *dassign1_2.v*

Write the Verilog module that implements the logical functions *Y* and *Z* in Problem #4(a) and (b) of Homework #1 as an assign statement. Verify your results with a simulation.

Design Task #3

File provided: *dassign1_3.v*

Write the Verilog module that implements the logic in Problem #2 of Homework #1 as a case statement where x[3:0]={A,B,C,D}. Verify your results with a simulation.

EE89 Students: Design Task

Synthesize the design of Design Task #3 using Vivado (Xilinx FPGA Design Environment). Compile the design for the Basys3 board and show the logic functionality to the TA during laboratory hours.