Digital Engineering
Project Task 1

Y3890959
Y3878784

28th February 2023

Task 2: Clock domain crossing using dual-clock FIFOs

1 - Description of FSMs

SOURCE_CTRL FSM

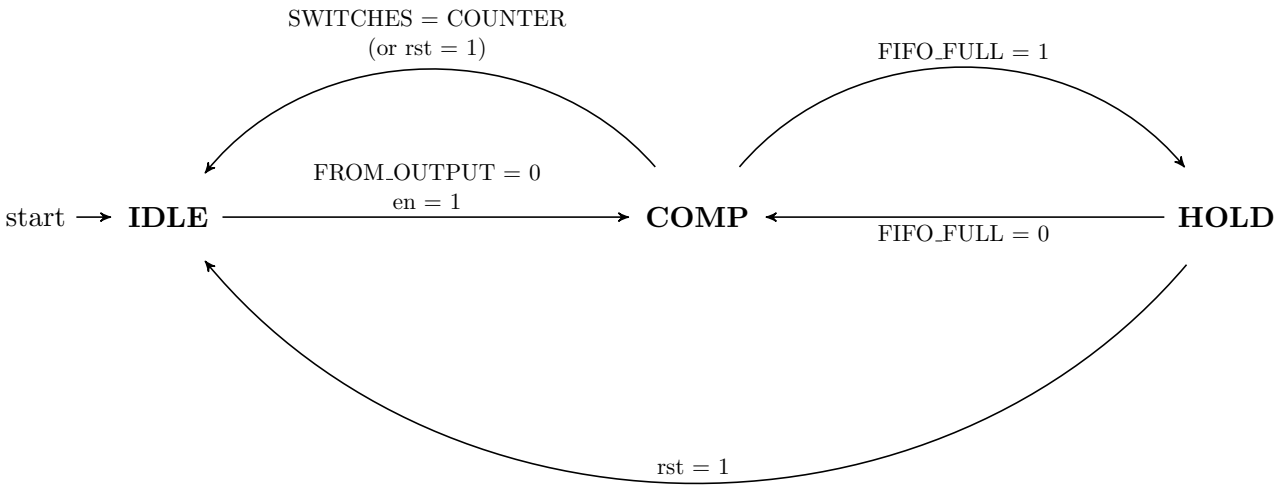

Figure 1: SOURCE_CTRL FSM state graph

The FSM starts at IDLE state, where all internal signals will reset and the LEDs are off. When the 'en' pushbutton is pressed and the output logic FSM has completed (FROM_SOURCE goes low) the state goes to COMP where the outputs are computed. As soon as 'en' is toggled, when the FSM is still in IDLE, the values of the SWITCHES is stored in a register 'LIMT_REG'. In the COMP state, the 'LIMT_CNT' is enabled and counts, 'EN_SOURCE' also goes high so the outputs are computed, and the 'FIFO_WR_EN' goes high so the values are stored.