Digital Engineering
Project Task 1

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28th February 2023

Task 1: Clock management through enable signals

1 - FSM Description

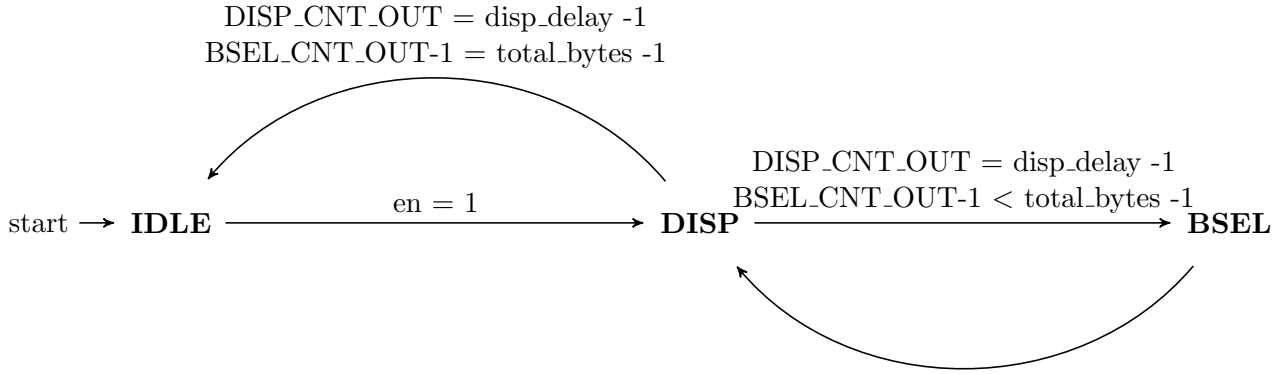

Figure 1: FSM state graph

The FSM starts in the IDLE state, when the user presses the enable 'en' pushbutton, the state goes to DISP. As soon as the DISP state is reached, and the DISP_CNT for the LED delay and BSEL_CNT byte index counter are reset to 0, 'EN_SOURCE' goes high computing the next value in the sequence. Once the display delay has reached its max value and there are still more bytes to display, the BSEL state is selected, otherwise, once the delay is complete and all bytes have been displayed, the logic goes back to the IDLE state. In the BSEL state, the BSEL counter is incremented.

STATE	***EN_SOURCE***	***DISP_CNT_EN***	***DISP_CNT_RST***	***BSEL_CNT_EN***	***BSEL_CNT_RST***	***LED_DISPLAY***
IDLE	0	0	1	0	1	00000000
DISP	1 when DISP_CNT_OUT and DISP_CNT_OUT = 0	1	0	0	0	SOURCE_DATA[7:0] when DISPL_CNT_OUT is 0
						SOURCE_DATA[15:8] when DISPL_CNT_OUT is 1
	0 otherwise					SOURCE_DATA[23:16] when DISPL_CNT_OUT is 2
						SOURCE_DATA[31:24] when DISPL_CNT_OUT is 3
BSEL	0	0	1	1	0	00000000

Table 1: FSM table of outputs