ECE3421/6421 Spring 2020
Prof. L. Wang Name_____

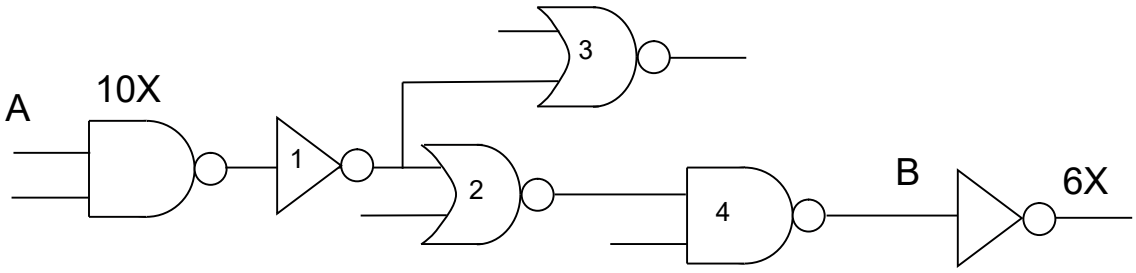
EXAM TWO

11:15AM-12:30PM, Wednesday, April 15, 2020
(Note: 12:30PM is the deadline for uploading your work to HuskyCT)

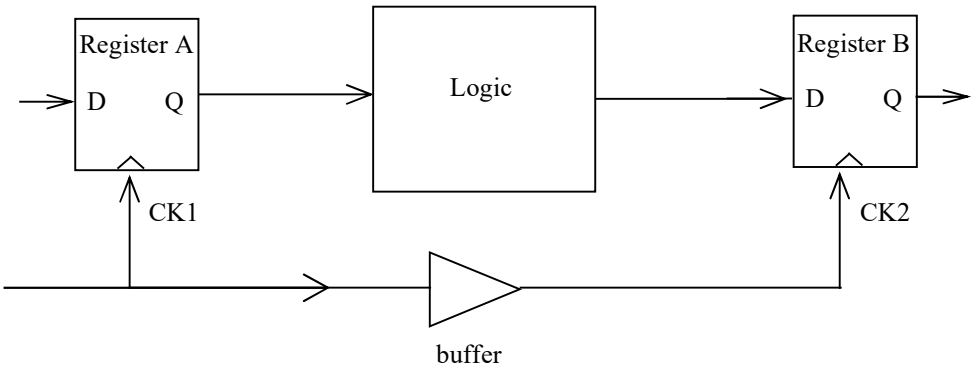
Please show all work so that partial credit can be given. GIVE UNITS FOR ALL NUMERICAL ANSWERS, IF APPLICATLBE!

1	(30)	
2	(20)	
3	(20)	
4	(30)	
Total	(100)	

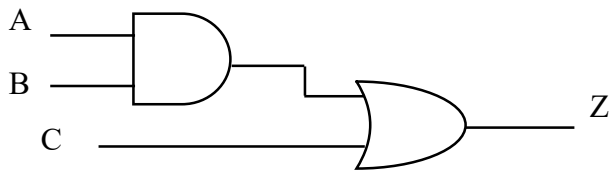
1. (30) For the circuit below, use the logical effort method to find the sizes of gates 1, 2, and 4 that minimize the path delay from A to B. Assume that gates 2 and 3 have the same size. The input NAND gate at A has been sized by a factor of 10X and the load inverter at B has been sized by a factor of 6X.



2. (20) For the circuit below, Register A has setup time of 6ps, hold time of 5ps, CK-to-Q delay of 3ps. Register B has setup time of 8ps, hold time of 10ps, CK-to-Q delay of 4ps. The delay of the buffer is 7ps.
   (a) Assume the clock cycle is 50ps. Determine the largest delay t_d^{max} of the logic to avoid setup time failures.
   (b) For the same clock cycle, determine the smallest delay t_d^{min} of the logic to avoid hold time failures.



3. (20) For the circuit below, assume that inputs A, B, C are independent and uniformly distributed.
   (a) Determine the switching activity α at node Z. Ignore the glitching effect.
   (b) Now connect B and C together, so that B and C become one input, called D. Inputs A and D are independent and uniformly distributed. Determine the switching activity α at node Z again. Ignore the glitching effect.



4. (30 points) Consider a two-input dynamic NOR gate and a two-input static NOR gate. The inputs of these NOR gates are A and B with ideal voltage waveforms shown below (assume these waveform patterns will repeat over time). Draw the output waveforms (assume zero gate propagation delays) and determine the capacitive power dissipation for both NOR gates. V_{DD} = 5V, f_{CK} = 500MHz, and C_{load} = 30fF.