TWO BIT MULTIPLIER

Design:

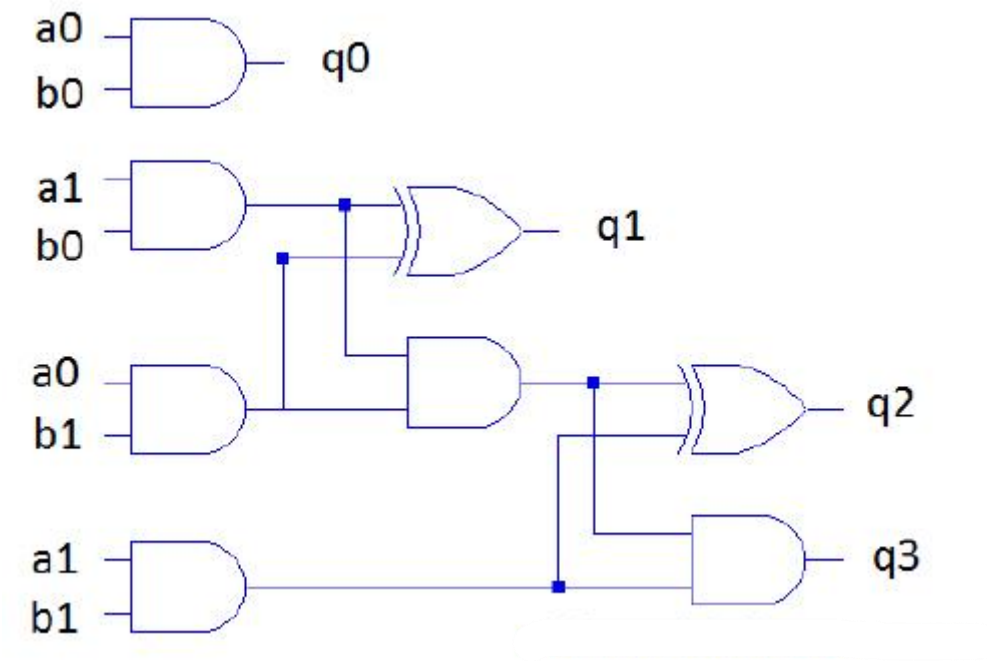


Figure 1 2bit multiplier

x_0	x_1	x_2	x_3	f_0	f_1	f_2	f_3
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

Figure 2 truthtable

verilog code:

```
module HA(input a,b, output sum,cout );
   assign sum = a^b;
   assign cout = a&b;
   endmodule

module two_bit_mul(input a0,a1,b0,b1,output [3:0]y);
wire w1,w2,w3,c1;
and g1(w1,a1,b0);
and g2(w2,a0,b1);
and g3(y[0],a0,b0);
and g4(w3,a1,b1);
HA h1(w1,w2,y[1],c1);
HA h2(w3,c1,y[2],y[3]);
endmodule
```

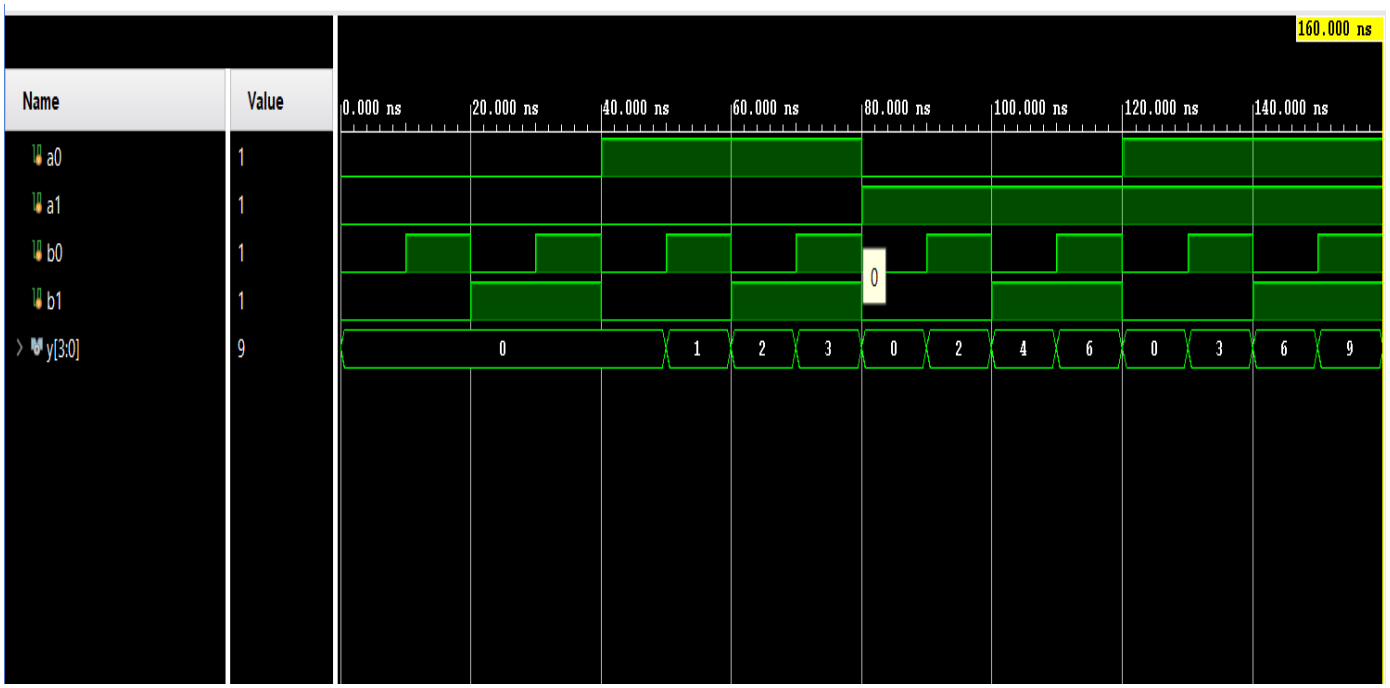


Figure 3 waveforms

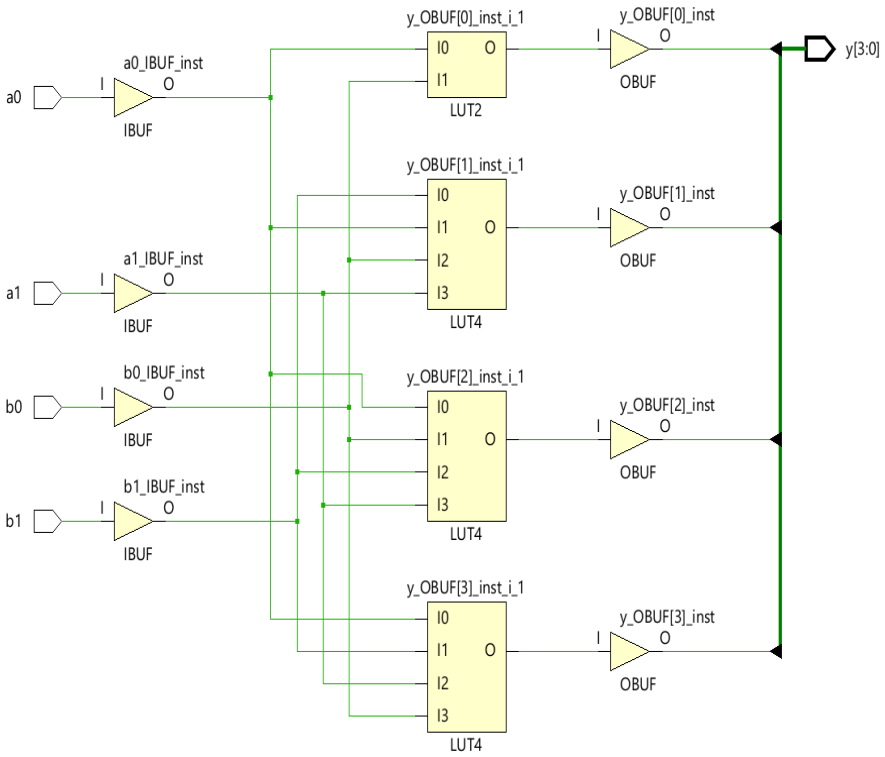


Figure 4synthesis schematic

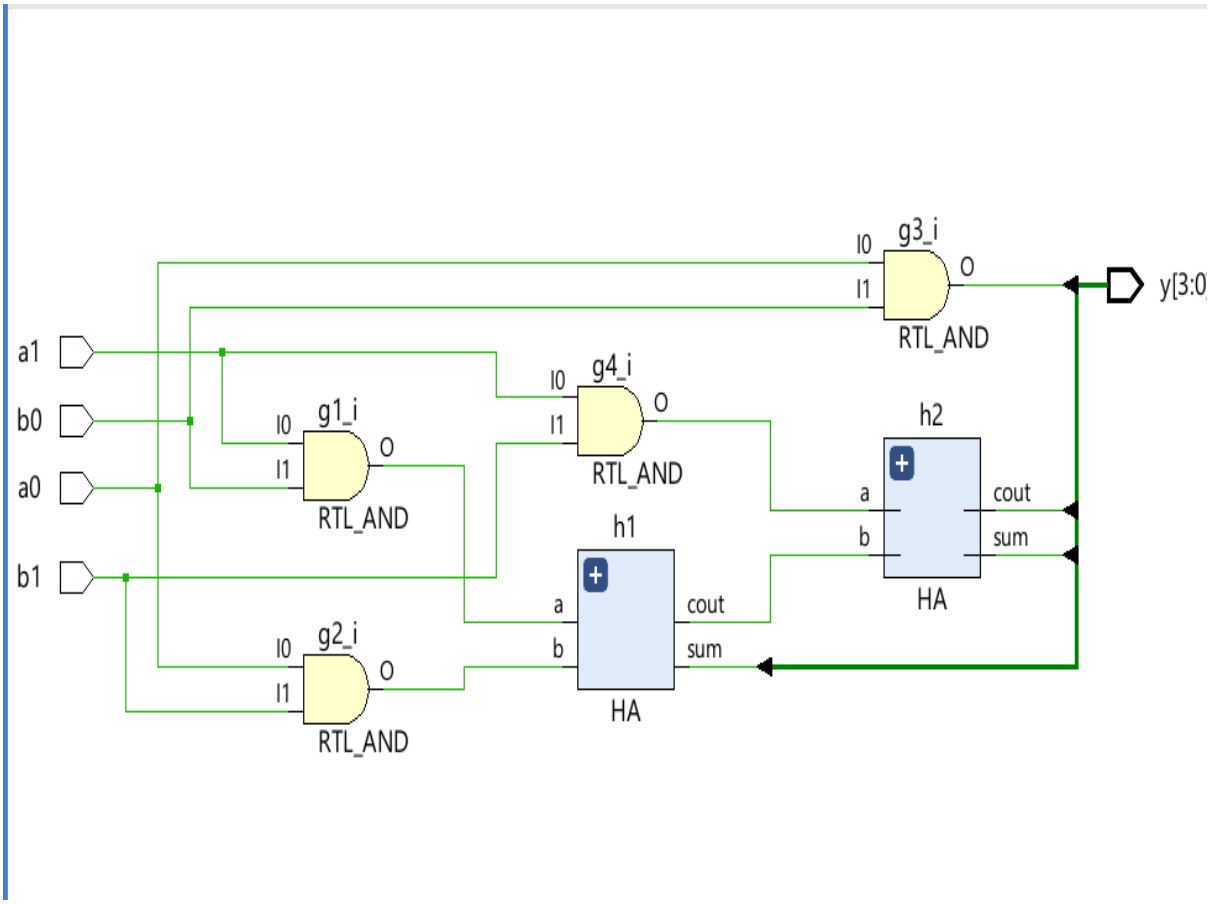
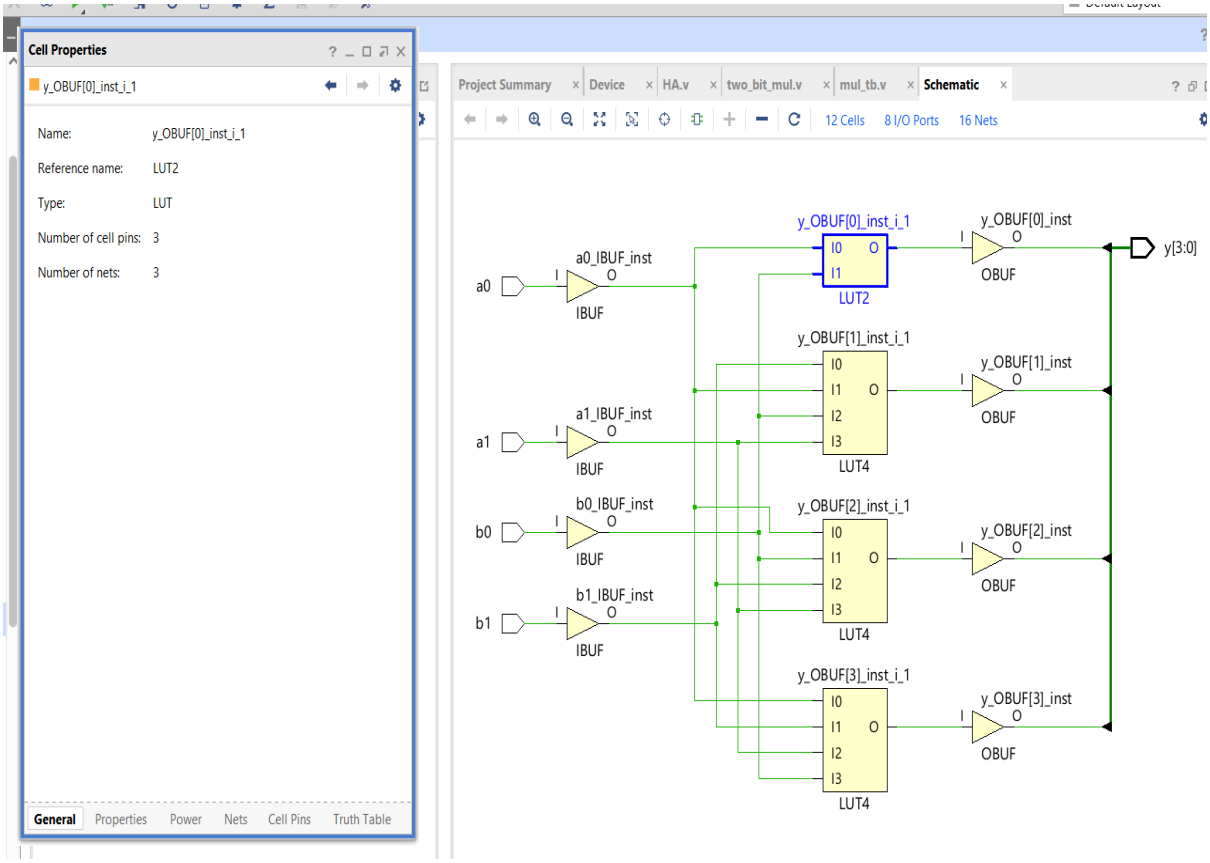
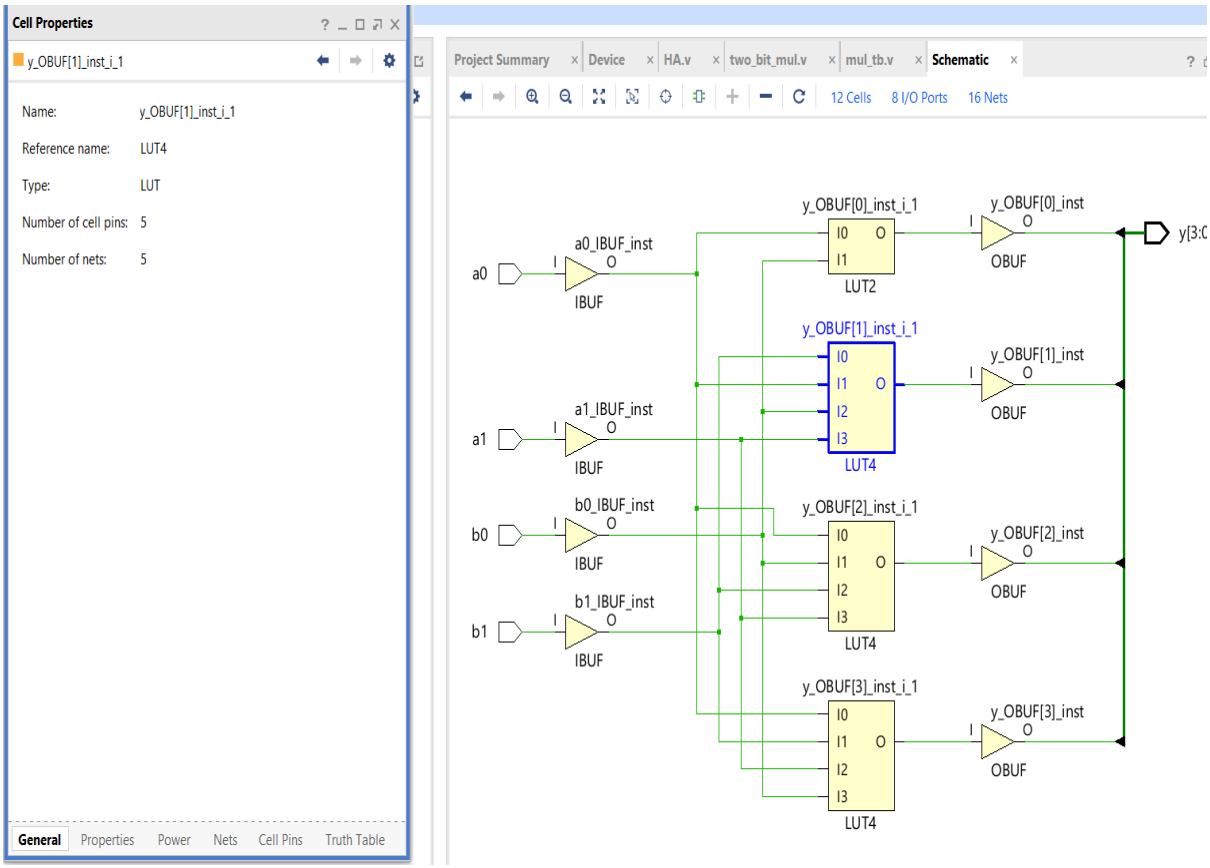
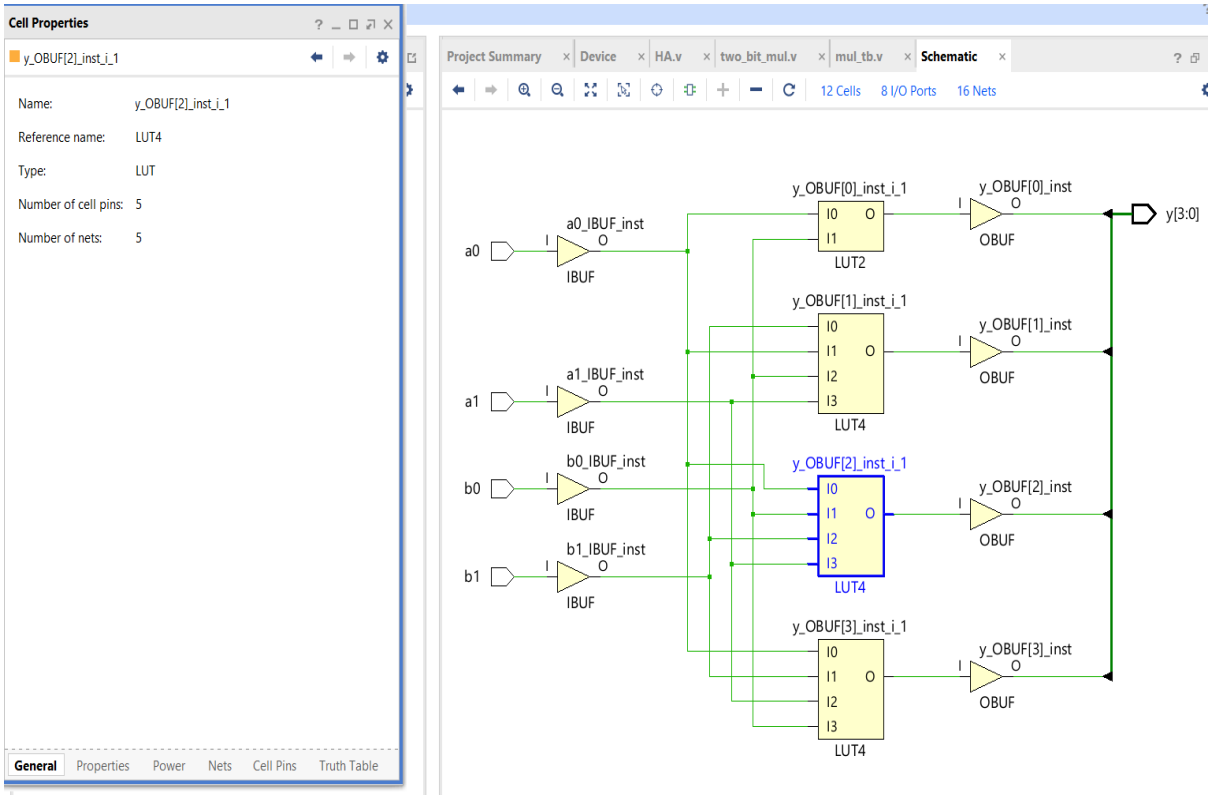
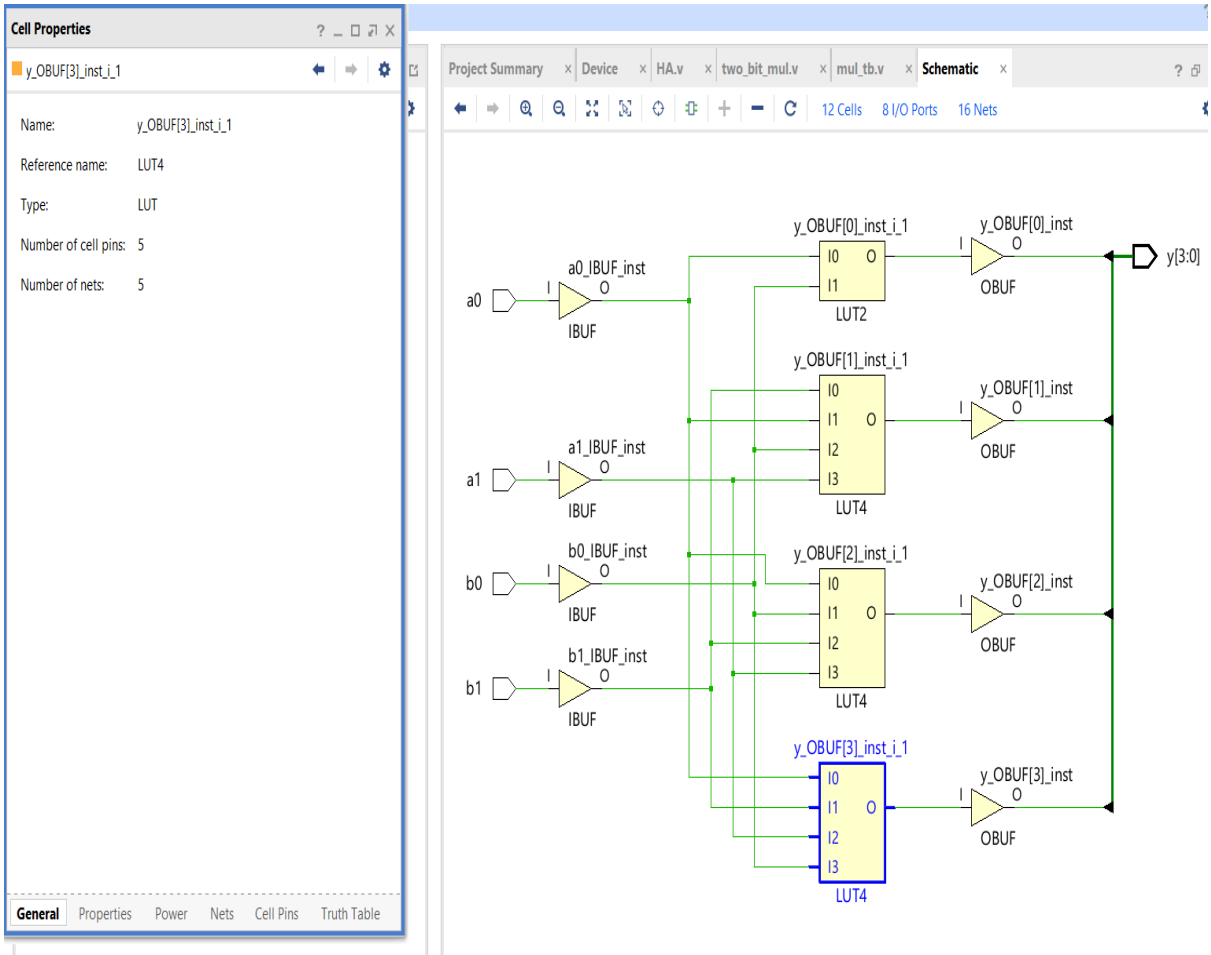


Figure 5 rtl schematic


Cell Properties
y_OBUF[0]_inst_i_1
Name: y_OBUF[0]_inst_i_1
Reference name: LUT2
Type: LUT
Number of cell pins: 3
Number of nets: 3
General Properties Power Nets Cell Pins Truth Table
Project Summary Device HA.v two_bit_mul.v mul_tb.v Schematic
12 Cells 8 I/O Ports 16 Nets
a0
a1
b0
b1
a0_IBUF_inst
a1_IBUF_inst
b0_IBUF_inst
b1_IBUF_inst
IBUF
y_OBUF[0]_inst_i_1
y_OBUF[1]_inst_i_1
y_OBUF[2]_inst_i_1
y_OBUF[3]_inst_i_1
LUT2
LUT4
y_OBUF[0]_inst
y_OBUF[1]_inst
y_OBUF[2]_inst
y_OBUF[3]_inst
OBUF
y[3:0]


Cell Properties
y_OBUF[1]_inst_i_1
Name: y_OBUF[1]_inst_i_1
Reference name: LUT4
Type: LUT
Number of cell pins: 5
Number of nets: 5
General Properties Power Nets Cell Pins Truth Table
Project Summary Device HA.v two_bit_mul.v mul_tb.v Schematic
12 Cells 8 I/O Ports 16 Nets
a0
a1
b0
b1
a0_IBUF_inst
a1_IBUF_inst
b0_IBUF_inst
b1_IBUF_inst
IBUF
y_OBUF[0]_inst_i_1
y_OBUF[1]_inst_i_1
y_OBUF[2]_inst_i_1
y_OBUF[3]_inst_i_1
LUT2
LUT4
y_OBUF[0]_inst
y_OBUF[1]_inst
y_OBUF[2]_inst
y_OBUF[3]_inst
OBUF


Cell Properties
y_OBUF[2]_inst_i_1
Name: y_OBUF[2]_inst_i_1
Reference name: LUT4
Type: LUT
Number of cell pins: 5
Number of nets: 5
General Properties Power Nets Cell Pins Truth Table
Project Summary Device HA.v two_bit_mul.v mul_tb.v Schematic
12 Cells 8 I/O Ports 16 Nets
a0 a1 b0 b1
a0_IBUF_inst a1_IBUF_inst b0_IBUF_inst b1_IBUF_inst
IBUF
y_OBUF[0]_inst_i_1
LUT2
y_OBUF[1]_inst_i_1
y_OBUF[2]_inst_i_1
y_OBUF[3]_inst_i_1
LUT4
y_OBUF[0]_inst y_OBUF[1]_inst y_OBUF[2]_inst y_OBUF[3]_inst
OBUF
y[3:0]


Cell Properties
y_OBUF[3]_inst_i_1
Name: y_OBUF[3]_inst_i_1
Reference name: LUT4
Type: LUT
Number of cell pins: 5
Number of nets: 5
General Properties Power Nets Cell Pins Truth Table
Project Summary Device HA.v two_bit_mul.v mul_tb.v Schematic
12 Cells 8 I/O Ports 16 Nets
a0 a1 b0 b1
a0_IBUF_inst a1_IBUF_inst b0_IBUF_inst b1_IBUF_inst
IBUF
y_OBUF[0]_inst_i_1
LUT2
y_OBUF[1]_inst_i_1
y_OBUF[2]_inst_i_1
y_OBUF[3]_inst_i_1
LUT4
y_OBUF[0]_inst y_OBUF[1]_inst y_OBUF[2]_inst y_OBUF[3]_inst
OBUF
y[3:0]