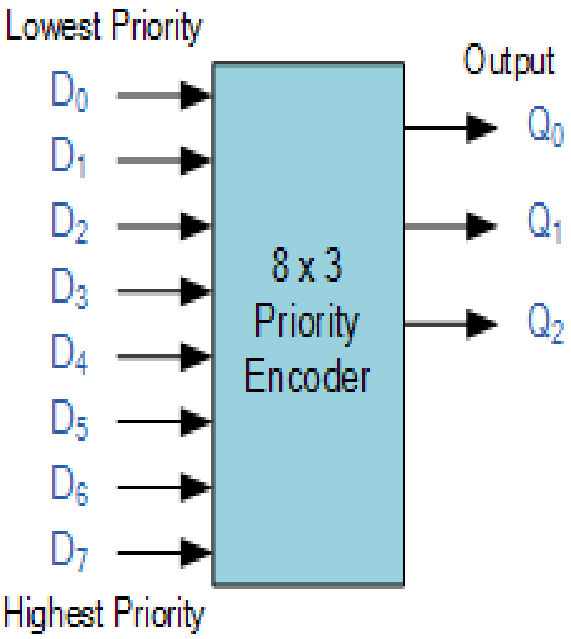
PRIORITY ENCODER



Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	x	0	0	1
0	0	0	0	0	1	x	x	0	1	0
0	0	0	0	1	x	x	x	0	1	1
0	0	0	1	x	x	x	x	1	0	0
0	0	1	x	x	x	x	x	1	0	1
0	1	x	x	x	x	x	x	1	1	0
1	x	x	x	x	x	x	x	1	1	1

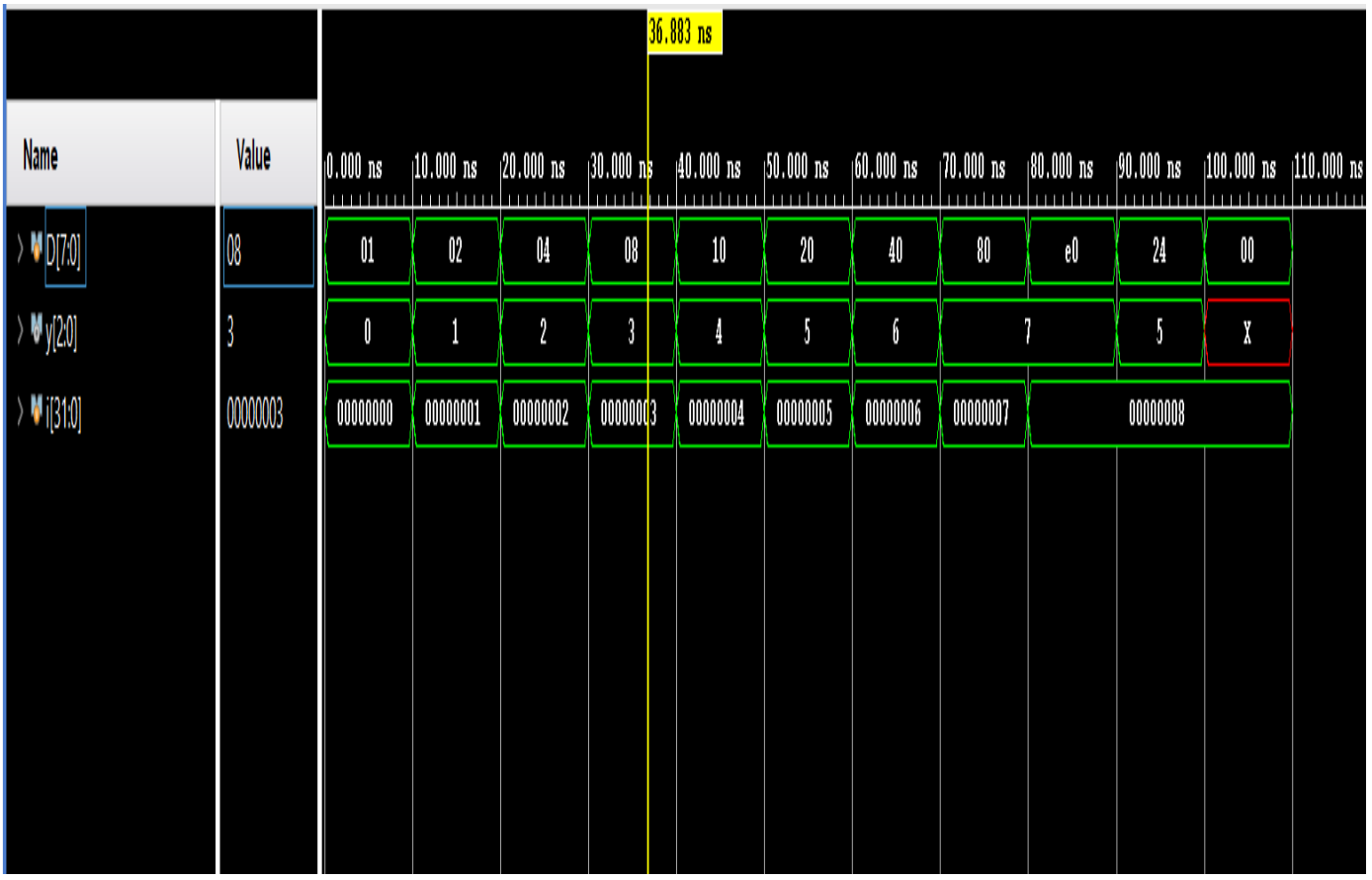
X = don't care

Verilog code:

```
module pr_encoder(
   input [7:0] D,
   output reg [2:0] y
);


always @(D) begin
   casex(D)
      8'b00000001 : y = 3'b000;
      8'b0000001x : y = 3'b001;
      8'b000001xx : y = 3'b010;
```

```
        8'b00001xxx : y = 3'b011;
        8'b0001xxxx : y = 3'b100;
        8'b001xxxxx : y = 3'b101;
        8'b01xxxxxx : y = 3'b110;
        8'b1xxxxxxx : y = 3'b111;
        default     : y = 3'bxxx;
    endcase
end
endmodule
```



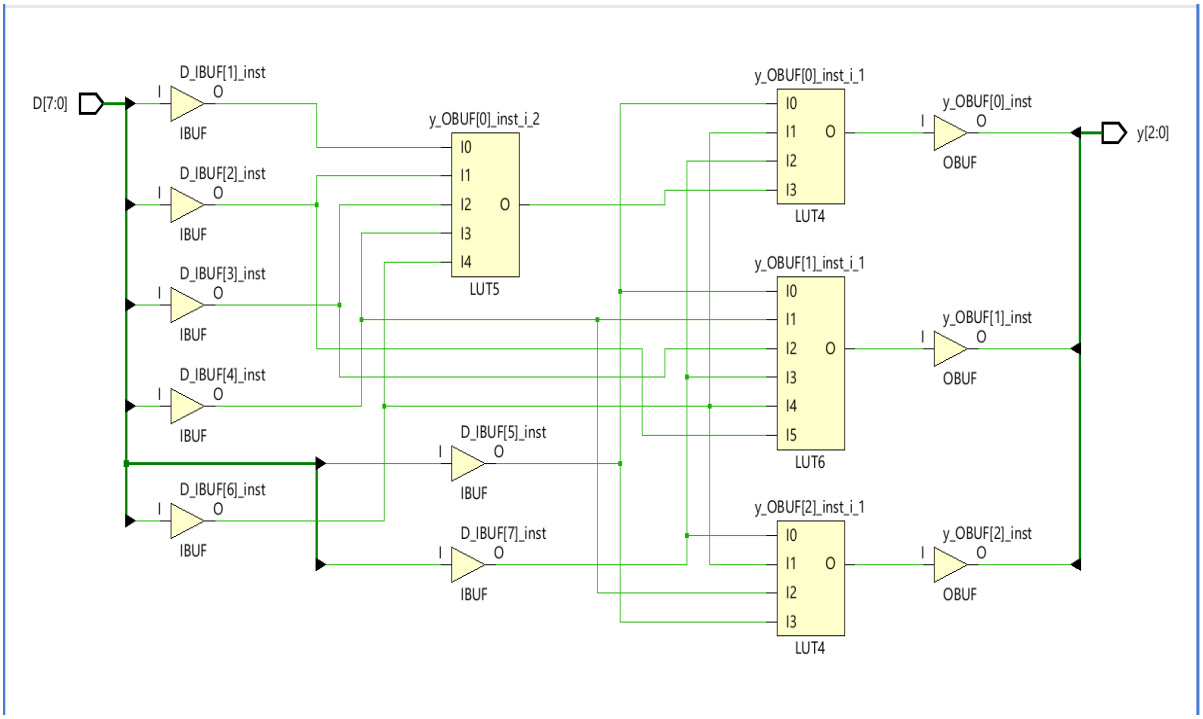


Figure 1 rtl schematic

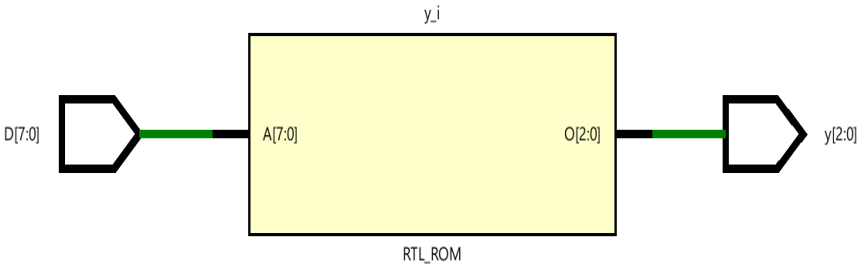
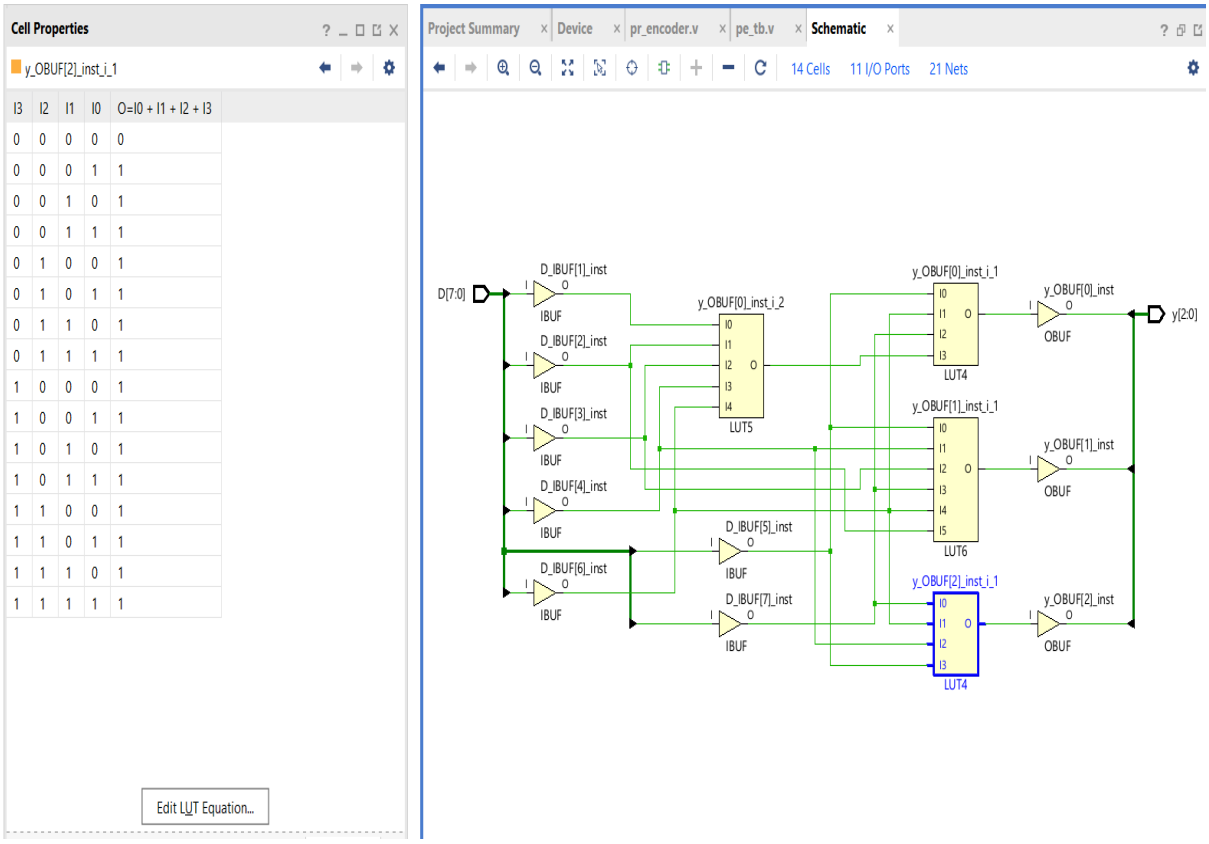


Figure 2 synthesis schematic

LUT’S:



I3	I2	I1	I0	O=I0 + I1 + I2 + I3
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Cell Properties

y_OBUF[1]_inst_i_1

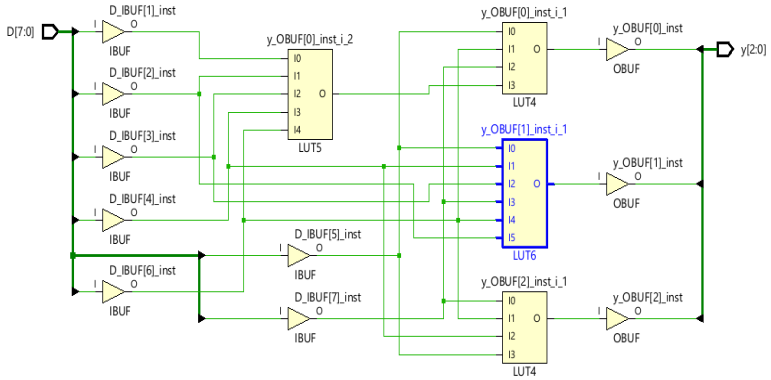
I5	I4	I3	I2	I1	I0	O=I3 + !I3 & I4 + !I0 & !I1 & I2 & !I4 + !I0 &
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	0
0	0	0	0	1	1	0
0	0	0	1	0	0	1
0	0	0	1	0	1	0
0	0	0	1	1	0	0
0	0	0	1	1	1	0
0	0	1	0	0	0	1
0	0	1	0	0	1	1
0	0	1	0	1	0	1
0	0	1	0	1	1	1
0	0	1	1	0	0	1
0	0	1	1	0	1	1
0	0	1	1	1	0	1
0	0	1	1	1	1	1
0	1	0	0	0	0	1
0	1	0	0	0	1	1
0	1	0	0	1	0	1
0	1	0	0	1	1	1
0	1	0	1	0	0	1

Edit LUT Equation...

General Properties Power Nets Cell Pins **Truth Table**

Project Summary | Device | pr_encoder.v | pe_tb.v | **Schematic**

14 Cells 11 I/O Ports 21 Nets



Cell Properties

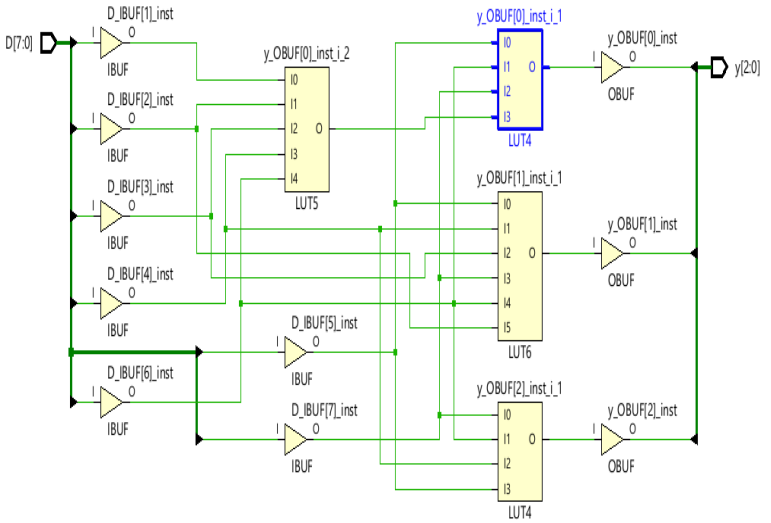
y_OBUF[0]_inst_i_1

I3	I2	I1	I0	O=I0 & !I1 + I2 + !I2 & I3
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Edit LUT Equation...

Project Summary | Device | pr_encoder.v | pe_tb.v | **Schematic**

14 Cells 11 I/O Ports 21 Nets



Cell Properties

y_OBUF[0]_inst_i_2

I4	I3	I2	I1	I0	O=I0 & !I1 & !I3 & !I4 + I2 & !I3 & !I4
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	0
0	0	0	1	1	0
0	0	1	0	0	1
0	0	1	0	1	1
0	0	1	1	0	1
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	0	1	0
0	1	0	1	0	0
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	0	1	0
0	1	1	1	0	0
0	1	1	1	1	0
1	0	0	0	0	0
1	0	0	0	1	0
1	0	0	1	0	0
1	0	0	1	1	0
1	0	1	0	0	0

Edit LUT Equation...

General | Properties | Power | Nets | Cell Pins | Truth Table

Project Summary | Device | pr_encoder.v | pe_tb.v | Schematic

14 Cells | 11 I/O Ports | 21 Nets