Negative edge detector

Verilog code:

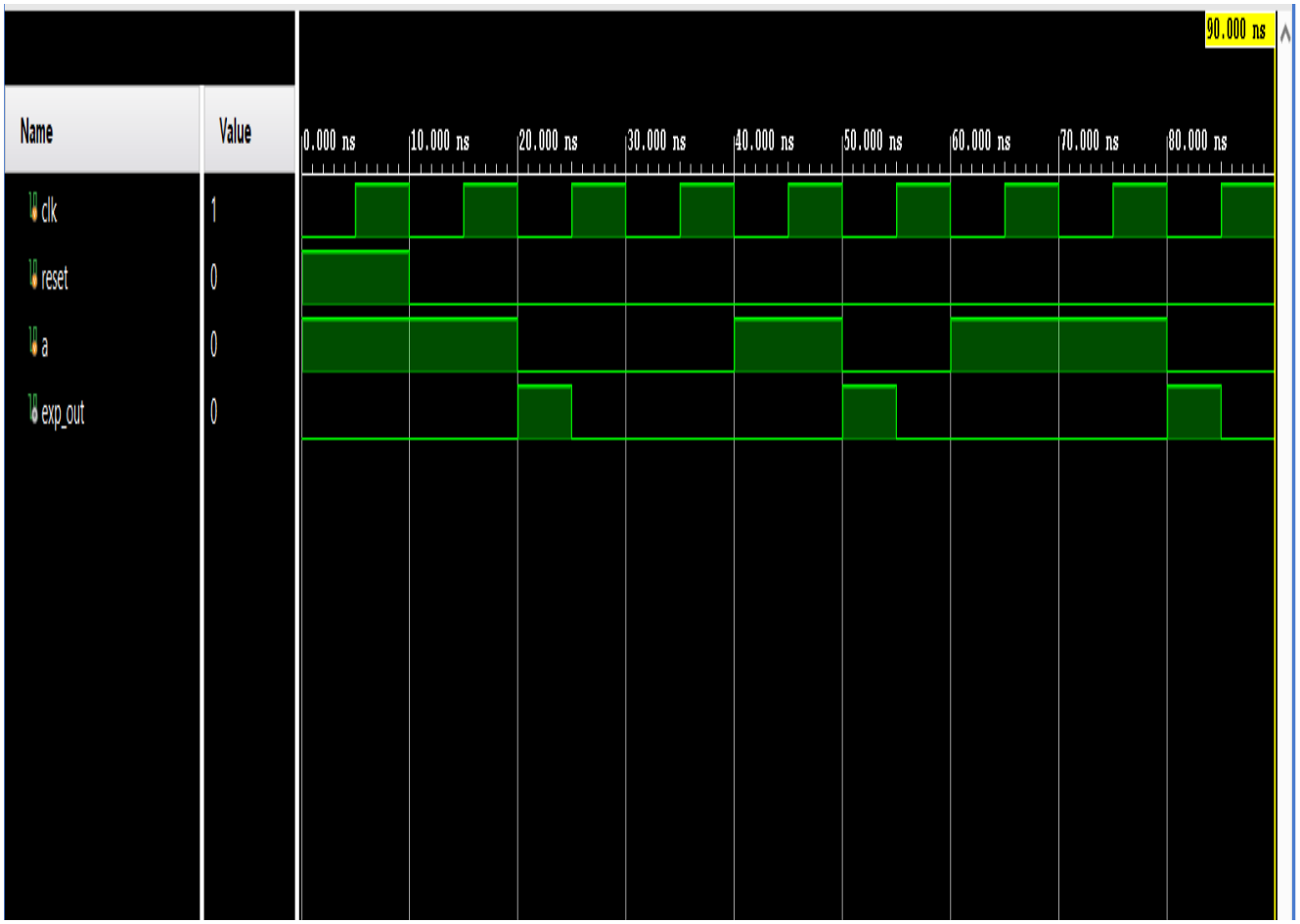
```
module neg_edge_detector_gate(
   input clk,
   input reset,
   input a,
   output exp_out
);

   reg q1;
   wire not_a;

   assign not_a = ~a;
   assign exp_out = not_a & q1;

   always @(posedge clk or posedge reset) begin
      if (reset)
         q1 <= 0;
      else
         q1 <= a;
   end

endmodule
```


90.000 ns
Name
Value
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns
60.000 ns
70.000 ns
80.000 ns
clk
1
reset
0
a
0
exp_out
0

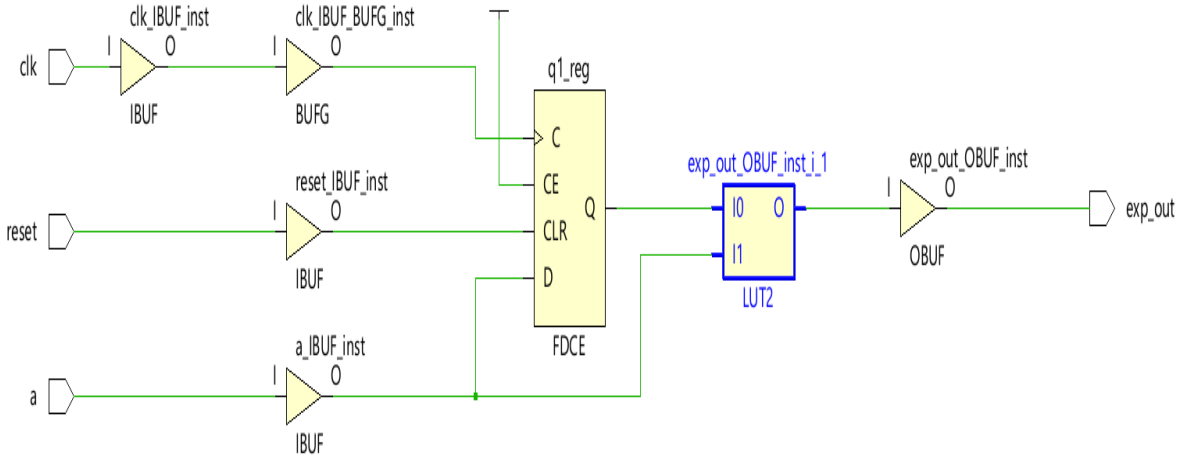


Figure 1 synthesis schematic

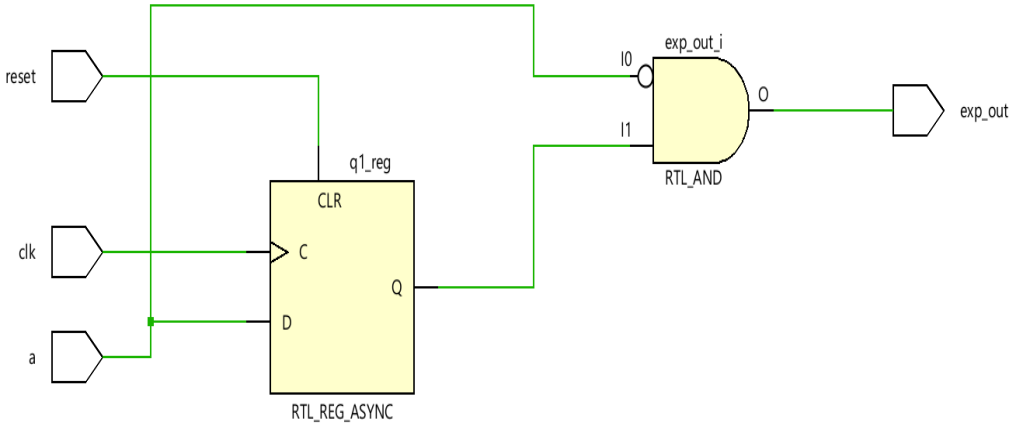


Figure 2 rtl schemaic

Cell Properties

exp_out_OBUF_inst_i_1

I1	I0	O=I0 & !I1
0	0	0
0	1	1
1	0	0
1	1	0

Figure 3 lut