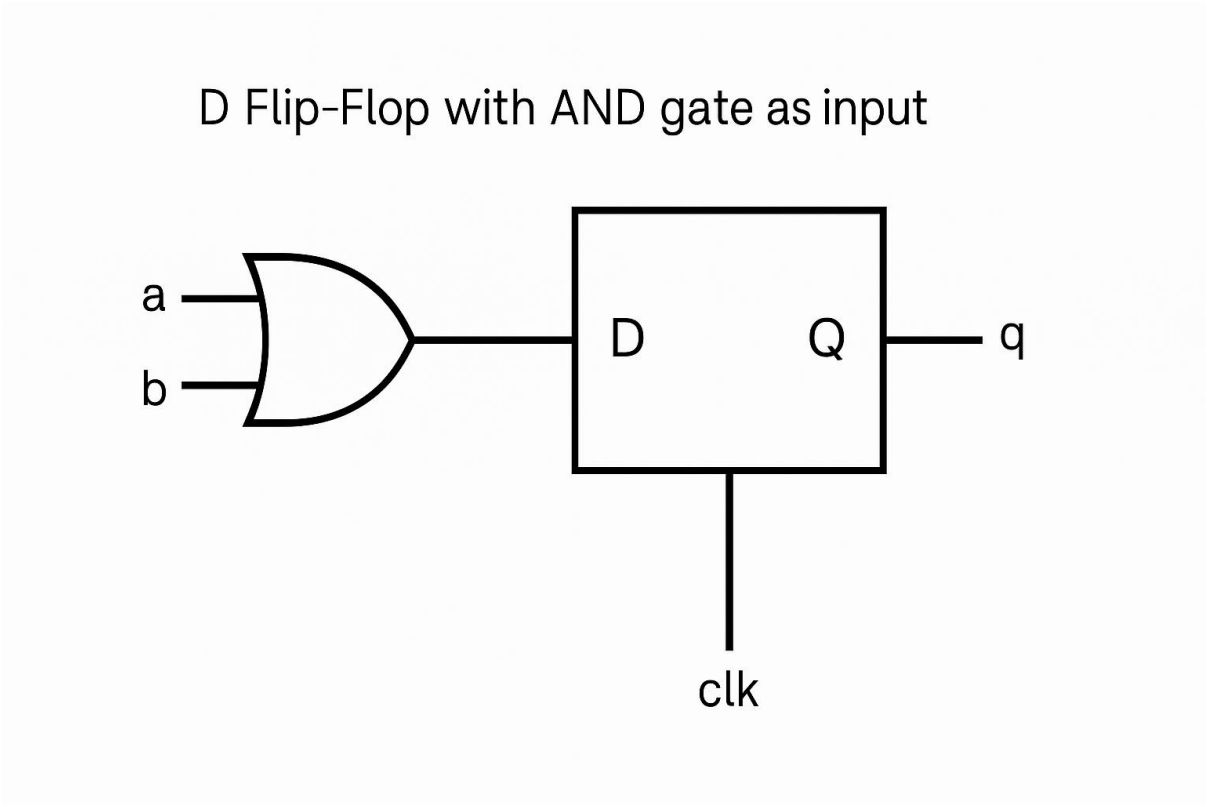
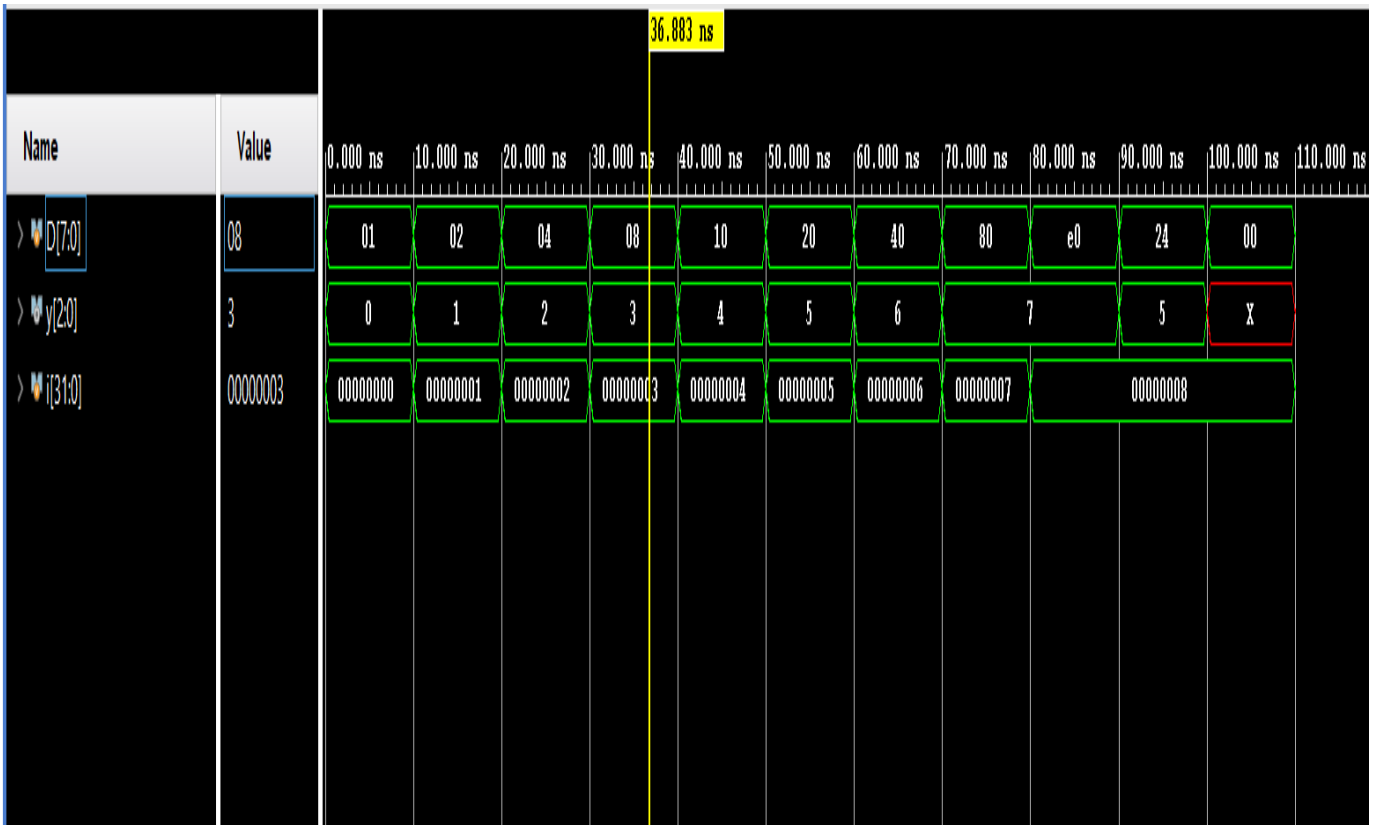
D- FF WIT AND GATE AS INPUT

Verilog code:

```
module d_ff_with_and (
    input clk,
    input rst,
    input a,
    input b,
    output reg q
);

    wire d;

    assign d = a & b;

    always @(posedge clk or posedge rst) begin
        if (rst)
            q <= 0;
        else
            q <= d;
    end

endmodule
```


D Flip-Flop with AND gate as input
a
b
D
Q
q
clk


36.883 ns
Name
Value
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns
60.000 ns
70.000 ns
80.000 ns
90.000 ns
100.000 ns
110.000 ns
D[7:0]
08
01
02
04
08
10
20
40
80
e0
24
00
y[2:0]
3
0
1
2
3
4
5
6
7
5
X
i[31:0]
00000003
00000000
00000001
00000002
00000003
00000004
00000005
00000006
00000007
00000008

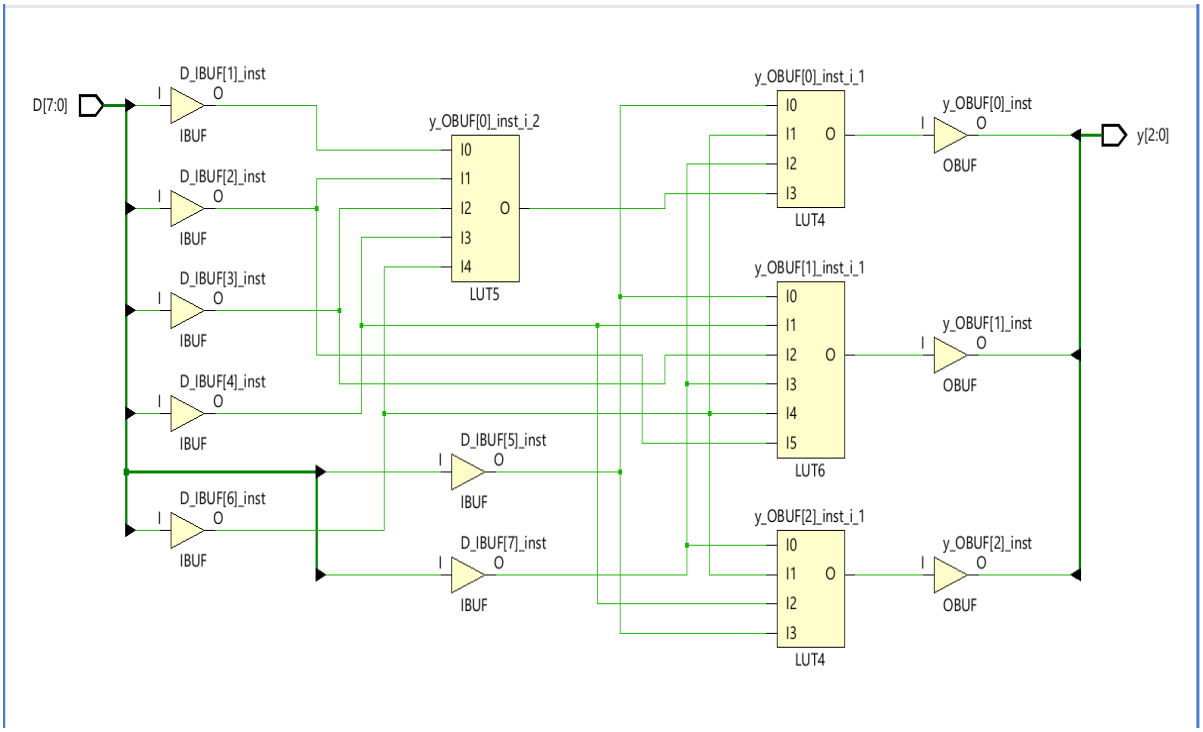


Figure 1 synthesis_schematic

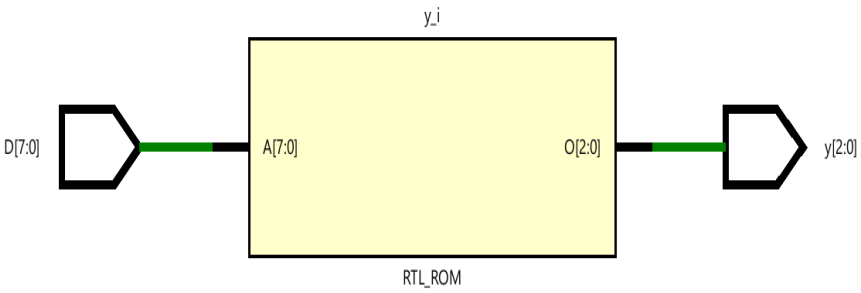


Figure 2 RTL_SCHEMATIC

Cell Properties

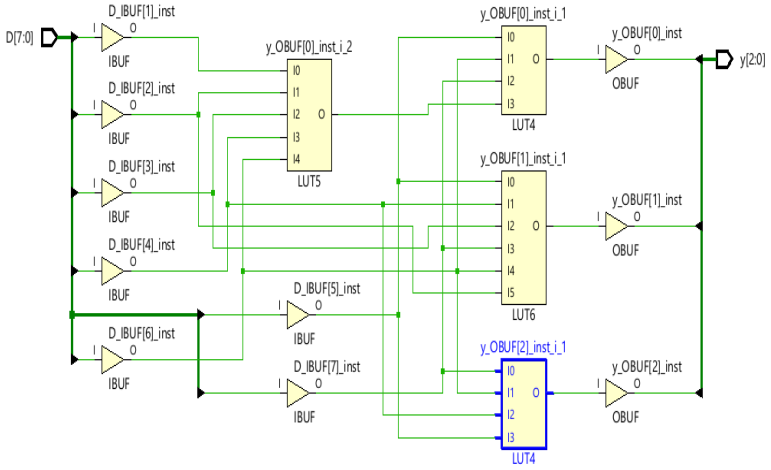
y_OBUF[2]_inst_i_1

I3	I2	I1	I0	O=I0 + I1 + I2 + I3
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Edit LUT Equation...

Project Summary | Device | pr_encoder.v | pe_tb.v | Schematic

14 Cells 11 I/O Ports 21 Nets



Cell Properties

y_OBUF[1]_inst_i_1

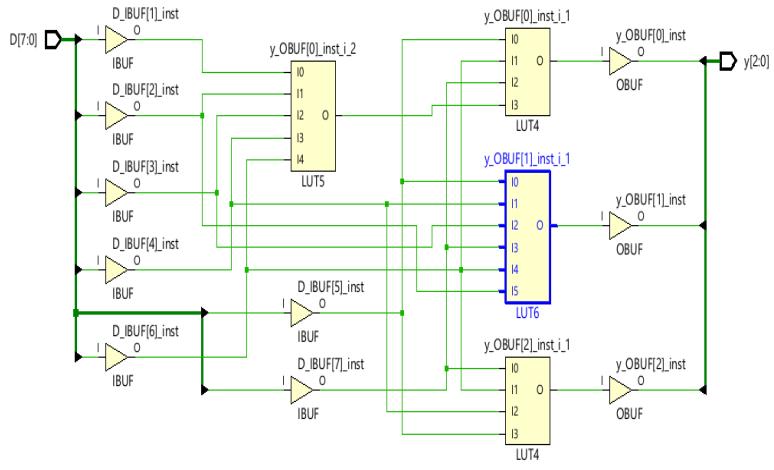
I5	I4	I3	I2	I1	I0	O=I3 + !I3 & I4 + !I0 & !I1 & I2 & !I4 + !I0 &
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	0
0	0	0	0	1	1	0
0	0	0	1	0	0	1
0	0	0	1	0	1	0
0	0	0	1	1	0	0
0	0	0	1	1	1	0
0	0	1	0	0	0	1
0	0	1	0	0	1	1
0	0	1	0	1	0	1
0	0	1	0	1	1	1
0	0	1	1	0	0	1
0	0	1	1	0	1	1
0	0	1	1	1	0	1
0	0	1	1	1	1	1
0	1	0	0	0	0	1
0	1	0	0	0	1	1
0	1	0	0	1	0	1
0	1	0	0	1	1	1
0	1	0	1	0	0	1

Edit LUT Equation...

General | Properties | Power | Nets | Cell Pins | Truth Table

Project Summary | Device | pr_encoder.v | pe_tb.v | Schematic

14 Cells 11 I/O Ports 21 Nets



Cell Properties

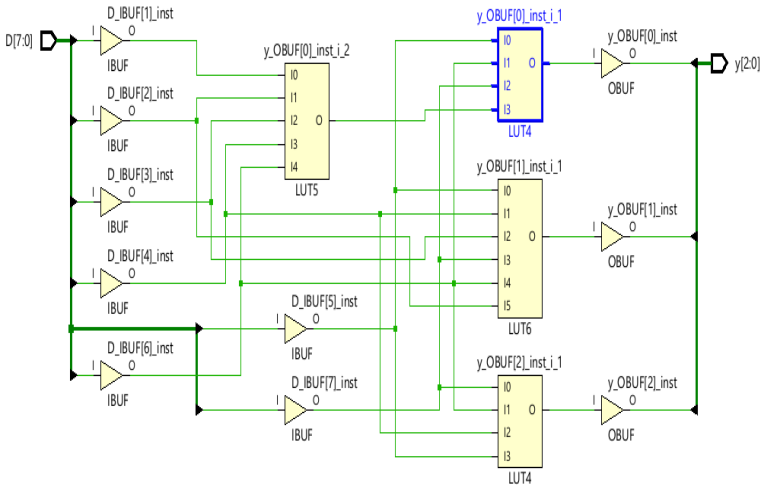
y_OBUF[0]_inst_i_1

I3	I2	I1	I0	O=I0 & !I1 + I2 + !I2 & I3
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Edit LUT Equation...

Project Summary | Device | pr_encoder.v | pe_tb.v | Schematic

14 Cells | 11 I/O Ports | 21 Nets



Cell Properties

y_OBUF[0]_inst_i_2

I4	I3	I2	I1	I0	O=I0 & !I1 & !I3 & !I4 + I2 & !I3 & !I4
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	0
0	0	0	1	1	0
0	0	1	0	0	1
0	0	1	0	1	1
0	0	1	1	0	1
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	0	1	0
0	1	0	1	0	0
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	0	1	0
0	1	1	1	0	0
0	1	1	1	1	0
1	0	0	0	0	0
1	0	0	0	1	0
1	0	0	1	0	0
1	0	0	1	1	0
1	0	1	0	0	0

Edit LUT Equation...

General | Properties | Power | Nets | Cell Pins | Truth Table

Project Summary | Device | pr_encoder.v | pe_tb.v | Schematic

14 Cells | 11 I/O Ports | 21 Nets