2-BIT COUNTER

Verilog Code:

```
module counter(input clk,reset,output reg[1:0]count );
always@(posedge clk)
   begin
if(reset)
   count <= 2'b00;
else
  count <= count+1;
   end
endmodule
```

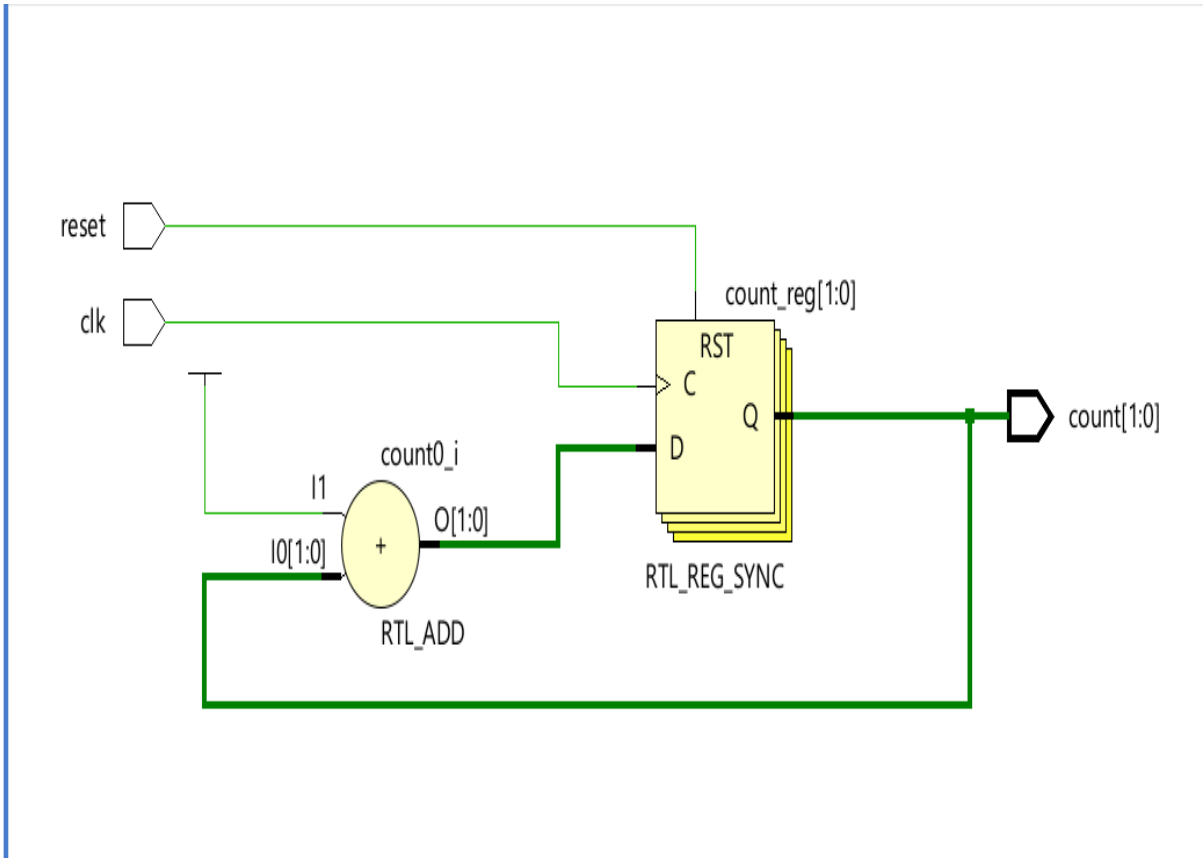


Figure 1 rtl_schematic

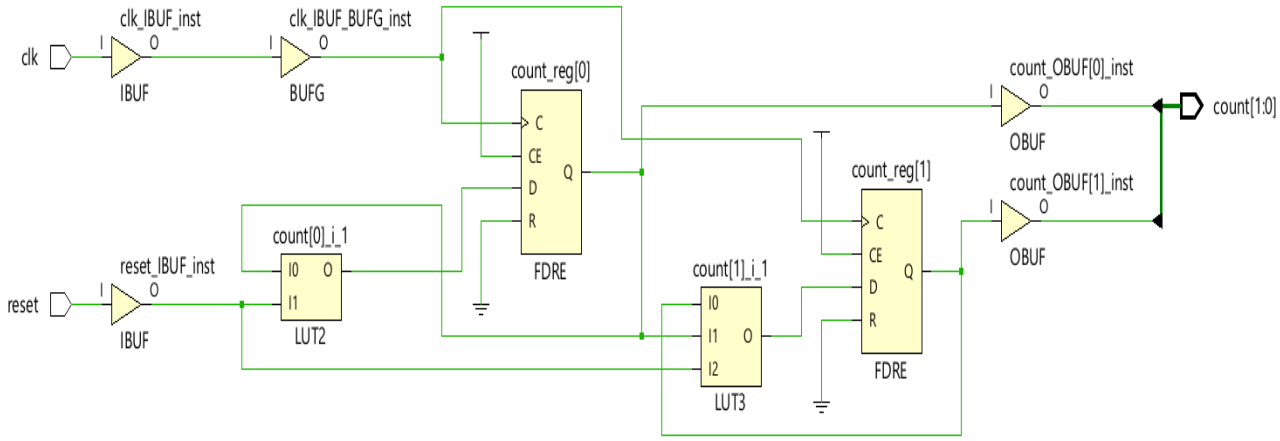
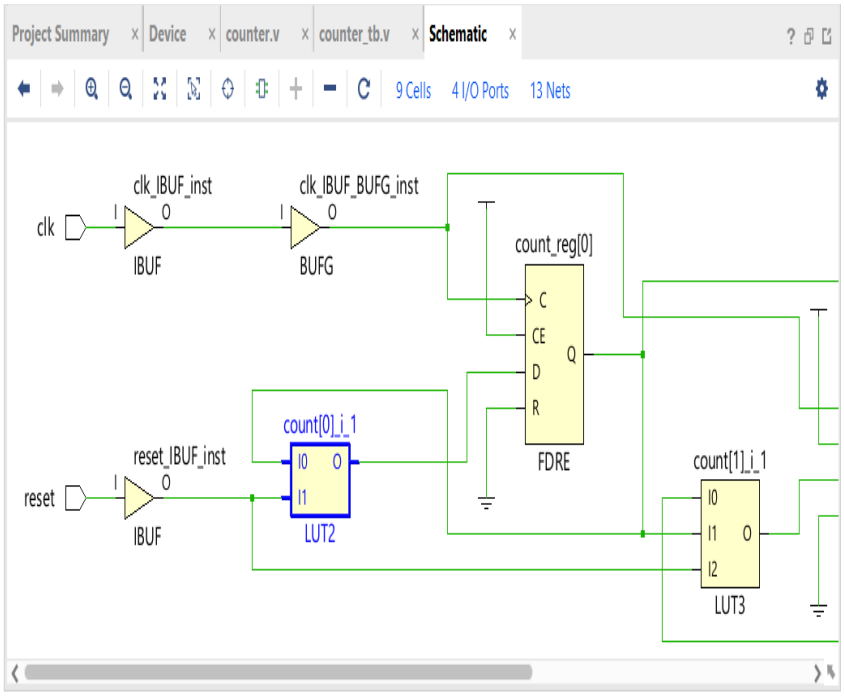


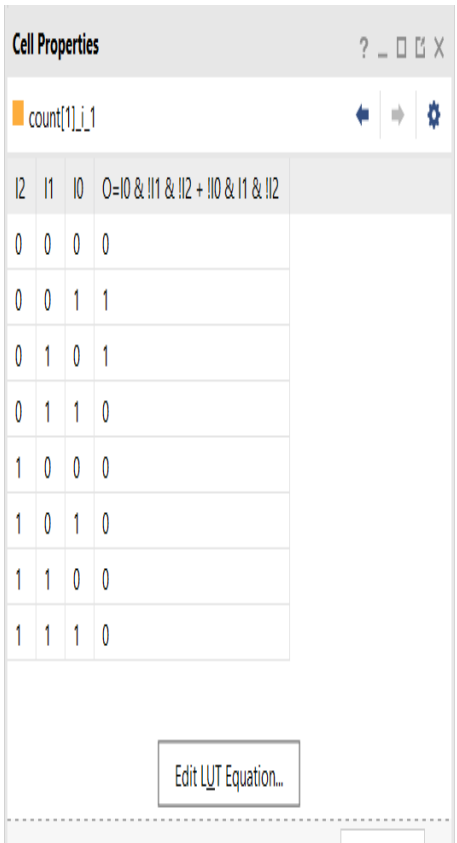
Figure 2 synthesis_schematic

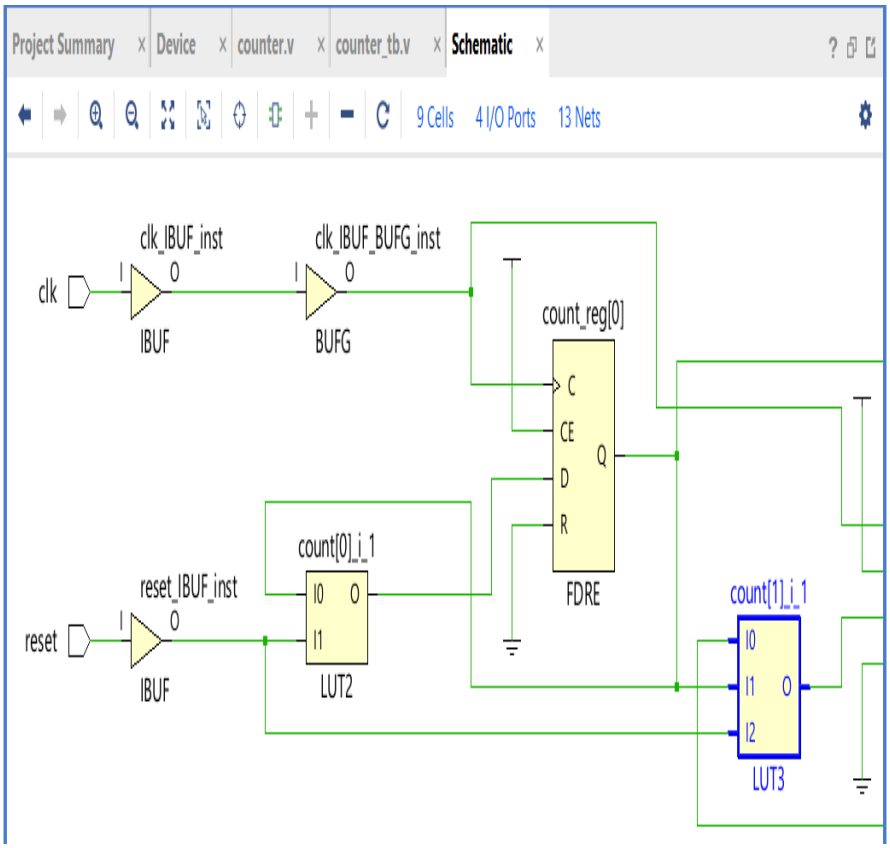
Figure 3 waveform

LUT'S:


Cell Properties
count[0]_i_1
I1 I0 O=!I0 & !I1
0 0 1
0 1 0
1 0 0
1 1 0
Edit LUT Equation...
General Properties Power Nets Cell Pins Truth Table


Project Summary
Device
counter.v
counter_tb.v
Schematic
9 Cells
4 I/O Ports
13 Nets
clk
clk_IBUF_inst
IBUF
clk_IBUF_BUFG_inst
BUFG
count_reg[0]
C
CE
D
R
Q
FDRE
reset
reset_IBUF_inst
IBUF
count[0]_i_1
I0
I1
O
LUT2
count[1]_i_1
I0
I1
I2
O
LUT3


Cell Properties
count[1]_i_1
I2 I1 I0 O=I0 & !I1 & !I2 + !I0 & I1 & !I2
0 0 0 0
0 0 1 1
0 1 0 1
0 1 1 0
1 0 0 0
1 0 1 0
1 1 0 0
1 1 1 0
Edit LUT Equation...


Project Summary
Device
counter.v
counter_tb.v
Schematic
9 Cells
4 I/O Ports
13 Nets
clk
clk_IBUF_inst
IBUF
clk_IBUF_BUFG_inst
BUFG
count_reg[0]
C
CE
D
R
Q
FDRE
reset
reset_IBUF_inst
IBUF
count[0]_i_1
I0
I1
O
LUT2
count[1]_i_1
I0
I1
I2
O
LUT3