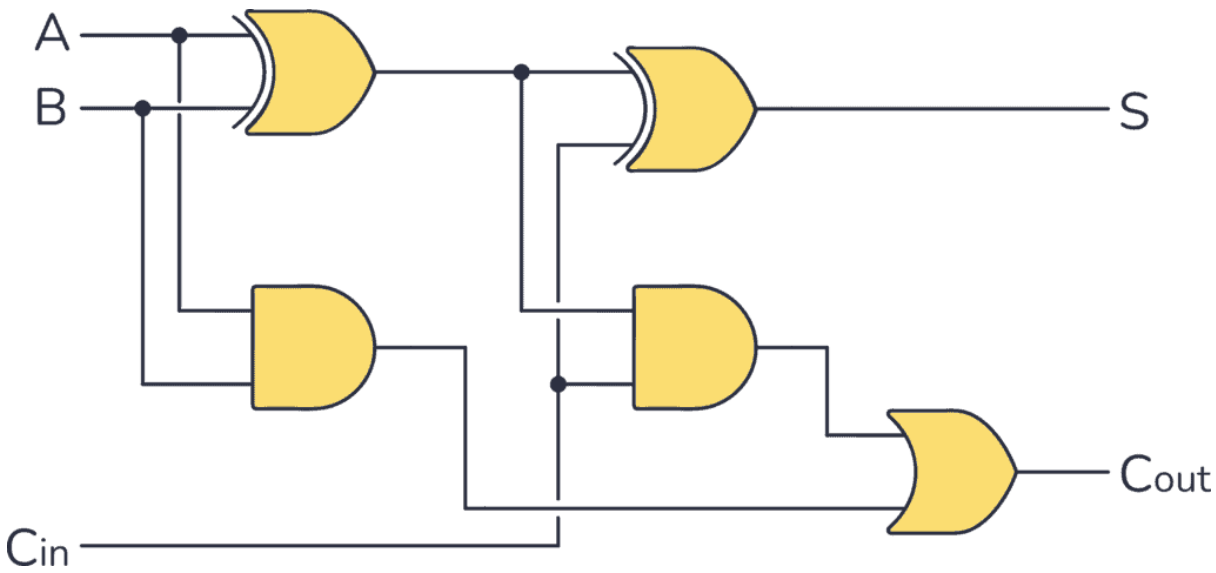
FULL ADDER



A	B	Cin	Sum (S)	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Verilog Code:

```
module FA(input A, B, CIN, output SUM, COUT);
    wire w1, w2, w3;

    xor (w1, A, B);
    xor (SUM, w1, CIN);
    and (w2, w1, CIN);
    and (w3, A, B);
    or (COUT, w2, w3);
endmodule
```

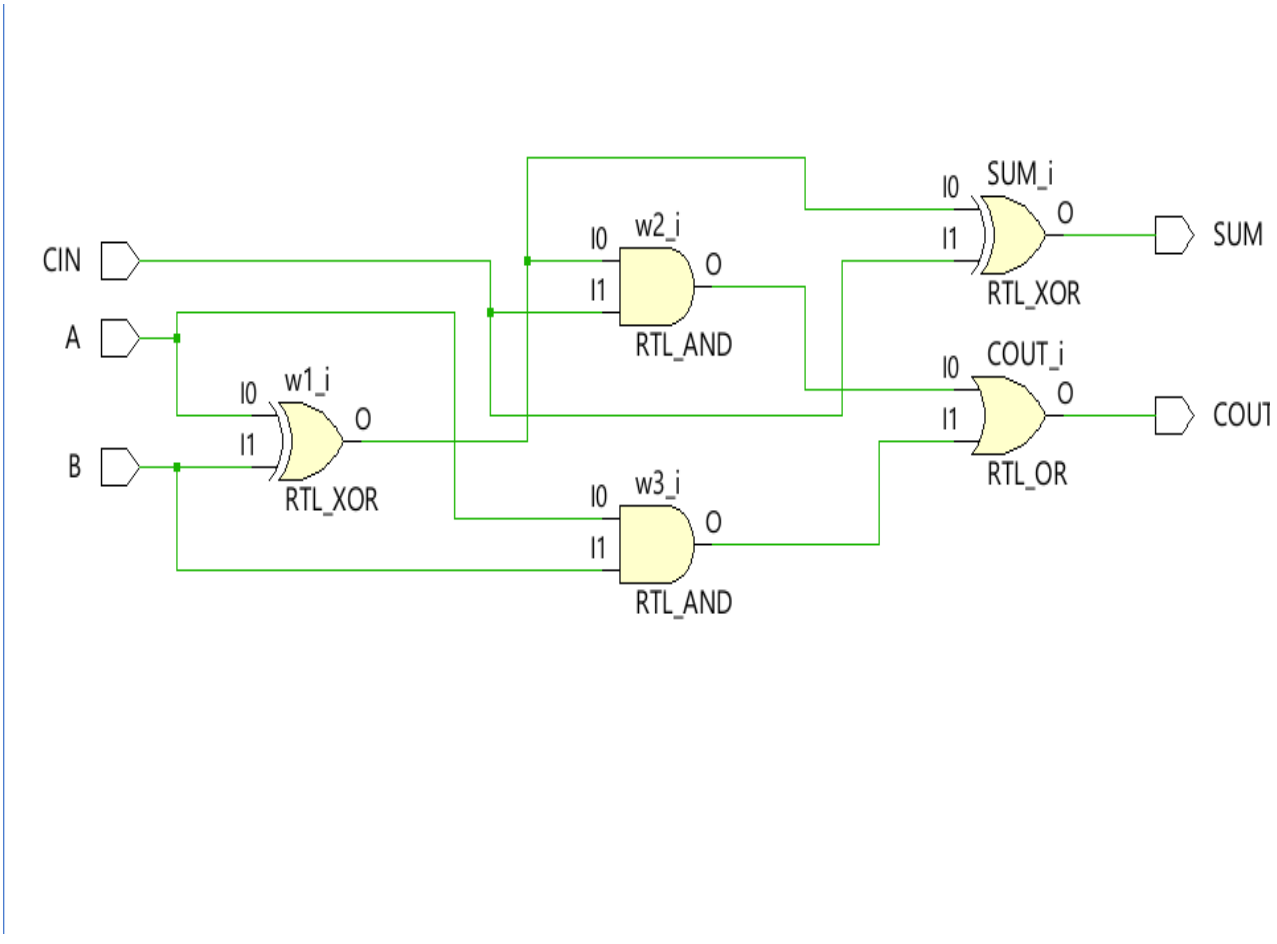


Figure 1 RTL SCHEMATIC

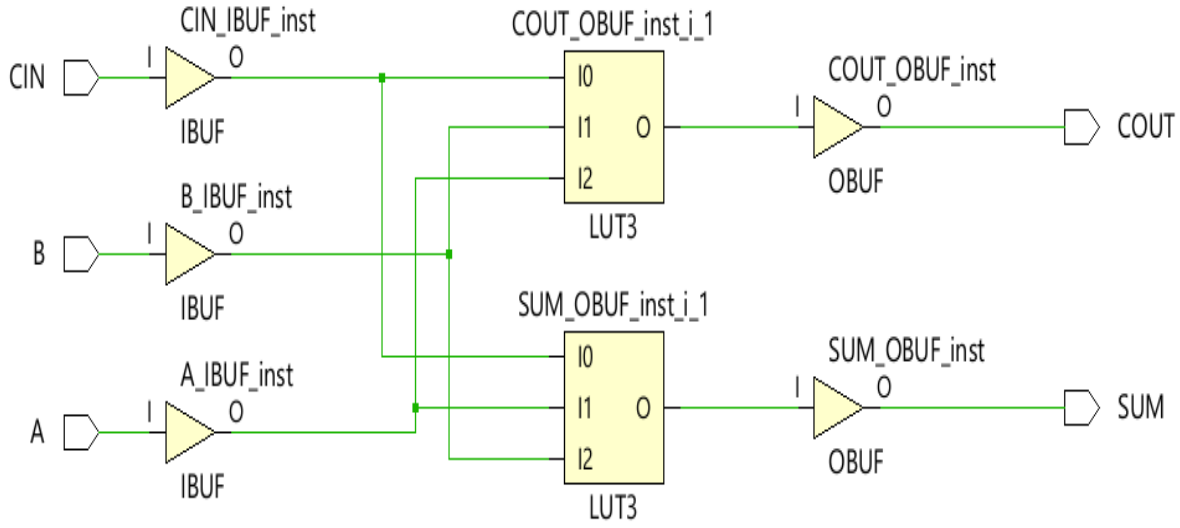


Figure 2 Synthesized Schematic

SUM_OBUF_inst_i_1

I2	I1	I0	O=I0 & !I1 & !I2 + !I0 & I1 & !I2 + !I0 & !I1 & I2 + I0 & I1 & I2
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

COUT_OBUF_inst_i_1

I2	I1	I0	O=I0 & I1 + I0 & I2 + I1 & I2
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

WAVEFORMS

Figure 3 Waveforms