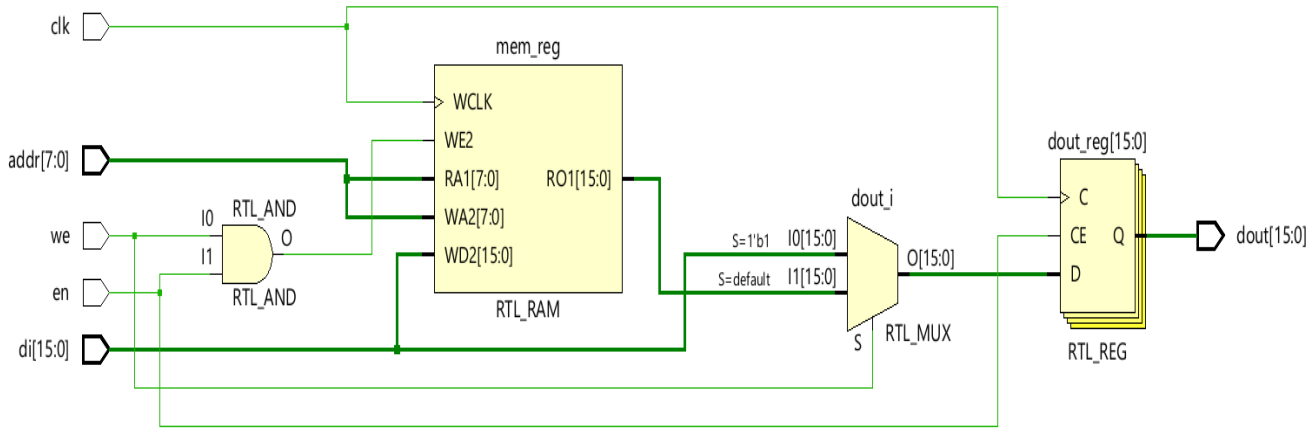
SINGLE PORT BRAM



Verilog code:

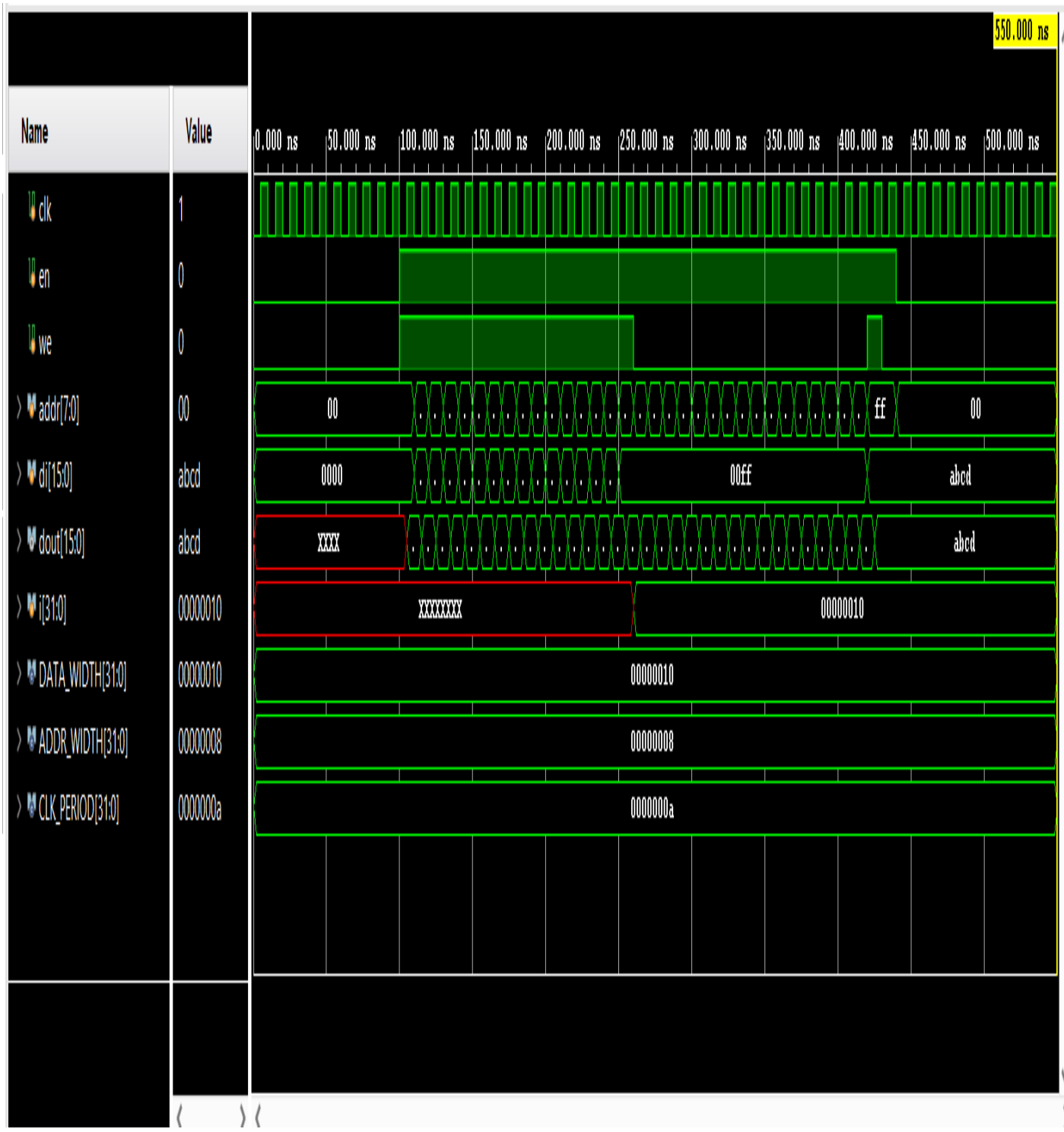
```
module bram_single_port #(
    parameter DATA_WIDTH = 16,    // Width of data bus
    parameter ADDR_WIDTH = 8      // Determines memory depth (2^ADDR_WIDTH)
) (
    input wire clk,              // System clock
    input wire en,               // Memory enable
    input wire we,               // Write enable (1 = write, 0 = read)
    input wire [ADDR_WIDTH-1:0] addr,  // Memory address
```

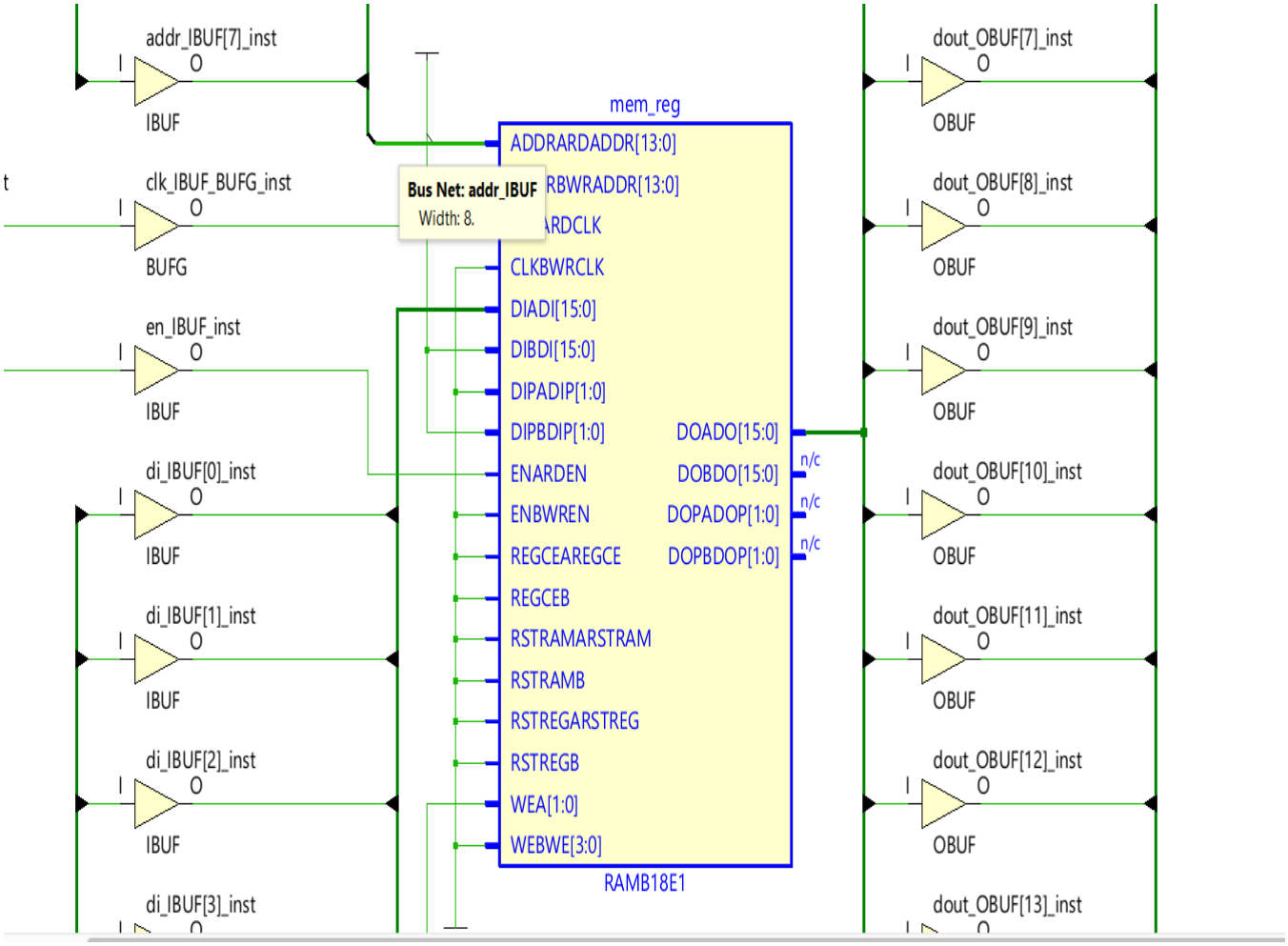
```
    input wire [DATA_WIDTH-1:0] di,    // Data input
    output reg [DATA_WIDTH-1:0] dout   // Data output
);

// Memory array declaration
reg [DATA_WIDTH-1:0] mem [0:(1 << ADDR_WIDTH)-1];

// Memory operation
always @(posedge clk) begin
    if (en) begin
        if (we) begin
            mem[addr] <= di;      // Write data to memory
            dout <= di;           // Write-first: output new data
        end else begin
            dout <= mem[addr];    // Read data from memory
        end
    end
end

endmodule
```


550.000 ns
Name
Value
0.000 ns
50.000 ns
100.000 ns
150.000 ns
200.000 ns
250.000 ns
300.000 ns
350.000 ns
400.000 ns
450.000 ns
500.000 ns
clk
1
en
0
we
0
addr[7:0]
00
00
ff
00
di[15:0]
abcd
0000
00ff
abcd
dout[15:0]
abcd
xxxx
abcd
i[31:0]
00000010
xxxxxxxx
00000010
DATA_WIDTH[31:0]
00000010
00000010
ADDR_WIDTH[31:0]
00000008
00000008
CLK_PERIOD[31:0]
0000000a
0000000a



Cell Properties

mem_reg

Name:	mem_reg
Reference name:	RAMB18E1
Type:	Block Memory
Number of cell pins:	116
Number of nets:	96