CS225 - Assignment

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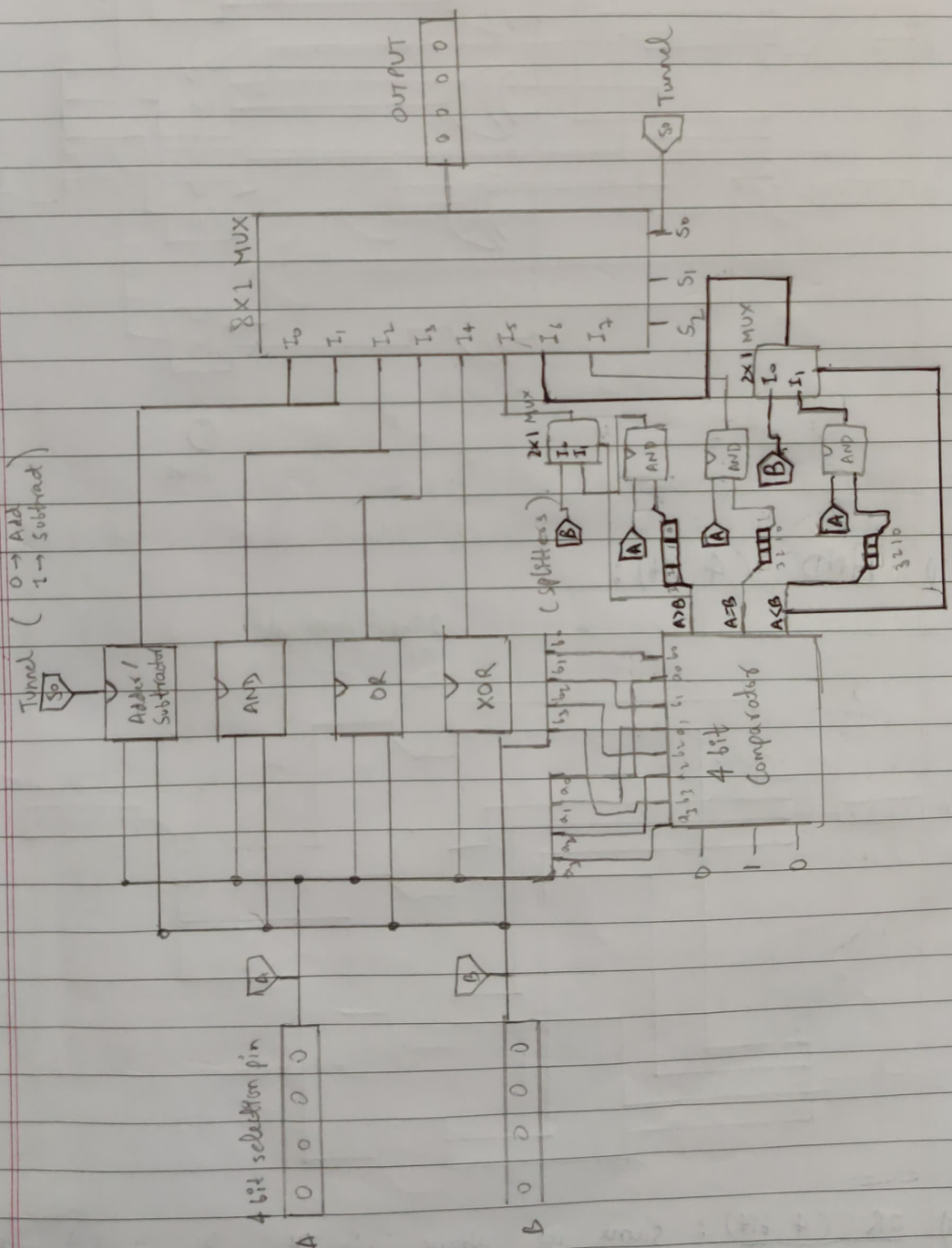
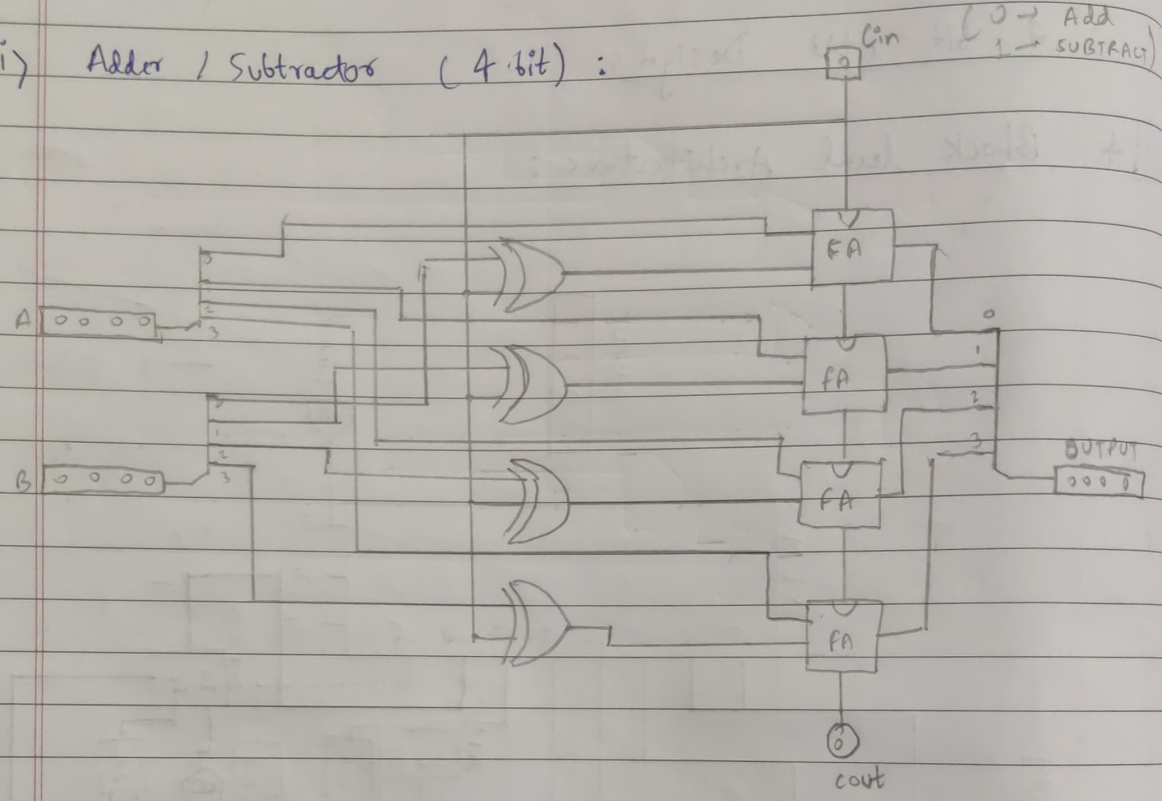
4 - bit ALU Design :

[Q2] * Block level Architecture :

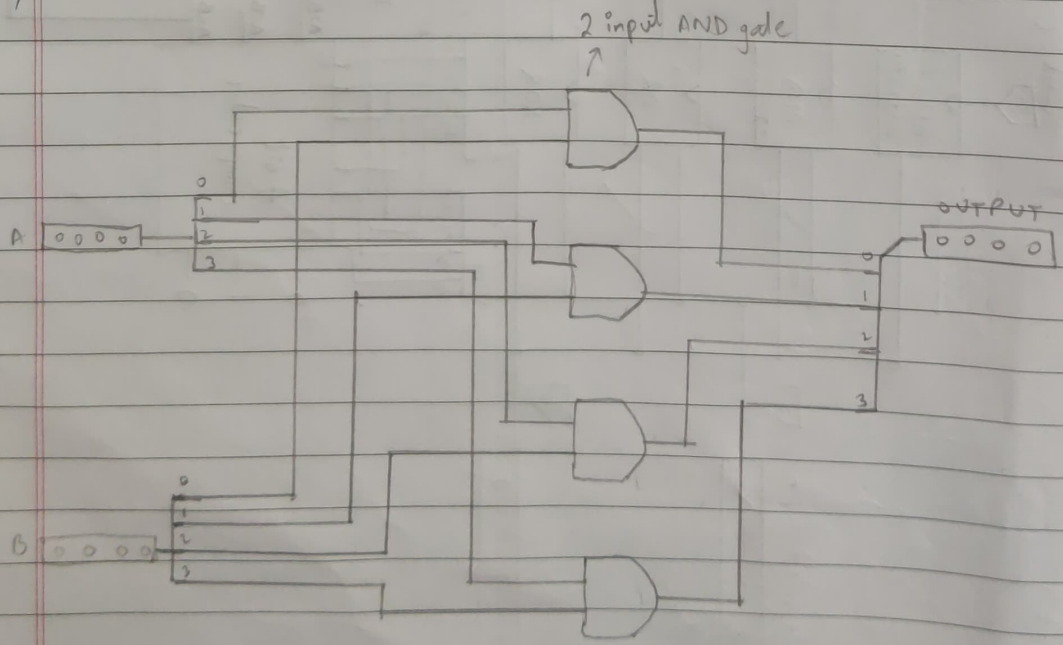


Q3 * Individual Components / Block design :

i) Adder / Subtractor (4 bit) :



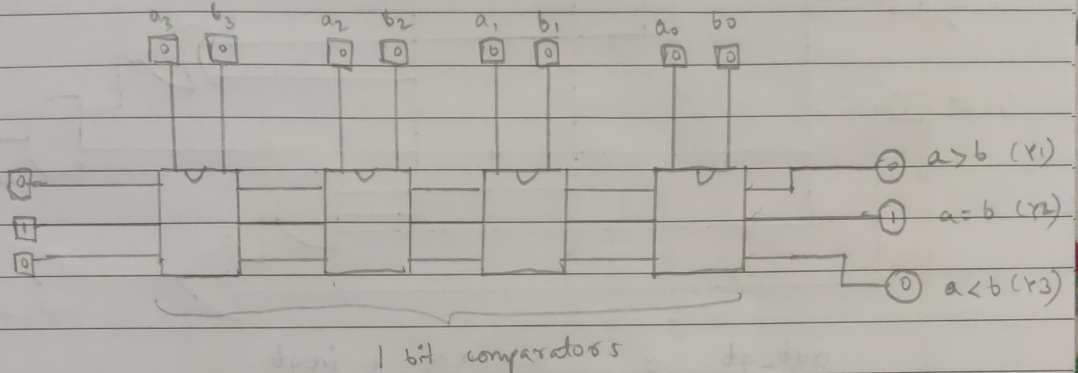
ii) AND (4 bit) :



iii) OR (4 bit) : same as above circuit with 2 bit AND gates (all 4) replaced by 2 bit OR gates.

iv) XOR (4 bits) : same as above circuit with 2 bit AND gates (all 4) replaced by 2 bit XOR gates.

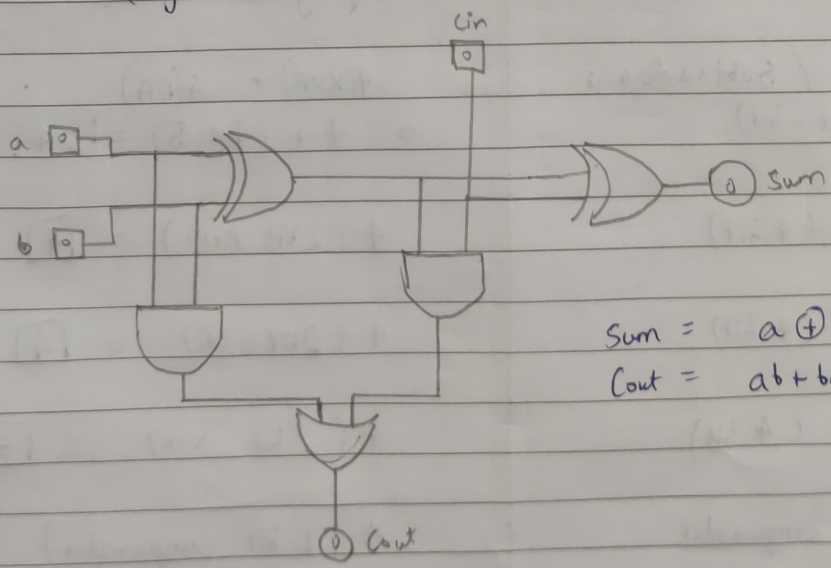
v) 4 bit comparator :



Y_1, Y_2, Y_3 are 1 respectively when $a>b$, $a=b$ and $a<b$.

* for the above 5 blocks / components few subcircuits / subblocks also used :

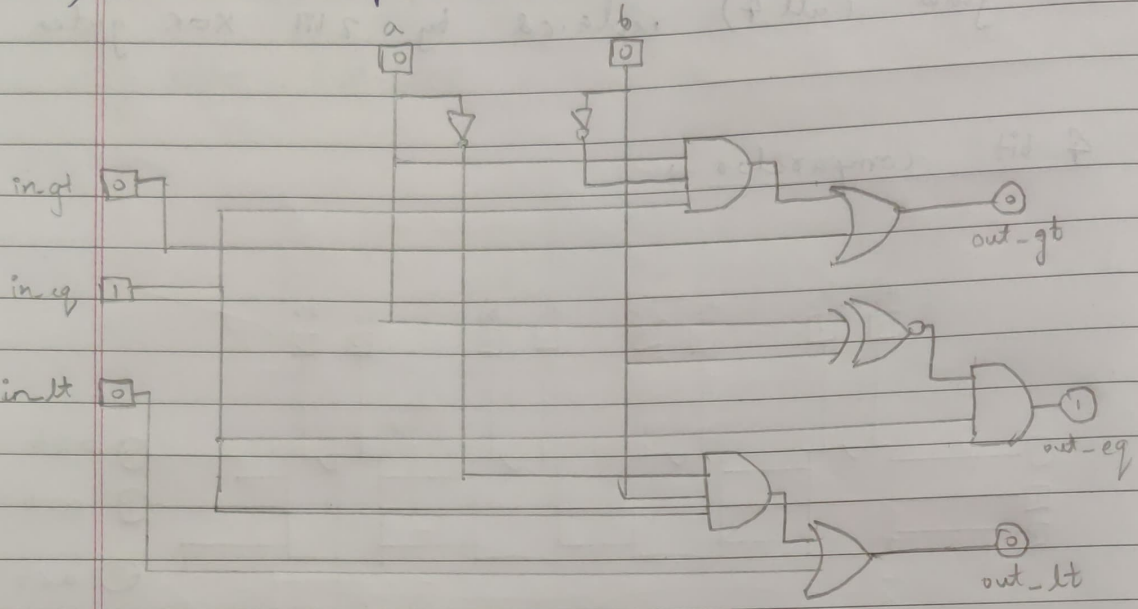
vi) FA (full adder) :



Sum = $a \oplus b \oplus Cin$

Cout = $ab + bc + ca$

vii) 1-bit comparator :



$out\_gt = a\bar{b}\, in\_eq + in\_gt$

$out\_eq = \overline{(a \wedge b)} \cdot in\_eq$

$out\_lt = \bar{a}\, b\, in\_eq + in\_lt$

*** Q4** Number of gates required in each block:

	Block Name	No. of gates used
i)	Adder / Subtractor : (4-bit)	4(XOR) + 4(FA) = 4 + (4 × 5) = **24**
ii)	AND (4 bit)	4 (2 bit AND) = **4**
iii)	OR (4 bit)	4 (2 bit OR) = **4**
iv)	XOR (4 bit)	4 (2 bit XOR) = **4**
v)	4-bit Comparator	4 (1 bit comparator) = 4 × 8 = **32**

* Q1 Truth table :

S_2	S_1	S_0	Function
0	0	0	A + B
0	0	1	A - B
0	1	0	$A \cap B$ / AB
0	1	1	$A \cup B$ / A + B
1	0	0	$A \oplus B$ / $A \wedge B$
1	0	1	A if A > B and B if B > A
1	1	0	A if A < B and B if B < A
1	1	1	A or B if A = B

—— END OF ASSIGNMEN ——

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