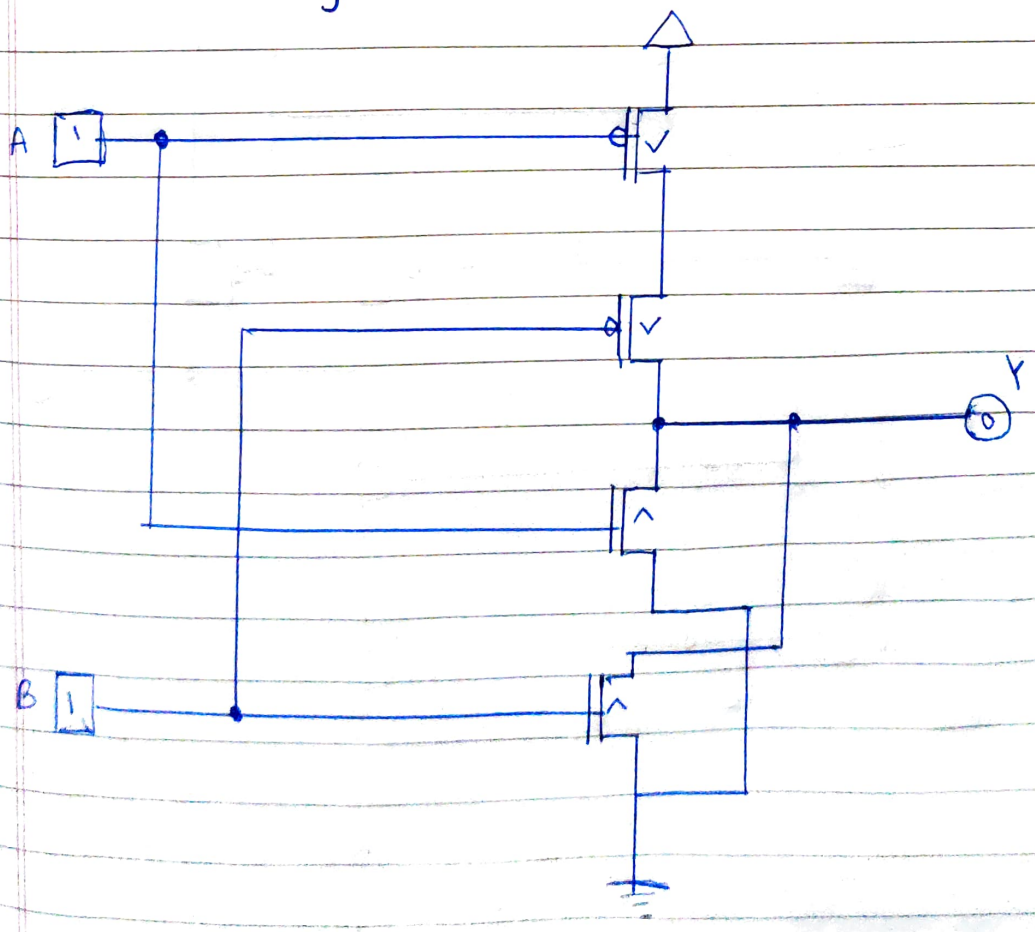
Name : Siddharth Sanskritayan
Roll No. : 1901CS75

1) NOR gate :

i) Truth table :

A	B	Y (output)
0	0	1
0	1	0
1	0	0
1	1	0

ii) Circuit Diagram :

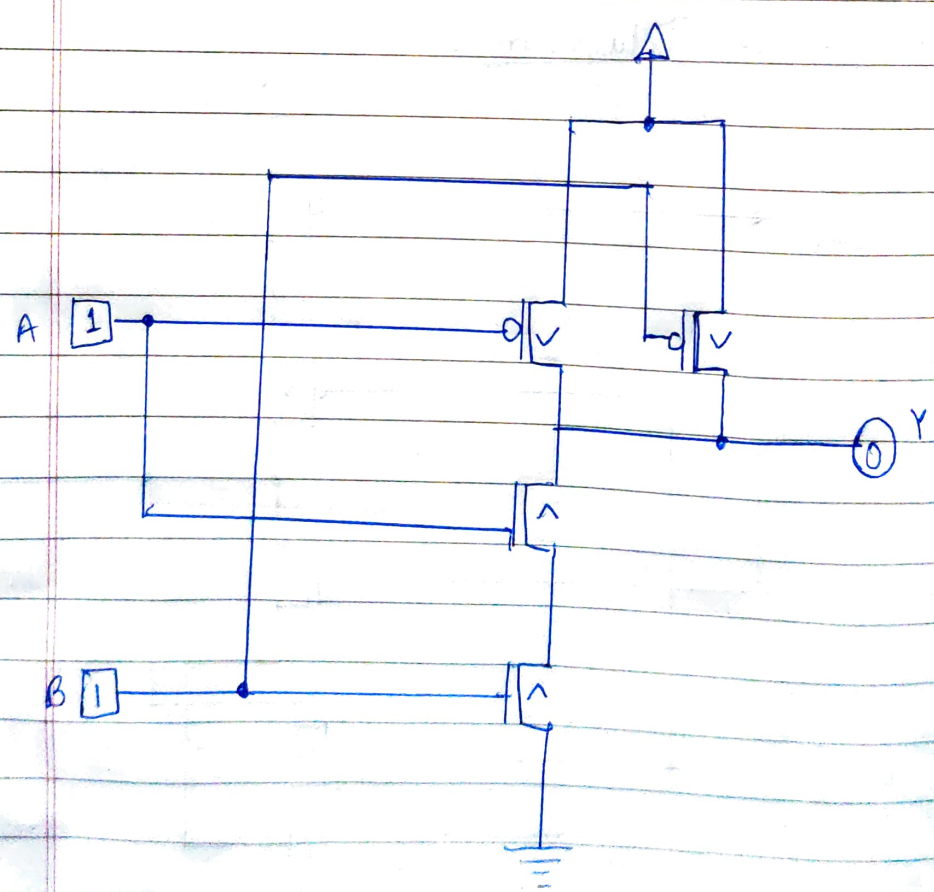


2) NAND gate :

i) Truth table :

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

ii) Circuit Diagram :

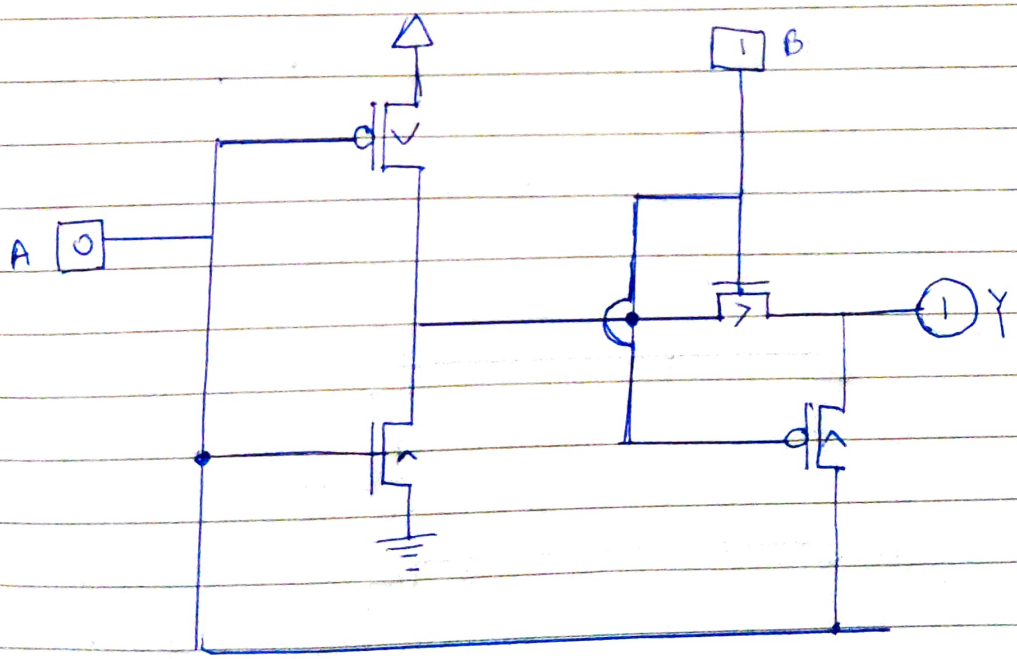


3) XOR Gate :

i) Truth table :

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

ii) Circuit Diagram :

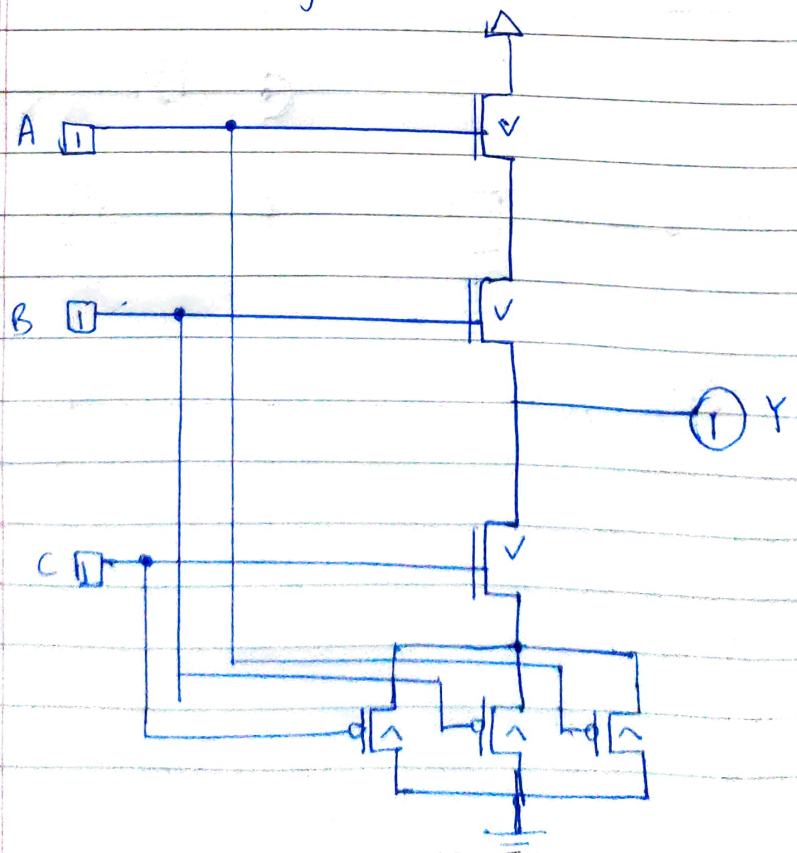


4) Three input AND gate:

i) Truth table:

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

ii) Circuit Diagram:

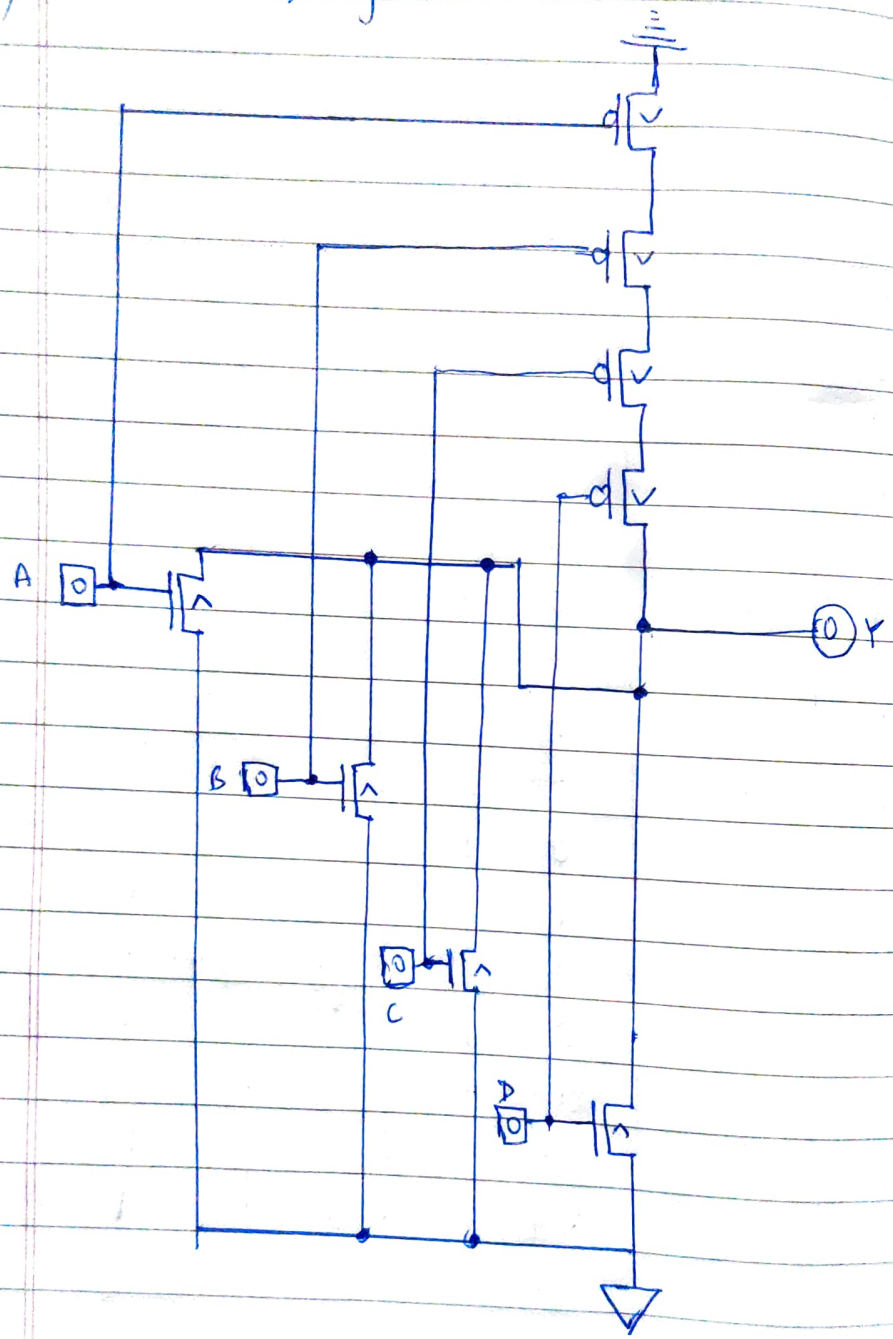


5) Four Input OR gate :

i) Truth table :

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

ii) Circuit Diagram :



6) XNOR Gate :

i) Truth table :

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

ii) Circuit Diagram :