CS225-Switching Theory

-End Semester Assignment

Siddharth Sanskritayan

1901CS75

IIT Patna

A1) Report on Computer memory Architectures: Past and Present –

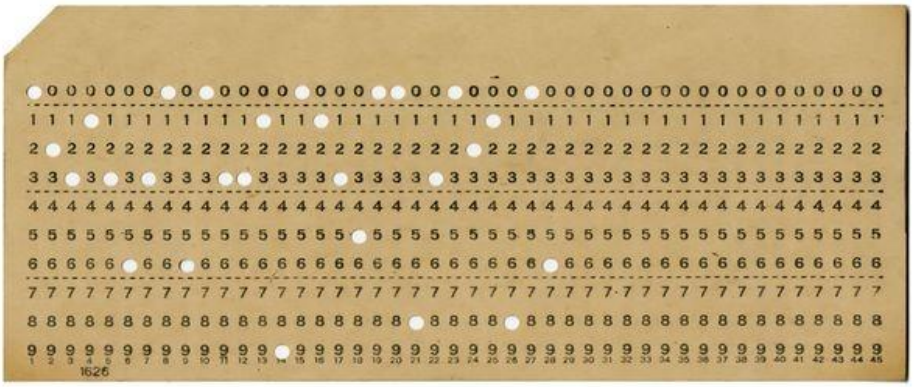
Introduction:

In computing, **memory** is a device or system that is used to store information for immediate use in a computer or related computer hardware and digital electronic devices.
Modern computers might be packed full of the fastest and most powerful computer memory and storage solutions ever, with 2TB hard drives and 4GB of RAM a common feature and dual-SSD drives becoming more and more prevalent, but computer memory was not always so effective. From floppy disks to flash drives, and from magnetic tape to complex hard drives which use magnetic forces to function, the evolution of computer memory has been rapid.

Evolution of Memory Architectures:

1. Punch Cards:

Punch cards (or "punched cards"), also known as Hollerith cards or IBM cards, are paper cards where holes may be punched by hand or machine to represent computer data and instructions. The cards were fed into a card reader connected to a computer, which converted the sequence of holes to digital information. They have been dated back to as early as **1725.**
The punch cards are read column wise and any program can be implemented on them by punching binary code on it and piling a ‘stack’ of such code to be read step by step by the computer. They are still used today in activities like voting and census.



2. Vacuum Tubes:

Introduced in the early **1940s** , the Vacuum Tubes were used to store numbers in an octal-base and were capable of operating on around 20 numbers at a time with each number ranging upto 10^{10}.

3. Delay Line Memory:

This came into the industry in the **early 1950s** . This memory was built using Mercury tubes. It analysed the sound waves in the tubes to store, read and write data.

4. Williams Tube: Introduced in the **late 1950s** , this is said to be the first random accessible memory in computing. It was a major improvement over its predecessor 'Selectron Tube' and was less expensive.

5. Magnetic Memory: The memories developed earlier were volatile and would not retain after power loss. This led to researchers to dive into creating memory which retained data written on it and which could be read from and written to. Researchers developed forms of magnetic memory which was improved over the years. This memory replaced all tube-based memories since it was highly space efficient and could store more data and also was non-volatile. Different forms of magnetic memory were developed:

a. Magnetic Tape: The magnetic tape works by using a magnetizable material coated on a plastic layer. It was developed in Germany in **1928** and revolutionised the sound and music industry. The cassettes used by us in the late 1990s and early 2000s all run on the principle of this magnetic tape.

b. Floppy Disk: These were developed in the late **1960** s and commercially available in **1971** . The floppy disk has certain **concentric magnetic tracks** . As the read/write control head passes over it, it uses magnetic polarisation to write and write data. The data is stored in binary form '0' or '1' and they are represented by magnetic north and south poles. Transfer Speeds go upto **300 kB/second** . The access time is around 200 milliseconds which is excessively slow as compared to modern memory. It can store upto around **1.4 MB** of data in an average disk. Therefore it consumes a large amount of space.

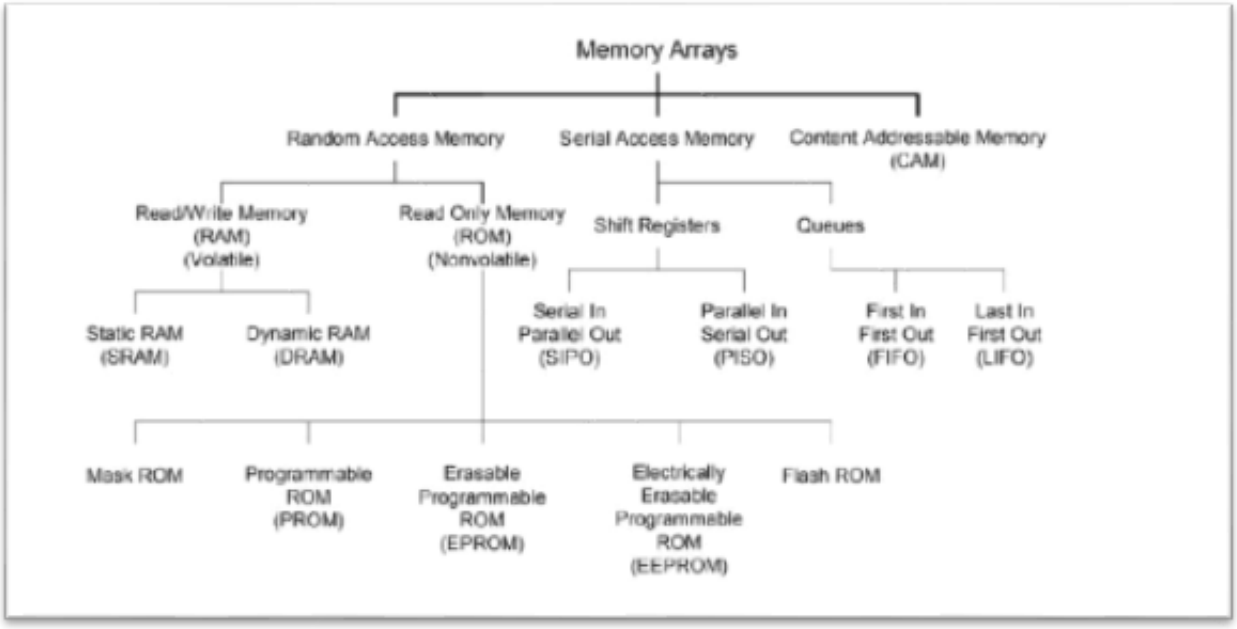
c. The Hard Disk Drive: First introduced and popularised in the **late 1970s** , the Hard Disk Drive was a significant improvement over the traditional Magnetic Memory like Floppy Disks. It worked on the same principle, however, it used very highly compact ferromagnetic films to store data. This allowed the disk to store larger amounts of data than the traditional floppy. HDDs were excessively cheap and became so popular that they were brought into use by IBM in almost all their computing devices. From there on the HDDs are used as mass storage inside the modern computers, even in today's times. As of 2020, the HDDs are capable of rotating at **5400-7200 RPM** which allows for very high speeds of data writing and reading. The compact size makes it one of the most efficient memories in terms of data stored: size ratio. The HDDs today are capable of storing upto **5-10 TBs** of data easily!

6.Optical Disk:

Data are recorded as tiny pits in a single spiral track on plastic discs that range from 3 to 12 inches (7.6 to 30 cm) in diameter, though a diameter of 4.8 inches (12 cm) is most common. The pits are produced by a laser or by a stamping machine and are read by a low-power laser and a photocell that generates an electrical signal from the varying light reflected from the pattern of pits. Optical discs are removable and have a far greater memory capacity than diskettes; the largest ones can store many gigabytes of information.

7.Semiconductor Memories:

Semiconductor memory is used in any electronics assembly that uses computer processing technology. Semiconductor memory is the essential electronics component needed for any computer based PCB assembly.



A. Static Random Access Memory (SRAM): Static RAM or SRAM is a volatile memory in which data is lost as soon as power cuts off. It is generally implemented as an array of an array of cells. Each of these cells is basically a latch formed with two not gates and two NMOS transistors. In total each cell contains **6 CMOS transistors** (2 PMOS and 4 NMOS). The data stored in SRAM is stored in a 'static' manner. This means that the data is not lost with time, unless the power is cut off.Thus, no need for refreshing the data is there. SRAM is very **highly fast** in terms of data access and read/write due to the fact that it does not require any refreshing time for its memory cells. Due to a large number of transistors in each cell, it is both **expensive and large in size** . It is typically used as a cache for the CPU since it is very fast.

B. Dynamic Random Access Memory (DRAM): Dynamic RAM is again a volatile memory in which data is lost as soon as power cuts off. Like SRAM, it is also implemented as an array of an array of cells. Each of these cells has one NMOS transistor and a small capacitor. The capacitor stores the voltage of the data bit to be stored in the cell. The transistor is used for conduction during writing. The main issue with the design is that the capacitor has very low capacitance due to which it discharges very quickly. Due to this the DRAM must be refreshed within stipulated intervals of time (~64ms for DDR2 RAM). This is why it is called Dynamic RAM.

C. Read Only Memory (ROM): Read Only Memory is a **non-volatile** memory in which the data is hardcoded on the circuit. The data is thus stored in a more or less permanent fashion on the circuit. The data is not changeable in the basic versions of the ROM.
However, ROM variants like EPROM(Erasable Programmable ROM) can be erased and reprogrammed electrically/UV light several times. The basics of EPROM come from the core concepts of quantum physics(electron tunnel oxide degradation).

D. Flash Memory: Flash Memory is a **non-volatile** Read Only Memory which is electrically erasable and programmable (EPROM). It uses Fowler-Nordheim Tunneling for programming and erasing. In terms of speed, it has a **read speed comparable to DRAM (~ns)** and **write speed comparable to a disk (~ms)** . Each individual cell of the flash memory is

implemented using a **floating gate MOSFET** . Charge inversion towards the floating gate is responsible for programming and charge accumulation away from the floating gate is responsible for erase of data. Data is read by measuring the effect of applying intermediate voltage (between possible threshold voltages according to the number of states) applied on the cell. The cell may even store more than just one bit since it may have more than two states.

E. Solid State Drive (SSD): A solid state memory is a **non-volatile** memory based on flash memory. However, along with the flash memory, it also has a built in controller inside it which has implementations that make the access time really quick and provide high latency. The controller makes the SSD excessively fast in comparison to traditional HDD and is nowadays used as the storage of Operating Systems allowing for fast booting of the system.

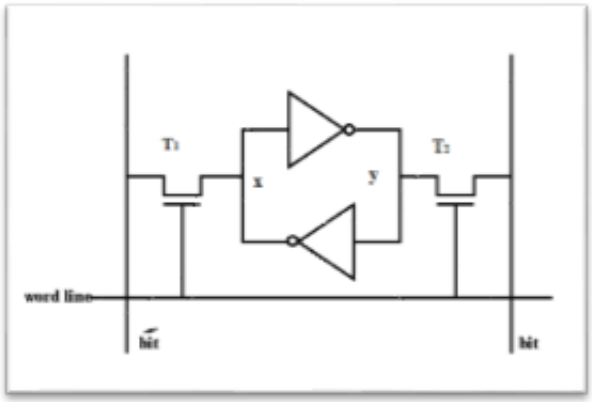


Fig: SRAM

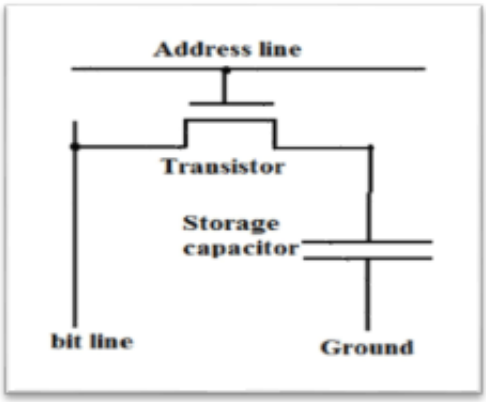


Fig: DRAM

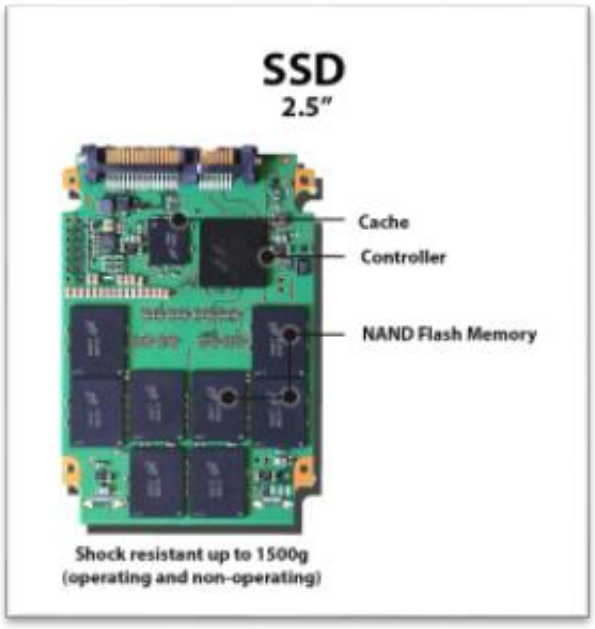


FIG: SSD

Comparison between various computer memory architectures:

Features	Tube Memory	Magnetic Tape	Optical Disk
Years Active	1940s	1971 - 2000	1982 - 2010
Technology	Physical properties of matter.	Magnetic polarisation on materials.	Laser light reflection
Capacity	~ 1 kB (very low)	~ 1 MB (low)	~ 600 MB (still low)
Power	High	Moderate	Very High
Volatile	Yes	No	No
Speed	very slow	~ 100 kB/s (slow)	~ 300 kB/s (still slow)
Transistors Used	0	0	0
Application	first form of RAM used in early computers.	Removable storage (portable data storage)	Removable storage (could store multimedia files)

The above table shows the memory architectures used in the past.
Now, we will compare the presently used memories on each of the above parameters.

Features	HDD (Hard Disk Drive)	DRAM (Dynamic RAM)	SRAM (Static RAM)	Flash Memory
Years Active	1956 - Present	1970 - Present	1987 - Present	1987 - Present
Technology	Magnetic polarisation on small materials.	MOSFET (CMOS) Architecture	MOSFET (CMOS) Architecture	f-N tunneling
Capacity	~ 1 TB (very high)	~ 16 GB (High)	~ 16 MB (moderate)	~ 256 GB (very high)
Power	High	Low	High	Very low
Volatile	No	Yes	Yes	No
Speed	~ 150 Mb/s (moderate)	~ 15 Gb/s (fast)	~ 80 Gb/s (faster)	~ 100 Mb/s (moderate)
Transistors used	0	1 CMOS	6 CMOS	1 floating gate MOSFET
Application	storage device for modern computers. (huge capacity)	Random memory in modern computers.	Cache memory in modern computers	used in SSD which is very fast compared to traditional HDD.

A2) **Problem**: To design a Overlapping sequence detector which detects the sequence '1001' and on detection outputs 1 otherwise 0.

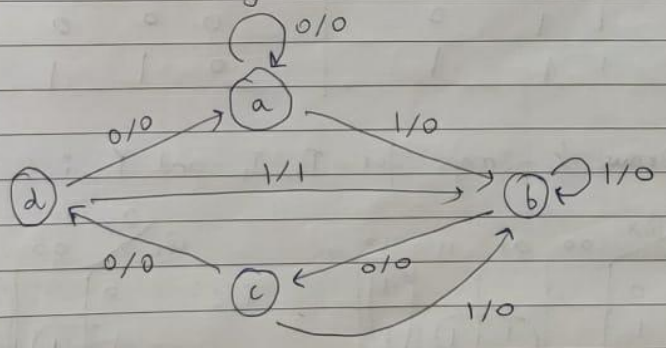
* A sequence detector is a sequential state machine that takes an input string of bits and generates an output 1 whenever the target sequence has been detected.

* In an overlapping sequence detector, the last bit of one sequence becomes the first bit of the next sequence.

eg: In the input sequence (100)(1001)0(1000)(1001), the target sequence is detected three times

Below are the steps to design the FSM:
(Mealy Machine used → O/P is a function of present state as well as input)

Step1: Drawing the state diagram:



State Assignment:
a → 00 → Initial state (reset)
b → 01 → '1' detected
c → 10 → '10' detected
d → 11 → '100' detected

Total 4 states (enclosed in circles), transitions show as arrows with label input / Output

Step 2 : Drawing the state table :

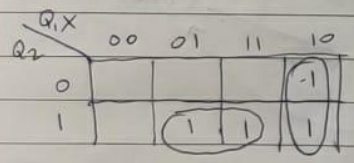
As there are total 4 states, we require two flip flops. Any flip flop may be used, here I have used T flip flops.

$X \rightarrow$ Input
$Y \rightarrow$ Output
$Q_2, Q_1 \longrightarrow$ Present states
$Q_2^+, Q_1^+ \longrightarrow$ Next states
$T_2, T_1 \longrightarrow$ T flip flops

Q_2	Q_1	X	Q_2^+	Q_1^+	Y	T_2	T_1
0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	1
0	1	0	1	0	0	1	1
0	1	1	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	1
1	1	0	0	0	0	1	1
1	1	1	0	1	1	1	0

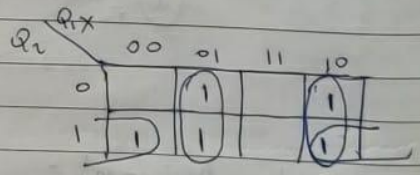
Step 3 Draw K-maps for T_2, T_1 and Y :

T_2 :



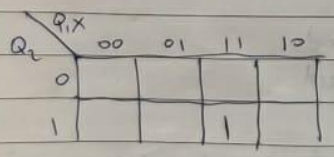
$T_2 = Q_1\bar{X} + Q_2X$

T_1 :



$T_1 = \bar{Q}_1X + Q_1\bar{X} + Q_2\bar{X}$

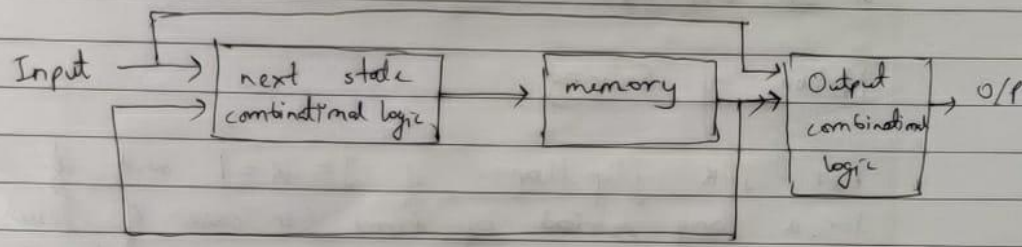
Y :

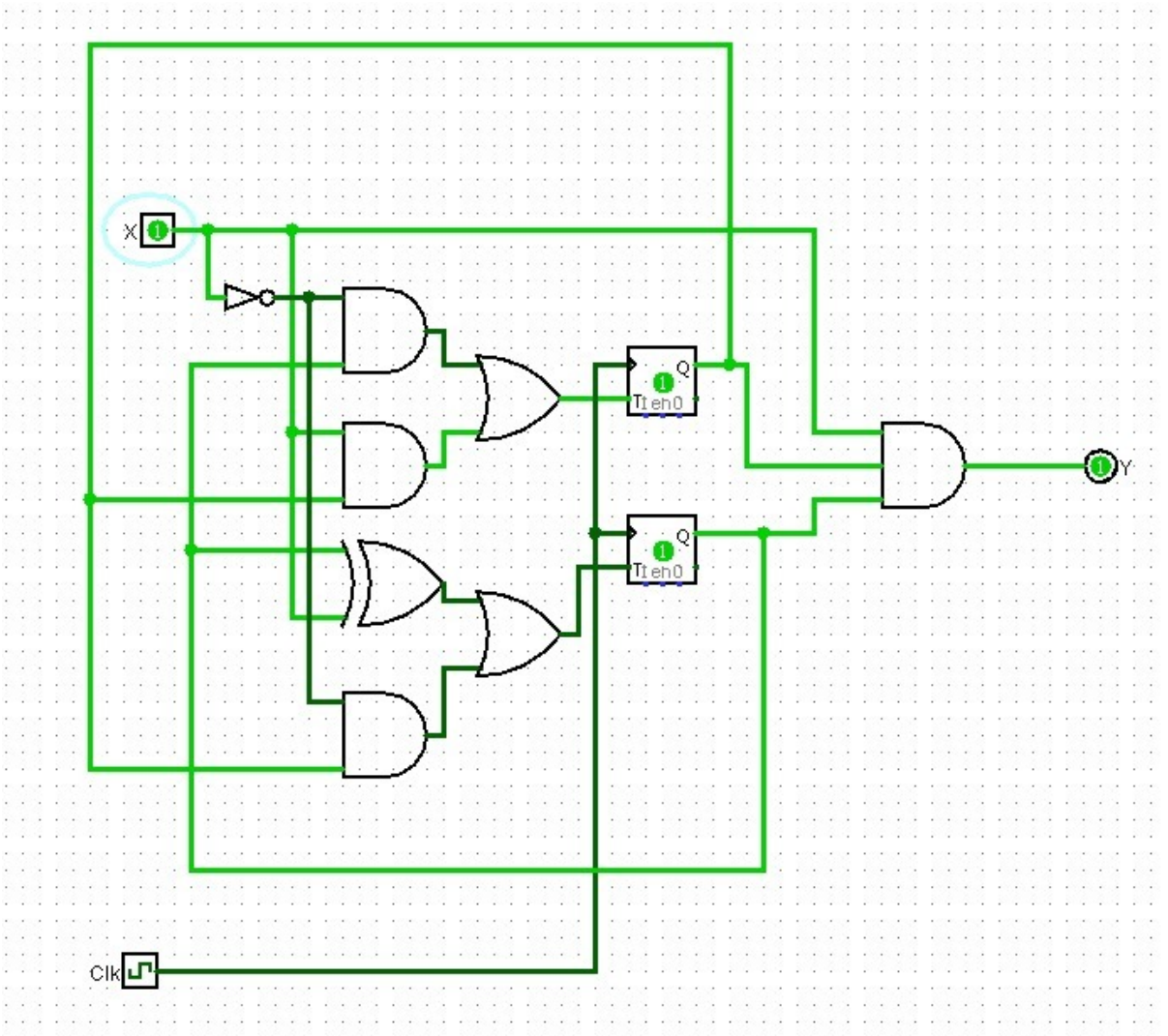


$Y = Q_2Q_1X$

Step 4 Implement the circuit
→ shown in Logisim

Basic Block Diagram :





A3) Aim of the Experiment:

To design and simulate a level sensitive JK Flip Flop and a Master - Slave JK Flip Flop in order to study the Race Around Condition in JK Flip Flop.

Method of Solving:

For J-K flip flop, if J = K = 1 and if clk = 1 for a long period of time (in case of level sensitive flip flops), output keeps on toggling as CLK is high which makes the output of the flip flop unstable and uncertain.
This problem is called Race Around condition in JK Flip Flop and it can be avoided by using a Master - Slave JK Flip Flop which is edge triggered (positive or negative) due to which the clock input is high for a very short time.

i) Designing Level Sensitive JK Flip Flop:

Requires 4 NAND gates and a clock.
Inputs : J and K
Outputs : Q and Q'

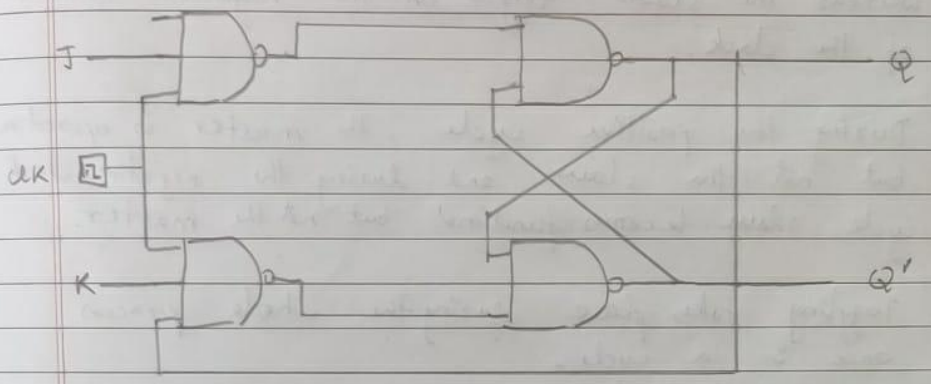
Design is similar to SR Flip Flop except in which feedback is taken from the outputs.

ii) Designing Master - Slave JK Flip Flop:

Requires 8 NAND gates and a clock
Here two JK Flip flops are connected (one called master and other slave) and the feed back goes from output of the slave Flip Flop to the Master flip flop.

Solution :

i) Level Sensitive JK Flip Flop :

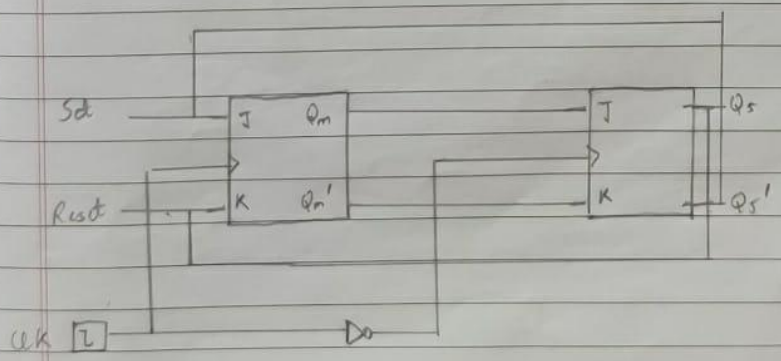


Truth table :

J	K	Q_{n+1}
1	0	1
0	1	0
0	0	Q_n
1	1	$\overline{Q_n}$

When J = K = 1, output toggles and hence uncertain when the clock is high for some time.

ii) Master - Slave JK flip flop :



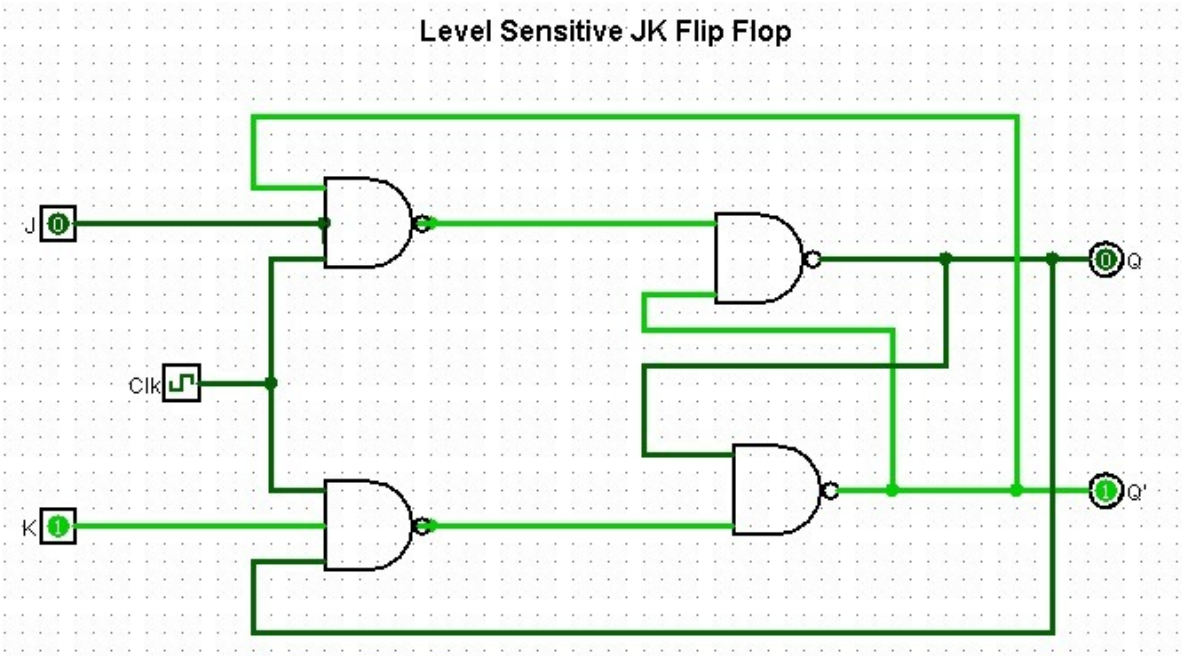
The truth table remains the same. It is important to note that the clock signal is inverted for the slave. Now when J = K = 1, the master flip flop's toggles on the positive transition of the clock whereas the slave toggles on the negative transition of the clock.

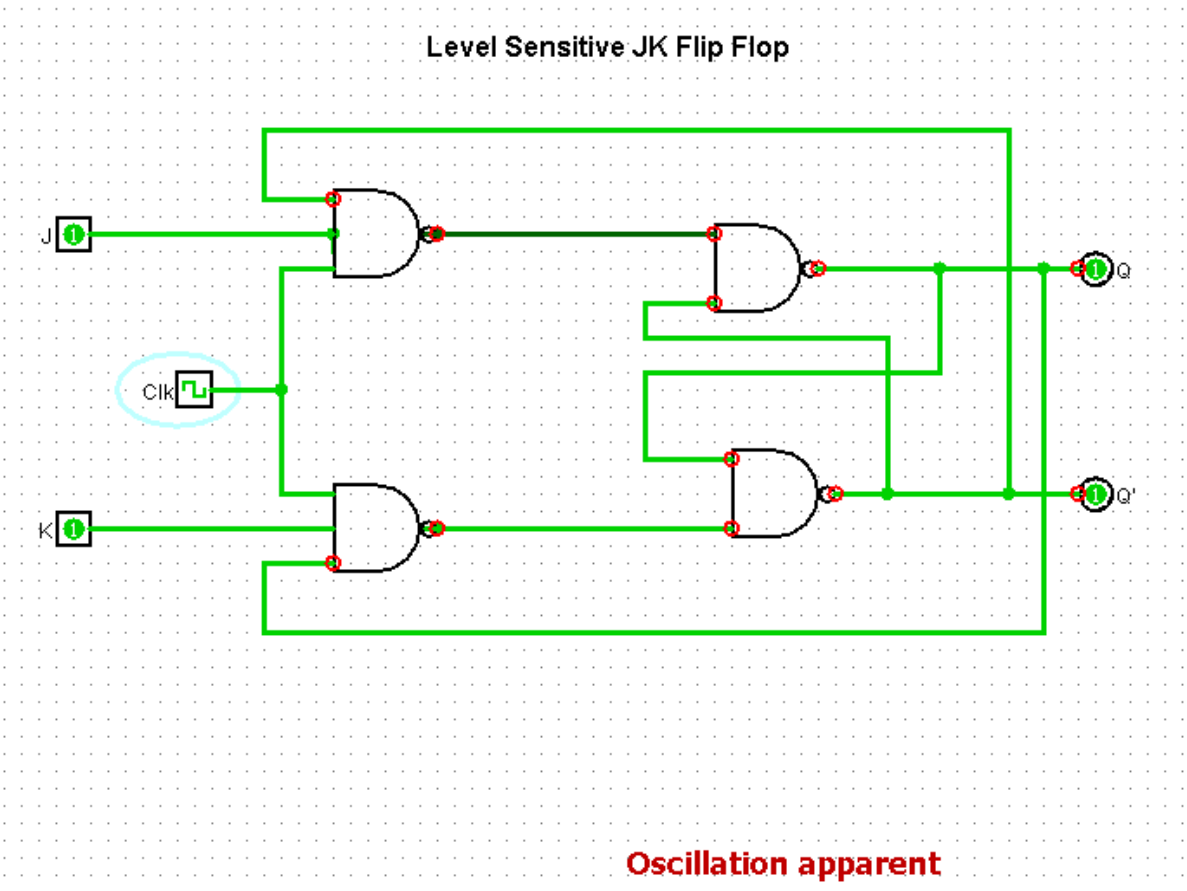
During the positive cycle, the master is operational but not the slave and during the negative clock cycle slave becomes functional but not the master.

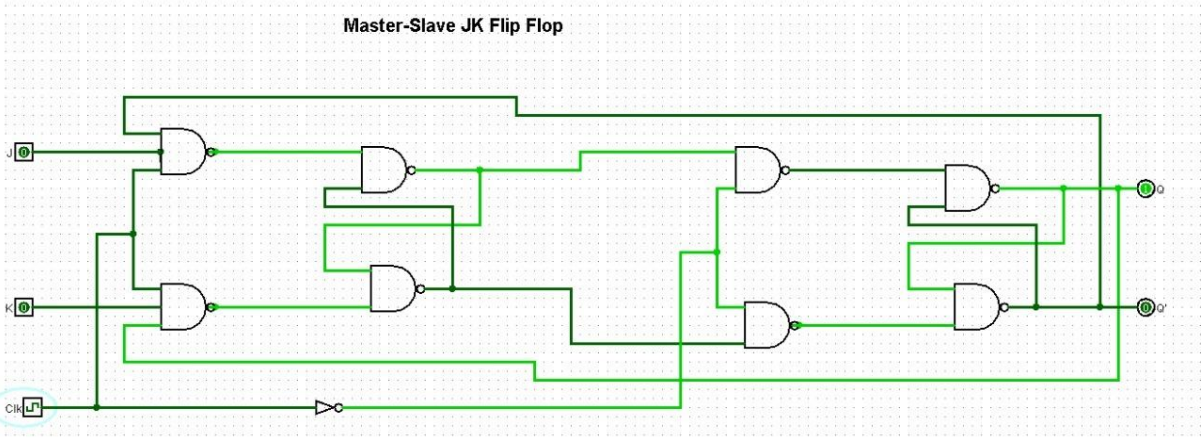
Toggling takes place during the whole process once in a cycle.

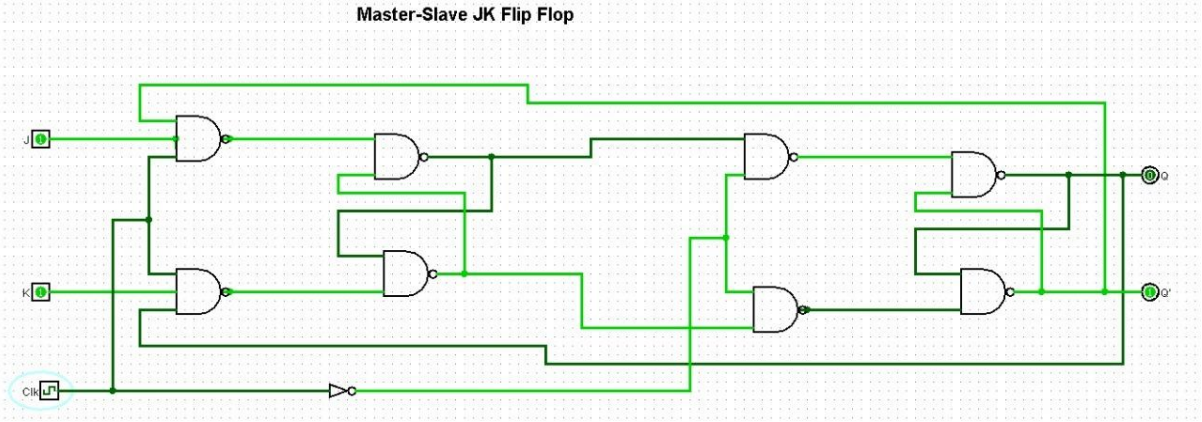
Timing Diagram :

Thus the final circuit behaves as a negative edge triggered flip flop without any race around condition.


Level Sensitive JK Flip Flop
J
Clk
K
Q
Q'


Level Sensitive JK Flip Flop
J
Clk
K
Q
Q'
Oscillation apparent


Master-Slave JK Flip Flop
J
K
Clk
Q
Q'


Master-Slave JK Flip Flop
J
K
Clk
Q
Q'