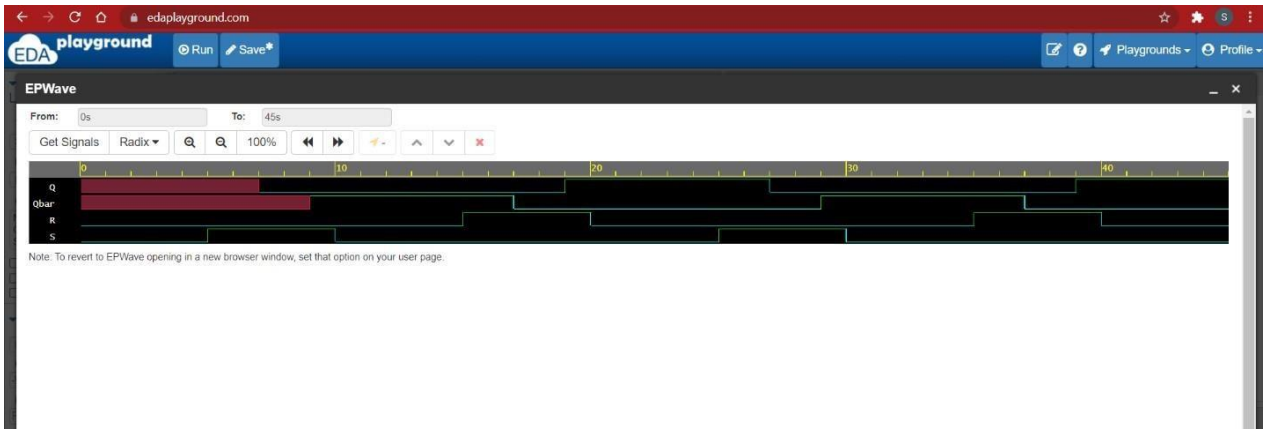
TESTBENCH:

```
//Siddansh Chawla E20CSE249 EB13
reg S,R;
wire Q,Qbar;
SR_latch dut(S,R,Q,Qbar);
initial
begin
  $dumpfile("dump.vcd");
$dumpvars(1);
R=1'b0;
S=1'b0;#5 S=1'b1;
#5 S=1'b0;
#5 R=1'b1;
#5 R=1'b0;
#5 S=1'b1;
#5 S=1'b0;
#5 R=1'b1;
#5
R=1'b0;
#5
$finish;
end
endmodule
```

DESIGN.SV:

```
//Siddansh Chawla E20CSE249 EB13
module SR_latch (input R, input S, output Q, Qbar);
assign #2 Q_i = Q;
assign #2 Qbar_i = Qbar;
assign #2 Q = ~ (R | Qbar);
assign #2 Qbar = ~ (S | Q);
endmodule
```

OUTPUT WAVEFORM:



2-TESTBENCH:

```
//Siddansh Chawla E20CSE249 EB13

module tb_q2;

reg
clk;
reg
s,r;
```

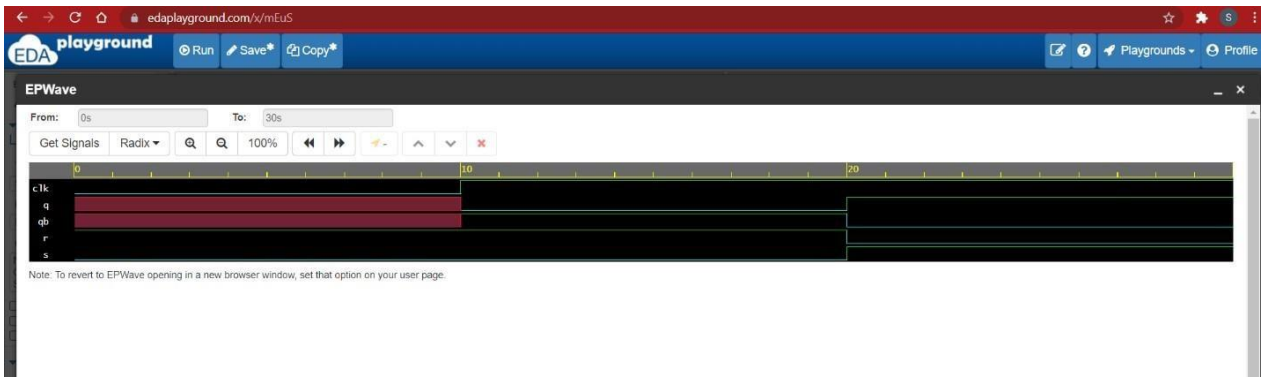
```
wire
q;
wire
qb;
```

```
SRFF check(.clk(clk), .s(s), .r(r), .q(q), .qb(qb));
 initial
  begin
  $dumpfile("dump.vcd");
 $dumpvars(1);
 $display("clk  0
 flop.  ");  clk=0;
 s=1'b0; r=1'b1;
 display;
 #5;
 $display("clk  1
 flop.  ");  clk=1;
 s=1'b0; r=1'b1;
 display;
 #5;
 s=1'b1;
 r=1'b0;
 displa
 y; #5;
 end task display;
 WINDOW
 #5 $display("s:%0h, r:%0hq:%0h, qb:%0h", s, r, q,
 qb);
 endtask
 endmodule
```

DESIGN.SV:

```
//Siddansh Chawla E20CSE249 EB13


 (input s, r, clk, output q,qb);

w1,w2,w3,w4;

nand (w1,s,clk);

nand (w2,r,clk);

nand (w3,w1,w4);

nand (w4,w2,w3);

assign q = w3;

assign qb=w4;

endmodule
```

WAVEFORM:



3- TESTBENCH:

```
    //Siddansh Chawla E20CSE249 EB13
module Q3 res;

reg S,R;

wire Q,Qbar;

  SRlatch res(S,R,Q,Qbar);

initial

begin
```

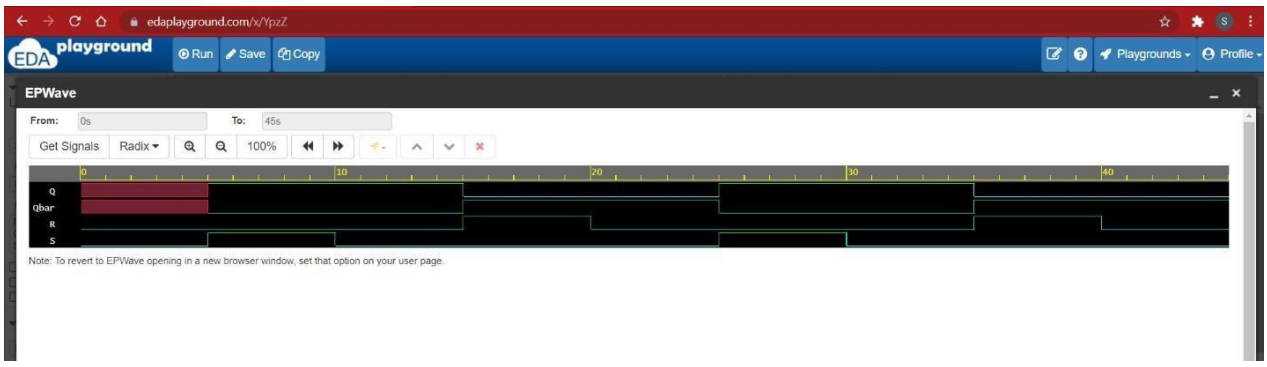
```
  $dumpfile("dump.vcd");
 $dumpvars(1);
 R=1'b0;
 S=1'b0;
 #5 S=1'b1;
 #5 S=1'b0;
 #5 R=1'b1;
 #5 R=1'b0;
 #5 S=1'b1;
 #5 S=1'b0;
 #5 R=1'b1;
 #5 R=1'b0;
 #5 $finish;
 end
 endmodule
```

DESIGN.SV:

```
SRlatch(input S,R, output Q, Qbar );
reg r1, r2;
 always@(S,R)
 begin
 if(S == 0 & R==1)
 begin
 r1 <=
 1'b0; r2
 <= 1'b1;
 end
```

```
else if(S==1 & R == 0)
begin
r1 <=
1'b1; r2
<= 1'b0;
end
else if(S == 1 & R == 1)
begin
r1 <=
0; r2
<= 0;
end
else begin r1 <= Q; r2 <= Qbar;
 end
end
assign Q= r1;
OUTPUT assign Qbar=r2;
endmodule
```

OUTPUT WAVEFORM:



4- TESTBENCH:

```
//Siddansh Chawla E20CSE249 EB13
module test; //MAKING OF TEST BENCH
```

```
reg
clk;
reg
s,r;
wire
q;
wire
qb;
SRFFLOP func(.Clk(clk), .S(s), .R(r), .Q(q), .Qbar(qb));
initial begin
  $dumpfile("dump.vcd");
$dumpvars(1);
$display("clk  0
flop.  ");  clk=0;
s=1'b0; r=1'b1;
display;
#1;
$display("clk  1
flop.  ");  clk=1;
s=1'b0; r=1'b1;
display;
#1;
s=1'b1
;
r=1'b0
;
display
; #1;
```

```
end task display;
WINDOW #1 $display("s:%0h, r:%0hq:%0h,
qb:%0h", s, r, q, qb); endtask endmodule
```

DESIGN.SV:

```
(input S,R,Clk, output Q, Qbar );
reg r1, r2;
always@(Clk,S,R)
begin
if (Clk==1)
begin
if(S == 1)
begin
r1  <=
1'b1;
r2  <=
1'b0;
end
else if(R == 1)
begin
r1 <= 0;
r2 <= 1;
end
else if(S == 0 & R
== 0) begin r1 <=
Q; r2 <= Qbar;
end end
```

```
else
begin
r1 <=
Q; r2
<=
Qbar;
end
end
assign Q= r1;
assign
Qbar=r2;
endmodule
```

OUTPUT WAVEFORM: