NANYANG TECHNOLOGICAL UNIVERSITY

Part 1

Operational Amplifiers (Op-amps)

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EE2002 Analog Electronics

Lesson Objectives

At the end of this lesson, you should be able to:

- Discuss the historical timeline of op-amps
- Identify the terminals of an op-amp
- Describe the ideal op-amp
- Explain the following concepts:
  - negative feedback, with some understanding of positive feedback
  - negative feedback op-amp for inverting and non-inverting configurations
  - equivalent circuit of an op-amp

Lesson Objectives

- Describe how the op-amp can be used as summer, subtractor, integrator, and differentiator
- Calculate input resistance and voltage at the output due to the various input voltage
- Apply the ideal characteristics to solve problems relating to ideal op-amps
- Identify the current coming in and out of an ideal op-amps based on the feedback configuration and voltage at its terminals

Lesson Objectives

- Discuss the effects of having the non-idealities in op-amp especially for I_+, I_-, and V_{IO}
- Analyse op-amp circuits in negative feedback in the presence of its non-ideal characteristics within the linear region of operations
- Calculate the AC and DC components at the op-amp output due to input sources that comprised of both non-ideal sources and its inputs
- Explain the limitation of slew rate for the op-amp

Lesson Objectives

- Explain the concept of gain-bandwidth product for op-amp
- Analyse and calculate bandwidth in relation to the gain
- Analyse how slew-rate could cause output to be distorted if slew-rate limitation is not observed

Outline

- Introduction
- Ideal Op-amps
- Special Functions of Op-amps
- Non-ideal Op-amps
- Slew Rate
- Bandwidth

Introduction

1940s

- The original concept of the operational amplifier (op-amp) came from the field of analog computers.
- It is derived from the concept of an extremely high gain, differential-input amplifier, the operating characteristics of which were determined by the feedback elements used with it.
- Different analog operations could be implemented by changing the types and arrangement of feedback elements.
- Early operational amplifiers used basic hardware of that era - the vacuum tube.

Introduction

1960s

- Significantly widespread use of op-amps did not really begin until the 1960s.
- Solid-state techniques were applied to op-amp circuit design.
- In the mid-1960s the first integrated circuit (IC) op-amp was produced which is well known as **μA709.**
- In 1968, **μA741** was produced (Lojek, 2007).

Some Op-amp Models

Figure1. GAP/R's K2-W: a vacuum-tube op-amp (1951).

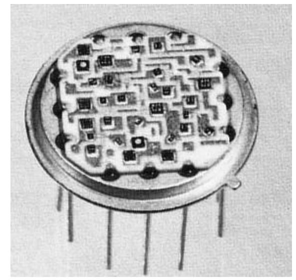
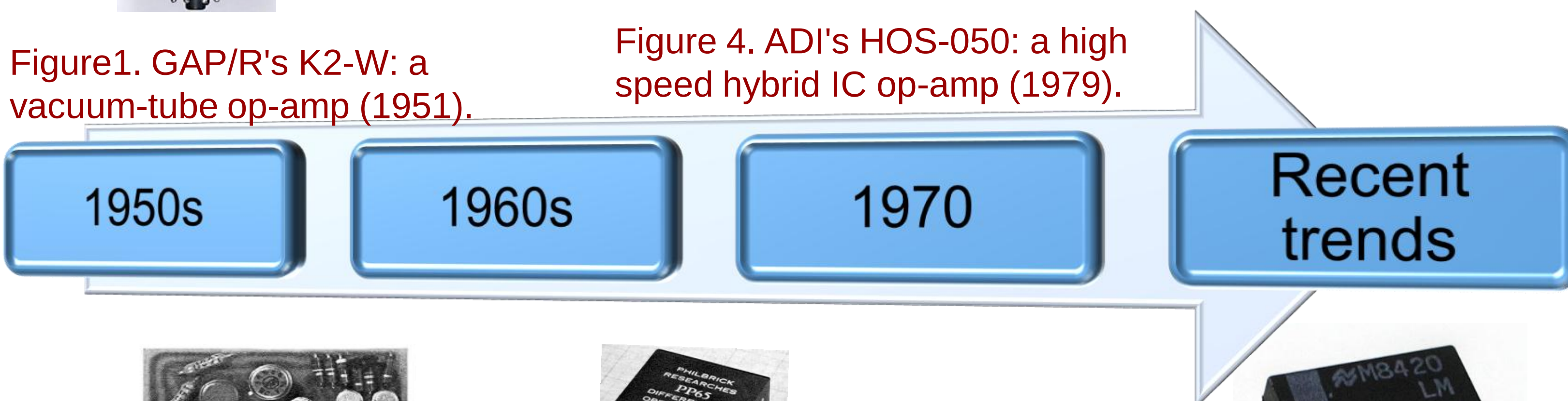


Figure 4. ADI's HOS-050: a high speed hybrid IC op-amp (1979).



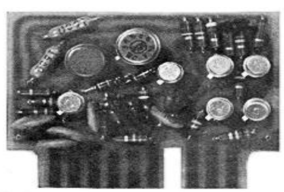


Figure 2. GAP/R's model P45: a solid-state, discrete op-amp (1961).

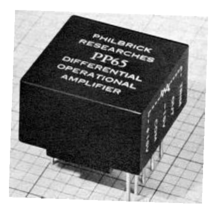


Figure 3. GAP/R's model PP65: a solid-state op-amp in a potted module (1962).

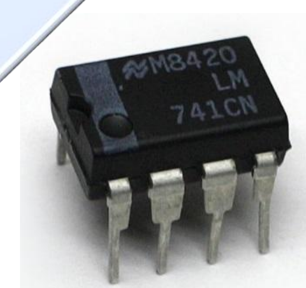


Figure 5. An op-amp in a modern mini Dual-in-line Package (DIP).

The 741 Op-amp

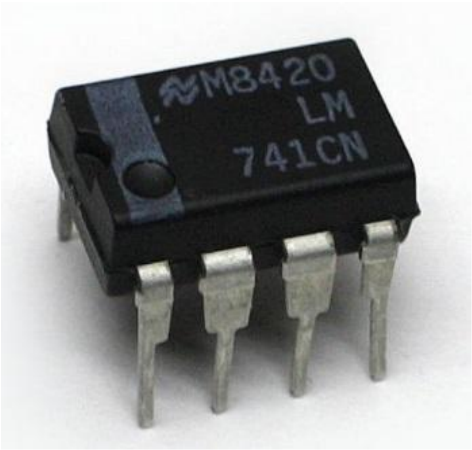


Figure 5. An op-amp in a modern mini Dual-in-line Package (DIP).

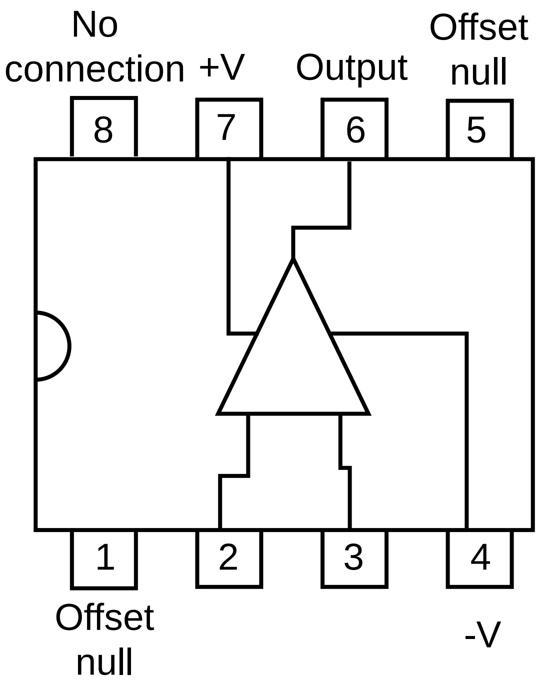


Figure 6. A typical 8 pin DIP op-amp integrated circuit.

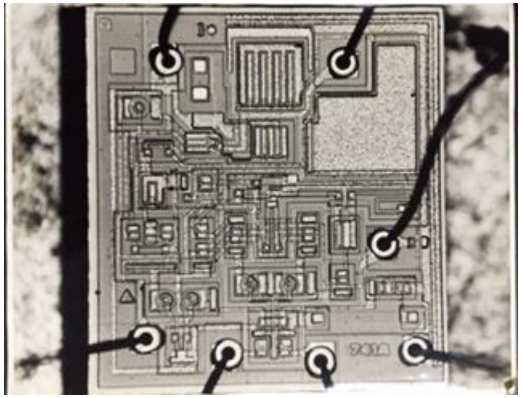


Figure 7. A micro-photograph of the 741 op-amp.

The 741 Op-amp

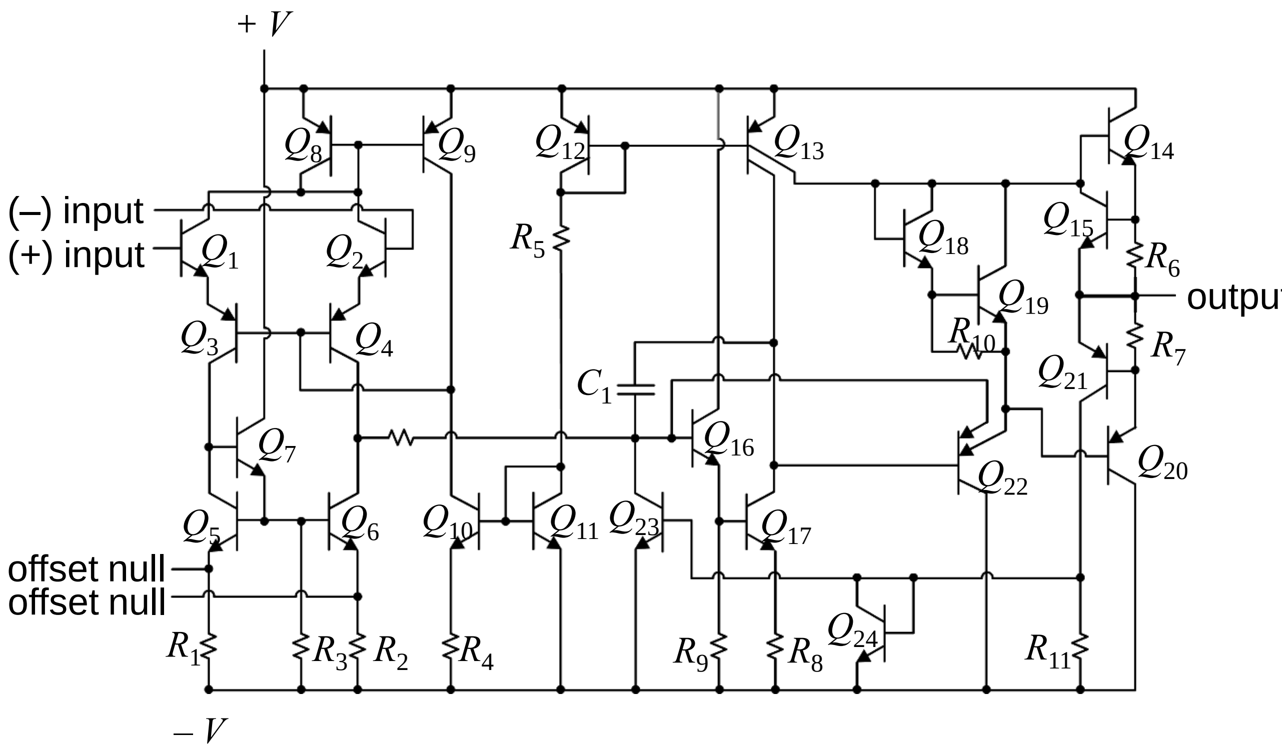


Figure 8. Internal schematic of a model 741 amplifier.

The Op-amp Terminals

- From a signal point of view, op-amp has three terminals: two input terminals for differential signal input and one single-ended output terminal.
- Figure 9 shows the symbol used to represent the op-amp; terminals 1 and 2 are input terminals, and terminal 3 is the output terminal.

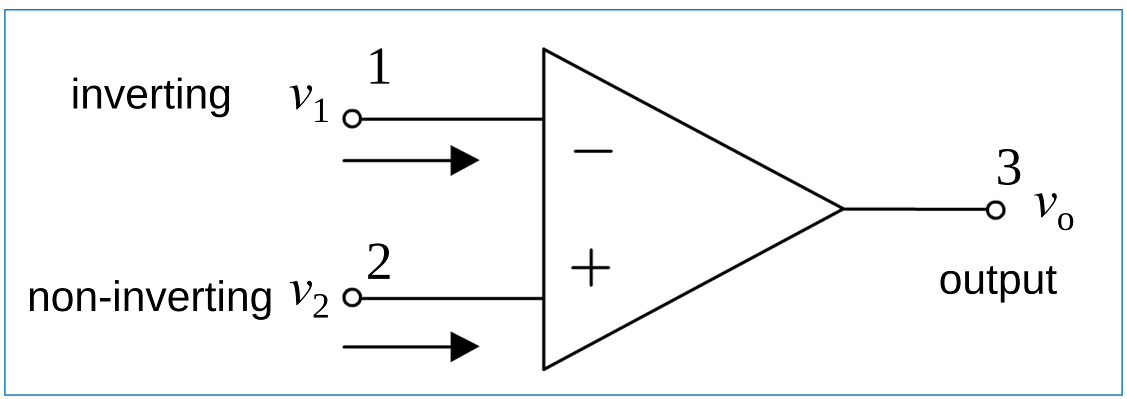


Figure 9. Circuit symbol for the op-amp.

$$v_o = A_{vOL} v_{id}$$

$$= A_{vOL}(v_2 - v_1)$$

where

$$v_{id} = (v_2 - v_1)$$

The Op-amp Terminals

- Most IC op-amps require two power supplies V^+ and V^- sometimes given as $[+V_{CC}; V_{CC}; V_{DD}]$ and $[-V_{CC}; V_{EE}; V_{SS}]$ as shown in Figure 10.

- No pin is provided for the reference grounding point; the reference grounding point in op-amp circuits is just the common terminal of the two power supplies.

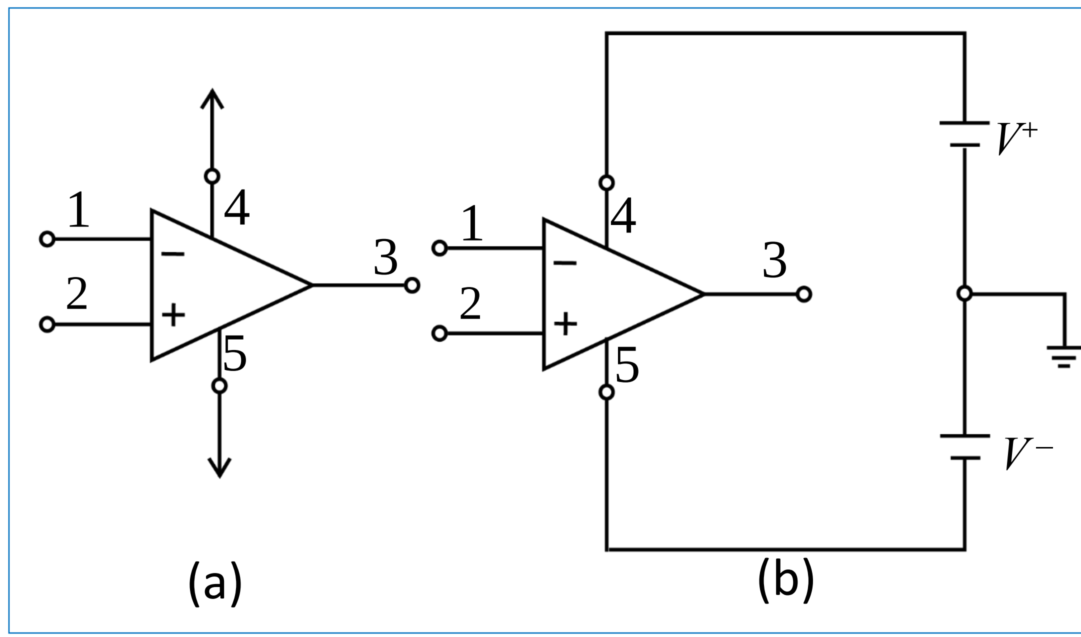
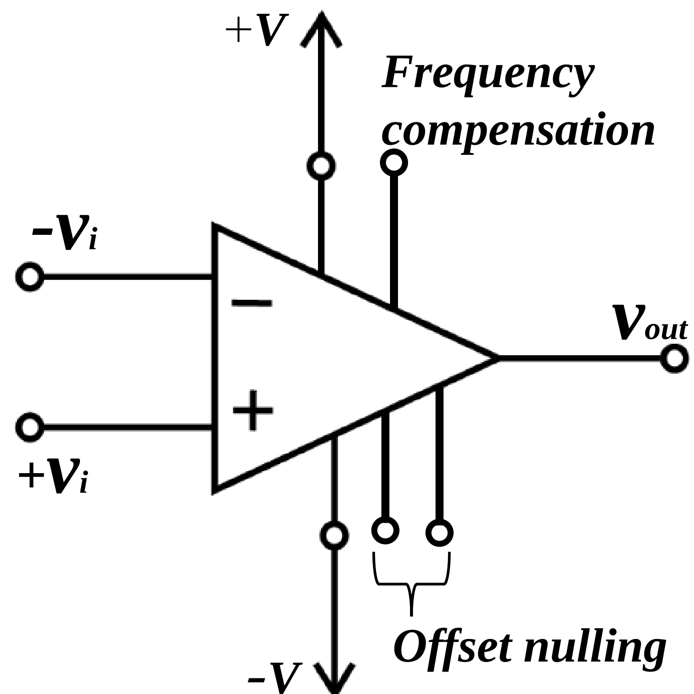


Figure 10. The op-amp shown connected to DC power supplies.

The Op-amp Terminals

- It is common that the power supply terminals are not shown explicitly in the schematic diagram.
- Note that all op-amp circuits require power for their operation.
- In addition to the three signal terminals and two power supply terminals, an op-amp may include terminals for frequency compensation and terminals for offset nulling.



The Ideal Op-amp

- An op-amp is suppose to sense the difference between the voltage signals applied at its two differential inputs, i.e., $v_2 - v_1$.
- Multiply $v_2 - v_1$ by a number A_{voL} (open-loop voltage gain) to cause $A_{\mathrm{voL}}(v_2 - v_1)$ to appear at the output terminal.

$$\boxed{\begin{aligned} v_{\mathrm{o}} &= A_{\mathrm{voL}}(v_2 - v_1) \\ &= A_{\mathrm{voL}} v_{\mathrm{id}} \end{aligned}}$$

- The real op-amp has a very large gain, A_{voL}, but not infinite.

Properties of Ideal Op-amp

i. The voltage gain is infinite i.e. $A_{\text{voL}} = \infty$.

This implies that with finite output voltage, the required differential input is zero.

$$v_{\text{id}} = (v_2 - v_1) = \frac{v_{\text{o}}}{A_{\text{voL}}} \rightarrow 0$$

as $A_{\text{vOL}} \rightarrow \infty$ and $v_0 \neq \infty$ since the output is finite.

ii. The input differential resistance is infinite, $R_{\text{id}} = R_{\text{in}} = \infty$.

Ideal op-amp does not draw any input current; the signal current into terminal 1 and terminal 2 are both zero.

Properties of Ideal Op-amp

iii. The output resistance is zero, $R_o = 0$.

The output voltage at terminal 3 with respect to the voltage at the input terminals is always $A_{voL}(v_2 - v_1) = A_{voL} v_{id}$; independent of the current that may be drawn from output terminal into a load if the load current is finite, $\left| I_{R_L} \right| < \infty$.

iv. The bandwidth is infinite, $BW = \infty$.

This implies that there will be no phase shift between the input and output signals.

v. There is zero input offset voltage, $v_{IO} = 0$. This implies that $v_o = 0$ if $v_{id} = 0$.

Properties of Ideal Op-amp

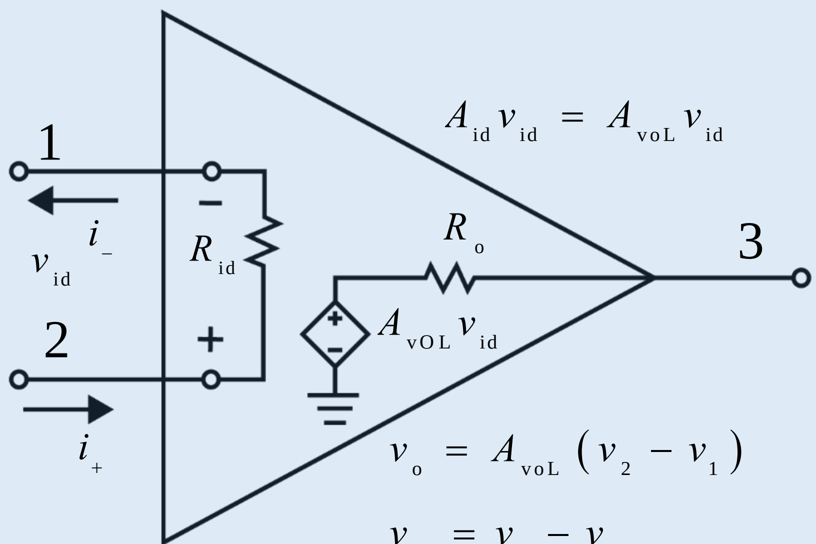
vi. Slew rate, $SR = \infty$.

However, slew rate is defined as the maximum rate of change of the output voltage, and therefore,

$$SR > \left.\frac{\mathrm{d}v_o}{\mathrm{d}t}\right|_{\max} = \infty$$

Equivalent Circuit

The equivalent circuit for an **op-amp**

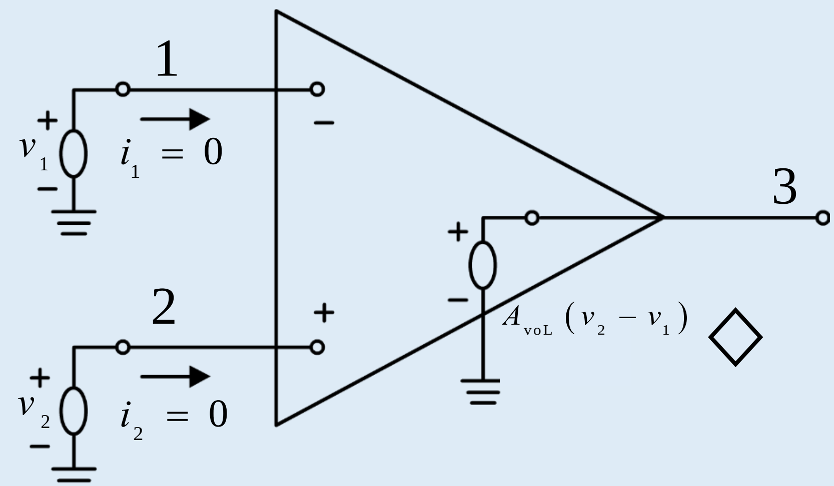


$$A_{id}v_{id} = A_{voL}v_{id}$$

$$v_o = A_{voL}(v_2 - v_1)$$

$$v_{id} = v_2 - v_1$$

The equivalent circuit for an **ideal op-amp**



For Ideal Op-amp

$$\because \quad R_{id} = \infty \quad \Rightarrow \quad i_+ = 0$$

$$i_- = 0$$

Equivalent Circuit

The differential transfer characteristic v_o versus $v_{id} = v_+ - v_-$ of the basic op-amp (Figure 11) is shown in Figure 12.

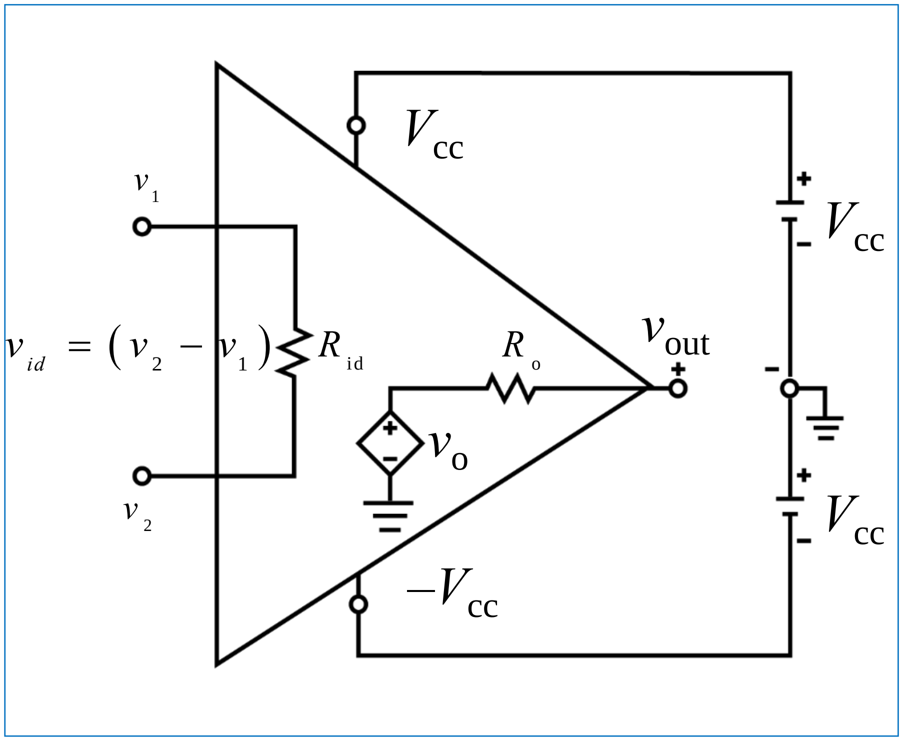


Figure 11. Simplified representation of basic operational amplifier.

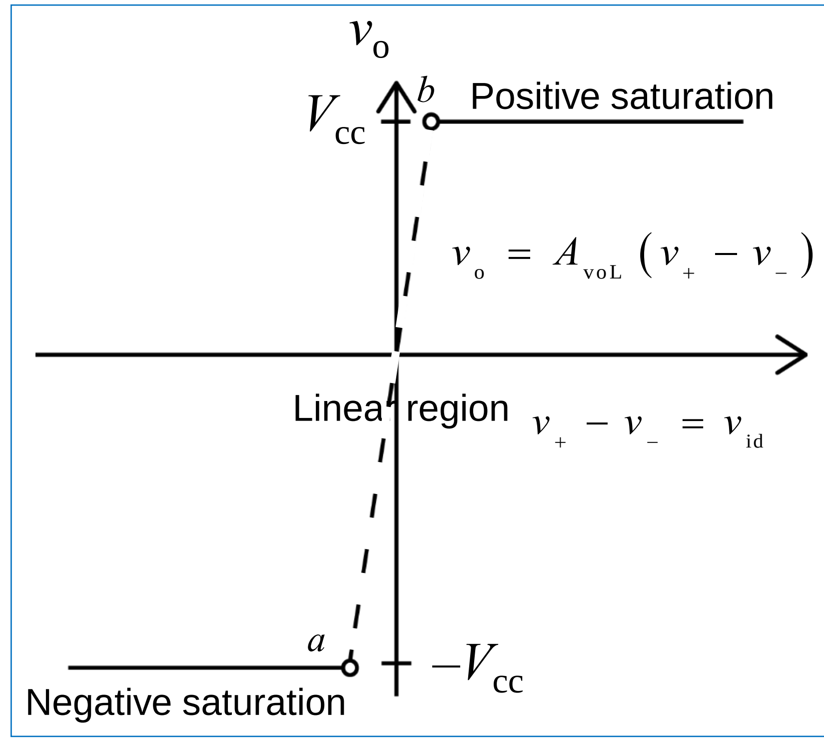


Figure 12. Differential mode voltage transfer characteristic v_o versus $(v_+ - v_-)$.

Equivalent Circuit

- The use of $\pm V_{cc}$ allows the v_o of the op-amp to swing in both positive and negative voltage directions.
- In the linear region, $v_o = A_{voL}(v_+ - v_-)$.
  - Op-amps used as amplifiers operate within this region.
  - This is usually ensured by employing **negative feedback** in the circuits.
- In the positive saturation region, $v_o = V_{cc}$ for $A_{voL}v_{id} > V_{cc}$.
- For negative saturation region, $v_o = -V_{cc}$ for $A_{voL}v_{id} < -V_{cc}$.

Equivalent Circuit

Practically the saturation limits of v_o are 1 V to 2 V below the absolute values of the supplies.

$$v_\mathrm{o} = A_\mathrm{vOL}(v_+ - v_-) \quad \text{———} \quad -V_\mathrm{cc} < v_\mathrm{o} < +V_\mathrm{cc}$$

$$v_\mathrm{o} = +V_\mathrm{cc} \quad \text{———} \quad v_\mathrm{o} > +V_\mathrm{cc}$$

$$v_\mathrm{o} = -V_\mathrm{cc} \quad \text{———} \quad v_\mathrm{o} < -V_\mathrm{cc}$$

If $R_\mathrm{o} = 0$, then

$$v_\mathrm{out} = A_\mathrm{vOL}(v_+ - v_-) \text{ for } -V_\mathrm{cc} < v_\mathrm{out} < +V_\mathrm{cc}$$

$$v_\mathrm{out} = +V_\mathrm{cc} \text{ for } v_\mathrm{out} > +V_\mathrm{cc}$$

$$v_\mathrm{out} = -V_\mathrm{cc} \text{ for } v_\mathrm{out} < -V_\mathrm{cc}$$

Concept of Feedback

If portion of amplifier or circuit output is brought back to the input through a specific network and mixed with input the process is known as feedback.

Classification of Feedback:

- Positive Feedback

  Feedback signal is returned to op-amp's non-inverting input.

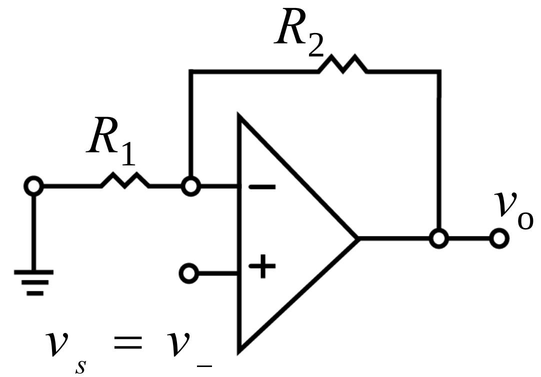
- Negative Feedback

  Feedback signal is connected to the inverting input of the op-amp.

Concept of Feedback

Examples of Negative Feedback:

Negative Feedback
Non-inverting Gain Amplifier



$$v_S = v_+ = v_- = v_{R_1}$$

$$\frac{v_{R_1}}{R_1} = i_{R_1}$$

$$v_{R_2} = i_{R_2} \times R_2$$

But $i_{R_1} = i_{R_2} \because I_- = I_+ = 0$

$$\therefore \quad v_{R_2} = \frac{v_{R_1}}{R_1} \times R_2 = \frac{v_s}{R_1} \times R_2$$

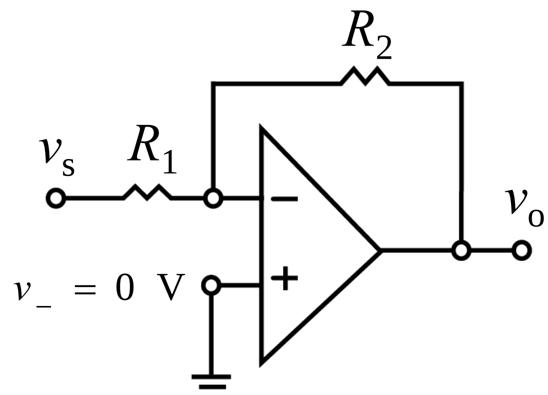
$$v_o = v_{R_1} + v_{R_2} = v_s + \frac{v_s}{R_1} \times R_2$$

$$\frac{v_o}{v_s} = 1 + \frac{R_2}{R_1} = A_{vCL}$$

Concept of Feedback

Examples of Negative Feedback:

Negative Feedback
Inverting Gain Amplifier



$$v_- = v_+ = 0$$

$$\frac{v_s}{R_1} = i_{R_1}$$

$$v_{R_2} = i_{R_2} \times R_2$$

But $i_{R_1} = i_{R_2} \because I_- = I_+ = 0$

$$v_o = -v_{R_2} = -i_{R_2} \times R_2$$

$$= -i_{R_1} \times R_2 = -\frac{v_s}{R_1} \times R_2$$

$$\frac{v_o}{v_s} = -\frac{R_2}{R_1} = A_{vCL}$$

Concept of Feedback

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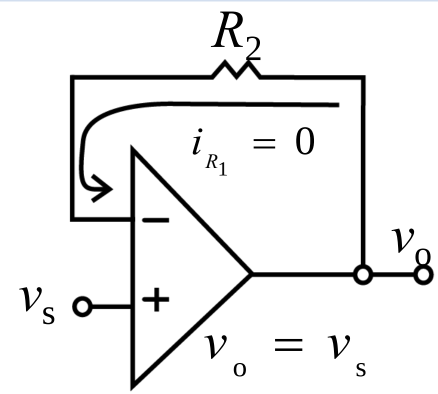
Examples of Negative Feedback:

Negative Feedback
Non-inverting Unity Gain Amplifier



$$v_s = v_+ = v_- = v_o$$

$$v_o = v_- + (i_- \times R_2)$$

$$= v_+ + (i_- \times R_2)$$

$$= v_s + (i_- \times R_2)$$

$$= v_s \quad \because \quad i_- = 0$$

Alternatively,

$$\frac{v_o}{v_s} = 1 + \frac{R_2}{R_1} = 1 + \frac{R_2}{\infty}$$

$$= 1 + 0$$

$$= 1 = A_{vCL}$$

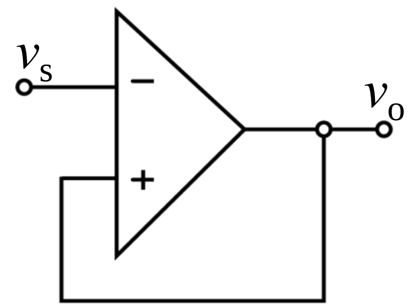
As $i_- = 0$, $v_{R_2} = 0$

Hence, R_2 has no effect, and can be shorted for convenience.

Concept of Feedback

Examples of Positive Feedback:

Note: Output is in Non-linear Region and Input Differential is not Zero



$$v_s \neq v_+ = v_o$$

$$v_S = v_-$$

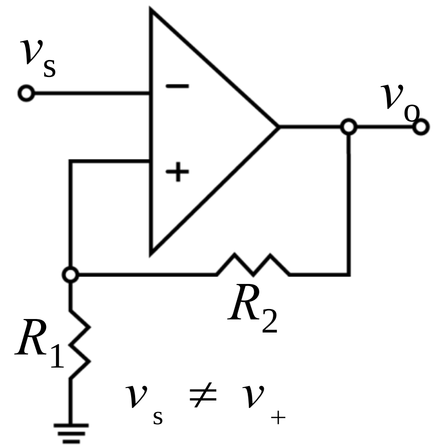
$$v_O = -V_{CC} \text{ for } v_- > v_+$$

$$v_O = +V_{CC} \text{ for } v_- < v_+$$

Concept of Feedback

Examples of Positive Feedback:

Note: Output is in Non-linear Region and Input Differential is not Zero



$$v_s = v_-$$

$$v_O = -V_{CC} \text{ for } v_- > v_+$$

$$\therefore v_+ = -V_{CC} \times \frac{R_1}{R_1 + R_2}$$

(a potential divided voltage of the output voltage, $-V_{CC}$)

$$v_O = +V_{CC} \text{ for } v_- < v_+$$

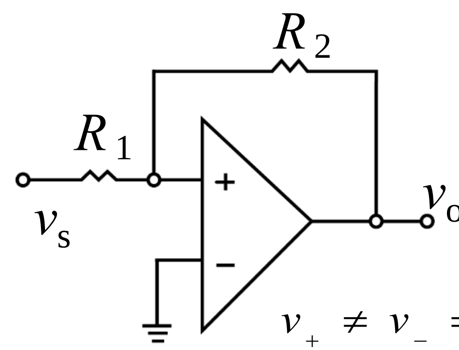
$$\therefore v_+ = +V_{CC} \times \frac{R_1}{R_1 + R_2}$$

(a potential divided voltage of the output voltage, $+V_{CC}$)

Concept of Feedback

Examples of Positive Feedback:

Note: Output is in Non-linear Region and Input Differential is not Zero



$v_+ \neq v_- = 0\ \text{V}$

$v_s > 0 \;\Rightarrow\; v_+ > v_-$ (ground)

$v_o = +V_{CC}$

$$\therefore\ v_+ = \left[(+V_{CC} - v_s) \times \frac{R_1}{R_1 + R_2} \right] + v_s$$

a potential divided voltage between the output and v_s, wrt to ground

$-v_s < 0 \;\Rightarrow\; v_+ < v_-$ (ground)

$v_o = -V_{CC}$

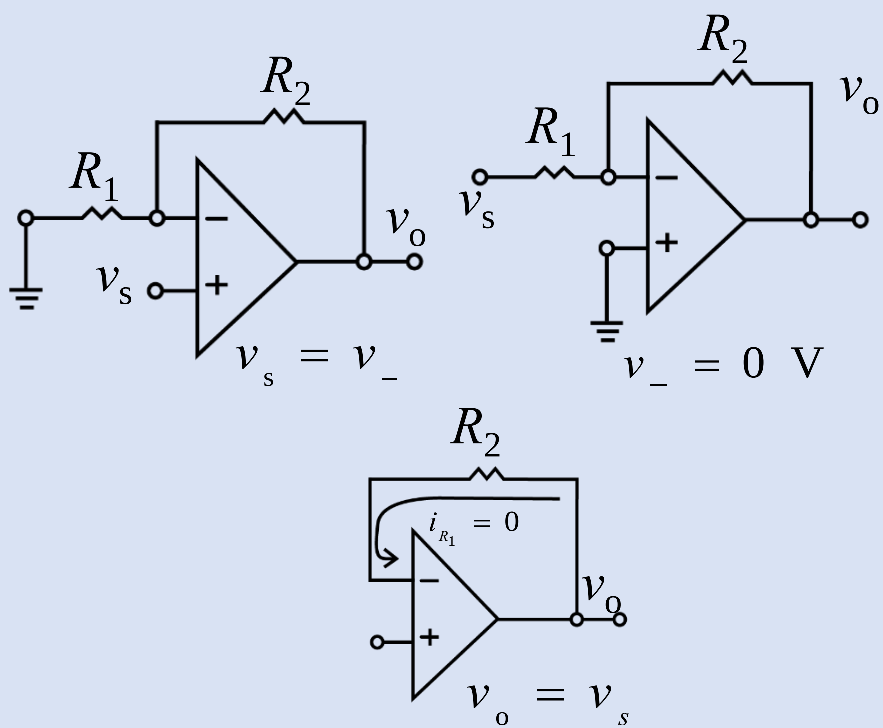
$$\therefore\ v_+ = \left[(-V_{CC} + v_s) \times \frac{R_1}{R_1 + R_2} \right] - v_s$$

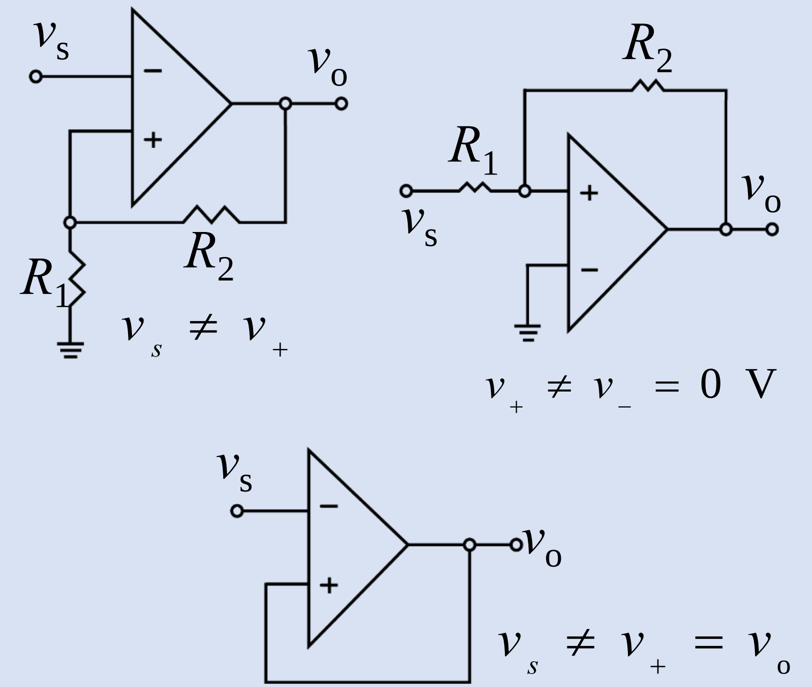
a potential divided voltage between the output and -v_s , wrt to ground

Concept of Feedback

Comparative Table

Examples of Negative Feedback	Examples of Positive Feedback





Concept of Feedback

For an ideal op-amp used in a negative feedback circuit:

$$v_{id} = (v_{+} - v_{-})$$

$$= \frac{v_{o}}{A_{voL}}$$

As $A_{voL} \rightarrow \infty \Rightarrow v_{id} \rightarrow 0$

i.e., $v_{-} = v_{+}$

This leads to :

For any output voltage in the linear operating region of an op-amp with negative feedback, the two inputs are virtually at the same potential.

Using in an op-amp circuit operating in the linear region, $v_{-} = v_{+}$

Analysis of Circuits Containing Op-amp

Op-amps used in circuits that employed negative feedback are working in linear region as amplifying devices.

*Under this condition, we have $v_{id} = 0 \Rightarrow v_{-} = v_{+}$

Under open-loop or positive feedback condition the op- amp is working in its non-linear region and its output is saturated and amplitude limited.

Generally, the output value is 1 to 2 volts below the supply voltage.

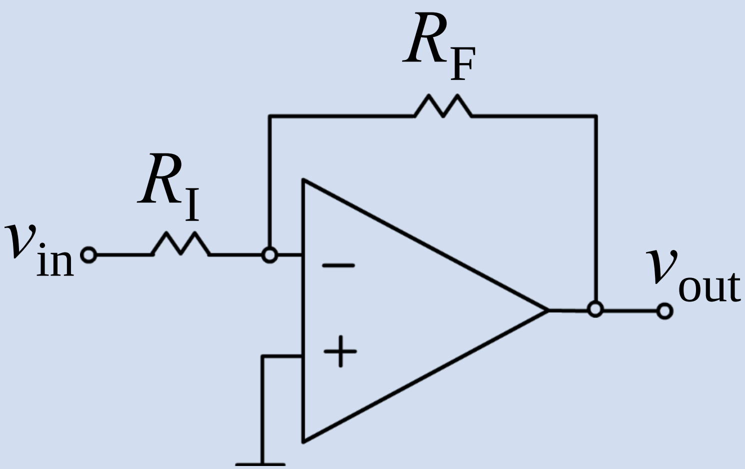
Analysis of Circuits Containing Op-amp

For $V_{cc} = \pm 15$ V then $v_o = \pm$ (13 to 14) V
The relationship $v_{id} = 0$ is no more valid and its value depends on the input voltage v_i.

From the above it is very important for one to decide the type of feedback, negative or positive, before performing the circuit analysis.

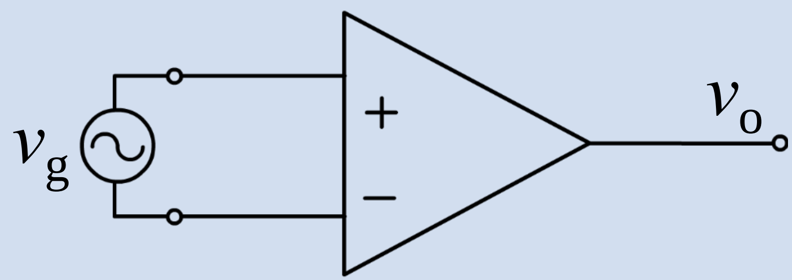
Analysis of Circuits Containing Op-amp

Op-amp in Closed-loop Operation



Linear region → Amplifier

Op-amp Open-loop Operation



Non-linear region → Not an amplifier

(Comparator)

Analysis of Circuits Containing Op-amp

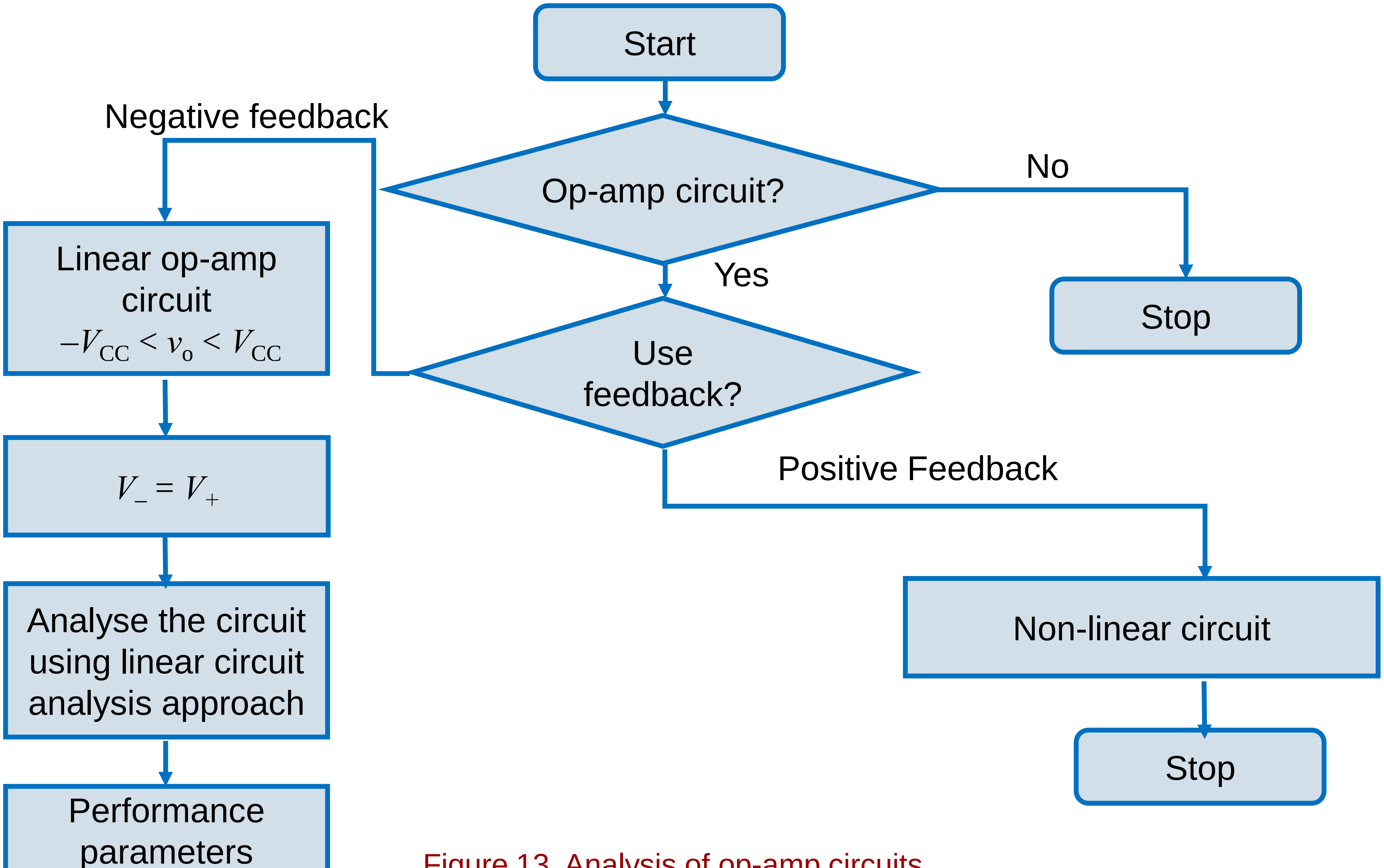
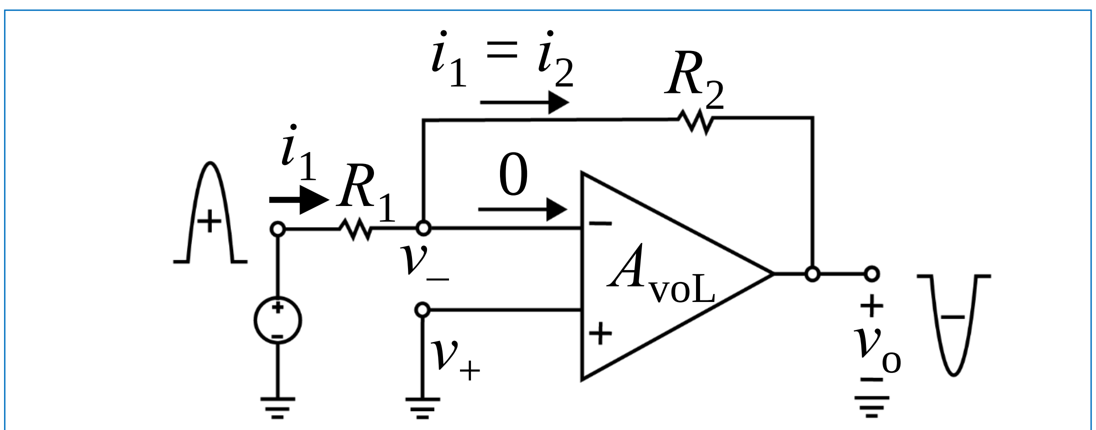


Figure 13. Analysis of op-amp circuits.

Inverting Negative Feedback Amplifier Circuits

- An inverting amplifier circuit using an op-amp is shown in Figure 14 and inverts the phase of the input signal while amplifying it.
- The feedback employed in the circuit, from v_o through feedback resistor R_2 back to the inverting input, is negative.
- Therefore, the op-amp is operating as an active linear device and $v_- = v_+$.

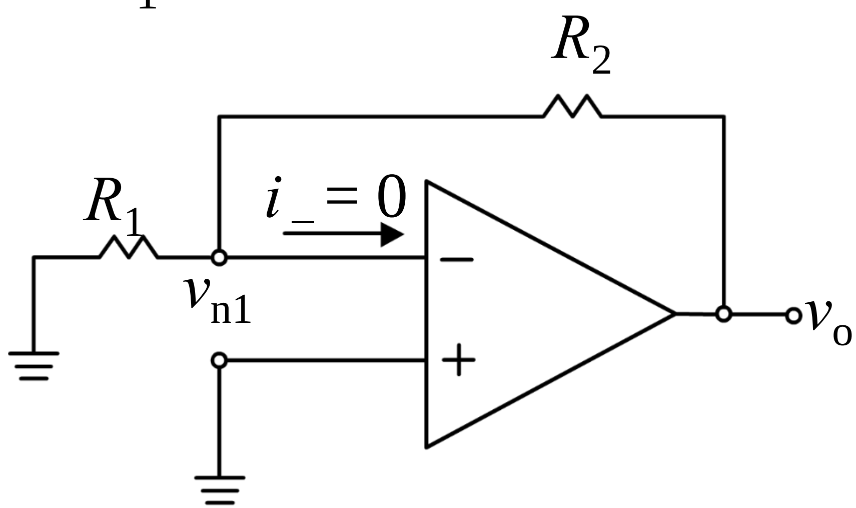


$$\boxed{v_- = v_+ = 0\ \text{V}}$$

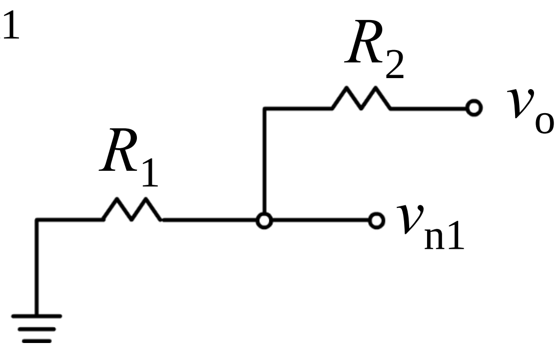
Figure 14. An Inverting feedback amplifier circuit using an op-amp.

Application of Linear Superposition Principle

i. Kill v_1



$v_{n1} = v_{R1}$



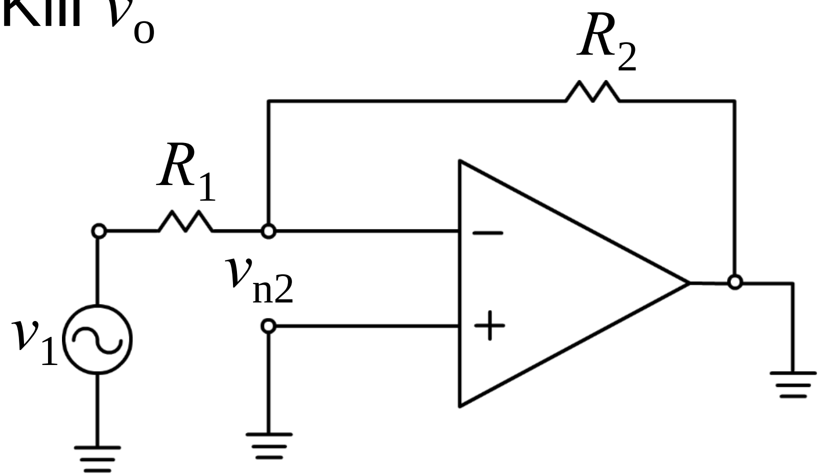
R_1 & R_2 form a voltage divider circuit in series with v_o.

Therefore,

$$\boxed{v_{n_1} = \left(\frac{R_1}{R_1 + R_2} \right) v_o}$$

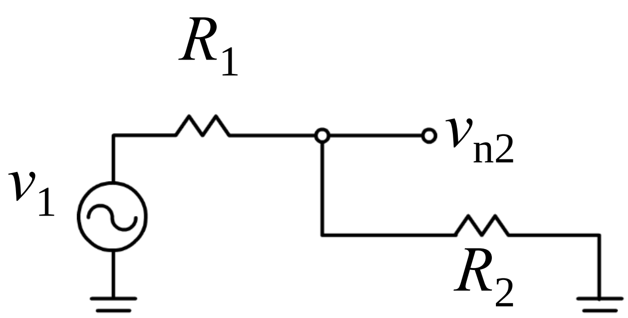
Application of Linear Superposition Principle

ii. Kill v_o



$\because \quad v_{n2} = v_{R2}$

Therefore,



$$\boxed{v_{n2} = \left(\frac{R_2}{R_1 + R_2} \right) v_1}$$

Application of Linear Superposition Principle

iii. $v_n = v_{n_1} + v_{n_2}$

$$\therefore \quad v_n = \left(\frac{R_1}{R_1 + R_2}\right) v_0 + \left(\frac{R_2}{R_1 + R_2}\right) v_1$$

Setting $v_n = 0$ yields:

$$\left(\frac{R_1}{R_1 + R_2}\right) v_o = -\left(\frac{R_2}{R_1 + R_2}\right) v_1$$

$$A_{voL} = \frac{v_o}{v_1}$$

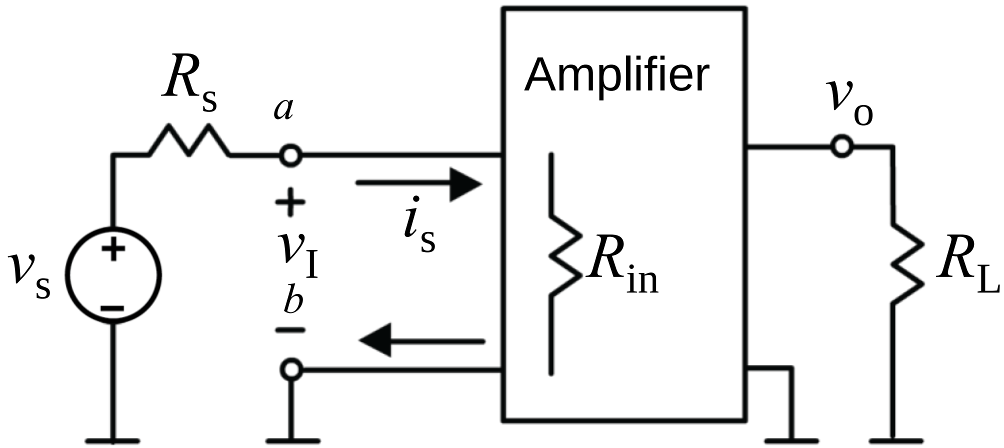
Inverting gain

$$= -\frac{R_2}{R_1} \left[\frac{\text{V}}{\text{V}}\right] = \left|\frac{R_2}{R_1}\right| \angle -180^\circ$$

This leads to:

Any voltage applied to the end of a resistor, connected to the inverting input of an op-amp in a circuit, will be multiplied by the inverting gain as it appears on the amplifier output.

Concept of R_{in} of a Circuit



$$R_{in} = \frac{v_I}{i_s} \qquad i_s = \frac{v_s}{R_s + R_{in}}$$

If $R_{in} \rightarrow \infty \Rightarrow i_s \rightarrow 0$

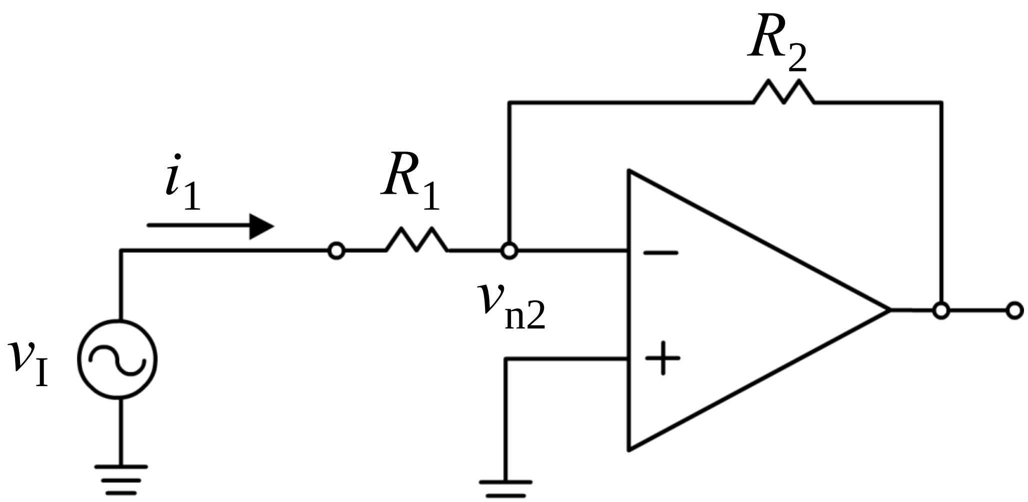
That is, the applied source v_s is not required to deliver signal power ($v_I i_s$) to the amplifier.

Concept of R_{in} of a Circuit

Where does the signal output power $\frac{v_o}{R_L}$ come from ?

- It is from the DC power supplies of the amplifier.
- The supplies are not shown in the figure.
- For applied voltage signal v_s,
  it requires R_{in} to be ∞ or $\geq 10R_s$ and $v_I \approx v_s$.

Input Resistance, R_{in}



$$v_- = v_+ = 0\ \text{V}$$

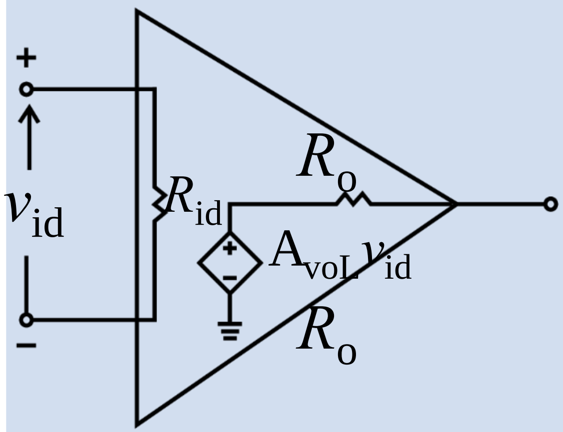
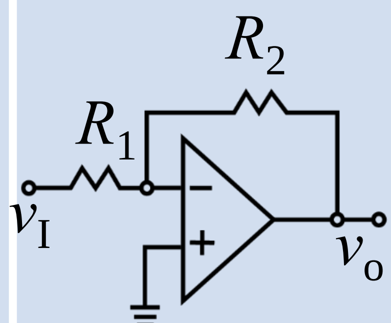
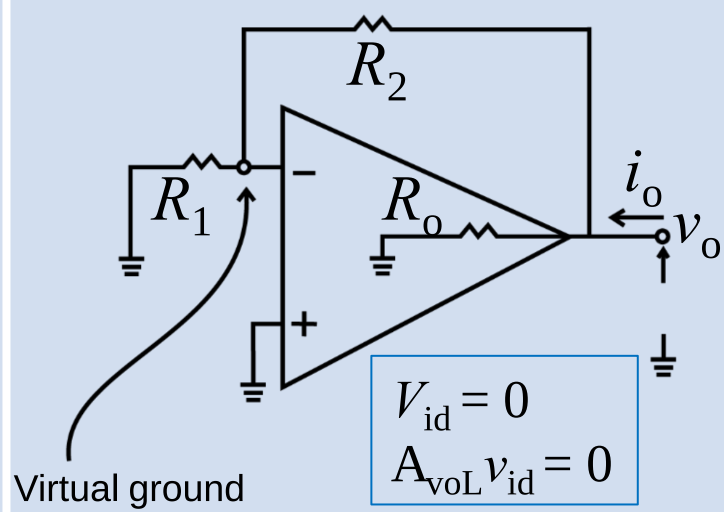
The input resistance of the inverting feedback circuit seen by v_I , by Ohm's Law, is :

$$v_{R_1} = v_I$$

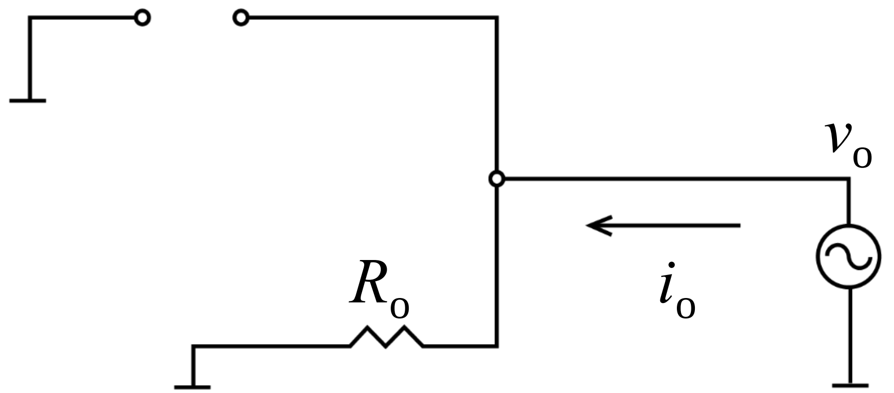
$$v_{R_1} = i_1 R_I$$

$$R_{in} = \frac{v_I}{i_1} = R_1$$

Output Resistance, R_{out}

Equivalent circuit of a practical op-amp	Op-amp used as an inverting amplifier	For an ideal op-amp:
		$R_{id} = \infty \Rightarrow i_{+} = 0, i_{-1} = 0$ $A_{voL} = \infty, R_{0} = 0 \Rightarrow v_{0} = A_{voL} v_{id}$ 

Output Resistance, R_{out}



The output resistance, R_{out}, looking into the output terminal of the op-amp circuit is

$$R_{out} = \frac{v_o}{i_o} = R_o$$

$$= 0$$

(R_o = 0 for ideal op-amp)

Non-inverting Feedback Amplifier Circuits

A non-inverting feedback amplifier using an op-amp is illustrated in Figure15.

This circuit has the same phase on the output as on the input; only the magnitude of the output voltage is different.

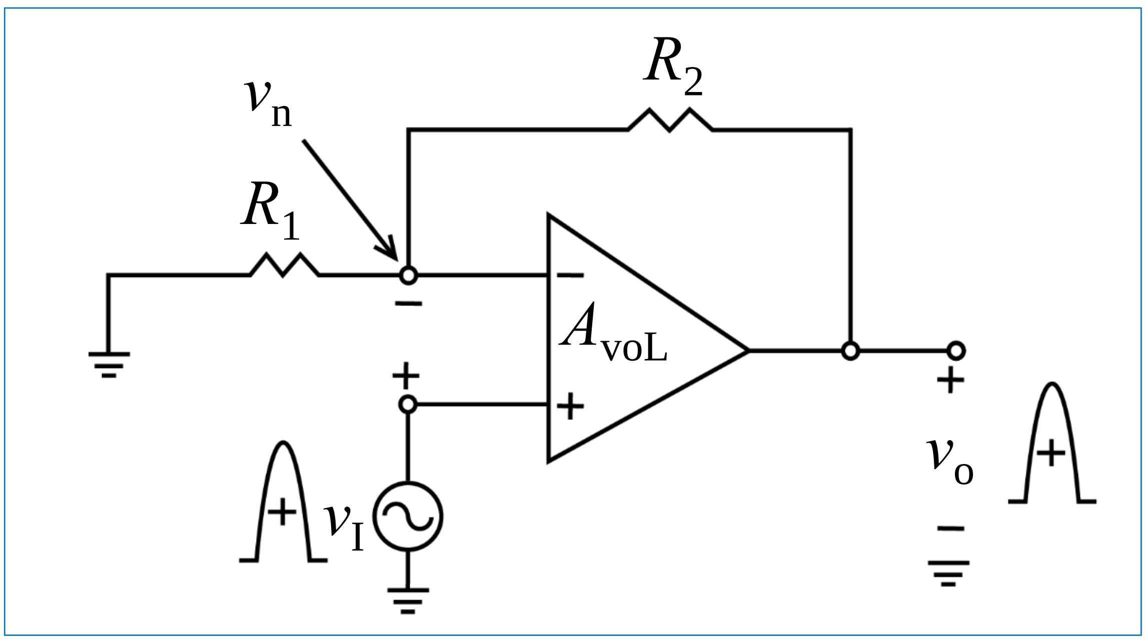


Figure 15. The non-inverting configuration.

Non-inverting Feedback Amplifier Circuits

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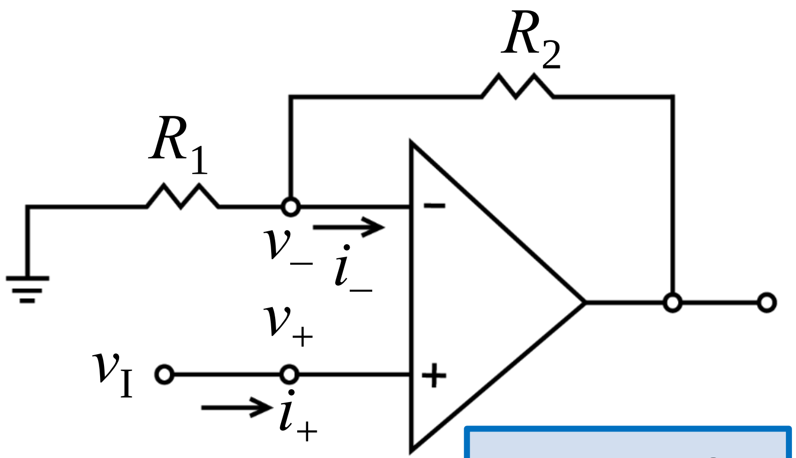


$$\boxed{i_- = i_+ = 0}$$

- It uses negative feedback (v_o through R_2 to negative input)
- $v_- = v_+$
- $v_+ = v_I$
- $v_- = \left(\dfrac{R_1}{R_1 + R_2}\right) v_o$

$$\therefore \quad v_I = \left(\frac{R_1}{R_1 + R_2}\right) v_o$$

$$\Rightarrow \quad \frac{v_I}{v_o} = \frac{R_1}{R_1 + R_2}$$

i.e., $A_{vcL} = \dfrac{R_1 + R_2}{R_1} = 1 + \dfrac{R_2}{R_1}$

Non-inverting gain

Non-inverting Feedback Amplifier Circuits

The potential on the inverting input is identical to that of the non-inverting input .

Reasons:

i. It uses negative feedback.

ii. The op-amp used is assumed to be ideal in the sense that $A_{\mathrm{voL}} \to \infty$.

iii. Op-amp is in linear region, $-V_{\mathrm{cc}} < v_{\mathrm{o}} < V_{\mathrm{cc}}$.

Non-inverting Feedback Amplifier Circuits

The voltage gain between the non-inverting input and the output is the non-inverting gain.

The voltage gain between the inverting input and output is also, the non-inverting gain.

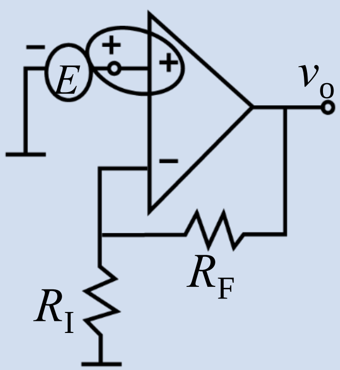
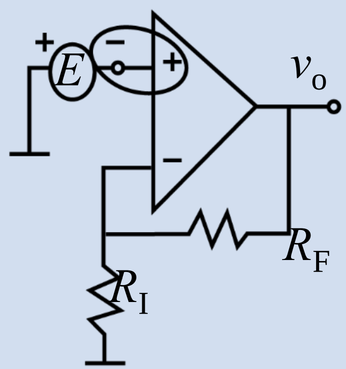
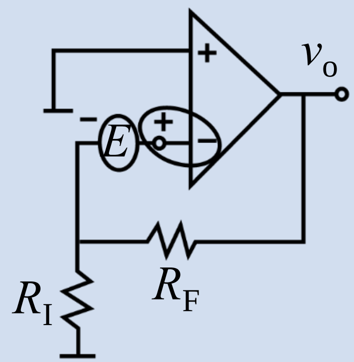
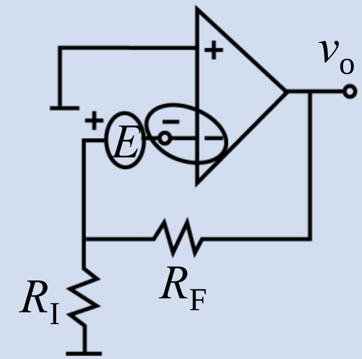
This leads to:

Any voltage appearing directly on either input of the op-amp will be multiplied by the following non-inverting gain.

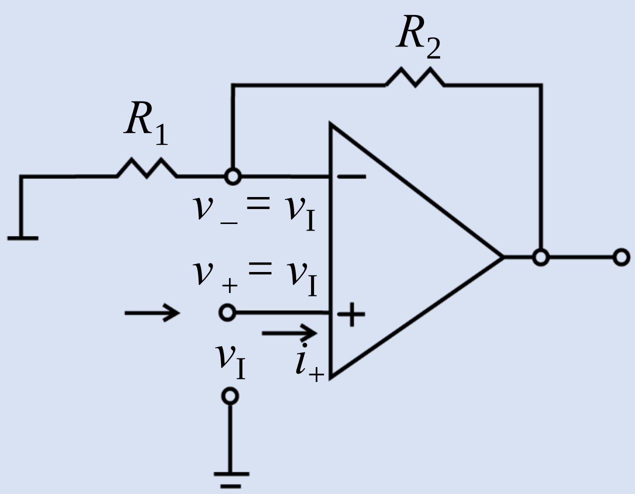
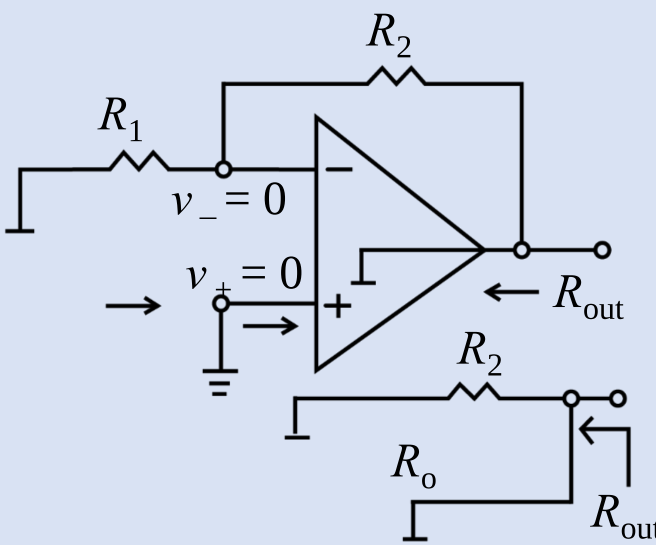
$$A_{vcL} = \frac{R_1 + R_2}{R_1} = 1 + \frac{R_2}{R_1}$$

Non-inverting Feedback Amplifier Circuits

Examples:

Output positive, non-inverting	Output negative, non-inverting	Output negative, inverting	Output positive, inverting
			
$v_o = (+)E\dfrac{R_F + R_I}{R_I}$	$v_o = (-)E\dfrac{R_F + R_I}{R_I}$	$v_o = (-)E\dfrac{R_F + R_I}{R_I}$	$v_o = (+)E\dfrac{R_F + R_I}{R_I}$

Non-inverting Feedback Amplifier Circuits

The input resistance of the non-inverting feedback amplifier is $$R_{in} = \frac{v_I}{i_+} = \frac{v_I}{0} = \infty$$	The output resistance is $$R_{out} = 0\ \Omega$$
	

Non-inverting Feedback Amplifier Circuits

With Voltage-Divider Input

This circuit is given in Figure 16, where a voltage divider consisting of R_2 and R_3 is used to reduce the signal amplitude to the input of a non-inverting feedback amplifier.

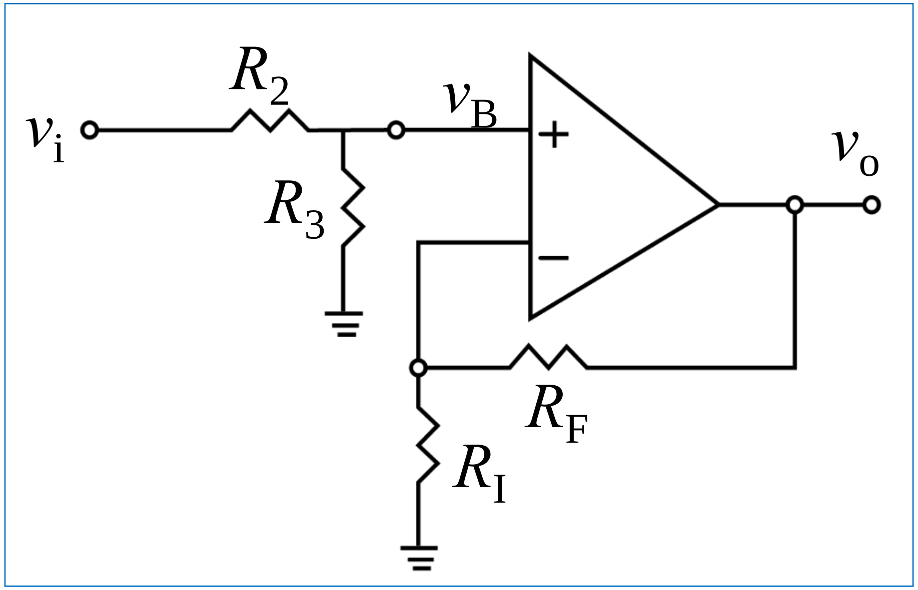
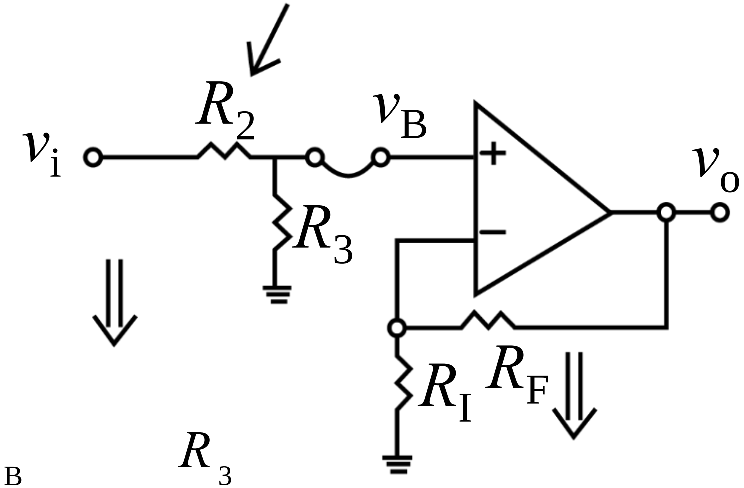


Figure 16. Non-inverting amplifier with voltage-divider input.

Non-inverting Feedback Amplifier Circuits

With Voltage-Divider Input

This circuit is used to reduce v_{i} to v_{B}



$$\frac{v_{\mathrm{B}}}{v_{\mathrm{i}}} = \frac{R_3}{R_2 + R_3}$$

Voltage divider gain

$$\frac{v_{\mathrm{o}}}{v_{\mathrm{i}}} = \frac{R_{\mathrm{F}} + R_{\mathrm{I}}}{R_{\mathrm{I}}}$$

Non-inverting closed- loop voltage gain

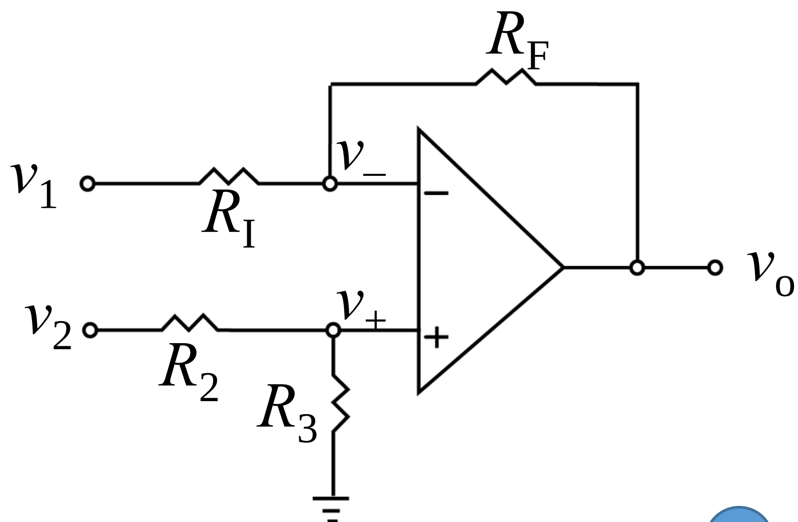
The closed-loop gain of the circuit is

$$A_{vcL} = \frac{v_o}{v_i}$$

$$= \frac{v_{\mathrm{B}}}{v_{\mathrm{i}}} \times \frac{v_{\mathrm{o}}}{v_{\mathrm{B}}}$$

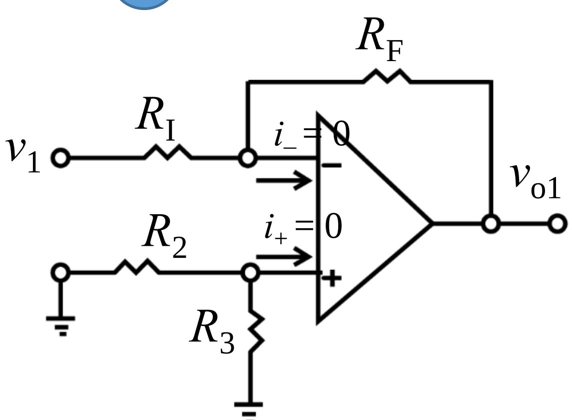
$$= \left(\frac{R_3}{R_3 + R_2} \right) \left(\frac{R_{\mathrm{F}} + R_{\mathrm{I}}}{R_{\mathrm{I}}} \right)$$

Scaling Subtractor

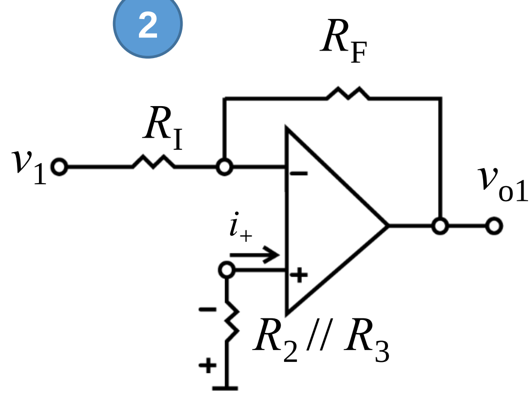


i.

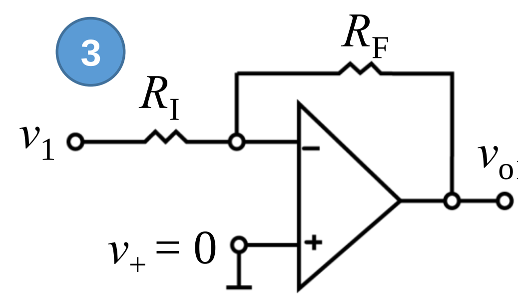
1



2

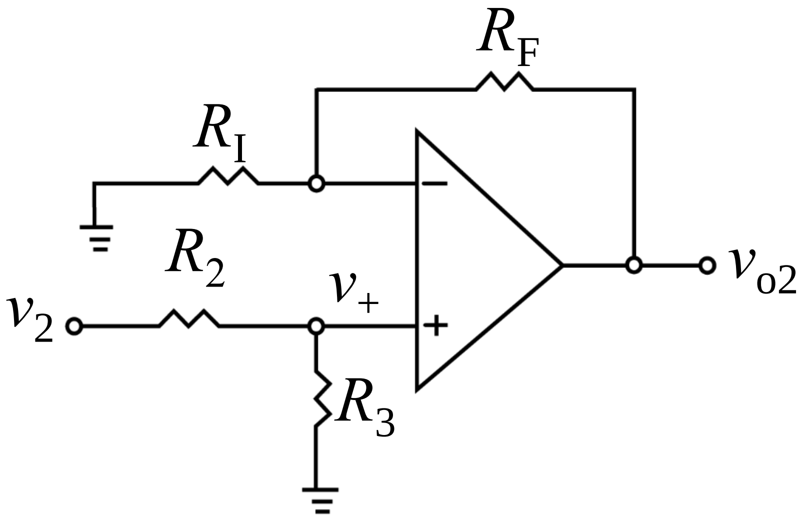


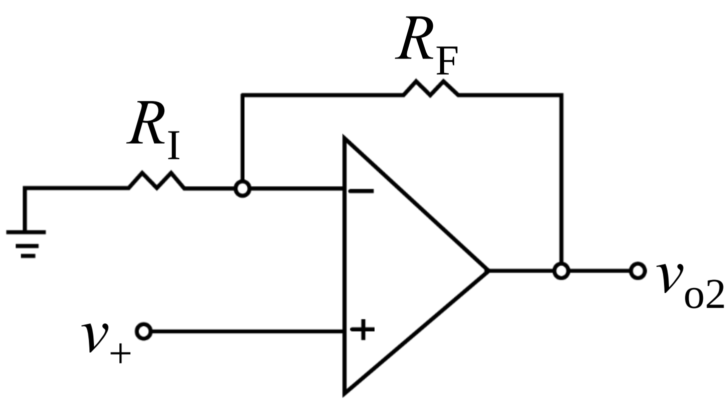
3



Scaling Subtractor

ii.





Non-inverting amplifier

$$v_{o2} = \left(\frac{R_3}{R_2 + R_3}\right)\left(\frac{R_F + R_I}{R_I}\right)v_2$$

$$v_+ = \left(\frac{R_3}{R_2 + R_3}\right)v_2$$

Scaling Subtractor

By using Linear Superposition Principle:

$$v_o = v_{o1} + v_{o2}$$

$$= \left(-\frac{R_F}{R_I}\right) v_1 + v_2 \left(\frac{R_3}{R_2 + R_3}\right)\left(\frac{R_F + R_I}{R_I}\right)$$

If $\frac{R_F}{R_I} = \frac{R_3}{R_2}$, then $v_o = -\frac{R_F}{R_I} v_1 + \frac{R_F}{R_I} v_2$

$$= \frac{R_F}{R_I}(v_2 - v_1)$$

Scaling Subtractor

Special Case

When $R_F = R_3$ and $R_I = R_2$ it is simply called,

Difference Amplifier with a gain of $\dfrac{R_F}{R_I}$.

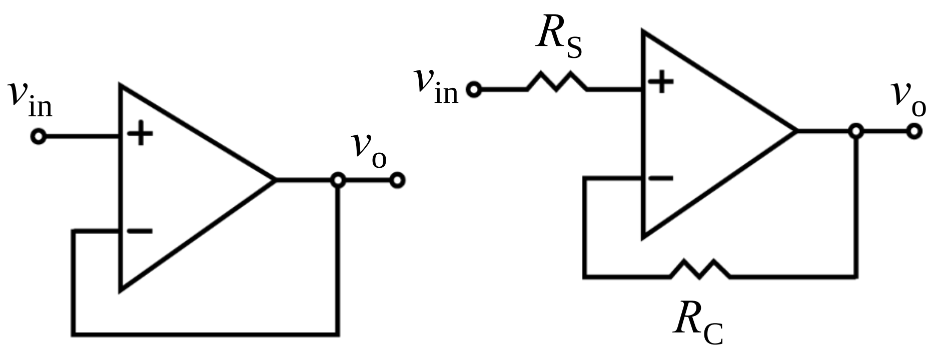
This scaling subtractor gives an output that is proportional to the difference between the two inputs.

For $R_F = R_I = R_3 = R_2$, then $v_o = v_2 - v_1$.

The circuit is called **subtractor.**

Voltage Follower (Buffer)

Figure 17 shows a voltage follower circuit.



(a) Basic circuit

(b) With current compensation resistors

Figure 17. Voltage follower.

$$v_+ = v_{in}$$
$$v_- = v_o$$

$\Rightarrow$ From $v_- = v_+$ yields $v_o = v_{in}$

$$R_1 = \infty, \; R_2 = 0$$

$$A_{vcL} = \frac{R_1 + R_2}{R_1} = 1$$

$$v_{in} - I_+ \times R_S = v_+$$

$$v_+ = v_-$$

$$v_- + I_- \times R_C = v_o$$

$$v_{in} - I_+ \times R_S = v_o - I_- \times R_C$$

$$\therefore \; v_{in} = v_o$$

Voltage Follower (Buffer)

This circuit is extremely useful as an impedance transformer. (Figure 18a).

The input impedance is nearly infinite, the output impedance is nearly zero, and the voltage gain is +1.

Note:

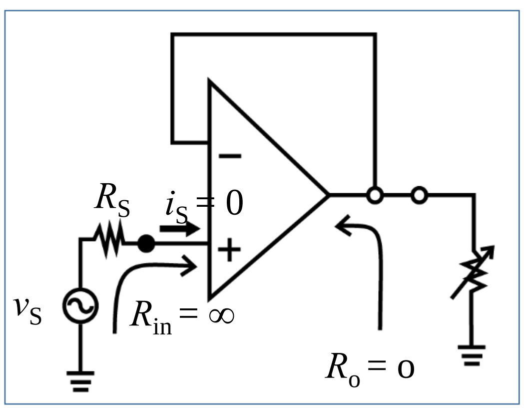


Figure 18a. Impedance transformer.

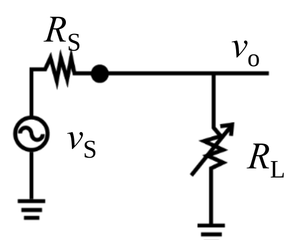


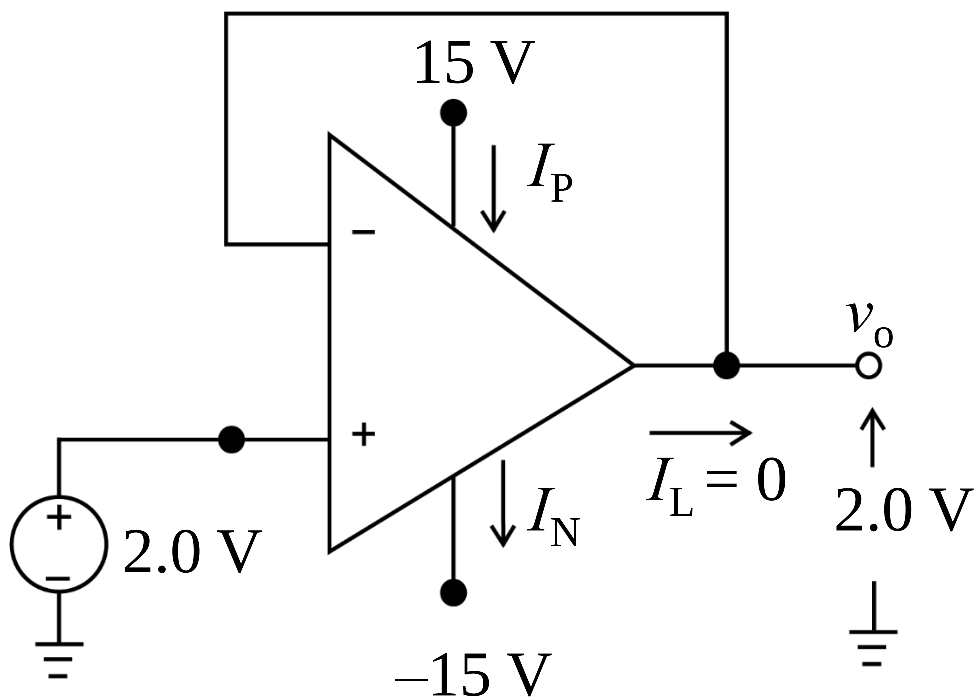
Figure 18b. Potential divider.

$$v_o = \frac{R_L}{R_L + R_s} v_s$$

By varying R_L the voltage across it, v_o, will not be affected and will always be maintained at a constant and is equal to v_s.

v_o does not depend on R_s.

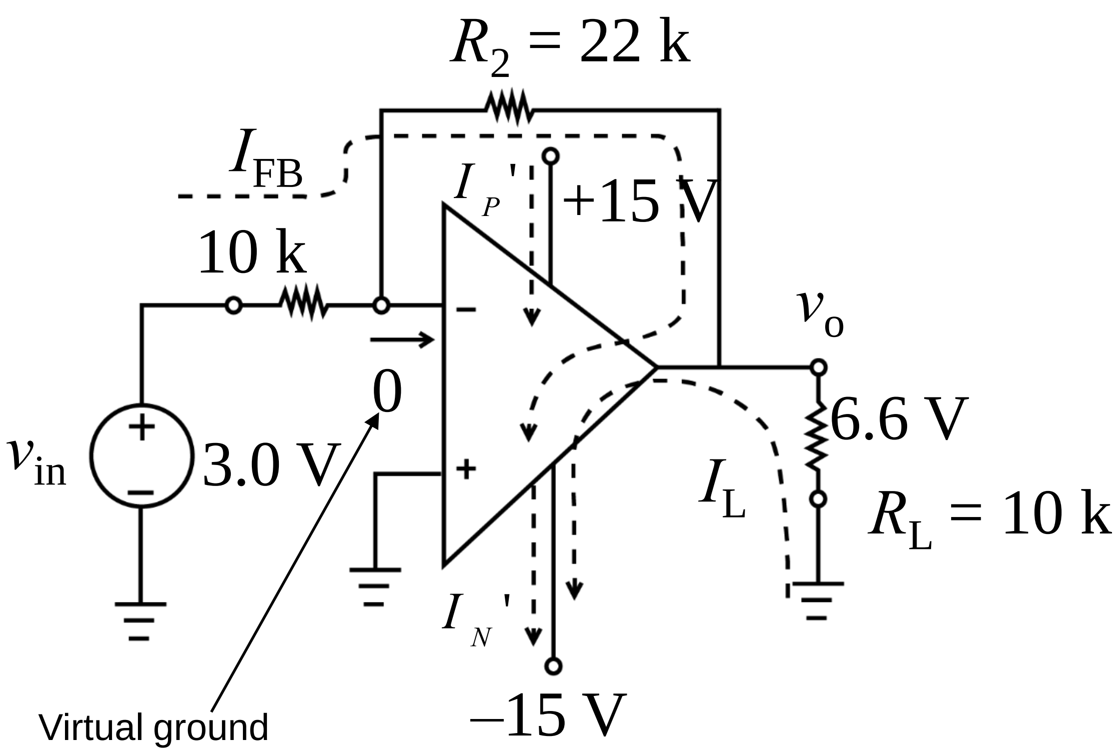
Current Flow in Op-amp



With $R_L = \infty$, $I_p = I_n$

Current Flow in Op-amp

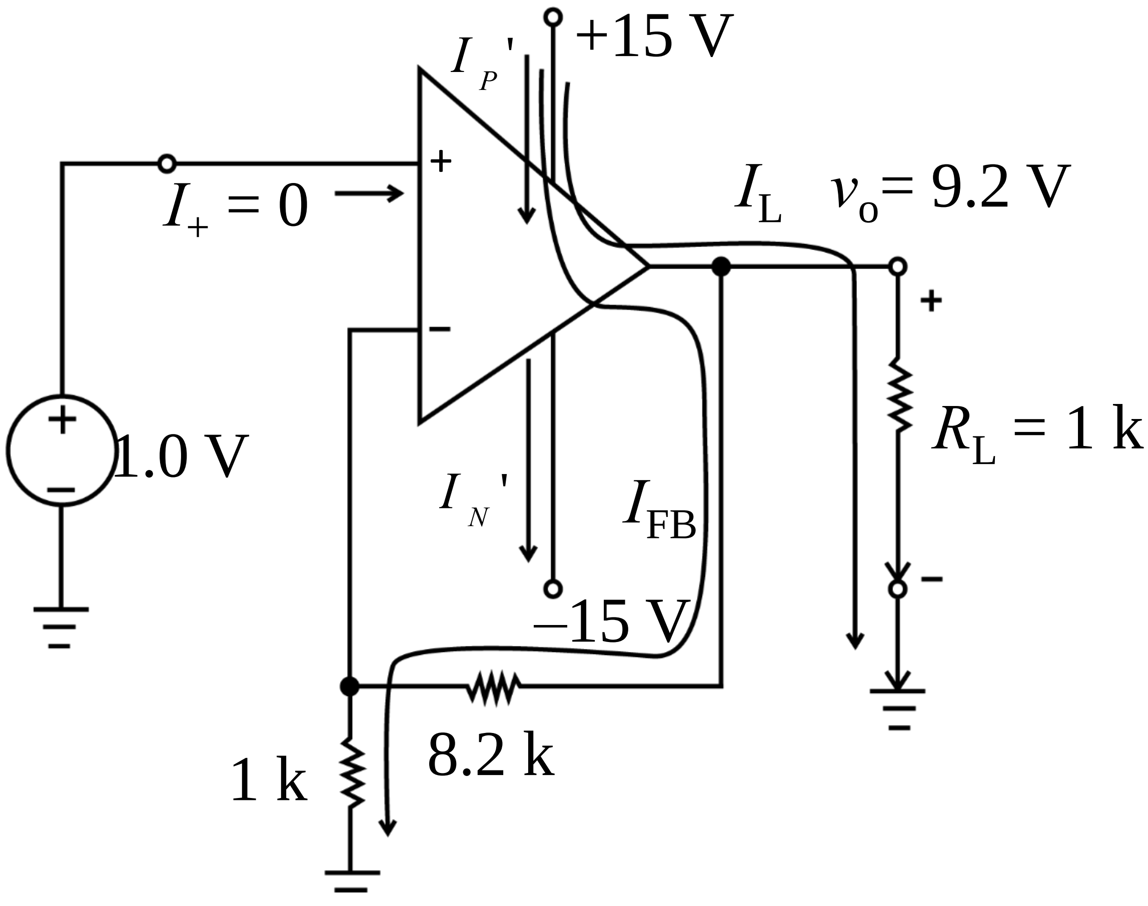
DC current is given in the op-amp's data sheet.



$$I_{FB} = \frac{3.0\ \text{V}}{10\ \text{k}} = 0.3\ \text{mA}$$

$$I_L = \frac{v_o}{R_L} = \frac{6.6\ \text{V}}{10\ \text{k}\Omega} = 0.66\ \text{mA}$$

Current Flow in Op-amp



$$I_L = \frac{9.2\ \text{V}}{1\ \text{k}} = 9.2\ \text{mA}$$

$$I_{FB} = \frac{9.2\ \text{V}}{9.2\ \text{k}} = 1.0\ \text{mA}$$

Inverting Integrator

An inverting integrator using an ideal op-amp is shown in Figure 19.

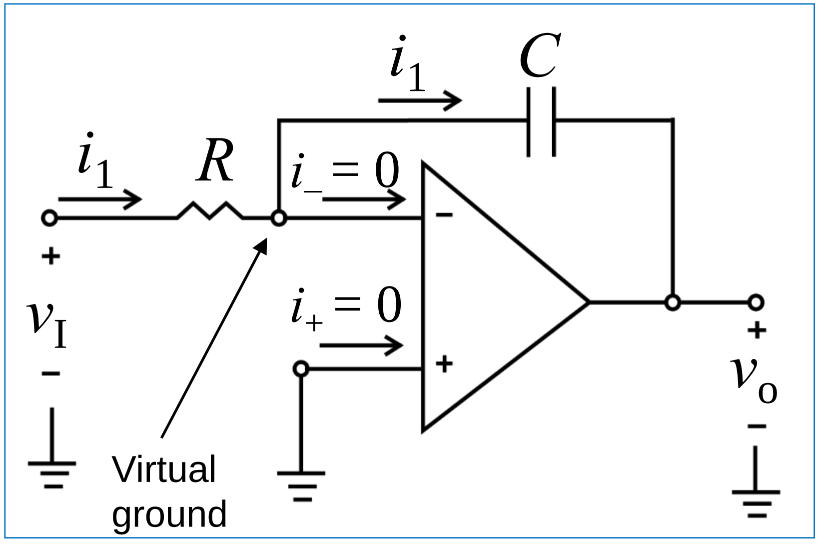


Figure 19. The miller or inverting integrator.

$$v_c(t) = v_o(t)$$

$$v_I(t) = i_1(t)R$$

$$i_1(t) = -C\frac{\mathrm{d}v_o}{\mathrm{d}t}$$

$$\therefore\ v_o(t) = -\frac{1}{C}\int_{-\infty}^{t} i_1(t)\,\mathrm{d}t$$

$$= -\frac{1}{RC}\int_{-\infty}^{t} v_I(t)\,\mathrm{d}t$$

The current i_1 is given by

$$\boxed{i_1 = \frac{v_I(t)}{R} \qquad (v_- = v_+ = v_o)}$$

Inverting Integrator

If at time $t = 0$ the voltage across the capacitor, measured in the direction indicated, is V_C, then

$$v_0(t) = V_C - \frac{1}{C}\int_0^t i_1(t)\,\mathrm{d}t$$

$$= V_C - \frac{1}{RC}\int_0^t v_\mathrm{I}(t)\,\mathrm{d}t$$

The time constant RC is called the integration time constant.

The integrator circuit is inverting because of the minus sign associated with its closed-loop gain; it is known as Miller integrator.

Inverting Differentiator

The circuit topology of inverting differentiator is shown in Figure 20.

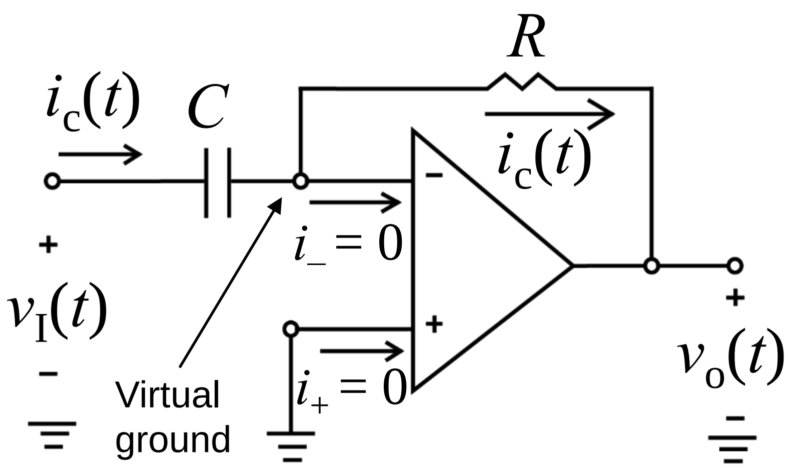


Figure 20. An inverting differentiator.

$$v_- = v_+ = 0$$

$$i_c(t) = C\frac{dv_I}{dt}$$

$$v_o(t) = -i_c(t)R$$

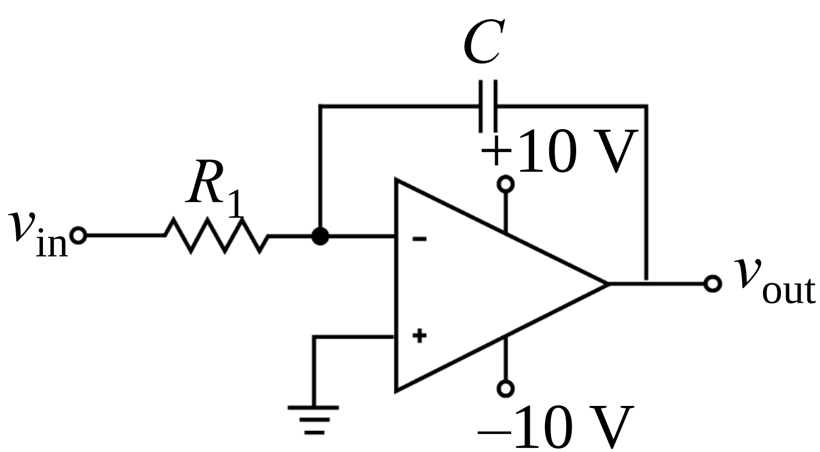
$$= -RC\frac{dv_i}{dt}$$

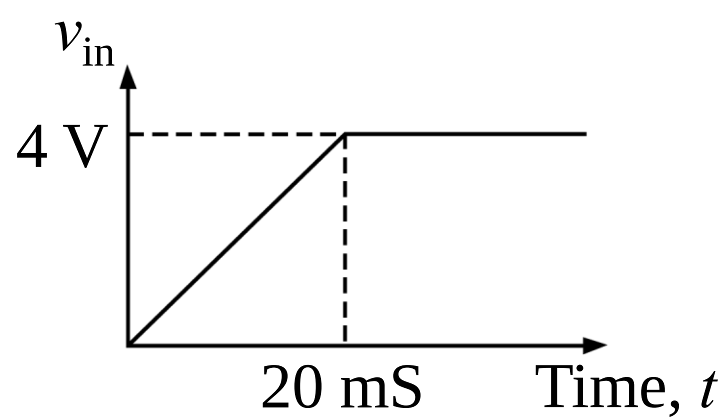
The output signal is proportional to the derivative of the input signal.

Thus it functions as a differentiator.

Inverting Integrator: Example

Plot the output, v_{out}, of the inverting integrator using an ideal op-amp if v_{in} is a ramp that levels off at the value $v_{in} = 4$ V after 20 mS. For the inverting integrator, R_1=5 kΩ and $C = 1$ μF. Assume the initial output is zero and the power supply voltages for the op-amp are ±10V.





Inverting Integrator: Example

For $0 < t < 20\ \text{mS}$, $v_{\text{out}} = -\dfrac{1}{R_1 C}\displaystyle\int_0^t v_{\text{in}}(t)\,dt$

Since v_{in} varies linearly during this period, hence,

$$v_{\text{out}} = -\frac{1}{R_1 C}\int_0^{20\ \text{mS}} \left[\frac{4}{20\ \text{mS}}\right](t)\,dt$$

$$= -\frac{1}{R_1 C}\left|\left[\frac{4}{20\ \text{mS}}\right]\frac{t^2}{2}\right|_0^{20\ \text{mS}}$$

$$= \frac{\dfrac{4}{20\times 10^{-3}}\left(20\times 10^{-3}\right)^2}{2\left(5\times 10^{3}\right)\left(1\times 10^{-6}\right)}$$

$$= -8\ \text{V}$$

Inverting Integrator: Example

For $t > 20$ mS, the input remains at 4 V, hence the integrator will continue to integrate this constant value.

$$v_{out} = -\frac{1}{R_1 C}\int_{20\ mS}^{t} v_{in}(t)\,dt - 8V$$

$$= -\frac{1}{R_1 C}\int_{20\ mS}^{t} 4\,dt - 8V$$

$$= -\frac{1}{R_1 C}(4)t\Big|_{20\ mS}^{t} - 8V$$

$$= -\frac{4}{\left(5\times 10^{3}\right)\left(1\times 10^{-6}\right)}\left(t - 20\times 10^{-3}\right) - 8V$$

$$= -0.8\ [\mathrm{V/mS}](t - 20\ \mathrm{mS}) - 8$$

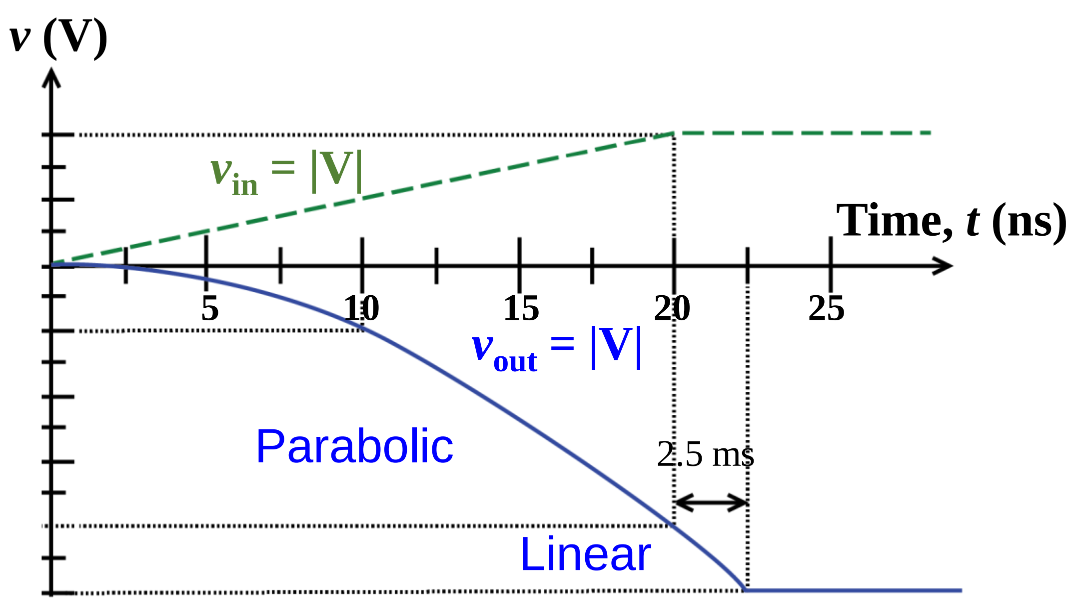
Inverting Integrator: Example

The integration cannot continue indefinitely, as the output will saturate with the negative supply, -10 V.

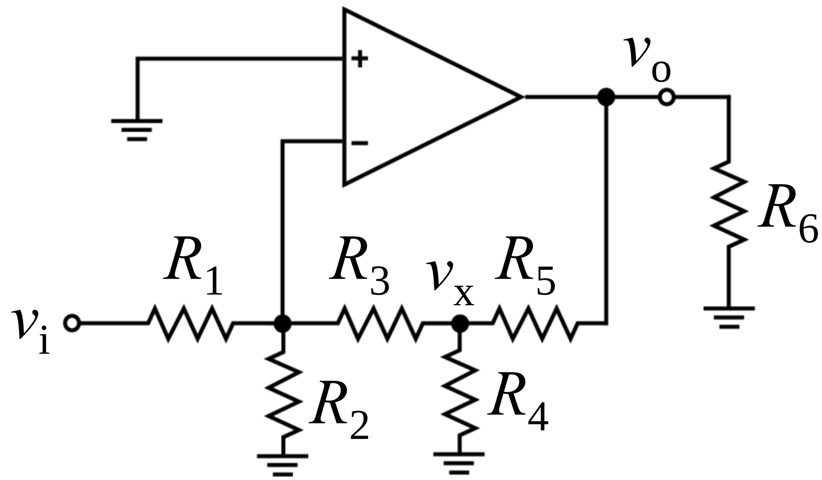
This will happen at

$$-0.8\ [\mathrm{V/mS}](t - 20\ \mathrm{mS}) - 8 = -10$$

$$t = 22.5\ \mathrm{mS}$$



Feedback with Multiple Resistors: Example



$$\frac{v_o}{v_I} = \frac{v_x}{v_I} \times \frac{v_o}{v_x}$$

$$= -\frac{R_3}{R_1} \times \frac{v_o}{v_x}$$

$$= -\frac{R_3}{R_1} \times \left[\frac{R_5 + (R_3 // R_4)}{R_3 // R_4}\right]$$

Check:

$$\left.\frac{v_0}{v_i}\right|_{R_4=\infty} = -\frac{(R_3 + R_5)}{R_1}$$

$$\left.\frac{v_0}{v_i}\right|_{R_5=0} = -\frac{R_3}{R_1}$$

$$\left.\frac{v_0}{v_i}\right|_{R_3=0} = -\frac{R_5}{R_1}$$

Input and Output Offset Voltages

Input Offset Voltage, V_{IO}

- V_{IO} is defined as negative of the DC voltage that must be applied between the inputs of an op-amp to force v_o to zero under open-loop conditions (Figure 21).
- The V_{IO} can be either positive or negative and typically has a value between $10\ \mathrm{mV}$ and $1\ \mu\mathrm{V}$, depending on the type of op-amp.
- It may also vary with temperature.

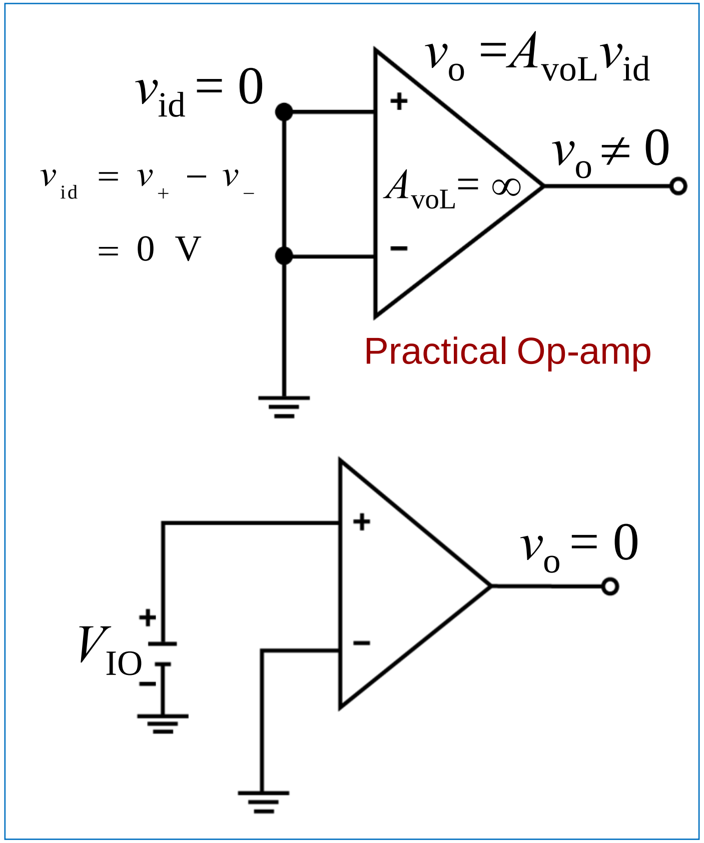


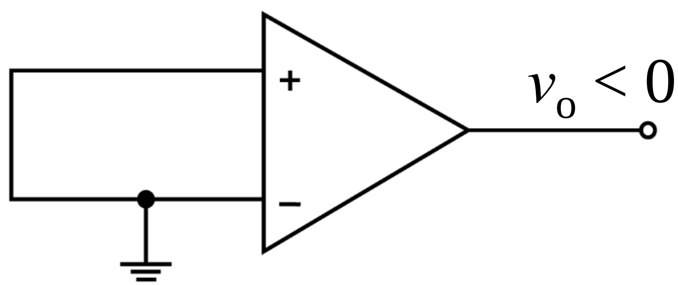
Figure 21. Definition of input offset voltage.

Input and Output Offset Voltages

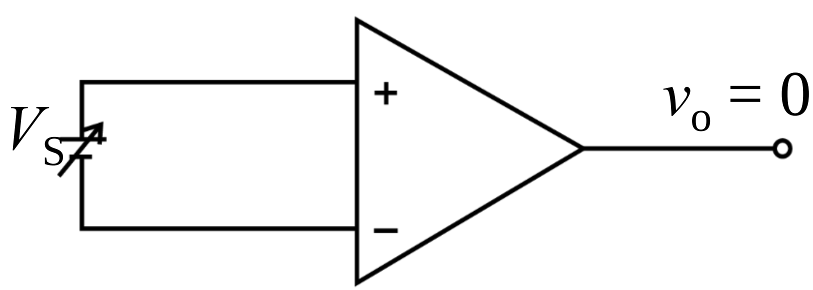
Input Offset Voltage, V_{IO}

An ideal op-amp has a V_{IO} of zero.

A)



To compensate $v_o = 0$, we use:



Adjust V_S until $v_o = 0$.

That value of V_S is the negative of the input offset voltage V_{IO}.

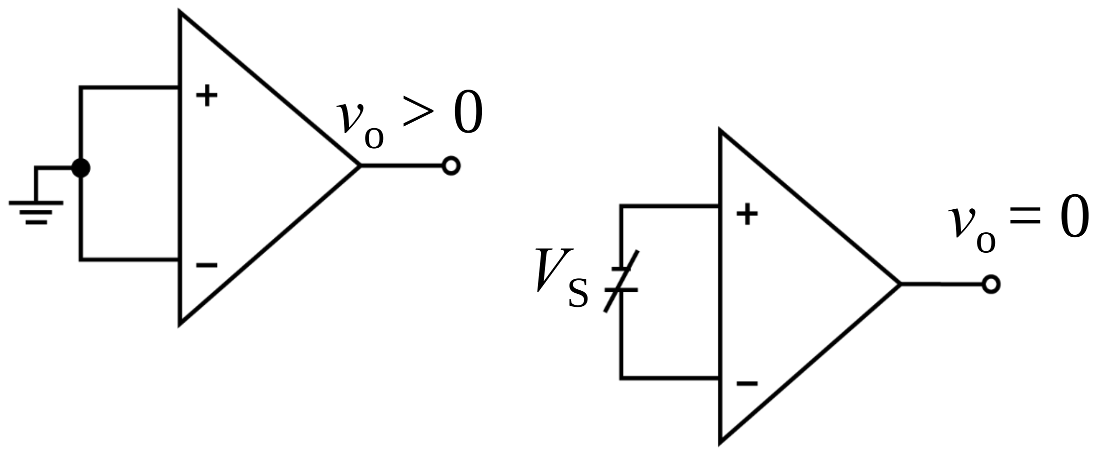
In this case $V_{IO} < 0$.

Input and Output Offset Voltages

Input Offset Voltage, V_{IO}

To force $v_o = 0$, we use:

B)



Adjust V_S until $v_o = 0$ and this V_S is the negative of the V_{IO} for the op-amp.

In this case $V_{IO} > 0$.

Input and Output Offset Voltages

Input Offset Voltage, V_{IO}

The effect of V_{IO} on an op-amp circuit can be modelled by adding a DC voltage source V_{IO} in series with the non-inverting input terminal, as shown in Figure 22.

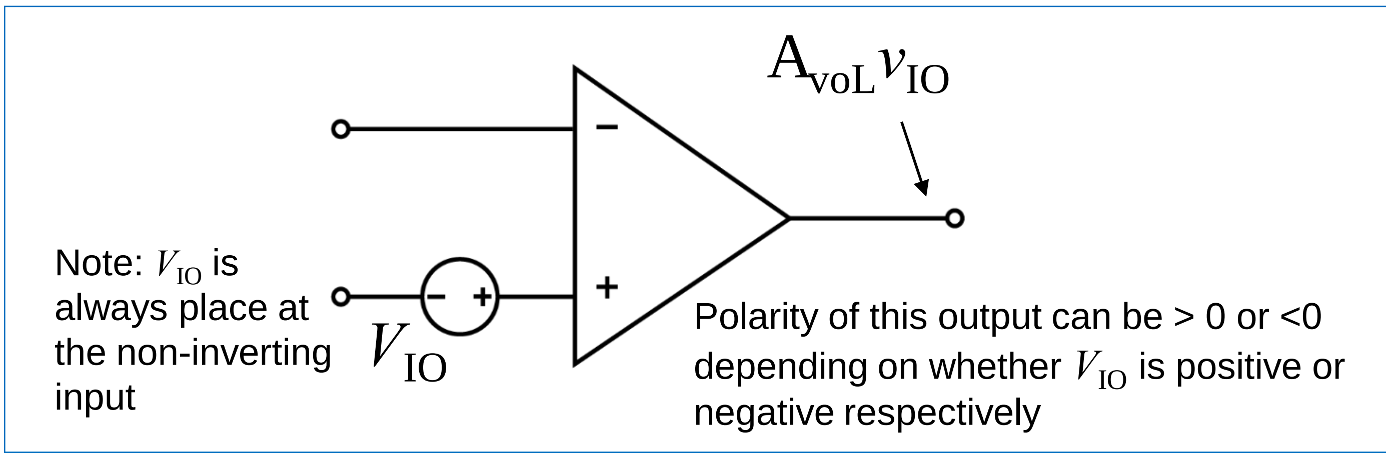


Figure 22. Offset-free op-amp with offset tagged at the non-inverting input.

Input and Output Offset Voltages

Output Offset Voltage

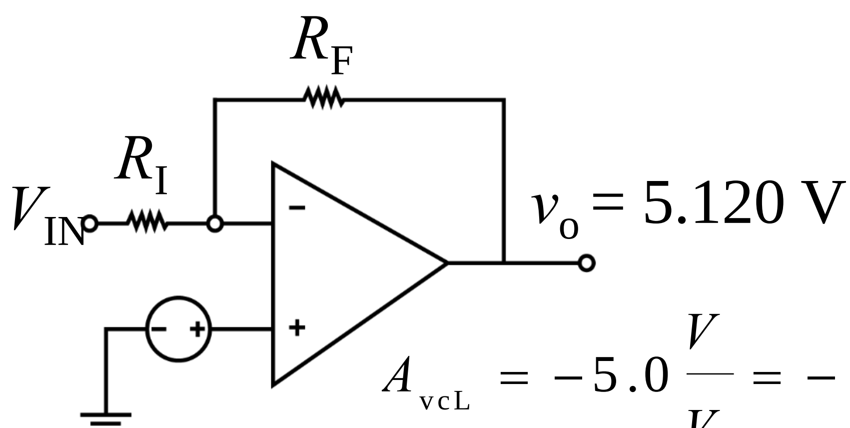
- The output offset voltage of an op-amp is due to the imbalance of its internal circuitry.
- The output offset voltage is equal to the input offset voltage V_{IO} multiplied by the A_{vOL}.
- The polarity of the output offset voltage can be either positive or negative.

Input and Output Offset Voltages

Input Offset Voltage Example

Example 1:

An inverting feedback amplifier has a closed-loop gain of $A_{vcL} = -5V/V$. The input signal V_{IN} is -1.0 VDC. The output voltage is 5.120 VDC. What's the V_{IO} for the op-amp ?



$$A_{vcL} = -5.0\frac{V}{V} = -\frac{R_F}{R_I}$$

Input and Output Offset Voltages

Input Offset Voltage Example

Solution:

i) The expected output voltage is $v_o = \left(-\frac{R_F}{R_I}\right)V_{IN}$

$$= -5(-1)$$

$$= 5.0 \text{ VDC}$$

ii) The actual $v_o = 5.120$ VDC

iii) The difference between (i) and (ii) is

$5.120 - 5.0 = 0.120$ VDC

Input and Output Offset Voltages

Input Offset Voltage Example

Solution (Cont.):

iv) The input offset voltage V_{IO} will contribute to an output given by

$$v_o = \left(1 + \frac{R_F}{R_I}\right)V_{IO}$$

$$= (1+5)V_{IO}$$

$$= 6\ V_{IO}$$

(v) The output obtained in (iv) must be 0.120 VDC.

Thus, $6V_{IO} = 120\ mV$

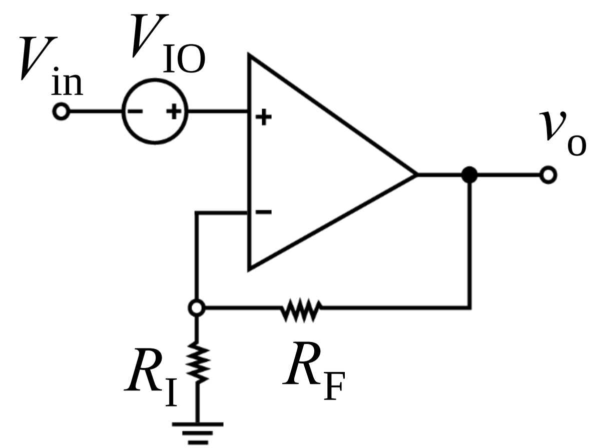
$$V_{IO} = 20\ mV$$

Input and Output Offset Voltages

Input Offset Voltage Example

Example 2.

An op-amp used in a non-inverting feedback amplifier with $A_{vcL} = 8\text{V/V}$ has an V_{IO} of $\pm 15\text{ mV}$ max. The output voltage is -5.85 V when the input is -0.75 VDC. Find the input offset voltage V_{IO}.



V_{IO} in series with signal input

Input and Output Offset Voltages

Input Offset Voltage Example

Solution:

i) The expected output voltage is

$$v_o = (-0.75)(8)$$

$$= -6.0 \text{ VDC}$$

ii) The actual output is –5.85 VDC.

iii) The difference between the two outputs is 0.15 VDC.

Input and Output Offset Voltages

Input Offset Voltage Example

Solution (Cont.):

iv) The output contributed by V_{IO} is

$$v_o = \left(1 + \frac{R_F}{R_I}\right) V_{IO}$$

$$= (1 + 7) V_{IO}$$

$$= 8\,V_{IO}$$

(v) The v_o must be equal to 0.15 V.

Thus, $8V_{IO} = 150\ \text{mV}$

$$V_{IO} = 18.75\ \text{mV}$$

$\Rightarrow$ **Specification limit**

Input Bias and Input Offset Current

- A real op-amp must draw a small amount of DC bias currents (I_+, I_-) into its v_+ and v_- terminals for proper operation of its internal circuit.
- These input bias currents are designated I_+ and I_- and they are modelled by placing DC current sources inside an otherwise ideal op-amp.
- This is shown in Figure 23a.

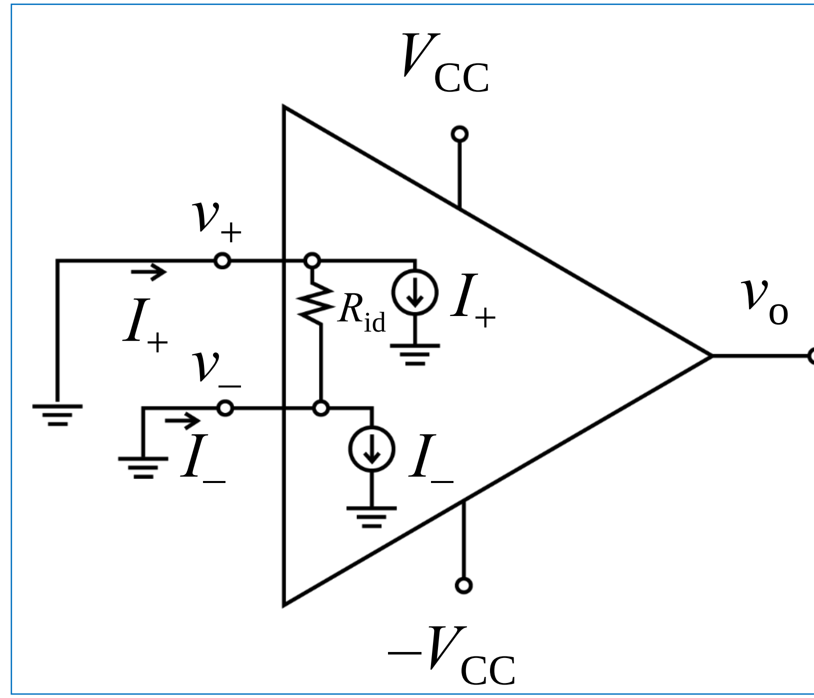


Figure 23a. Modeling of input bias currents I_+ and I_-.

Input Bias and Input Offset Current

As shown in Figure 23b, I_+ and I_- augment whatever signal current I_s flows through R_{id}.

The input bias current is formally defined as the average of I_+ and I_-:

$$I_{BIAS} = \frac{1}{2}(I_+ + I_-)$$

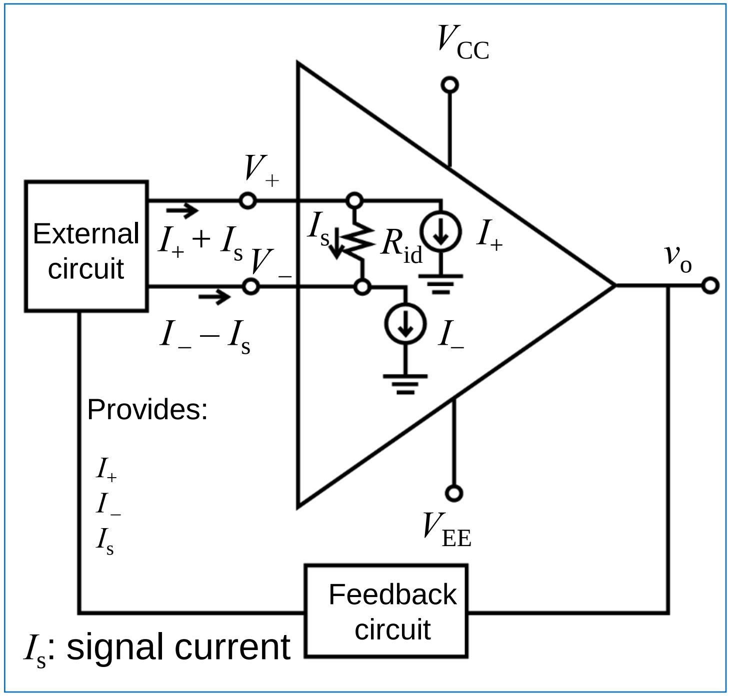


Figure 23b. I_+ and I_- augment the signal current is that flows through r_{in}.

Typical input bias currents range in value from 0.1 pA to 10 μA and can be positive or negative, depending on the type of op-amp.

Input Bias and Input Offset Current

In some op-amps, the DC input bias currents I_+ and I_- are not equal.

Their difference is called the input offset current, defined by the relation $I_{IO} = I_+ - I_-$

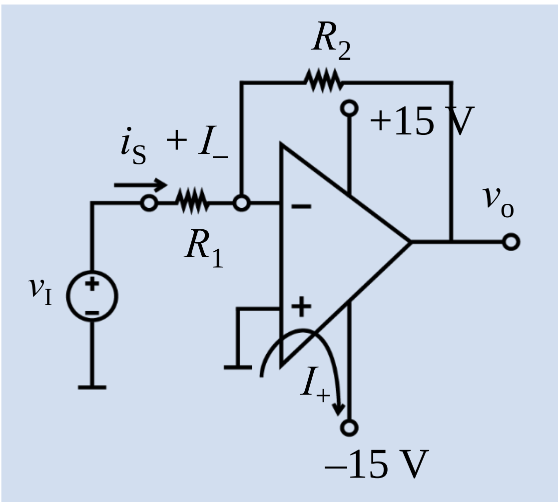
The imbalance is typically of 5 to 10% of the average input bias current.

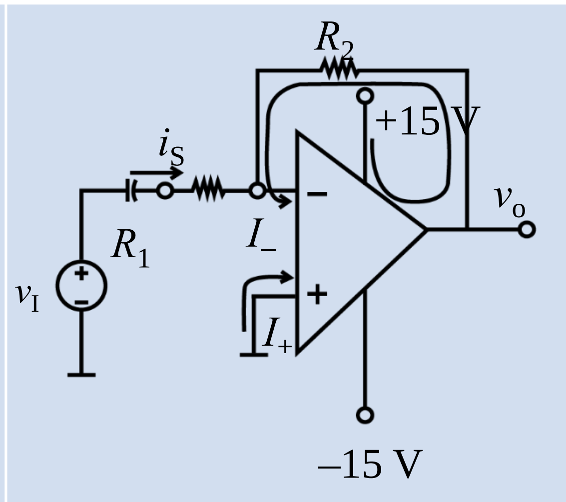
$I_{BIAS} = \frac{1}{2}(I_+ + I_-)$	$I_{IO} = I_+ - I_-$
Input bias current (0.1 pA to 10 μA)	Input offset current (5 to 10% of I_{BIAS})

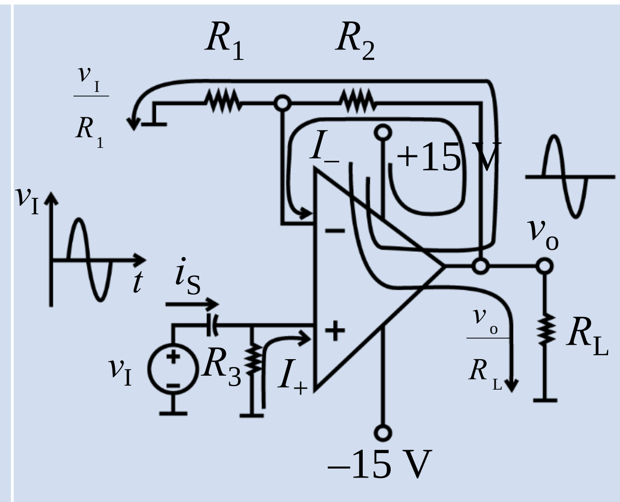
Input Bias and Input Offset Current

For real op, the I_{BIAS} or I_+ & I_- must be provided for proper op-amp operation.

(i)	(ii)	(iii)







Ensure v_{I} is able to provide i_{S}, signal current.

If without R_3?

$\Rightarrow$ No contribution from I_+ biasing at output of the op-amp

The Effects of Input Bias Current

Consider the linear amplifier in Figure 24.

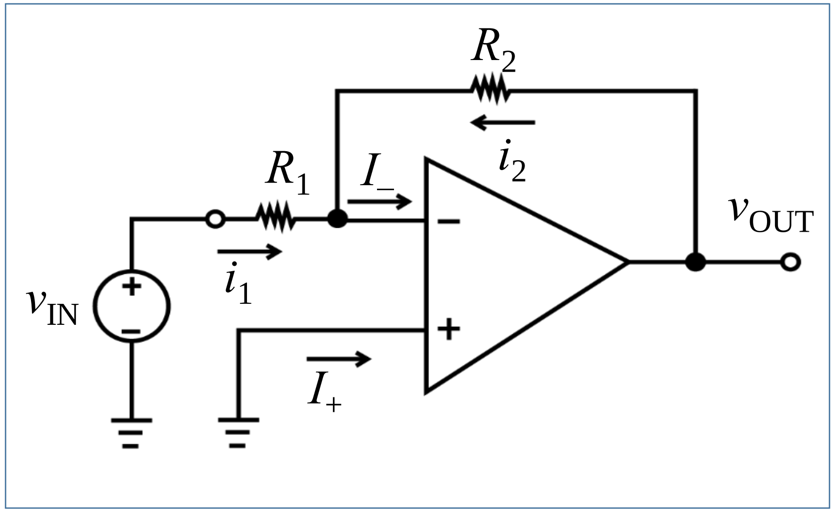


Figure 24. Inverting amplifier with input bias currents.

Assume that the op-amp is ideal except $I_+ \neq 0$ and $I_- \neq 0$.

With $v_{IN} = 0$, $I_+ = 0$, and $v_- = 0 \Rightarrow i_1 = 0$

By KLC, $i_2 = I_-$

The Effects of Input Bias Current

Thus, the V_{OUT} with $V_{\mathrm{IN}} = 0$ is $V_{\mathrm{OUT}} = I\_R_2$

With $I\_ = I_+ = 0$, the output due to V_{IN} is $-\left(\frac{R_2}{R_1}\right)V_{\mathrm{IN}}$

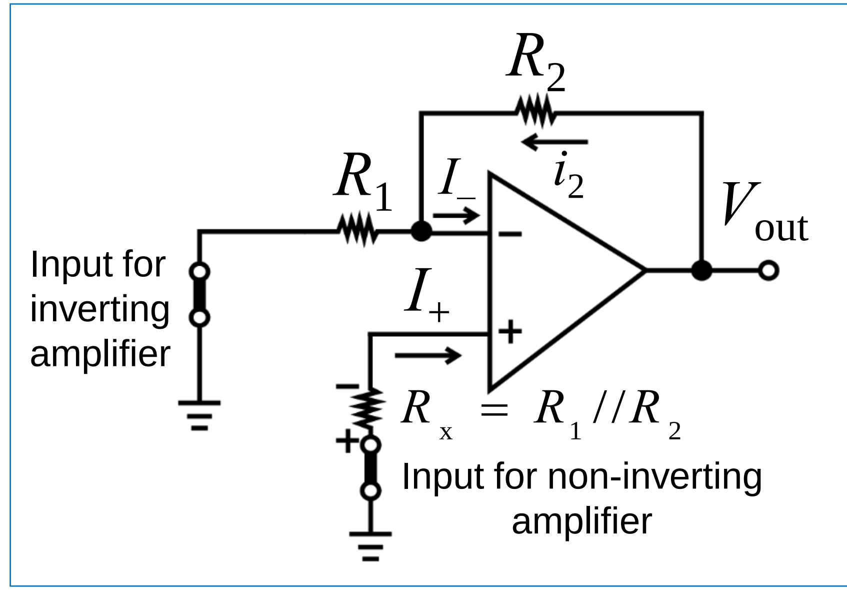
The total output voltage is $\boxed{V_{\mathrm{OUT}} = -\left(\frac{R_2}{R_1}\right)V_{\mathrm{IN}} + I_- R_2}$

What if there is a resistor R_x connected between V_+ and ground?

Then, $\boxed{V_{\mathrm{OUT}} = -\left(\frac{R_2}{R_1}\right)V_{\mathrm{IN}} + I_- R_2 - I_+ R_x\left(1 + \frac{R_2}{R_1}\right)}$

The Effects of Input Bias Current

In order to compensate the effect of the bias currents, a resistor R_x is added to the circuit in Figure 24, as shown in figure at the right with external V_{IN} removed.



Resistor, $R_x = R_1 // R_2$, cancels the effect of input bias current.

The input voltage is set to zero.

The Effects of Input Bias Current

Using Linear Superposition, the DC output voltage for circuit in the figure can be derived as follows:

i) With $I_+ = 0$, evaluate with I_- only: $V_{OUT1} = I_- R_2$

ii) Set $I_- = 0$, evaluate with I_+ only: $V_{OUT2} = -I_+ R_x \left[1 + \frac{R_2}{R_1}\right]$

iii) Then by Linear Superposition Principle,

$$V_{OUT1} + V_{OUT2} = I_- R_2 - I_+ R_x \left[1 + \frac{R_2}{R_1}\right]$$

If $R_x = R_1 // R_2$, then $V_{OUT} = R_2 (I_- - I_+)$

$= -R_2 I_{IO}$ (If $I_- = I_+$, then $I_{IO} = 0$)

$= 0$

Slew Rate Limitation

The output of an ideal op-amp is able to change instantaneously.

In real op-amp the rate of change of the output is **finite**, in V/μs, can never exceed a specified value called the **slew rate, S_R.**

For μA741, SR = 0.5 V/μs

$$S_R = \mathrm{Max}\left|\frac{\mathrm{d}v_o}{\mathrm{d}t}\right| \text{ of an op-amp}$$

Slew Rate Limitation

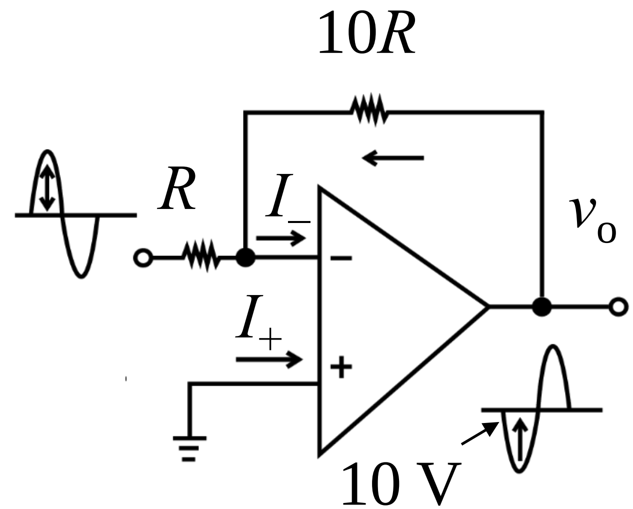
When op-amp is driven to its slew rate limit, the **output exhibits non-linear behavior**.

Under such conditions, the output of an otherwise linear circuit will not be a faithful reproduction of the input signal and will exhibit **non-linear distortion.** Here, $V_+ \neq V_-$.

Slew Rate Limitation

Example

An op-amp with $S_R = 1\ \text{V}/\mu\text{s} = 10^6\ \text{V/s}$ is used to build an inverting amplifier with a gain of $-10\ \text{V/V}$. With a $1.0V_p$ sinusoid the output has a peak of $10\ \text{V}$.



a) At what frequency will the output be affected by S_R?

b) If the sinusoidal input is increased to $1.5\ \text{V}$ at this frequency, sketch the resulting waveform.

Slew Rate Limitation

Solution: $v_{in} = a_m \cos\omega t$

a) The slope of $v_o = a_m \times A_{VCL} \cos\omega t$ is $\dfrac{dv_o}{dt} = \omega a_m \times A_{VCL} \sin\omega t$ and

$$\max\left\{\frac{dv_o}{dt}\right\} = \omega a_m A_{VCL}$$

$$= 2\pi f a_m A_{VCL}$$

The $\max\left|\dfrac{dv_o}{dt}\right|$ should be less than S_R to avoid non-linear distortion, i.e., $\omega a_m A_{VCL} \le S_R$.

For a $10V_p$ sinusoid, the frequency at which S_R limitation begins is

$$S_R = 2\pi f_m a_m A_{VCL}$$

$$f_m = \frac{S_R}{2\pi a_m A_{VCL}}$$

$$= \frac{10^6 \text{ V/s}}{2\pi(10)}$$

$$\approx 16 \text{ kHz}$$

Slew Rate Limitation

Solution (Cont.):

b) If the input is changed to a $16\ \mathrm{kHz}$ sinusoid of $1.5\ \mathrm{V}$, the output will attempt to increase to $15\ \mathrm{V}$. Over a certain portion of its cycle, the slope of this intended output will exceed the S_R and the output will not be a faithful replica of the input.

The slope of $v_o = a_m A_{VCL} \cos \omega t$

(where $a_m A_{VCL} = 15\ \mathrm{V}$) is

$$\frac{dv_o}{dt} = \omega a_m A_{VCL} \sin \omega t \Rightarrow \omega a_m A_{VCL} \sin \omega t \leq S_R$$

Slew Rate Limitation

Solution (Cont.):

The slope will reach the S_R limit of the $1\text{V}/\mu\text{s}$ at the time, t_1, given by

$$t_1 = \left(\frac{1}{\omega}\right)\sin^{-1}\left(\frac{S_R}{\omega a_m A_{VCL}}\right)$$

$$= \left[\frac{1}{2\pi(16\ \text{kHz})}\right]\sin^{-1}\left[\frac{10^6}{2\pi(16\ \text{kHz})(15\ \text{V})}\right]$$

$$\approx 7.3\ \mu\text{s}$$

After time t_1, the actual output will fall behind the intended output and will continue at the max S_R until it 'catches up' at time t_2.

Slew Rate Limitation

This plot of v_o is shown in Figure 25.

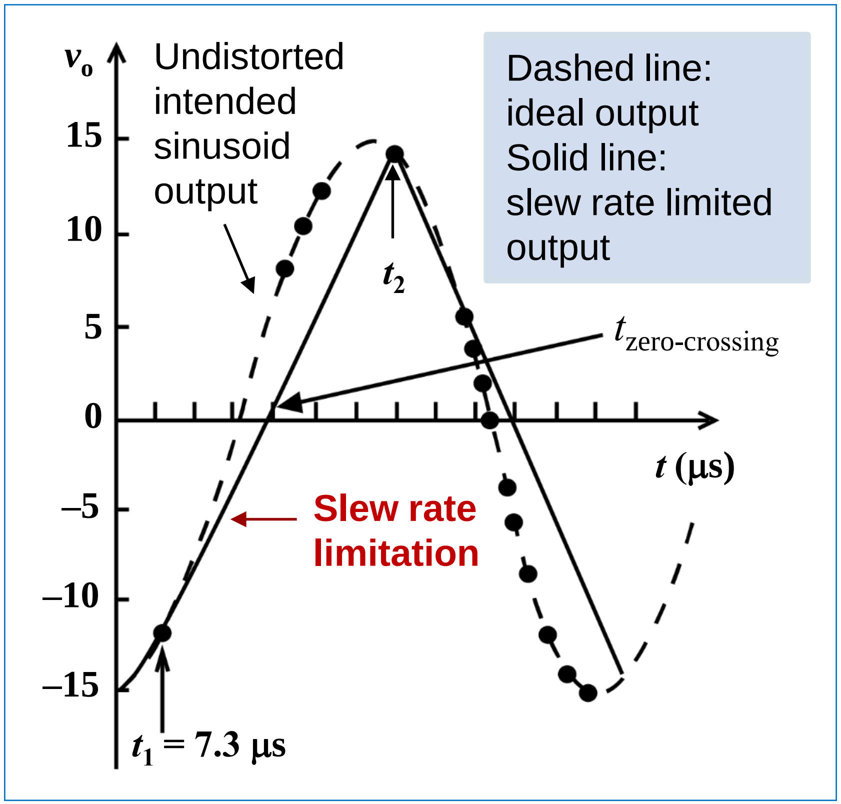


Figure 25. Effect of slew rate limitation on amplifier output.

Note that between t_1 and $t_{zero\text{-}crossing}$, $v_- > v_+$; and between $t_{zero\text{-}crossing}$ and t_2 , $v_- < v_+$.

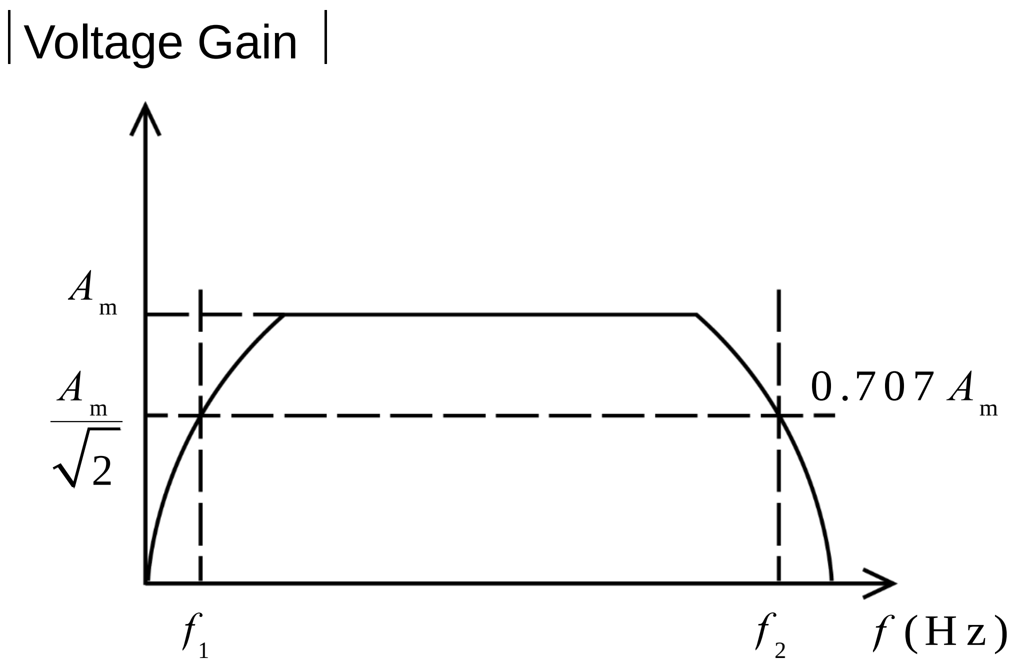
Hence, the relation $v_- = v_+$ is not valid anymore.

"The op-amp is in non-linear mode/open-loop" for $t \in [t_1, t_2]$.

|rate of change| at these points > S_R of the op- amp i.e., 1 V/μs.

$$v_- \neq v_+ \left(|v_{id}| = |v_- - v_+| > 0 \right)$$

Bandwidth (BW)



Bandwidth

$$BW = f_2 - f_1$$

f_1 = lower cutoff frequency

f_2 = upper cutoff frequency

BW: Finite Frequency Response

The infinite bandwidth of an ideal op-amp implies that the frequency response is flat for all signals to be amplified with equal gain regardless of frequency.

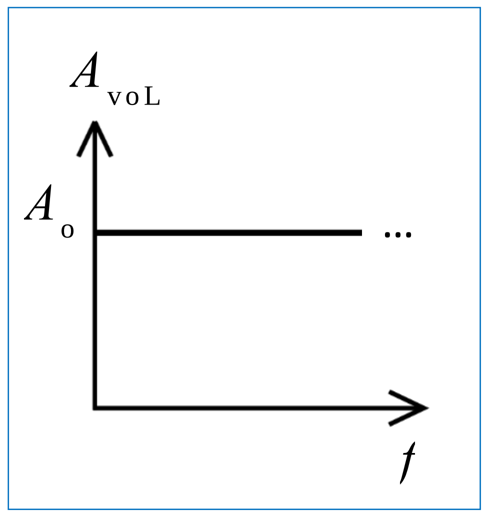


Figure 26. Frequency response of an ideal op-amp.

BW: Finite Frequency Response

The frequency response of a real op-amp is actually very limited and can be modeled by the typical Bode plot in Figure 27.

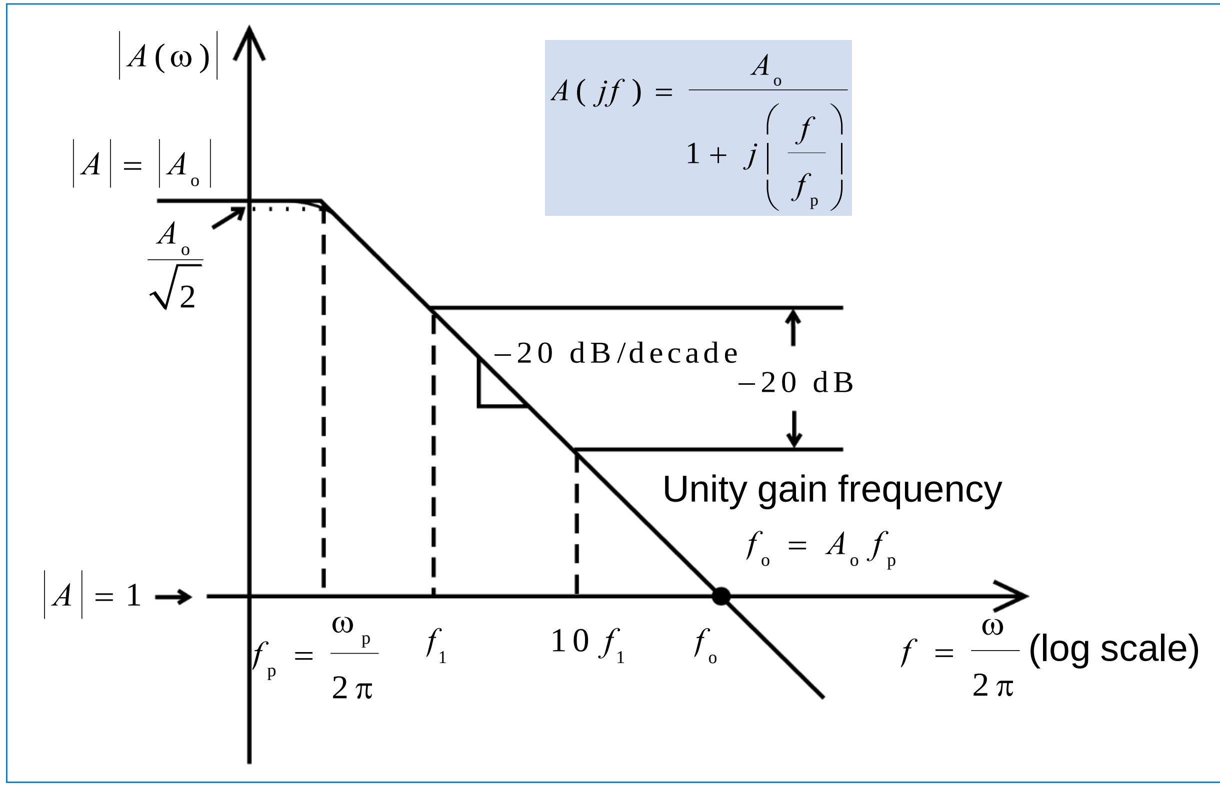


Figure 27. Frequency response of a typical op-amp

The dominant pole frequency f_p is often in the low frequency hertz range (normally below 1 kHz).

BW: Finite Frequency Response

Above f_p, the gain falls at a rate of -20 dB/decade.

Gain [in dB] = 20 log Gain

$$A(jf) = \frac{A_o}{1 + j\dfrac{f}{f_p}}$$

$$\therefore \left|A(jf)\right| = \frac{A_o}{\sqrt{1 + \left(\dfrac{f}{f_p}\right)^2}}$$

BW: Finite Frequency Response

At unity-gain frequency, f_o, $\left| A(jf_o) \right| = 1$

$$A_o = \left[1 + \left(\frac{f_o}{f_p} \right)^2 \right]^{\frac{1}{2}}$$

$$\left(\frac{f_o}{f_p} \right)^2 = A_o^2 - 1$$

$$f_o = f_p \left(A_o^2 - 1 \right)^{\frac{1}{2}}$$

$$\boxed{\therefore \; f_o = A_o f_p \quad (A_o >> 1)}$$

where

f_o = unity-gain frequency (freq.) of the op-amp $A(jf)$

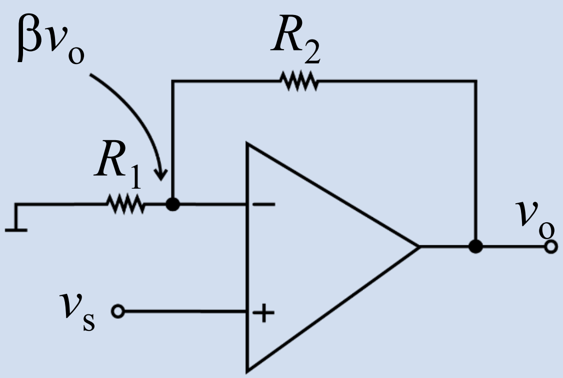
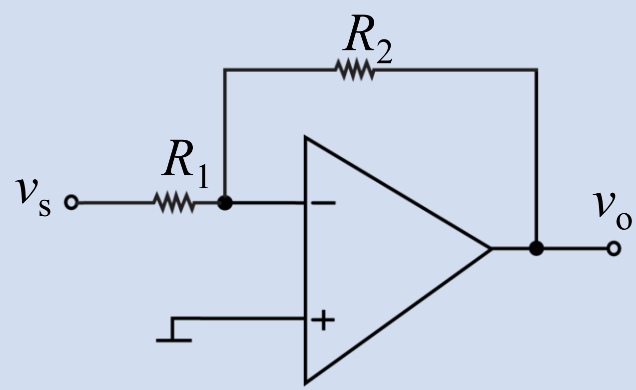
A_o = DC value of $A(jf)$

f_p = –3dB cutoff freq. of $A(jf)$

$A_o f_p$ = gain-bandwidth product

BW: Finite Frequency Response

When this op-amp is used in non-inverting or inverting feedback amplifier :

Non-inverting Gain	Inverting Gain
	
$\frac{v_o}{v_s} = \frac{R_1 + R_2}{R_1} = \frac{1}{\beta} \Rightarrow \beta = \frac{R_1}{R_1 + R_2}$	$A_{VCL} = \frac{v_o}{v_s} = -\frac{R_2}{R_1} = 1 - \frac{1}{\beta} \Rightarrow \beta = \frac{R_1}{R_1 + R_2}$

β is known as the **feedback factor.**

BW: Finite Frequency Response

The product of the reciprocal of the feedback factor, $\frac{1}{\beta}$, and the closed-loop bandwidth (BW_{CL}) for the circuits (both inverting & non-inverting) is

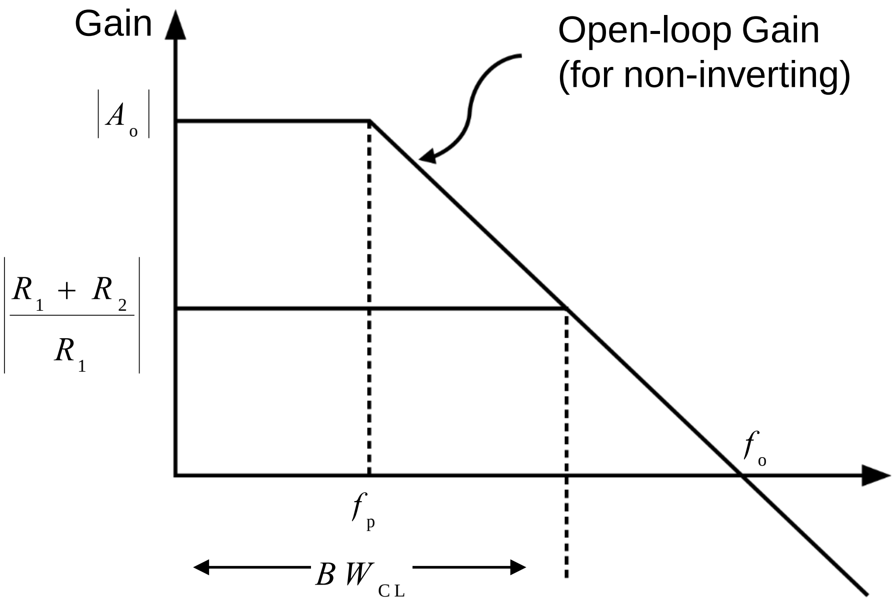
$$\boxed{\frac{1}{\beta} BW_{CL} = f_o = A_o f_p}$$

where, f_o = unity-gain frequency of the op-amp

A_o= DC value of $A(jf)$

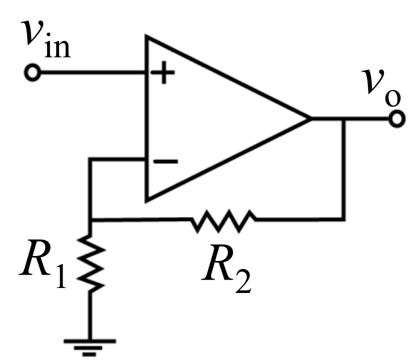
f_p = –3 dB cut off frequency of $A(jf)$

BW: Finite Frequency Response

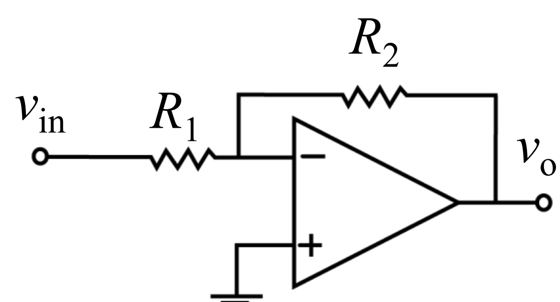


where $\beta = \dfrac{R_1}{R_1 + R_2}$

(β is feedback factor)



Non-inverting



Inverting

For both inverting and non-inverting:

$$\frac{1}{\beta} BW_{CL} = A_o f_p = f_o$$

$$BW_{CL} = \beta A_o f_p = \beta f_o$$

BW: Finite Frequency Response

When output voltage changes by ΔV, the minimum time that is required is

$$\Delta t = \frac{\Delta V}{SR} \text{ (in seconds)}$$

In terms of input quantities, the minimum time allowed for an input change of ΔV_{in} volts is

$$\Delta t = \frac{(A_{VCL})\Delta V_{in}}{SR} \text{ (in seconds)}$$

BW: Finite Frequency Response

An amp's bandwidth also affects, Δt for its output to change in response to a pulse input.

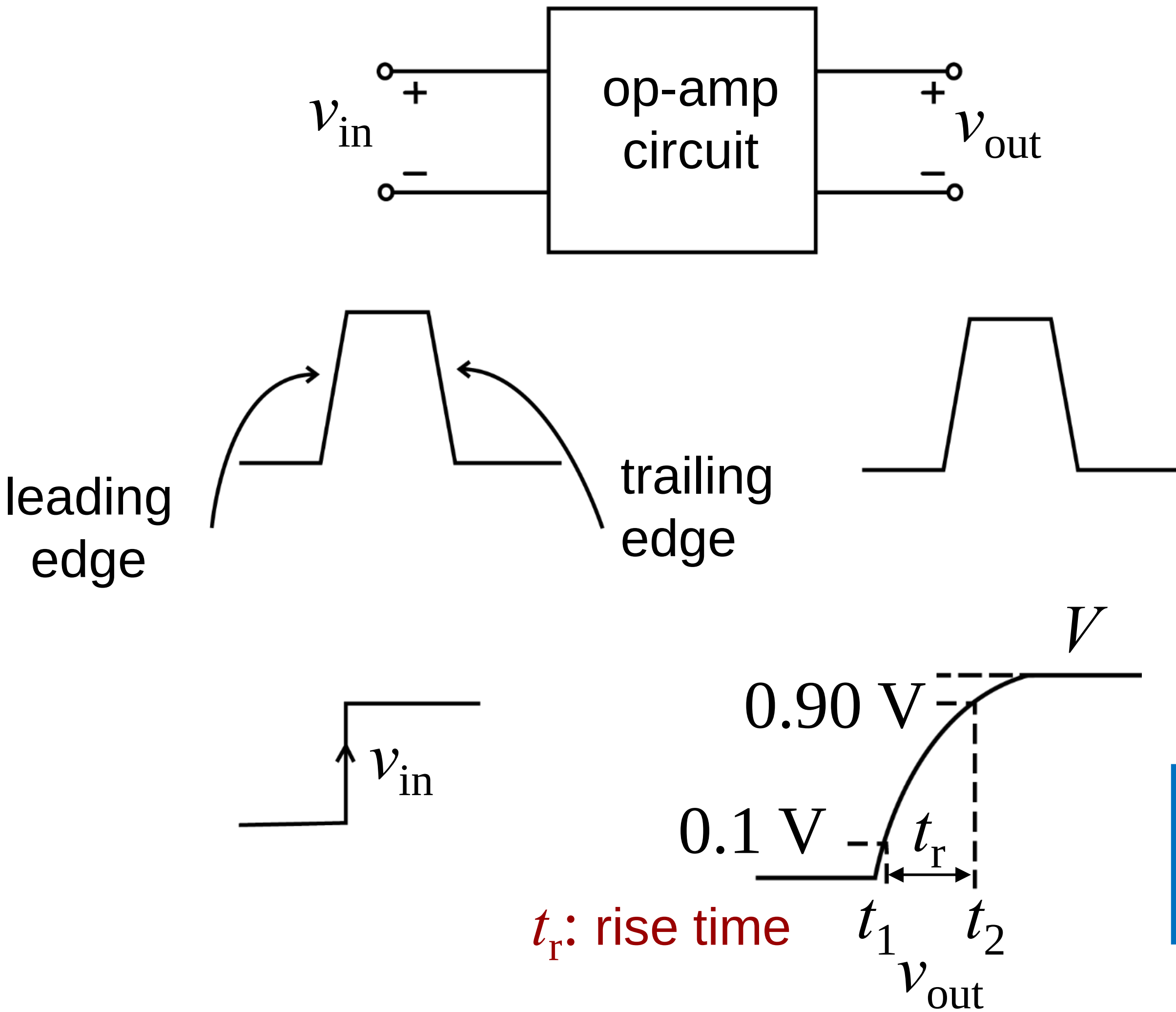
$$\boxed{t_r = \frac{0.35}{BW_{CL}}} \qquad \text{(a)}$$

For output to follow a pulse through its entire variation in t, the BW required should be larger than required by equation (a).

The amplifier must satisfy $\frac{\Delta V}{SR} \leq \Delta t$ and $\frac{0.35}{BW_{CL}} << \Delta t$

in order to track the input correctly .

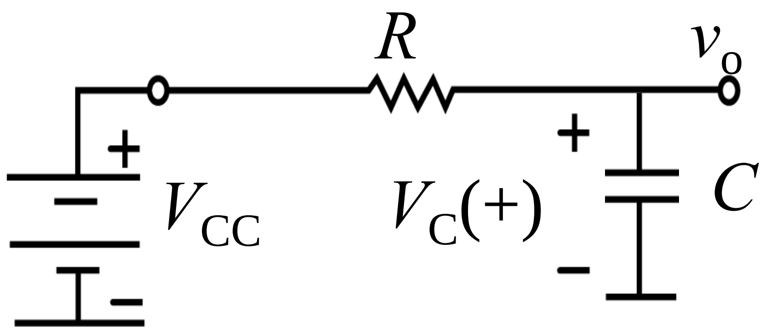
BW: Finite Frequency Response



$$t_r = \frac{0.35}{BW_{CL}}$$

Rise Time and Bandwidth

Consider the following simple RC circuit:



Assuming that the initial voltage across C is 0 V, then

$$v_c(t) = V_{cc}\left[1 - e^{-\frac{t}{RC}}\right]$$

The rise time for the circuit can be formed as follows:

$$0.1V_{cc} = V_{cc}\left[1 - e^{-\frac{t_1}{RC}}\right] \quad \text{—— (1)}$$

$$0.9V_{cc} = V_{cc}\left[1 - e^{-\frac{t_2}{RC}}\right] \quad \text{—— (2)}$$

Rise Time and Bandwidth

$t_r = t_2 - t_1$ and is given, $t_r = 2.2RC$ —— (3)

The –3 dB BW for the circuit is $BW = \dfrac{1}{2\pi RC}$ —— (4)

(3) × (4),

$$t_r \times BW = \frac{2.2}{2\pi}$$

$$= 0.35$$

$$\therefore \boxed{t_r = \frac{0.35}{BW}} \quad —— (5)$$

References for Images

Image	Slide No.	Reference
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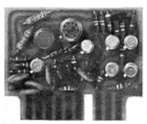
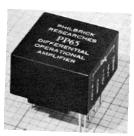
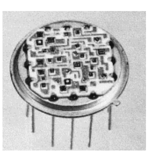
	9	By Analog Devices (Op Amp Applications Handbook) [CC BY-SA 3.0 (http://creativecommons.org/licenses/by-sa/3.0)], via Wikimedia Commons
	9	By Analog Devices (Op Amp Applications Handbook) [CC BY-SA 3.0 (http://creativecommons.org/licenses/by-sa/3.0)], via Wikimedia Commons
	9	By Analog Devices (Op Amp Applications Handbook) [CC BY-SA 3.0 (http://creativecommons.org/licenses/by-sa/3.0)], via Wikimedia Commons
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