Memory Controller IP Core for Avant Devices

User Guide

FPGA-IPUG-02208-1.2

December 2023

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Contents

Figures

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
APB	Advanced Peripheral Bus
AXI4	Advanced eXtensible Interface 4
BL	Burst Length
CA	Command and Address
CS	Chip Select
CBT	Command Bus Training
DBI	Data Bus Inversion
DDR	Double Data Rate
DDRPHY	Double Data Rate Physical Layer
DM	Data Mask
DQ	Data
DQS	Data Strobe
ECC	Error Correction Code
ECLK	Edge Clock
FPGA	Field Programmable Gate Array
I/F	Interface
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LPDDR	Low Power Double Data Rate
LVSTL	Low Voltage Swing Terminated Logic
MC	Memory Controller
MR	Mode Register
MRS	Mode Register Set
ODT	On-Die Termination
PRBS	Pseudorandom Binary Sequence
PVT	Process, Voltage, and Temperature
RTL	Register Transfer Level
SCLK	System Clock
SDR	Single Data Rate
SDRAM	Synchronous Dynamic Random Access Memory
SSN	Simultaneous Switching Noise
TCL	Tool Command Language
VREF	Voltage Reference

1. Introduction

The Lattice Semiconductor Memory Controller IP Core for Avant Devices provides a turnkey solution consisting of a controller, DDRPHY, and associated clocking and training logic to interface with DDR4 and LPDDR4 SDRAM. The IP Core is implemented in System Verilog HDL using the Lattice Radiant™ software integrated with the Synplify Pro® synthesis tool. The Memory Controller simplifies the interfacing of Avant™ devices with external DDR4 and LPDDR4 memory for user applications.

1.1. Quick Facts

The following table presents a summary of the Memory Controller IP Core for Avant Devices.

Table 1.1. Quick Facts

IP Requirements	Supported FPGA Family	DDR4 mode – Lattice Avant LPDDR4 mode – Lattice Avant
Resource Utilization	Targeted Device	LAV-AT-E70 LAV-AT-G70 LAV-AT-X70
	Supported User Interfaces	AXI4 for data access APB for configuration access
	Resources	Refer to Table A.1 and Table A.2
Design Tool Support	Lattice Implementation	Lattice Radiant software 2023.2
	Synthesis	Synopsys® Synplify Pro for Lattice
	Simulation	For a list of supported simulators, refer to the Lattice Radiant Software User Guide

1.2. Features

The Memory Controller IP Core for Avant Devices supports the following key features for DDR4 and LPDDR4 SDRAM.

1.2.1. DDR4

The Memory Controller for Avant Devices supports the following key features when configured in DDR4 mode:

- DDR4 SDRAM protocol, compliant to DDR4 JEDEC Standard
  - Avant™-AT-E DDR4 SDRAM speeds ranging from 350 MHz - 933 MHz (700 Mbps - 1866 Mbps)
  - Avant™-AT-G DDR4 SDRAM speeds ranging from 350 MHz - 1200 MHz (700 Mbps - 2400 Mbps)
  - Avant™-AT-X DDR4 SDRAM speeds ranging from 350 MHz - 1200 MHz (700 Mbps - 2400 Mbps)
- DDR4-Specific Memory Controller features
  - Component support for interface data widths of x16, x32, and x64
  - Up to 16 Gb density support
  - x8 DDR4 device support (8:1 DQ:DQS ratio)
  - Fixed burst length of BL8
  - 8:1 gearing mode (DDR4:FPGA logic interface clock ratio)
  - Read DBI support only
  - Configurable CAS latencies for Reads and Writes based on target interface speed
  - Configurable Address widths to support various memory densities
- AXI4 data interface support:
  - INCR read/write operations
  - Unaligned transfer using byte strobes
  - Narrow transfers
  - Narrow AXI widths of 32, 64, and 128
  - Aligned addressing to AxSIZE only

- APB configuration interface support:
  - Automatic DDR4 SDRAM initialization
  - Dynamic valid window optimization for Read/Write paths
  - DQ-DQS skew optimization for Write training
- Periodic training support featuring:
  - ZQ calibration (ZQCAL START and LATCH only)

Table 1.2. DDR4 Features Overview

Key Features	DDR4 Support Details
Device Format	Component, DIMM not yet supported
Data Widths	x16, x32, x64
Data User Interface	AXI4
Configuration Interface	APB
Maximum Data Rate	Refer to Table 1.6
HW Managed Periodic Events[1]	
Refresh	All bank auto refresh
ZQ Calibration	Yes for ZQ start and latch, No for ZQ reset
Low Power Features	Not yet supported
Other Features[1]	
Error Correction Code (ECC)	Not yet supported
Dual-rank	Not yet supported
Data Bus Inversion (DBI)	Yes for reads, No for writes
On-Die Termination (ODT)	Yes for DQ, No for CA
Training[1]	
Initialization	Yes
Command Training	Yes
Write Leveling	Yes
Read Training	Yes
Write Training	Yes
VREF Training	Not yet supported

Notes:

1. *Yes* implies that a configurable option exists to enable or disable the feature. *No* implies that the feature is currently not supported and will not be supported in the future.

1.2.2. LPDDR4

The Memory Controller for Avant Devices supports the following key features when configured in LPDDR4 mode:

- LPDDR4 SDRAM protocol, compliant to LPDDR4 JEDEC Standard
  - Avant-AT-E LPDDR4 SDRAM speeds ranging from 350 MHz - 933 MHz (700 Mbps - 1866 Mbps)
  - Avant-AT-G LPDDR4 SDRAM speeds ranging from 350 MHz - 1200 MHz (700 Mbps - 2400 Mbps)
  - Avant-AT-X LPDDR4 SDRAM speeds ranging from 350 MHz - 1200 MHz (700 Mbps - 2400 Mbps)
- LPDDR4-Specific Memory Controller features
  - Component support for interface data widths of x16, x32, and x64
  - Up to 16 Gb density support
  - x16 DDR4 device support (8:1 DQ:DQS ratio)
  - Burst length of BL16 and BL32, including On-The-Fly (OTF)
  - 8:1 gearing mode (LPDDR4:FPGA logic interface clock ratio)
  - Read DBI support only
  - Configurable CAS latencies for Reads and Writes based on target interface speed
  - Configurable Address widths to support various memory densities

- AXI4 data interface support:
  - INCR read/write operations
  - Unaligned transfer using byte strobes
  - Narrow transfers
  - Narrow AXI widths of 32, 64, and 128
  - Aligned addressing to AxSIZE only
- APB configuration interface support:
  - Automatic LPDDR4 SDRAM initialization
  - Dynamic valid window optimization for Read/Write paths
  - DQ-DQS skew optimization for Write training
- Periodic training support featuring:
  - Temperature tracking
  - Adaptive/Derate refresh rate for extended temperature support
  - ZQ calibration (ZQCAL START and LATCH only)
- Automatic detection of idle triggering Self-Refresh with Power-down entry
- Polling and Out-of-band interrupt support for error and extended temperature support

Table 1.3. LPDDR4 Features Overview

Key Features	LPDDR4 Support Details
Device Format	Component
Data Widths	x16, x32, x64
Data User Interface	AXI4
Configuration Interface	APB
Maximum Data Rate	Refer to Table 1.6
HW Managed Periodic Events[1]	
Refresh	All bank auto refresh
ZQ Calibration	Yes for ZQ start and latch, No for ZQ reset
Low Power Features	Self-refresh with power-down
Other Features[1]	
Error Correction Code (ECC)	Not yet supported
Dual-rank	No
Data Bus Inversion (DBI)	Yes for reads, No for writes
Temperature Tracking	Yes
Refresh Adaptation (derate) to Temperature Variation	Yes
On-Die Termination (ODT)	Yes for DQ, No for CA
Training[1]	
Initialization	Yes
Command Training	Yes
Write Leveling	Yes
Read Training	Yes
Write Training	Yes
Automatic VREF Training	Yes

Notes:

1. *Yes* implies that a configurable option exists to enable or disable the feature. *No* implies that the feature is currently not supported and will not be supported in the future.

1.3. Licensing and Ordering Information

The Memory Controller IP Core for Avant Devices supports Lattice's IP evaluation capability for supported FPGA families and target devices. A bitstream can be generated for evaluation purposes without the purchase of an IP license, allowing hardware operation for a limited period of time (maximum of four hours), before the device resets itself. The IP evaluation setting is disabled by default and can be enabled/disabled within the Lattice Radiant software by performing the following steps:

1. Launch the Lattice Radiant software and select Project > Active Strategy > Bitstream Settings. This will open the Strategies dialog box.
2. Enable bitstream generation for IP evaluation purposes by setting IP Evaluation to True (checked) or disable this feature by setting IP Evaluation to False (unchecked).

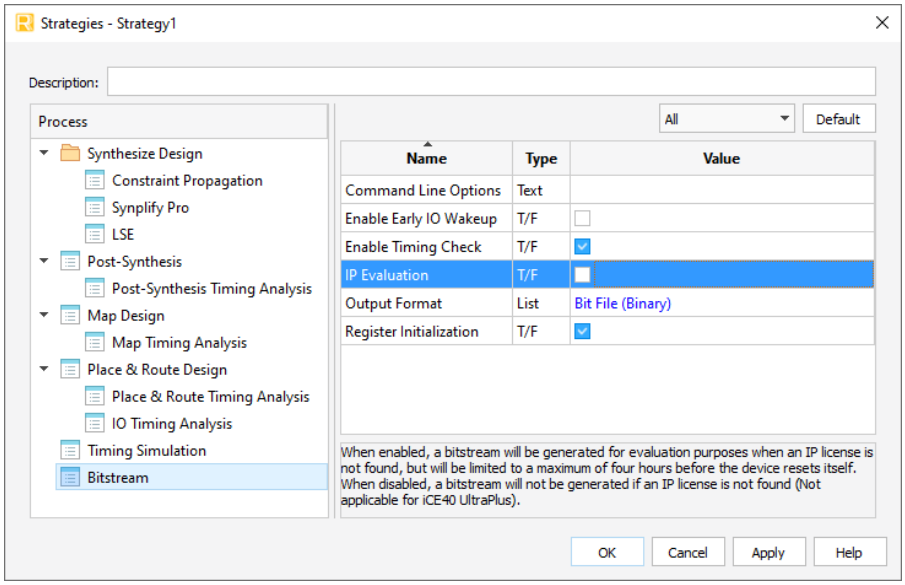

Figure 1.1. Enabling Bitstream for IP Evaluation

An IP specific license string is required to enable full use of the Memory Controller for Avant IP in a complete design. For more information about pricing and availability of the Memory Controller for Avant IP, contact your local Lattice Sales Office.

Table 1.4. Ordering Part Number

Device Family	Part Number	
	Single Machine Annual	Multi-site Perpetual
DDR4		
Avant-AT-E	DDR4-PHY-AVE-US	DDR4-PHY-AVE-UT
Avant-AT-G	DDR4-PHY-AVG-US	DDR4-PHY-AVG-UT
Avant-AT-X	DDR4-PHY-AVX-US	DDR4-PHY-AVX-UT
LPDDR4		
Avant-AT-E	LPDDR4-PHY-AVE-US	LPDDR4-PHY-AVE-UT
Avant-AT-G	LPDDR4-PHY-AVG-US	LPDDR4-PHY-AVG-UT
Avant-AT-X	LPDDR4-PHY-AVX-US	LPDDR4-PHY-AVX-UT

1.4. IP Validation Summary

The Memory Controller IP Core for Avant Devices supports Avant-AT-E, Avant-AT-G, and Avant-AT-X devices. The following table summarizes the compilation, simulation, and hardware validation for the Memory Controller IP.

Table 1.5. IP Validation Summary

Device/Mode	Compilation	Simulation	Hardware
DDR4			
Avant-AT-E	Yes	Yes	No
Avant-AT-G	Yes	Yes	No
Avant-AT-X	Yes	Yes	No
LPDDR4			
Avant-AT-E	Yes	Yes	Yes[1]
Avant-AT-G	Yes	Yes	Yes[1, 2]
Avant-AT-X	Yes	Yes	Yes[1, 2]

Notes:

1. For x16 and x32 data widths only. Data width of x64 is not HW validated.
2. Up to 1066MHz only. 1200MHz is not yet HW validated.

1.5. Minimum Device Requirements

The Memory Controller IP Core for Avant Devices supports Avant-AT-E, Avant-AT-G, and Avant-AT-X devices. The following table summarizes the minimum device requirements for the Memory Controller IP Core.

Table 1.6. Minimum Device Requirements

Device/Mode	Interface Speed	DDR Data Width	Supported Speed Grades
DDR4			
Avant-AT-E	350 MHz (700 Mbps) – 933 MHz (1866 Mbps)	x16, x32, x64	1, 2, 3
Avant-AT-G/X	350 MHz (700 Mbps) – 933 MHz (1866 Mbps)	x16, x32, x64	1, 2, 3
Avant-AT-G/X	1066 MHz (2133 Mbps)	x16, x32, x64	2, 3
Avant-AT-G/X	1200 MHz (2400 Mbps)	x16, x32, x64	3
LPDDR4			
Avant-AT-E	350 MHz (700 Mbps) – 933 MHz (1866 Mbps)	x16, x32, x64	1, 2, 3
Avant-AT-G/Avant-AT-X	350 MHz (700 Mbps) – 933 MHz (1866 Mbps)	x16, x32, x64	1, 2, 3
Avant-AT-G/Avant-AT-X	1066 MHz (2133 Mbps)	x16, x32, x64	2, 3
Avant-AT-G/Avant-AT-X	1200 MHz (2400 Mbps)	x16, x32, x64	3

1.6. Naming Conventions

This section provides information regarding terminology used within this document.

1.6.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.6.2. Signal Names

Signal Names that end with:

- *_n* are active low
- *_i* are input signals
- *_o* are output signals
- *_io* are bi-directional input/output signals

2. Functional Description

This section provides a detailed functional description of the Memory Controller IP Core for Avant Devices. Including information regarding clock and reset handling, available user data and configuration interfaces, the calibration sequence, and operation descriptions.

2.1. IP Architecture

The Memory Controller IP Core for Avant Devices consists of three main blocks: the Memory Controller, DDRPHY, and Training Engine. The following figure represents the Memory Controller submodules and its connectivity.

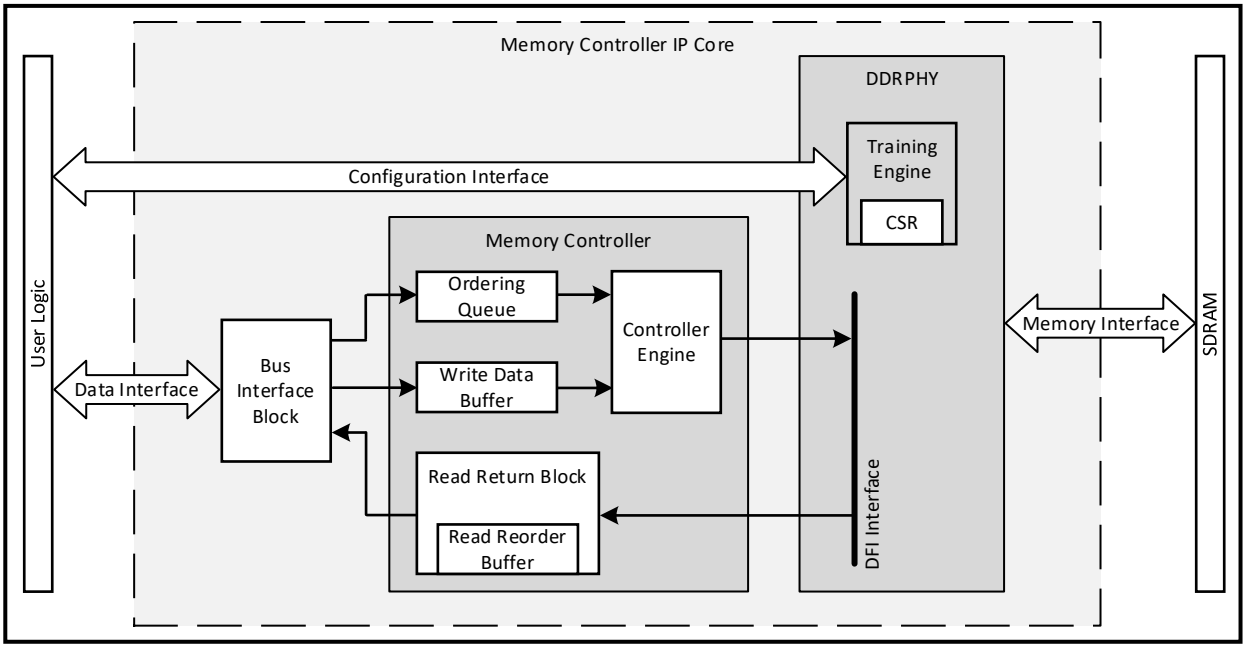

Figure 2.1. Memory Controller IP Core Functional Diagram

The data interface allows users to initiate command/address/control and read/write operations to external DDR4/LPDDR4 SDRAM. The configuration interface provides access to the Training Engine and the Configuration Set Registers (CSRs), which configure the Memory Controller and perform the DDR4/LPDDR4 training sequences. The memory interface allows the selected Lattice FPGA to communicate with the external DDR4/LPDDR4 memory. For more information on the data and configuration interfaces, refer to the User Interfaces section of this User Guide.

2.1.1. Hardened Memory Controller

The Hardened Memory Controller consists of the following submodules:

- Bus Interface Block
- Controller Engine
- Read Return Block

2.1.1.1. Bus Interface Block

The Bus Interface Block is responsible for accepting user-initiated operations on the selected data interface and translating them for processing within the Memory Controller. The data provided to the Controller Engine consists of:

- Address interface size: determined based on the selected SDRAM device density and DDR4/LPDDR4 data width
- Read and Write interface sizes: determined based on the selected DDR4/LPDDR4 data width

The ordering queue is responsible for queuing the address, command, and control information coming from the Bus Interface Block. It prioritizes the execution of commands targeting an already opened bank and maintains correct order of

execution when multiple requests target the same bank in DDR4/LPDDR4 SDRAM. The write data buffer is responsible for buffering the incoming data for write commands.

2.1.1.2. Controller Engine

The Controller Engine accepts the received requests from the Bus Interface and is responsible for translating the address to row, column, and bank format. The Controller Engine supports outstanding writes and reads, which is a write/read request that is entered into a queue and arbitrated for processing. The following table describes the three different types of requests and how they are processed.

Table 2.1. MCE Request Handling

Request type	Prioritization and Definition	Comments
Read	Varies depending on selected data interface protocol. Refer to the Data Interface Protocols section of this User Guide for details.	The read request size is equal to the supported DDR4/LPDDR4 burst length.
Write	Write requests are defined as a write, where the entire data needs to be written for the supported DDR4/LPDDR4 burst length.	Example: For a 32-bit DDR4/LPDDR4 data bus width, with burst length 8 (BL8), a full write would be 8×4B = 32B.
Partial write	Partial write requests are defined as a write, where the entire data *is not* written.	Example: For a 32-bit DDR4/LPDDR4 data bus width, a partial write would be a write request that is less than 32B. This is equivalent to a masked write.

All write requests may be processed out of order if a data dependency is not present. For example, an incoming request tied to an already opened page in DDR4/LPDDR4 SDRAM can be prioritized if it is not dependent on the requests already in the queue. Read requests may also be processed out of order if a data dependency is not present depending on the selected data interface protocol. Refer to the Data Interface Protocols section of this User Guide for information regarding outstanding write/read support.

The Controller Engine contains bank management logic to track all the opened and closed pages within each bank, along with timers for each bank and rank. This allows issued memory commands to meet the operational sequence and timing requirements of the DDR4/LPDDR4 SDRAM. The last layer of logic within the Controller Engine handles handshaking between the PHY and external memory. The Controller Engine is also responsible for supporting periodic events compliant with the DDR4/LPDDR4 SDRAM requirements. For more information on supported periodic features, refer to the Operation Descriptions section of this User Guide.

2.1.1.3. Read Return Block

The Read Return Block is responsible for responding to the Controller Engine issued read requests. Execution of commands can be out of order, so the Read Return Block handles the reordering to ensure that the read data is sent to the Bus Interface in order. The Read Return Block also handles Data Bus Inversion (DBI), which is an I/O signaling technique that reduces power consumption and improves signal integrity.

2.1.2. Hardened DDRPHY

The DDRPHY Hard IP is an implementation of the DFI 4.0 Specification (© Cadence Design Systems, Inc.). It is instantiated in the DDRPHY module, which also contains a dedicated PLL and quarter rate clock generator. The DDRPHY is responsible for implementing 8:1 gearing and training of the DDR4/LPDDR4 interface. Figure 2.2 represents a high-level block diagram of the DDRPHY module.

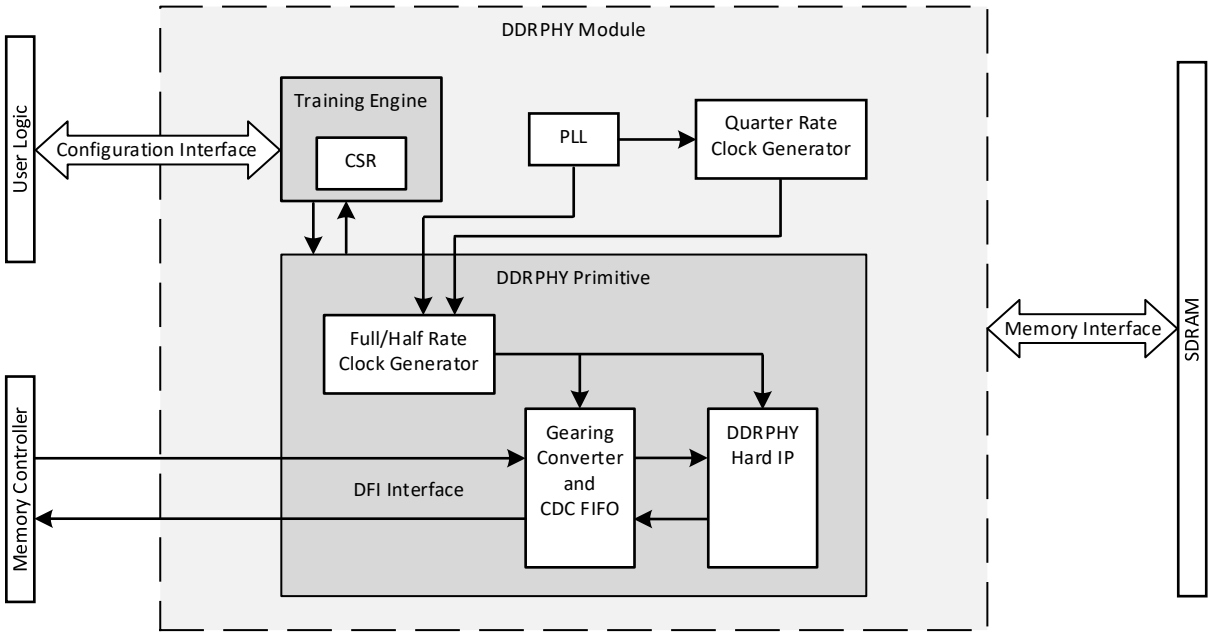

Figure 2.2. DDRPHY

2.1.2.1. DDRPHY Primitive

The PHY utilizes hardened logic, called I/O modules or hardware primitives, to implement clock synchronization logic and the command/address and data input/output paths. The clock synchronization logic handles Clock Domain Crossing (CDC) between the Edge Clock (ECLK) and System Clock (SCLK). ECLK is an internal clock used to clock the DDR primitives and SCLK is used to clock the Memory Controller IP Core. Without proper synchronization, the bit order on individual elements might become desynchronized, causing the data bus to become scrambled.

The Memory Controller operates in 8:1 gearing mode, which means that ECLK operates at the same frequency as the DDR4/LPDDR4 interface and that SCLK operates at a quarter of the DDR4/LPDDR4 memory clock. In other words, for a 400 MHz DDR4/LPDDR4 interface, ECLK operates at 400 MHz and SCLK operates at 100 MHz. This clocking ratio and DDR transfer relationship means that the user data bus is eight times the width of the DDR4/LPDDR4 memory data bus. For example, a 32-bit DDR4/LPDDR4 memory interface would require a 256-bit write and read data bus on the DDR PHY (DFI) side, which is an interface protocol between the Memory Controller and PHY. For more information regarding the DDRPHY, hardware primitives, and clock synchronization logic, refer to the Avant DDR Memory PHY Module IP User Guide.

2.1.2.2. Training Engine

The Training Engine is responsible for initializing and training the external DDR4/LPDDR4 memory. It provides a configuration interface from user logic to the Configuration Set Registers (CSR). Users can issue commands to the Training Engine to perform reads and writes to these registers, allowing users to handle interrupts and obtain details during the memory training sequence. It consists of user-accessible registers, a RISC-V CPU subsystem and hardened PHY. For more information regarding the training engine, refer to the Avant DDR Memory PHY Module IP User Guide.

2.2. Clocking and Reset

The Memory Controller IP requires a differential POD12 input reference clock for DDR4 and a differential LVSTL input reference clock for LPDDR4 interfaces. Users need to provide this clock (pll_refclk_i) via an external source and route it to an appropriate pin on the FPGA. Refer to the IP Parameter Description section of this User Guide for a list of valid frequencies supported by the input reference clock.

The provided input clock is then routed through a dedicated PLL within the Memory Controller IP to generate the Edge Clock (ECLK) and System Clock (SCLK). The ECLK signal is used internally to the IP Core to clock the I/O modules and SCLK is used to clock the IP Core. The Primary Clock (PCLK) signal is used to implement clock synchronization logic to synchronize

SCLK and ECLK. For additional details regarding clock synchronization, refer to the Avant DDR Memory PHY Module IP User Guide.

The Memory Controller IP contains an asynchronous active low reset: rst_n_i. When asserted, the Memory Controller and SDRAM are reset to their default values. The IP Core contains internal logic to synchronously de-assert the internal reset once rst_n_i is de-asserted, so users do not need to worry about implementing their own deassertion logic.

The configuration interface for the Memory Controller operates off the pclk_i signal and is reset via the preset_n_i signal. The clock for the configuration interface is the same one used to implement clock synchronization for SCLK and ECLK. The preset_n_i signal is an asynchronous active low reset, where users must ensure it is synchronously de-asserted to pclk_i. Refer to the Data Interface Protocols section of this User Guide for information regarding the clocks and resets for the Memory Controller supported data interfaces.

2.3. User Interfaces

This section describes the supported protocols for data and configuration interfaces available to the user and supported by the Memory Controller.

2.3.1. AXI4 Data Interface

The data interface allows users to initiate read and write operations to external SDRAM. The AXI4 I/F is intended for high-bandwidth and low-latency operation. The AXI4 I/F is a multi-channel bus consisting of 5 independent channels: write address, read address, write data, read data, and write response channels (read response is sent along with the read data). The AXI4 I/F operates off the aclk_i signal when the *Enable Local Bus Clock* attribute is checked. The AXI4 I/F is reset via the areset_n_i signal, which is an asynchronous active low reset, where users must ensure it is synchronously de-asserted to aclk_i.

The Memory Controller IP supports the following AXI4 types of burst transfers:

- Burst Type (AxBURST):
  - INCR: incrementing burst that does not wrap at address boundaries
- Burst Size (AxSIZE):
  - [1, 2, 4, 8, 16, 32, 64] Bytes
- Burst Length (AxLEN):
  - 1-256 beat burst
- Burst Address (AxADDR):
  - Unaligned addressing is not supported so all transfers must be aligned to AxSIZE
  - Unaligned transfer is supported using byte strobes
  - For maximum burst length of 64, address is required to be aligned to (DDR_WIDTH / 8) × 32
- Write Strobes (WSTRB):
  - Only the first and last beats of a burst can have incomplete byte strobes (WSTRB cannot go low in middle of burst)

The AXI4 protocol supports out of order transaction completion and contains support for multiple outstanding transactions per bus master. As a result, when AXI4 is configured as the user data interface, the Memory Controller can support up to 8 outstanding writes and 8 outstanding reads, where both reads and writes are of the same priority. For more information regarding the AXI4 protocol, refer to the AMBA AXI Protocol Specification.

Table 2.2. Supported AXI4 Transactions

Transaction Type	AxBURST	AxLEN[3:0]	AxSIZE[2:0]	Comment
Write	INCR	[0-254]	[0, 1, 2, 4, 5, 6][1]	[1-4096] Byte write
Read	INCR	[0-254]	[0, 1, 2, 4, 5, 6][1]	[1-4096] Byte read

Notes:

1. For AxSIZE=4, only DDR_WIDTH=16 is supported. For AxSIZE=5, only DDR_WIDTH=32 is supported. For AxSIZE=6, only DDR_WIDTH=64 is supported.

2.3.2. APB Configuration Interface

The configuration interface allows users to initialize and train the memory interface. The Memory Controller IP Core utilizes the APB protocol for its configuration interface. The APB I/F is a low-power protocol intended for accessing programmable control registers. It is not pipelined and is a synchronous protocol with a single address bus and two data busses: write and read. For more information regarding the APB protocol, please refer to the AMBA APB Protocol Specification.

The Memory Controller leverages this protocol to initialize and train the interface between FPGA logic and SDRAM. The APB I/F operates off the pclk_i signal and is reset via the preset_n_i signal. Refer to the Clocking and Reset section of this User Guide for more details.

The APB I/F is not available when the *Enable APB I/F* attribute is unchecked. For details on how to initialize and train SDRAM without the APB I/F, refer to the Initialization and Training without APB Interface section of this User Guide.

2.4. Calibration

To ensure proper device functionality, the external SDRAM must be initialized and trained before the Memory Controller can perform data accesses. Upon device power-up, the soft RISC-V CPU located inside the Training Engine is held in reset. To start the initialization and training sequence of the SDRAM device, the user should execute the following steps via the configuration interface:

- Enable initialization and training by writing 9'h1DF to the Training Operation Register (TRN_OP_REG). This will enable initialization, command bus training, write leveling, read training, and write training sequences to execute. For simulation purposes, it is recommended to shorten the initialization and training sequences (including command bus training) by writing 9'h01C to TRN_OP_REG. For more information, refer to the Avant DDR Memory PHY Module IP User Guide.
- Pull the CPU and Training Engine out of reset by writing 2'h3 to the Reset Register (RESET_REG). This begins the initialization and training sequence.
- Wait until initialization and training completes using one of the following methods:
  - Poll the Status Register (STATUS_REG) until the write_trn_done signal is asserted (STATUS_REG[4]=1). This indicates that write training has completed, which is the final stage in the initialization and training process.
  - Wait for the trn_done_int signal (INT_STATUS_REG[0]=1) or the trn_error_int signal (INT_STATUS_REG[1]=1) to assert in the Interrupt Status Register (INT_STATUS_REG). This method requires the trn_done_en signal (INT_ENABLE_REG[0]=1) and the trn_err_en signal (INT_ENABLE_REG[1]=1) to be asserted in the Interrupt Enable Register (INT_ENABLE_REG)

After the above steps complete, the control of the PHY is transferred to the Memory Controller and the user can now start accessing the SDRAM memory through the data interface. Once init_done_o asserts, the RISC-V CPU and Training Engine enter reset to save power.

2.4.1. Initialization and Training Sequence

The Memory Controller IP performs initialization according to the DDR4/LPDDR4 JEDEC Standards. For more information on the stages that occur during the initialization and training sequence, refer to the Avant DDR Memory PHY Module IP User Guide.

2.4.2. Initialization and Training without APB Interface

The APB I/F will not be available when the *Enable APB I/F* attribute is unchecked. In this case, the init_start_i and trn_opr_i signals will be available for starting and configuring the DDR4/LPDDR4 initialization and training. The trn_opr_i sets the value of the Training Operation Register (TRN_OP_REG), thus controlling which specific training steps to perform based on the asserted bits. For hardware implementation, it is recommended to set trn_opr_i=0x1DF to perform: command bus training, write leveling, read training, and write training procedures. For simulation purposes, it is recommended to shorten the initialization and training sequences (including command bus training) by setting trn_opr_i=0x01C. Refer to the Register Description section of this User Guide for more details.

The user should execute the following steps to start the initialization and training sequence of the DDR4/LPDDR4 SDRAM:

1. Set init_start_i=0 while the Memory Controller IP is in reset or while pll_lock_o=0
2. Set init_start_i=1 and maintain this value until init_done_o asserts
3. Once init_done_o=1, set init_start_i=0 to hold the training CPU in reset to save power

2.5. Operation Descriptions

This section provides details on various operations and features supported by the Memory Controller IP.

2.5.1. DDR4

The following section describes the operations supported in DDR4 mode.

2.5.1.1. Write and Read Data Access

Once the init_done_o signal asserts, users can initiate write and read accesses. The types of data accesses supported by the Memory Controller IP depends on the selected data interface protocol. Refer to Table 2.2 for a list of all supported AXI4 data accesses.

The Memory Controller decodes the memory-mapped address to check if the row and bank addresses are already opened in the memory device. When a WRITE/READ command is issued to DDR4 memory the following commands are issued:

- If the target row and bank are not open, an ACTIVATE command is issued by the Memory Controller to the DDR4 SDRAM to open the row. This is followed by the WRITE/READ command.
- If there is an opened row in the current bank, and the target row address is different from the opened row, a PRECHARGE command is issued by the Memory Controller to close the opened row. This is followed by an ACTIVATE command to open the target row and then the WRITE/READ command.
- If the target row is already opened, only a WRITE/READ command is issued.

The Memory Controller does not immediately close a row after a WRITE/READ command, it issues a separate PRECHARGE command as needed.

2.5.1.2. Auto Refresh Support

Ideally, REFRESH commands should be issued every refresh interval, specified by the *Refresh Period* attribute. To improve efficiency in scheduling and switching between tasks, the DDR4 memory allows a maximum of 8 REFRESH commands to be postponed throughout the DDR4 operation. The Memory Controller has an internal auto refresh generator that sends out a set of consecutive AUTO REFRESH commands to the memory once when it reaches the time specified in the following calculation: *Refresh Period* × *No. of Outstanding Refresh*.

For high performance applications, it is recommended to set *No. of Outstanding Refresh* to the maximum value. This increases the DDR4 bus throughput by minimizing Memory Controller intervention.

2.5.1.3. Periodic ZQ Calibration

ZQ Calibration calibrates the output driver impedance across PVT. There are two ZQ Calibration modes initiated with the Multi-Purpose Command (MPC): ZQCAL START and ZQCAL LATCH. The ZQCAL START command initiates the SDRAM's calibration procedure, and the ZQCAL LATCH command captures the result and loads it into the SDRAM's drivers.

The Memory Controller IP periodically performs ZQ Calibration as the voltage and temperature may fluctuate during operation. The user can configure the frequency at which ZQ Calibration is performed and its duration via the *ZQ Calibration Period* and *ZQ Calibration Start to Latch* attributes. When SETTINGS_REG[16]=0, ZQ Calibration is set to Short, whereas when SETTINGS_REG[16]=1, ZQ Calibration is set to Long. Refer to the Register Description section of this User Guide for more details.

2.5.2. LPDDR4

The following section describes the operations supported in LPDDR4 mode.

2.5.2.1. Write and Read Data Access

Once the init_done_o signal asserts, users can initiate write and read accesses. The types of data accesses supported by the Memory Controller IP depends on the selected data interface protocol. Refer to Table 2.2 for a list of all supported AXI4 data accesses.

The Memory Controller decodes the memory-mapped address to check if the row and bank addresses are already opened in the memory device. When a WRITE/READ command is issued to LPDDR4 memory the following commands are issued:

- If the target row and bank are not open, an ACTIVATE command is issued by the Memory Controller to the LPDDR4 SDRAM to open the row. This is followed by the WRITE/READ command.
- If there is an opened row in the current bank, and the target row address is different from the opened row, a PRECHARGE command is issued by the Memory Controller to close the opened row. This is followed by an ACTIVATE command to open the target row and then the WRITE/READ command.
- If the target row is already opened, only a WRITE/READ command is issued.

The Memory Controller does not immediately close a row after a WRITE/READ command, it issues a separate PRECHARGE command as needed.

2.5.2.2. Auto Refresh Support

Ideally, REFRESH commands should be issued every refresh interval, specified by the *Refresh Period* attribute. To improve efficiency in scheduling and switching between tasks, the LPDDR4 memory allows a maximum of 8 REFRESH commands to be postponed throughout the LPDDR4 operation. The Memory Controller has an internal auto refresh generator that sends out a set of consecutive AUTO REFRESH commands to the memory once when it reaches the time specified in the following calculation: *Refresh Period* × *No. of Outstanding Refresh*.

For high performance applications, it is recommended to set *No. of Outstanding Refresh* to the maximum value. This increases the LPDDR4 bus throughput by minimizing Memory Controller intervention.

2.5.2.3. Power Saving Feature

The Memory Controller supports power-saving when the *Enable Power Down* attribute is set. The Memory Controller IP tracks the period of inactivity on the local data bus by monitoring the System Clock (SCLK), which is the main clock used by the Memory Controller IP. When the period of inactivity on the bus reaches the value set in the *Number of SCLK to enter Self-Refresh from no traffic* attribute, the Memory Controller will issue SELF REFRESH and Power-Down Entry commands. This will put the memory into Power-Down mode to save power until a new request is received on the local data bus, at which the Memory Controller will issue SELF REFRESH and Power-Down Exit commands, followed by an additional REFRESH command.

2.5.2.4. Periodic ZQ Calibration

ZQ Calibration calibrates the output driver impedance across PVT. There are two ZQ Calibration modes initiated with the Multi-Purpose Command (MPC): ZQCAL START and ZQCAL LATCH. The ZQCAL START command initiates the SDRAM's calibration procedure, and the ZQCAL LATCH command captures the result and loads it into the SDRAM's drivers.

The Memory Controller IP periodically performs ZQ Calibration as the voltage and temperature may fluctuate during operation. The user can configure the frequency at which ZQ Calibration is performed and its duration via the *ZQ Calibration Period* and *ZQ Calibration Start to Latch* attributes. When SETTINGS_REG[16]=0, ZQ Calibration is set to Short, whereas when SETTINGS_REG[16]=1, ZQ Calibration is set to Long. Refer to the Register Description section of this User Guide for more details.

2.5.2.5. Temperature Tracking and Extended Temperature Support

LPDDR4 SDRAM devices support temperature tracking, where the device's refresh rate can change based on the operational temperature. When the memory device's temperature is within normal operating conditions, the rate is set to 1x refresh, which is the default case. As the temperature fluctuates below or above the default case, the Memory Controller will decrease or increase the frequency of refreshes respectively. The required refresh rate according to temperature is

specified in MR4 within LPDDR4 SDRAM. When the Temperature Update Flag (TUF) is set in MR4, it indicates that the refresh rate has changed from the last read issued to MR4.

LPDDR4 SDRAM devices also support operation for extended temperature. When the operational temperature increases beyond normal operation conditions, the refresh frequency begins to increase. When the refresh rate in MR4 is set to 3'b110, timing derating is required for certain commands, slowing performance. For more information regarding temperature derating timing requirements, refer to the LPDDR4 JEDEC Standard.

The Memory Controller IP reads MR4 periodically to track the temperature of the LPDDR4 memory device. Based on the refresh rate set in MR4, the Memory Controller IP issues REFRESH commands at the required frequency. Note that when the refresh rate in MR4 is set to either 3'b000 or 3' b111, the LPDDR4 memory may not work as expected due to exceeding of low/high temperature operating limits.
When the refresh rate is set to 3'b110 in MR4, the Memory Controller accommodates the temperature derating timing requirements when issuing commands to the memory. The user can change the frequency at which the memory's MR4 register is read through the *Temperature Check Period* attribute. When reading MR4, the Memory Controller IP sets STATUS_REG[18:16] to the read refresh rate value, and INT_STATUS_REG[4]=1 when TUF is set in MR4. Refer to the Register Description section of this User Guide for more details.

3. IP Parameter Description

The configurable attributes of the Memory Controller IP Core for Avant Devices are shown and described in the following tables. These attributes can be configured through the IP Catalog's Module/IP Block Wizard of the Lattice Radiant software. Refer to the Designing and Simulating the IP section of this User Guide for information on how to configure and generate the Memory Controller IP.

3.1. DDR4

The following section describes the parameters available in DDR4 mode.

3.1.1. General

The following section describes the parameters available in the General tab of the IP parameter editor.

Table 3.1. DDR4 General Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
Interface Type	DDR4	DDR4	Display only
I/O Buffer Type	POD12	POD12	Display only
DDR Command Frequency (MHz)[1]	666, 800, 933, 1066, 1200	800	—
Gearing Ratio	8:1	8:1	Display only
Enable Side-band ECC	Checked, Unchecked	Unchecked	Display only
Enable Power Down	Checked, Unchecked	Unchecked	Display only
Enable DBI	Checked, Unchecked	Unchecked	Display only
Read Latency	Calculated	N/A	Calculated based off selection for *DDR Command Frequency*
Write Latency	Calculated	N/A	Calculated based off selection for *DDR Command Frequency*
Enable Internal RISC-V CPU	Checked, Unchecked	Checked	Display only (Disabling of Internal RISC-V CPU is not yet supported)

Notes:

1. Only Avant-AT-G and Avant-AT-X devices can support DDR command frequencies greater than 933MHz. For Avant-AT-G and Avant-AT-X devices, speed grades of 2 and 3 can support DDR command frequencies up to 1066MHz, and only device speed grade of 3 can support up to 1200MHz.

Table 3.2. DDR4 Clock Settings Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
Enable PLL	Checked	Checked	Display only
Reference Clock Frequency (MHz)	Integer	100.0	—
DDR Memory Actual Frequency (MHz)	Calculated	N/A	Display only Based off selection for *DDR Command Frequency*

Table 3.3. DDR4 Memory Configuration Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
DDR Density (per Channel)	2 Gb, 4 Gb, 8 Gb, 16 Gb	4 Gb	—
DDR Bus Width (DDR_WIDTH)	16, 32, 64	32	—
Number of Ranks (CS_WIDTH)	1	1	Display only (Only single rank is supported)
Number of DDR Clocks (CK_WIDTH)	1, 2	1	—

Table 3.4. DDR4 Local Data Bus Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
Local Data Bus Type	AXI4	AXI4	Display only
Address Width	Calculated	N/A	Display only Calculated based off selection for *DDR Density*
Data Width	32, 64, 128, 256	256	—
ID Width	2, 3, 4, 5, 6, 7, 8	4	—
Maximum Burst Length	64, 256	64	—
Write Ordering Queues	1, 2, 3, 4	2	—
Read Ordering Queues	1, 2, 3, 4	2	—
Enable Local Bus Clock	Checked/Unchecked	Checked	—
Enable APB I/F	Checked/Unchecked	Checked	—

Table 3.5. DDR4 General Definitions

Attribute	Description
General Group	
Interface Type	Specifies the SDRAM Memory interface: DDR4
I/O Buffer Type	I/O Standard for the memory interface signals
DDR Command Frequency (MHz)	Speed at which the memory controller will issue commands to the memory device
Gearing Ratio	Specifies the ratio relationship between the DDR data speed and the memory controller speed
Enable Power Down	Enables memory controller automatically placing the memory device into power-down mode after a specified number of idle controller clock cycles (not yet supported)
Enable DBI	Enables data bus inversion (DBI) for better signal integrity and read/write margins
Read Latency	Specifies the delay from issuing of a read command to receiving of read data from SDRAM
Write Latency	Specifies the delay from issuing of a write command to providing of write data to SDRAM
Enable Internal RISC-V CPU	Enables RISC-V subsystem to support initialization and training of the memory device (disabling is not yet supported)
Clock Settings Group	
Enable PLL	Enables PLL
Reference Clock: Frequency (MHz)	Indicates the PLL reference clock speed
DDR Memory Actual Frequency (MHz)	Specifies the actual operating frequency of the memory interface (calculated by the PLL – includes tolerance)
Memory Configuration Group	
DDR Density (per Channel)	Density of SDRAM (# of chips on memory module). Only DDR Density with power of 2 is supported.
DDR Bus Width	Total number of data pins in memory interface
Number of Ranks	Specifies number of ranks in memory interface (only single rank is supported)
Number of DDR Clocks	Specifies the number of CK/CK# clock pairs to be driven to SDRAM
Local Data Bus Group	
Local Data Bus Type	Indicates bus for local data interface: AXI4 or NATIVE
Address Width	Specifies number of address pins in memory interface, dependent on the SDRAM density
Data Width (AXI_DATA_WIDTH)	Indicates data width for local data bus
ID Width	Indicates bit width of AXI4 ID
Maximum Burst Length	Specifies the maximum AXI4 burst length. Recommended to set based off system requirements to save EBR resources.
Write Ordering Queues	The number of write/read ordering queues process write and read data requests. The higher the value, the better bandwidth on the interface since gaps between accesses is lessened at the cost of consuming more LUTs.
Read Ordering Queues	

Attribute	Description
Enable Local Bus Clock	Enables clock domain crossing logic for the local data bus
Enable APB I/F	Enables APB interface. Should be enabled if target application includes a CPU. When disabled, initialization and training of SDRAM should be handled via init_start_i and trn_opr_i signals. Please refer to the Initialization and Training without APB Interface section of this User Guide for more information.

3.1.2. Memory Device Timing

The following section describes the parameters available in the Memory Device Timing tab of the IP parameter editor. The default value for the attributes listed under Memory Device Timing Setting Group is different for each DDR Command Frequency value, and is based off what is specified in the JESD79-4D SDRAM standard. These values may need to be manually adjusted based on the selected DDR4 device.

Table 3.6. DDR4 Memory Device Timing Setting Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
Manual Timing Adjust Enable	Checked/Unchecked	Unchecked	—
TRCD (tCLK)	4-65536	Calculated	Enabled when *Manually Adjust* is Checked
TRAS (tCLK)	4-65536	Calculated	Enabled when *Manually Adjust* is Checked
TRPPB (tCLK)	4-65536	Calculated	Enabled when *Manually Adjust* is Checked
TWR (tCLK)	4-65536	Calculated	Enabled when *Manually Adjust* is Checked
TRTP (tCLK)	8-65536	Calculated	Enabled when *Manually Adjust* is Checked
TCCD (tCLK)	8-65536	Calculated	Enabled when *Manually Adjust* is Checked
MWR2MWR (tCLK)	32-65536	Calculated	Enabled when *Manually Adjust* is Checked
TRRD (tCLK)	6-65536	Calculated	Enabled when *Manually Adjust* is Checked
TRFC (tCLK)	24-28080	Calculated	Enabled when *Manually Adjust* is Checked
TFAW (tCLK)	40-65536	Calculated	Enabled when *Manually Adjust* is Checked
TZQCAL (tCLK)	4-65536	Calculated	Enabled when *Manually Adjust* is Checked
TMRR (tCLK)	8-65536	Calculated	Enabled when *Manually Adjust* is Checked
TMRD (tCLK)	10-65536	Calculated	Enabled when *Manually Adjust* is Checked
TRPAB (tCLK)	4-65536	Calculated	Enabled when *Manually Adjust* is Checked
TRTW (tCLK)	21-65536	Calculated	Enabled when *Manually Adjust* is Checked
TDQSS (tCLK)	Integer	0	Enabled when *Manually Adjust* is Checked
TRD2PRE (tCLK)	4-65536	Calculated	Enabled when *Manually Adjust* is Checked
TWR2PRE (tCLK)	4-65536	Calculated	Enabled when *Manually Adjust* is Checked
TXP (tCLK)	4-65536	Calculated	Enabled when *Manually Adjust* is Checked
TXPSR (tCLK)	4-65536	Calculated	Enabled when *Manually Adjust* is Checked

Table 3.7. DDR4 Periodic Event Setting Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
No. of SCLK to enter Self Refresh from no traffic	Integer	1000	Enabled when *Enable Power Down* is Checked
Refresh Period (tSCLK)	Calculated	Calculated	Default value is calculated based off selection for *DDR Command Frequency*
No. of Outstanding Refresh	1-7	7	—
ZQ Calibration Period (sec)	Integer	32	—
ZQ Calibration Start to Latch (usec)	Integer	1	—
Temperature Check Period (sec)	Integer	32	—

Table 3.8. DDR4 Trim Settings

Attribute	Selectable Values	Default	Dependency on Other Attributes
DDR Clock Delay Value	0-9	7	—

Table 3.9. DDR4 Memory Device Timing Definitions

Attribute	Description
Memory Device Timing Setting Group[1]	
Manual Timing Adjust Enable	Enables user to manually set any of the memory timing parameters
TRCD	Indicates the delay between the ACTIVATE command (RAS) and the internal access to data (CAS)
TRAS	Indicates how long memory must wait after an ACTIVATE command before a PRECHARGE command can be issued to close the row
TRPPB	Row PRECHARGE time for a single bank
TWR	Specifies the amount of clock cycles needed to complete a WRITE before a PRECHARGE command can be issued
TRTP	Internal READ to PRECHARGE delay
TCCD	Minimum time between two READ/WRITE (CAS) commands (burst length / 2)
MWR2MWR	Masked WRITE to masked WRITE
TRRD	Minimum time interval between two ACTIVATE commands to different banks
TRFC	Indicates how long memory must wait after a REFRESH command before an ACTIVATE command can be accepted by memory
TFAW	Specifies the period duration during which only four banks can be active
TZQCAL	ZQ calibration time from START to LATCH command
TMRR	Mode register READ command period
TMRD	Minimum time between two MRS commands
TRPAB	Row PRECHARGE time for all banks
TRTW	READ to WRITE command delay
TDQSS	Describes skew between the output data strobe with respect to the memory clock for writes (DQS to CK)
TRD2PRE	READ to PRECHARGE time
TWR2PRE	WRITE to PRECHARGE time
TXP	Power-down exit latency to next valid command
TXPSR	Power-down exit latency to next self-refresh
Periodic Event Setting Group	
Number of SCLK to enter Self-Refresh from no traffic	The memory controller puts the memory in self-refresh when there is no traffic for the specified number of SCLK cycles
Refresh Period	Specifies the number of SCLK cycles between refresh commands
Number of Outstanding Refresh	Specifies the maximum number of outstanding refresh commands. Refer to the Auto Refresh Support section of this User Guide for more information.
ZQ Calibration Period	Indicates period for performing ZQ Calibration in seconds
ZQ Calibration Start to Latch	Indicates time from start to latch during ZQ Calibration in microseconds
Temperature Check Period	Indicates period for reading the temperature register (MR4) in DDR4 memory in seconds
Trim Settings	
DDR Clock Delay Value	Specifies the DDR clock delay .so that the first DQS toggle is at CK = 0 during write leveling. It is recommended to increase this value if write leveling fails

Notes:

1. The memory device timing parameters listed under the Memory Device Timing tab are defined according to the JESD79-4D SDRAM standard. Refer to the memory device data sheet for detailed descriptions and allowed values for these parameters.

3.2. LPDDR4

The following section describes the parameters available in LPDDR4 mode.

3.2.1. General

The following section describes the parameters available in the General tab of the IP parameter editor.

Table 3.10. LPDDR4 General Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
Interface Type	LPDDR4	LPDDR4	Display only
I/O Buffer Type	LVSTL11_I, LVSTL11_II	LVSTL11_II	—
DDR Command Frequency (MHz)[1]	350, 400, 533, 666, 800, 933, 1066, 1200	800	—
Gearing Ratio	8:1	8:1	Display only
Enable Power Down	Checked, Unchecked	Unchecked	Display only
Enable DBI	Checked, Unchecked	Unchecked	Enabled when *DDR Command Frequency* is 800 or less
Read Latency	Calculated	N/A	Display only Calculated based off selection for *DDR Command Frequency*
Write Latency	Calculated	N/A	Display only Calculated based off selection for *DDR Command Frequency*
Enable Internal RISC-V CPU	Checked, Unchecked	Checked	Display only (Disabling of Internal RISC-V CPU is not yet supported)

Notes:

1. Only Avant-AT-G and Avant-AT-X devices can support DDR command frequencies greater than 933MHz. For Avant-AT-G and Avant-AT-X devices, speed grades of 2 and 3 can support DDR command frequencies up to 1066MHz, and only device speed grade of 3 can support up to 1200MHz.

Table 3.11. LPDDR4 Clock Settings Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
Enable PLL	Checked	Checked	Display only
Reference Clock: Frequency (MHz)	25.0, 50.0, 100.0	100.0	—
DDR Memory Actual Frequency (MHz)	Calculated	N/A	Display only Based off selection for *DDR Command Frequency*

Table 3.12. LPDDR4 Memory Configuration Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
DDR Density (per Channel)	2 Gb, 4 Gb, 8 Gb, 16 Gb	4 Gb	—
DDR Bus Width (DDR_WIDTH)	16, 32, 64	32	—
Number of Ranks (CS_WIDTH)	1	1	Display only (Only single rank is supported)
Number of DDR Clocks (CK_WIDTH)	1, 2	1	—

Table 3.13. LPDDR4 Local Data Bus Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
Local Data Bus Type	AXI4	AXI4	—
Address Width	Calculated	N/A	Display only Calculated based off selection for *DDR Density*
Data Width (AXI_DATA_WIDTH)	32, 64, 128, 256	256	—
ID Width	2, 3, 4, 5, 6, 7, 8	4	—
Maximum Burst Length	64, 128, 256	64	—
Write Ordering Queues	1, 2, 3, 4	4	—
Read Ordering Queues	1, 2, 3, 4	4	—
Enable Local Bus Clock	Checked/Unchecked	Checked	—
Enable APB I/F	Checked/Unchecked	Checked	—

Table 3.14. LPDDR4 General Definitions

Attribute	Description
General Group	
Interface Type	Specifies the SDRAM Memory interface: LPDDR4
I/O Buffer Type	I/O Standard for the memory interface signals
DDR Command Frequency (MHz)	Speed at which the memory controller will issue commands to the memory device
Gearing Ratio	Specifies the ratio relationship between the DDR data speed and the memory controller speed
Enable Power Down	Enables memory controller automatically placing the memory device into power-down mode after a specified number of idle controller clock cycles (not yet supported)
Enable DBI	Enables data bus inversion (DBI) for better signal integrity and read/write margins (not yet supported)
Read Latency	Specifies the delay from issuing of a read command to receiving of read data from SDRAM
Write Latency	Specifies the delay from issuing of a write command to providing of write data to SDRAM
Enable Internal RISC-V CPU	Enables RISC-V subsystem to support initialization and training of the memory device (disabling is not yet supported)
Clock Settings Group	
Enable PLL	Enables PLL
Reference Clock: Frequency (MHz)	Indicates the PLL reference clock speed
DDR Memory Actual Frequency (MHz)	Specifies the actual operating frequency of the memory interface (calculated by the PLL – includes tolerance)
Memory Configuration Group	
DDR Density (per Channel)	Density of SDRAM (# of chips on memory module). Only DDR Density with power of 2 is supported.
DDR Bus Width	Total number of data pins in memory interface
Number of Ranks	Specifies number of ranks in memory interface (only single rank is supported)
Number of DDR Clocks	Specifies the number of CK/CK# clock pairs to be driven to SDRAM (multiple clocks is not yet supported)
Local Data Bus Group	
Local Data Bus Type	Indicates bus for local data interface: AXI4 or NATIVE
Address Width	Specifies number of address pins in memory interface, dependent on the SDRAM density
Data Width	Indicates data width for local data bus
ID Width	Indicates bit width of AXI4 ID
Maximum Burst Length	Specifies the maximum AXI4 burst length. Recommended to set based off system requirements to save EBR resources.

Attribute	Description
Write Ordering Queues	The number of write/read ordering queues process write and read data requests. The higher the value, the better bandwidth on the interface since gaps between accesses is lessened at the cost of consuming more LUTs.
Read Ordering Queues	
Enable Local Bus Clock	Enables clock domain crossing logic for the local data bus
Enable APB I/F	Enables APB interface. Should be enabled if target application includes a CPU. When disabled, initialization and training of SDRAM should be handled via init_start_i and trn_opr_i signals. Please refer to the Initialization and Training without APB Interface section of this User Guide for more information.

3.2.2. Memory Device Timing

The following section describes the parameters available in the Memory Device Timing tab of the IP parameter editor. The default value for the attributes listed under Memory Device Timing Setting Group is different for each DDR Command Frequency value, and is based off what is specified in the JESD209-4C SDRAM standard. These values may need to be manually adjusted based on the selected LPDDR4 device.

Table 3.15. LPDDR4 Memory Device Timing Setting Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
Manual Timing Adjust Enable	Checked/Unchecked	Unchecked	—
TRCD (tCLK)	4-65536	Calculated	Enabled when *Manually Adjust* is Checked
TRAS (tCLK)	4-65536	Calculated	Enabled when *Manually Adjust* is Checked
TRPPB (tCLK)	4-65536	Calculated	Enabled when *Manually Adjust* is Checked
TWR (tCLK)	4-65536	Calculated	Enabled when *Manually Adjust* is Checked
TRTP (tCLK)	8-65536	Calculated	Enabled when *Manually Adjust* is Checked
TCCD (tCLK)	8-65536	Calculated	Enabled when *Manually Adjust* is Checked
MWR2MWR (tCLK)	32-65536	Calculated	Enabled when *Manually Adjust* is Checked
TRRD (tCLK)	6-65536	Calculated	Enabled when *Manually Adjust* is Checked
TRFC (tCLK)	24-28080	Calculated	Enabled when *Manually Adjust* is Checked
TFAW (tCLK)	40-65536	Calculated	Enabled when *Manually Adjust* is Checked
TZQCAL (tCLK)	4-65536	Calculated	Enabled when *Manually Adjust* is Checked
TMRR (tCLK)	8-65536	Calculated	Enabled when *Manually Adjust* is Checked
TMRD (tCLK)	10-65536	Calculated	Enabled when *Manually Adjust* is Checked
TRPAB (tCLK)	4-65536	Calculated	Enabled when *Manually Adjust* is Checked
TRTW (tCLK)	21-65536	Calculated	Enabled when *Manually Adjust* is Checked
TDQSS (tCLK)	Integer	1	Enabled when *Manually Adjust* is Checked
TRD2PRE (tCLK)	4-65536	Calculated	Enabled when *Manually Adjust* is Checked
TWR2PRE (tCLK)	4-65536	Calculated	Enabled when *Manually Adjust* is Checked
TXP (tCLK)	4-65536	Calculated	Enabled when *Manually Adjust* is Checked
TXPSR (tCLK)	4-65536	Calculated	Enabled when *Manually Adjust* is Checked

Table 3.16. LPDDR4 Periodic Event Setting Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
No. of SCLK to enter Self Refresh from no traffic	Integer	1000	Enabled when *Enable Power Down* is Checked
Refresh Period (tSCLK)	Calculated	Calculated	Default value is calculated based off selection for *DDR Command Frequency*
No. of Outstanding Refresh	1-7	7	—
ZQ Calibration Period (sec)	Integer	32	—

Attribute	Selectable Values	Default	Dependency on Other Attributes
ZQ Calibration Start to Latch (usec)	Integer	1	—
Temperature Check Period (sec)	Integer	32	—

Table 3.17. LPDDR4 Memory Device Timing Definitions

Attribute	Description
Memory Device Timing Setting Group[1]	
Manual Timing Adjust Enable	Enables user to manually set any of the memory timing parameters
TRCD	Indicates the delay between the ACTIVATE command (RAS) and the internal access to data (CAS)
TRAS	Indicates how long memory must wait after an ACTIVATE command before a PRECHARGE command can be issued to close the row
TRPPB	Row PRECHARGE time for a single bank
TWR	Specifies the amount of clock cycles needed to complete a WRITE before a PRECHARGE command can be issued
TRTP	Internal READ to PRECHARGE delay
TCCD	Minimum time between two READ/WRITE (CAS) commands (burst length / 2)
MWR2MWR	Masked WRITE to masked WRITE
TRRD	Minimum time interval between two ACTIVATE commands to different banks
TRFC	Indicates how long memory must wait after a REFRESH command before an ACTIVATE command can be accepted by memory
TFAW	Specifies the period duration during which only four banks can be active
TZQCAL	ZQ calibration time from START to LATCH command
TMRR	Mode register READ command period
TMRD	Minimum time between two MRS commands
TRPAB	Row PRECHARGE time for all banks
TRTW	READ to WRITE command delay
TDQSS	Describes skew between the output data strobe with respect to the memory clock for writes (DQS to CK)
TRD2PRE	READ to PRECHARGE time
TWR2PRE	WRITE to PRECHARGE time
TXP	Power-down exit latency to next valid command
TXPSR	Power-down exit latency to next self-refresh
Periodic Event Setting Group	
Number of SCLK to enter Self-Refresh from no traffic	The memory controller puts the memory in self-refresh when there is no traffic for the specified number of SCLK cycles
Refresh Period	Specifies the number of SCLK cycles between refresh commands
Number of Outstanding Refresh	Specifies the maximum number of outstanding refresh commands. Refer to the Auto Refresh Support section of this User Guide for more information.
ZQ Calibration Period	Indicates period for performing ZQ Calibration in seconds
ZQ Calibration Start to Latch	Indicates time from start to latch during ZQ Calibration in microseconds
Temperature Check Period	Indicates period for reading the temperature register (MR4) in LPDDR4 memory in seconds

Notes:

1. The memory device timing parameters listed under the Memory Device Timing tab are defined according to the JESD209-4C SDRAM standard. Refer to the memory device data sheet for detailed descriptions and allowed values for these parameters.

3.2.3. Training Settings

The following section describes the parameters available in the Training Settings tab of the IP parameter editor.

Table 3.18. LPDDR4 Training Settings Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
DDR Clock Delay Value	0-20	0	—
DDR Clock Delay Value Incr/Decr	Checked/Unchecked	Checked	—
Address Control Delay Value	0-20	0	—
Address Control Delay Incr/Decr	Checked/Unchecked	Checked	—
CA_ODT Value	Disable, RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, RZQ/6	RZQ/6	—
DQ_ODT Value	Disable, RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, RZQ/6	RZQ/6	—
Controller ODT Value for VOH calibration	Disable, RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, RZQ/6	RZQ/6	—
CK_ODT Override Enable	Checked/Unchecked	Unchecked	—
CS_ODT Override Enable	Checked/Unchecked	Unchecked	—
CA_ODT Override Disable	Checked/Unchecked	Unchecked	—
ODT-CS/CA/CLK Disable	Checked/Unchecked	Unchecked	—

Table 3.19. LPDDR4 Training Settings Definitions

Attribute	Description
Training Settings Group[1]	
DDR Clock Delay Value	Specifies the DDR clock delay so that the first DQS toggle is at CK = 0 during write leveling. It is recommended to increase this value if write leveling fails
DDR Clock Delay Value Incr/Decr	Specifies the adjustment direction. Checked: DDR Clock Delay Value is added to the ddr_ck_o signal Unchecked: DDR Clock Delay Value is subtracted from the ddr_ck_o signal
Address Control Delay Value	Specifies the DDR address/control signals delay. It is recommended to increase this value if command bus training fails
Address Control Delay Incr/Decr	Specifies the adjustment direction. Checked: Address Control Delay Value is added to the DDR address/control signals Unchecked: Address Control Delay Value is subtracted from the DDR address/control signals
CA_ODT Value	Specifies the CA ODT value that is written to MR11 in LPDDR4 memory
DQ_ODT Value	Specifies the DQ ODT value that is written to MR11 in LPDDR4 memory
SoC_ODT Value	Specifies the SoC ODT value that is written to MR22 in LPDDR4 memory
CK_ODT Override Enable	Specifies the ODTE-CK value that is written to MR22 in LPDDR4 memory
CS_ODT Override Enable	Specifies the ODTE-CS value that is written to MR22 in LPDDR4 memory
CA_ODT Override Disable	Specifies the ODTE-CA value that is written to MR22 in LPDDR4 memory
ODT-CS/CA/CLK Disable	Specifies the x80DTD[7:0] and x8ODTD[15:8] values that is written to MR22 in LPDDR4 memory

Notes:

1. These attributes should only be modified when an error is encountered during LPDDR4 memory training.

4. Signal Description

The input and output signals of the Memory Controller IP Core for Avant Devices are covered in the following section. The signals available are based off the selected configuration of the Memory Controller IP.

4.1. DDR4

The following section describes the signals available in DDR4 mode.

Table 4.1. DDR4 Clock and Reset Port Definitions

Port Name	I/O	Width	Description
pll_refclk_i	In	1	PLL reference clock input
pll_rst_n_i	In	1	PLL reset active low
pclk_i	In	1	Clock for APB interface, training CPU and control logic of the internal PLL. This clock is independent of sclk_o, since sclk_o stops during clock frequency changes.
preset_n_i	In	1	Asynchronous active low reset for APB interface. This reset must be de-asserted synchronous to pclk_i.
aclk_i	In	1	Clock for AXI4 interface
sclk_o	Out	1	System clock. This is ¼ of the DDR clock frequency and is the main clock of the Memory Controller IP.
rst_n_i	In	1	Asynchronous active low reset. When asserted, output ports and registers are forced to their reset values. The Memory Controller IP implements logic to de-assert the internal reset synchronous to the internal clocks after rst_n_i de-asserts.
reset_n_i	In	1	Asynchronous active low reset for AXI4 I/F. This reset must be de-asserted synchronous to aclk_i. This is only available when *Enable Local Bus Clock* attribute is checked.

4.1.1. Interrupts and Initialization/Training

The following section describes the interface ports for interrupts and initialization/training control in the Memory Controller IP.

Table 4.2. DDR4 Interrupts and Initialization/Training Port Definitions

Port Name	I/O	Width	Description
irq_o	Out	1	Interrupt signal Reset value is 1'b0
init_start_i	In	1	Starts the memory initialization and training according to trn_opr_i. This signal is available when *Enable APB I/F* attribute is unchecked.
init_done_o	Out	1	Indicates completion of initialization and training and the memory is available for access through the data interface.
pll_lock_o	Out	1	PLL lock output indicating when PLL is locked
trn_err_o	Out	1	Indicates memory training has failed when asserted (1'b1)

4.1.2. AXI4 Data Interface

The following section describes the AXI4 data interface ports in the Memory Controller IP. Refer to the AMBA AXI Protocol Specification for a description of these signals. The transactions allowed on the AXI4 interface to the Memory Controller are described in Table 2.2.

Table 4.3. DDR4 AXI4 Interface Port Definitions

Port Name	I/O	Width	Description
axi_arid_i	In	AXI_ID_WIDTH	AXI4 read address channel: Read address ID signal
axi_araddr_i[1]	In	AXI_ADDR_WIDTH	AXI4 read address channel: Read address signal
axi_arlen_i	In	8	AXI4 read address channel: Burst length signal Supports up to burst length 64 only, it is prohibited to issue more than this
axi_arsize_i	In	3	AXI4 read address channel: Burst size signal
axi_arburst_i	In	2	AXI4 read address channel: Burst type signal Only INCR is supported
axi_arqos_i	In	4	AXI4 read address channel: Quality of service signal This signal is currently unused
axi_arvalid_i	In	1	AXI4 read address channel: Read address valid signal
axi_arready_o	Out	1	AXI4 read address channel: Read address ready signal
axi_rid_o	Out	AXI_ID_WIDTH	AXI4 read data channel: Read ID tag signal
axi_rdata_o[1]	Out	AXI_DATA_WIDTH	AXI4 read data channel: Read data signal
axi_rresp_o	Out	2	AXI4 read data channel: Read response signal
axi_rlast_o	Out	1	AXI4 read data channel: Read last signal
axi_rvalid_o	Out	1	AXI4 read data channel: Read valid signal
axi_rready_i	In	1	AXI4 read data channel: Read ready signal
axi_awid_i	In	AXI_ID_WIDTH	AXI4 write address channel: Write address ID signal
axi_awaddr_i[1]	In	AXI_ADDR_WIDTH	AXI4 write address channel: Write address signal
axi_awlen_i	In	8	AXI4 write address channel: Burst length signal
axi_awsize_i	In	3	AXI4 write address channel: Burst size signal
axi_awburst_i	In	2	AXI4 write address channel: Burst type signal
axi_awqos_i	In	4	AXI4 write address channel: Quality of service signal
axi_awvalid_i	In	1	AXI4 write address channel: Write address valid signal
axi_awready_o	Out	1	AXI4 write address channel: Write address ready signal
axi_wdata_i[1]	In	AXI_DATA_WIDTH	AXI4 write data channel: Write data signal
axi_wstrb_i	In	AXI_STRB_WIDTH	AXI4 write data channel: Write strobe signal
axi_wlast_i	In	1	AXI4 write data channel: Write last signal
axi_wvalid_i	In	1	AXI4 write data channel: Write valid signal
axi_wready_o	Out	1	AXI4 write data channel: Write ready signal
axi_bid_o	Out	AXI_ID_WIDTH	AXI4 write response channel: Response ID tag signal
axi_bresp_o	Out	2	AXI4 write response channel: Write response signal
axi_bvalid_o	Out	1	AXI4 write response channel: Write response valid signal
axi_bready_i	In	1	AXI4 write response channel: Response ready signal

Notes:

1. The bit width of axi_araddr_i/axi_rdata_o/axi_awaddr_i/axi_wdata_i is calculated based on the *DDR density* and *DDR Bus Width* attributes in Table 3.3. Refer to the Avant DDR Memory PHY Module IP User Guide for the address mapping.

4.1.3. APB Register Interface

The following section describes the configuration interface port when the *Enable APB I/F* attribute is checked in the Memory Controller IP. Refer to the AMBA APB Protocol Specification for a description of these signals.

Table 4.4. DDR4 APB Interface Port Definitions

Port Name	I/O	Width	Description
apb_psel_i	In	1	APB Select signal Indicates that the subordinate device is selected and a data transfer is required
apb_paddr_i	In	12	APB Address signal
apb_pwdata_i	In	32	APB Write data signal Bits [31:8] are not used
apb_pwrite_i	In	1	APB Direction signal 1 = Write, 0 = Read
apb_penable_i	In	1	APB Enable signal Indicates the second and subsequent cycles of an APB transfer
apb_pready_o	Out	1	APB Ready signal Indicates transfer completion. Subordinate uses this signal to extend an APB transfer. Reset value is 1'b0.
apb_pslverr_o	Out	1	APB Error signal Indicates a transfer failure. This signal is tied to 1'b0.
apb_prdata_o	Out	32	APB Read data signal

4.1.4. Memory Interface

The following section describes the interface ports for DDR4 SDRAM.

Table 4.5. DDR4 Interface Port Definitions

Port Name	I/O	Width	Description
ddr_ck_o[1]	Out	CK_WIDTH	DDR4 CK signal
ddr_cke_o[1]	Out	CK_WIDTH	DDR4 CKE signal
ddr_cs_o[1]	Out	CS_WIDTH	DDR4 CS signal
ddr_ca_o	Out	CA_WIDTH	DDR4 CA signal
ddr_we_n_o	Out	1	DDR4 WE signal
ddr_cas_n_o	Out	1	DDR4 CAS signal
ddr_ras_n_o	Out	1	DDR4 RAS signal
ddr_act_n_o	Out	1	DDR4 ACT_n signal
ddr_ba_o	Out	BANK_WIDTH	DDR4 BA signal
ddr_bg_o	Out	BG_WIDTH	DDR4 BG signal
ddr_odt_o	Out	ODT_WIDTH	DDR4 ODT signal
ddr_reset_n_o	Out	1	Memory reset signal
ddr_dq_io[1]	In/Out	BUS_WIDTH	DDR4 DQ signal
ddr_dqs_io[1]	In/Out	DQS_WIDTH	DDR4 DQS signal
ddr_dmi_io[1]	In/Out	DQS_WIDTH	DDR4 DMI signal

Notes:

1. The bit width of SDRAM Memory Interface signals is defined based on the attributes listed in Table 3.3.

4.2. LPDDR4

The following section describes the signals available in LPDDR4 mode.

4.2.1. Clock and Reset

The following section describes the interface ports for clock and reset in the Memory Controller IP.

Table 4.6. LPDDR4 Clock and Reset Port Definitions

Port Name	I/O	Width	Description
pll_refclk_i	In	1	PLL reference clock input
pll_rst_n_i	In	1	PLL reset active low
pclk_i	In	1	Clock for APB interface, training CPU and control logic of the internal PLL. This clock is independent of sclk_o, since sclk_o stops during clock frequency changes.
preset_n_i	In	1	Asynchronous active low reset for APB interface. This reset must be de-asserted synchronous to pclk_i.
aclk_i	In	1	Clock for AXI4 interface
sclk_o	Out	1	System clock. This is ¼ of the DDR clock frequency and is the main clock of the Memory Controller IP.
rst_n_i	In	1	Asynchronous active low reset. When asserted, output ports and registers are forced to their reset values. The Memory Controller IP implements logic to de-assert the internal reset synchronous to the internal clocks after rst_n_i de-asserts.
reset_n_i	In	1	Asynchronous active low reset for AXI4 I/F. This reset must be de-asserted synchronous to aclk_i. This is only available when *Enable Local Bus Clock* attribute is checked.

4.2.2. Interrupts and Initialization/Training

The following section describes the interface ports for interrupts and initialization/training control in the Memory Controller IP.

Table 4.7. LPDDR4 Interrupts and Initialization/Training Port Definitions

Port Name	I/O	Width	Description
irq_o	Out	1	Interrupt signal Reset value is 1'b0
init_start_i	In	1	Starts the memory initialization and training according to trn_opr_i. This signal is available when *Enable APB I/F* attribute is unchecked.
init_done_o	Out	1	Indicates completion of initialization and training and the memory is available for access through the data interface.
pll_lock_o	Out	1	PLL lock output indicating when PLL is locked
trn_err_o	Out	1	Indicates memory training has failed when asserted (1'b1)

4.2.3. AXI4 Data Interface

The following section describes the AXI4 data interface ports in the Memory Controller IP. Refer to the AMBA AXI Protocol Specification for a description of these signals. The transactions allowed on the AXI4 interface to the Memory Controller are described in Table 2.2.

Table 4.8. LPDDR4 AXI4 Interface Port Definitions

Port Name	I/O	Width	Description
axi_arid_i	In	AXI_ID_WIDTH	AXI4 read address channel: Read address ID signal
axi_araddr_i[1]	In	AXI_ADDR_WIDTH	AXI4 read address channel: Read address signal
axi_arlen_i	In	8	AXI4 read address channel: Burst length signal Supports up to burst length 64 only, it is prohibited to issue more than this
axi_arsize_i	In	3	AXI4 read address channel: Burst size signal
axi_arburst_i	In	2	AXI4 read address channel: Burst type signal Only INCR is supported
axi_arqos_i	In	4	AXI4 read address channel: Quality of service signal This signal is currently unused
axi_arvalid_i	In	1	AXI4 read address channel: Read address valid signal
axi_arready_o	Out	1	AXI4 read address channel: Read address ready signal
axi_rid_o	Out	AXI_ID_WIDTH	AXI4 read data channel: Read ID tag signal
axi_rdata_o[1]	Out	AXI_DATA_WIDTH	AXI4 read data channel: Read data signal
axi_rresp_o	Out	2	AXI4 read data channel: Read response signal
axi_rlast_o	Out	1	AXI4 read data channel: Read last signal
axi_rvalid_o	Out	1	AXI4 read data channel: Read valid signal
axi_rready_i	In	1	AXI4 read data channel: Read ready signal
axi_awid_i	In	AXI_ID_WIDTH	AXI4 write address channel: Write address ID signal
axi_awaddr_i[1]	In	AXI_ADDR_WIDTH	AXI4 write address channel: Write address signal
axi_awlen_i	In	8	AXI4 write address channel: Burst length signal
axi_awsize_i	In	3	AXI4 write address channel: Burst size signal
axi_awburst_i	In	2	AXI4 write address channel: Burst type signal
axi_awqos_i	In	4	AXI4 write address channel: Quality of service signal
axi_awvalid_i	In	1	AXI4 write address channel: Write address valid signal
axi_awready_o	Out	1	AXI4 write address channel: Write address ready signal
axi_wdata_i[1]	In	AXI_DATA_WIDTH	AXI4 write data channel: Write data signal
axi_wstrb_i	In	AXI_STRB_WIDTH	AXI4 write data channel: Write strobe signal
axi_wlast_i	In	1	AXI4 write data channel: Write last signal
axi_wvalid_i	In	1	AXI4 write data channel: Write valid signal
axi_wready_o	Out	1	AXI4 write data channel: Write ready signal
axi_bid_o	Out	AXI_ID_WIDTH	AXI4 write response channel: Response ID tag signal
axi_bresp_o	Out	2	AXI4 write response channel: Write response signal
axi_bvalid_o	Out	1	AXI4 write response channel: Write response valid signal
axi_bready_i	In	1	AXI4 write response channel: Response ready signal

Notes:

1. The bit width of axi_araddr_i/axi_rdata_o/axi_awaddr_i/axi_wdata_i is calculated based on the *DDR density* and *DDR Bus Width* attributes in Table 3.12. Refer to the Avant DDR Memory PHY Module IP User Guide for the address mapping.

4.2.4. APB Register Interface

The following section describes the configuration interface port when the *Enable APB I/F* attribute is checked in the Memory Controller IP. Refer to the AMBA APB Protocol Specification for a description of these signals.

Table 4.9. LPDDR4 APB Interface Port Definitions

Port Name	I/O	Width	Description
apb_psel_i	In	1	APB Select signal Indicates that the subordinate device is selected and a data transfer is required
apb_paddr_i	In	12	APB Address signal
apb_pwdata_i	In	32	APB Write data signal Bits [31:8] are not used
apb_pwrite_i	In	1	APB Direction signal 1 = Write, 0 = Read
apb_penable_i	In	1	APB Enable signal Indicates the second and subsequent cycles of an APB transfer
apb_pready_o	Out	1	APB Ready signal Indicates transfer completion. Subordinate uses this signal to extend an APB transfer. Reset value is 1'b0.
apb_pslverr_o	Out	1	APB Error signal Indicates a transfer failure. This signal is tied to 1'b0.
apb_prdata_o	Out	32	APB Read data signal

4.2.5. Memory Interface

The following section describes the interface ports for LPDDR4 SDRAM.

Table 4.10. LPDDR4 Interface Port Definitions

Port Name	I/O	Width	Description
ddr_ck_o[1]	Out	CK_WIDTH	LPDDR4 CK signal
ddr_cke_o[1]	Out	CK_WIDTH	LPDDR4 CKE signal
ddr_cs_o[1]	Out	CS_WIDTH	LPDDR4 CS signal
ddr_ca_o	Out	6	LPDDR4 CA signal
ddr_reset_n_o	Out	1	Memory reset signal
ddr_dq_io[1]	In/Out	BUS_WIDTH	LPDDR4 DQ signal
ddr_dqs_io[1]	In/Out	DQS_WIDTH	LPDDR4 DQS signal
ddr_dmi_io[1]	In/Out	DQS_WIDTH	LPDDR4 DMI signal

Notes:

1. The bit width of SDRAM Memory Interface signals is defined based on the attributes listed in Table 3.12.

5. Register Description

The Memory Controller IP contains user accessible registers. For a description of these registers, refer to the Avant DDR Memory PHY Module IP User Guide.

6. Memory Controller Example Design

This section describes the Memory Controller Example Design that is available to users for synthesis and simulation after successful IP generation.

6.1. Overview

The following table summarizes the IP parameter configurations that are reflected in the Memory Controller Example Design. For steps on how to generate the Memory Controller IP Core, refer to the Designing and Simulating the IP section of this User Guide.

Table 6.1. Supported Example Design Configurations

Attribute	Supported Setting
I/O Buffer Type	All
DDR Command Frequency	All
Enable Power Down	Checked, Unchecked
Enable DBI	Checked, Unchecked
PLL Reference Clock from Pin	Checked, Unchecked
DDR Bus Width	16, 32, 64
Local Data Bus Type	AXI4
ID Width	All
Number of Outstanding Writes/Reads	All
Write/Read Ordering Queues	All
Enable Local Bus Clock	Checked, Unchecked
Enable APB I/F	Checked, Unchecked
Memory Device Timing Tab[1]	All
Training Settings Tab[1]	All

Notes:

1. *DDR Clock Delay Value* and *Address Control Delay Value* are not supported/reflected in Memory Controller Simulation Example Design. All other configurable attributes are supported in the Memory Controller Example Design

6.2. Synthesis Example Design

After successful generation of the Memory Controller IP Core for Avant Devices, a synthesizable example design becomes available to users. This design contains a test program that allows users to evaluate the Memory Controller IP on hardware. Figure 6.1 represents a block diagram of the Memory Controller Example Design.

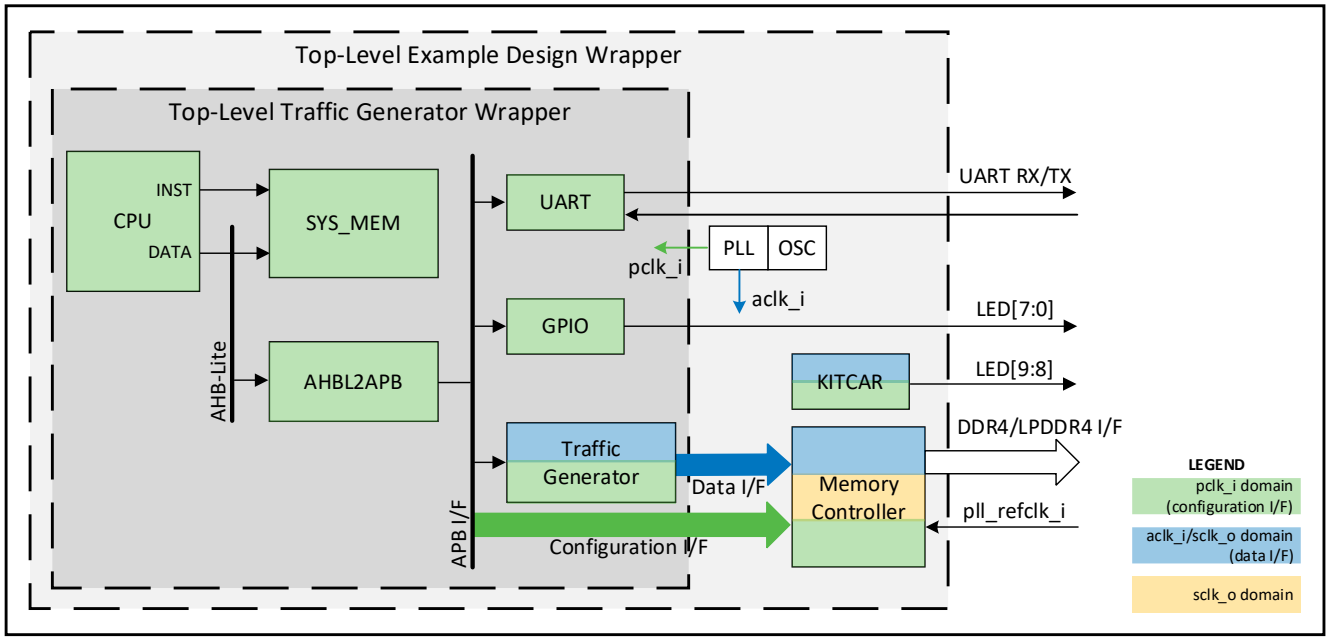

Figure 6.1. Synthesis Example Design

The main blocks that make up the synthesizable example design include the following:

- RISC-V CPU subsystem – handles initialization and training of the DDR4/LPDDR4 interface and performs data access checks.
- System Memory (SYS_MEM) – stores the instruction code for the example design test program.
- AHBL2APB bridge – converts the CPU data interface (AHB-Lite) to the configuration interface (APB).
- UART block – allows users to interface with the test program and prints out results via a serial terminal connection.
- GPIO block – allows users to verify the result of DDR4/LPDDR4 training sequences and the functionality of pclk_i and aclk_i clock signals.
- Traffic generator block – implements a series of pseudo-random (PRBS) writes and reads, and compares the read data to the expected data, displaying the result over a UART connection.
- Memory Controller IP – provides an interface to external DDR4/LPDDR4 memory to issue reads and writes.
- Oscillator (OSC) – generates a 90 MHz clock for the configuration interface (pclk_i).
- PLL – takes the oscillator output as an input reference clock to the PLL. The PLL generates both the configuration interface clock (pclk_i) and the user data interface AXI clock (aclk_i).

The synthesizable example design consists of a test program that is stored in system memory and is fetched by the CPU instruction port. The CPU data port accesses system memory and connects to the following: Configuration Set Registers (CSRs), UART, GPIO, traffic generator and Memory Controller. The test program associated with the example design performs the following:

- Waits for user input over a serial terminal connection upon the assertion of the reset signal: rstn_i
- Configures the Memory Controller to perform complete reset, initialization, and training (TRN_OP_REG=0x1DF) of the DDR4/LPDDR4 interface.
- Performs a series of loop-back data access checks
- Calculates performance of the DDR4/LPDDR4 interface

The top-level example design wrapper file, eval_top.sv, provides ports for a PLL reference clock, DDR4/LPDDR4 interface, UART interface, and a 10-bit LED output. LED[7:0] corresponds to bits STATUS_REG[8:1], whereas toggling on LED[8] signifies aclk_i is functioning and toggling on LED[9] signifies pclk_i is functioning. For information on the example design test program and instructions on how to generate and perform hardware evaluation of the Memory Controller Example Design, refer to the Designing and Simulating the IP section of this User Guide.

6.3. Simulation Example Design

The simulation example design is similar to the synthesizable example design, apart from the following changes:

- Disables UART connection
- External DDR4/LPDDR4 memory is replaced with DDR4/LPDDR4 memory model

The UART connection is disabled in simulation since it takes a long time to simulate and the DDR4/LPDDR4 memory model allows simulation of user-initiated operations to DDR4/LPDDR4 SDRAM. For instructions on how to simulate the Memory Controller, including the example design, refer to the Designing and Simulating the IP section of this User Guide.

7. Designing and Simulating the IP

This section describes the steps required within Lattice Radiant software to configure and generate the Memory Controller IP Core for Avant Devices. This section also provides information regarding design implementation and hardware evaluation of the synthesizable example design.

7.1. Generating the IP

This section describes the steps required to create, configure, and generate an instance of the Memory Controller IP Core for Avant Devices.

7.1.1. Creating a Radiant Project

In order to generate an instance of the Memory Controller IP, a Lattice Radiant project must first be created.

1. Launch the Lattice Radiant software and select **File > New > Project**. This will open the **New Project** dialog box. Click **Next**.

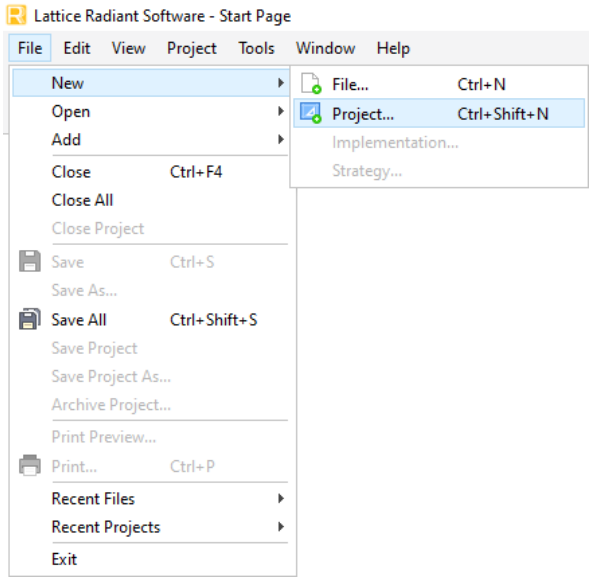

Figure 7.1. Creating a New Radiant Project

2. Specify a name (<project_name>) for the Lattice Radiant project, a directory (<project_directory>) to store the project files, and a top-level design implementation name (<top_level_instance_name>). Click **Next** two times.

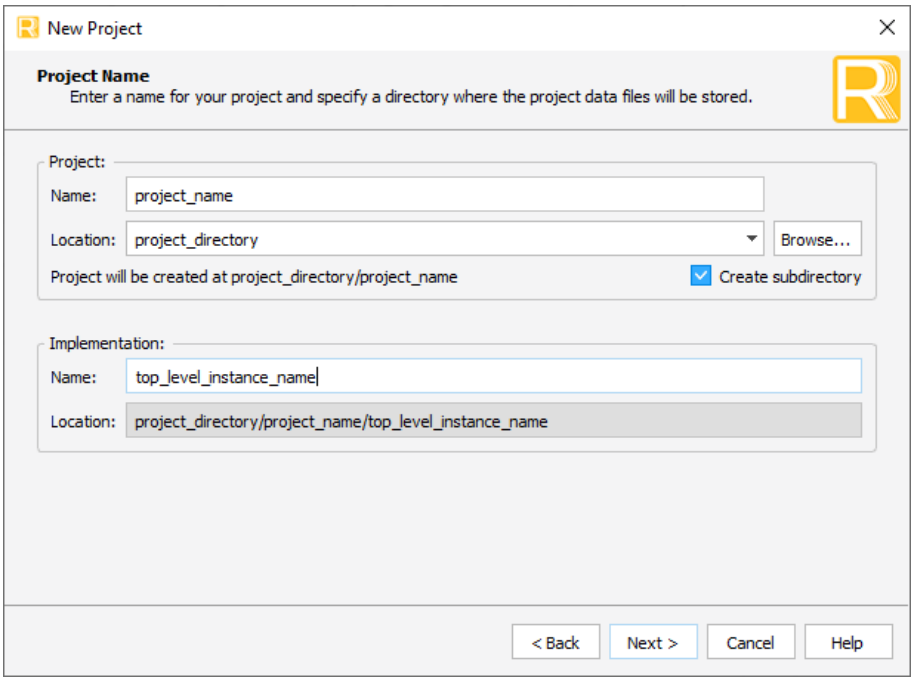

Figure 7.2. New Project Settings

3. Under **Family**, select Avant. Under **Device, Package, Operating Condition, and Performance Grade**, make the appropriate selections representative of the selected device part number. Click **Next**.

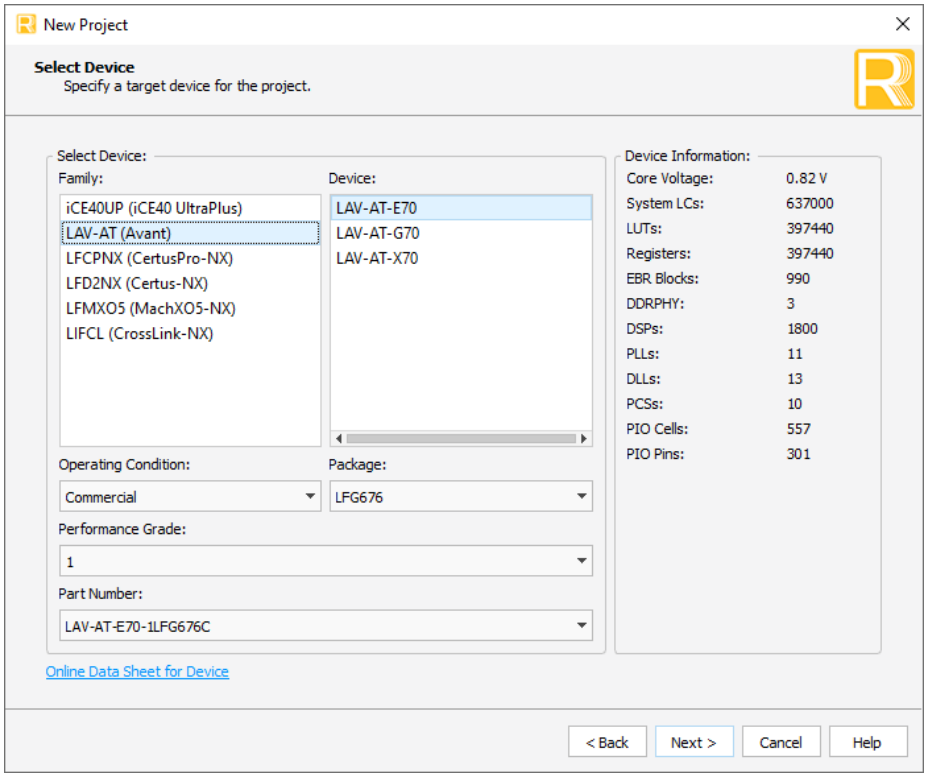

Figure 7.3. Project Device Settings

4. Specify the desired synthesis tool for implementation of the Lattice Radiant project. Click **Next** and **Finish**.

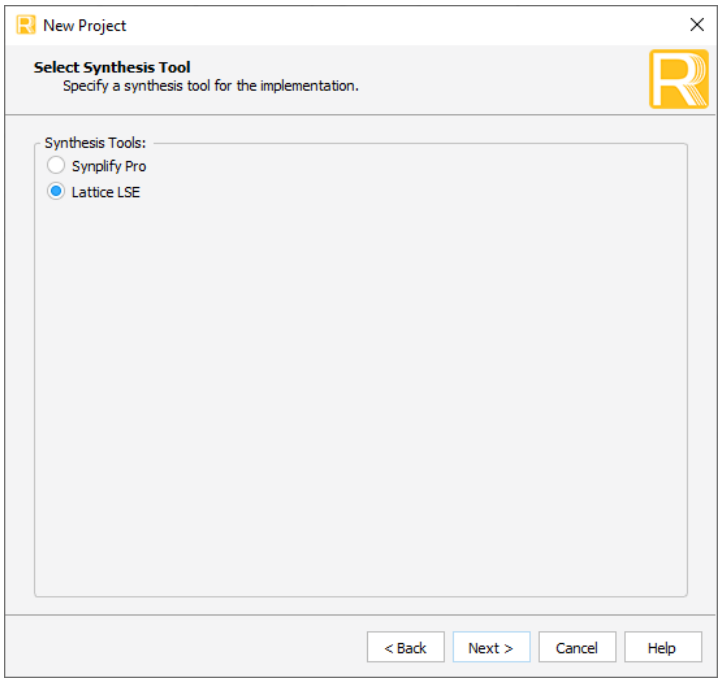

Figure 7.4. Project Synthesis Tool Selection

7.1.2. Configuring and Generating the IP

The following steps illustrate how to generate the Memory Controller IP Core in Lattice Radiant software.

1. Under the **IP Catalog** (Tools > IP Catalog), locate and double-click on the desired Memory Controller IP listed under **IP > Processors_Controllers_and_Peripherals**.
    a. If no Memory Controller IPs are installed on the system, select the **IP on Server** tab within the IP Catalog.
    b. Click on **Download from Lattice IP Server** icon next to the desired Memory Controller IP for installation. This will open an **IP License Agreement** dialog box.
    c. Click **Accept** and then click on the **Refresh IP Catalog** icon.
    d. Locate the installed Memory Controller IP under the **IP on Local** tab within the IP Catalog and double-click.
        - IP Core v1.x.x = Memory Controller for Avant Devices (LPDDR4 mode)
        - IP Core v2.x.x = Memory Controller for Avant Devices (DDR4 mode)
2. The **Module/IP Block Wizard** dialog box will open. Provide a name (<instance_name>) and directory (<instance_directory>) for the Memory Controller IP, where the default directory is set to <project_directory>/<project_name>. Click **Next**.

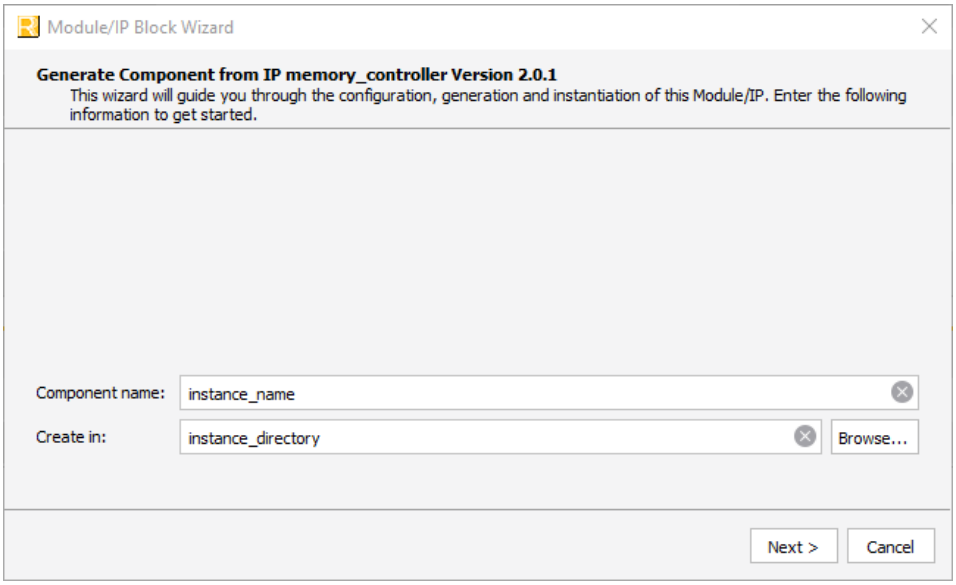

Figure 7.5. IP Instance Settings

3. The Memory Controller IP editor contains multiple tabs that needs to be configured according to the desired DDR4/LPDDR4 memory interface implementation. The following table provides high-level guidance for configuring the tabs in the Memory Controller IP editor. For detailed information on the individual attributes, refer to the IP Parameter Description section of this User Guide.

Table 7.1. Memory Controller Attribute Guidelines

Memory Controller IP Attribute Tab	Guidelines1
DDR4	
General	- Ensure that the Memory clock frequency (*DDR Command Frequency*) is entered correctly
Memory Device Timing	- Refer to the datasheet for the selected DDR4/LPDDR4 memory device to modify the default timing parameters as needed - DDR Clock Delay (in DDR4 mode) should only be modified if an error has occurred during write leveling
LPDDR4	
General	- Ensure that the Memory clock frequency *(DDR Command Frequency)* is entered correctly
Memory Device Timing	- Refer to the datasheet for the selected DDR4/LPDDR4 memory device to modify the default timing parameters as needed
Training Settings	- DDR Clock Delay should only be modified if an error has occurred during write leveling - Address Control Clock Delay should only be modified if an error has occurred during command bus training

4. Click **Generate**. The **Check Generating Result** dialog box opens, showing design block messages and results as shown in Figure 7.6. Click **Finish**.

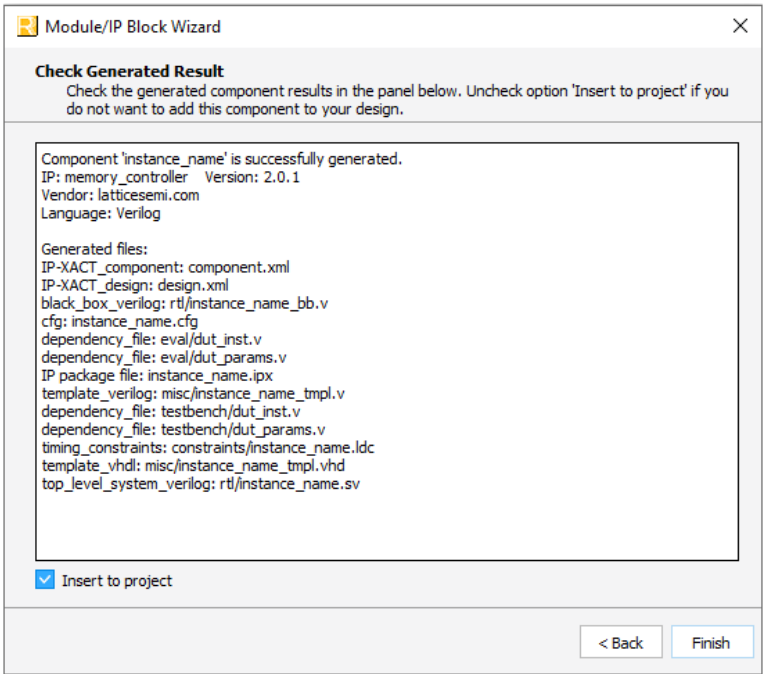

Figure 7.6. IP Generation Result

5. All the generated files are placed under the <instance_directory>/<instance_name> directory path. The generated files under the <instance_directory>/<instance_name> directory are listed in the following table.

Table 7.2. Generated File List

File Name	Description
component.xml	Contains the ipxact:component information of the IP
design.xml	Lists the set parameters of the IP in IP-XACT 2014 format
<instance_name>.cfg	Lists only the configured/changed parameter values set during IP configuration
<instance_name>.ipx	Lists the files associated with IP generation
constraints/<instance_name>.ldc	Defines the I/O standard for DDR4/LPDDR4 memory interface signals
eval/apb2init.sv	Implements handshaking between APB accesses and internal RISC-V CPU for initialization of DDR4/LPDDR4 memory in Memory Controller Example Design
eval/clock_constraint.sdc	Pre-synthesis constraint for setting the PLL reference clock frequency of the Memory Controller Example Design
eval/constraint.pdc	Post-synthesis constraints for the Memory Controller Example Design
eval/dut_inst.v	Instantiation of generated IP core in eval_top.sv for Memory Controller Example Design
eval/dut_params.v	Defines local parameters for eval_top based on parameter values set during IP configuration for Memory Controller Example Design
eval/eval_top.sv	Top-level RTL file for the Memory Controller Example Design
eval/kitcar.v	Counter that drives LEDs to indicate that internal clocks (pclk and aclk_i) are active in Memory Controller Example Design
eval/pll0.v	PLL responsible for generating APB clock (pclk) and AXI4 (aclk_i) in Memory Controller Example Design
eval/select_protocol.py	Script that defines DDR4/LPDDR4 protocol for eval_top and tb_top files in Memory Controller Example Design

File Name	Description
eval/axi_bridge/	Contains RTL for AXI bus interface to Native I/F
eval/traffic_gen/	Contains RTL files for the Memory Controller Example Design
misc/<instance_name>_tmpl.v misc/<instance_name>_tmpl.vhd	These files provide instance templates for the IP core
rtl/<instance_name>.sv	Example RTL top-level file that instantiates the IP core
rtl/<instance_name>_bb.v	Example synthesizable RTL black box file that instantiates the IP core
testbench/debug_c_code.sv	For internal use only
testbench/dut_inst.v	Template instance files
testbench/dut_params.v	List of parameters based on user IP configurations
testbench/tb_top.sv	Top level testbench file
testbench/ddr4/	Contains DDR4/LPDDR4 memory model and instances for simulation
testbench/lpddr4/	

7.2. Design Implementation

This section describes the steps required to properly run a Memory Controller for Avant IP design on hardware.

7.2.1. Pin Placement

Typically, all external memory interfaces require the following FPGA resources:

- Data, data mask, and data strobe signals
- Command, address, and control signals
- PLL and clock network signals
- RZQ and VREF signals
- Other FPGA resources

In Lattice Avant FPGA devices, external memory interfaces are supported in the DDRPHY, where each DDRPHY is composed of 3 High Performance I/O (HPIO) banks. These banks are labeled as HIGHSPEED in the device pinout tables. Since Avant leverages a hardened PHY, the external memory interface pinouts are in fixed locations. Where each pin location is specified under DDRPHY in the device pinout tables. Dedicated clock routing within HPIO banks is represented as PLL or PCLK, and dedicated reference voltage pins are represented as VREF, in the device pinout tables. Refer to the High-Speed I/O User Guide and Pinout files located on the Avant-AT-E/G/X web pages on www.latticesemi.com for more information.

Observe the following guidelines when placing pins for external memory interfaces:

- Ensure that pins for external memory interfaces reside within a DDRPHY.
- The input reference clock to the PLL must be assigned to use dedicated clock routing (PLL or PCLK). It is recommended to place the input reference clock on a dedicated PLL pin (PLL) within the HPIO bank for better performance and to minimize jitter and routing.
- At least one VREF pin per HPIO bank that is used to implement an external memory interface, must be available and used as a reference voltage input. Internal VREF is supported for DDR4 and LPDDR4 interfaces, as a result, the pins labeled as VREF in the device pinout tables can be used for DQ/DM signal placement.

Proposed pinouts should always be tested in Lattice Radiant software with correct I/O standards before finalizing.

7.2.2. Constraints

To ensure proper design coverage and hardware functionality, users must include the following necessary constraints in their Memory Controller for Avant IP project.

Table 7.3. Project Constraints

File Name	Description	Action Required
Memory Controller IP LDC file: constraints/<instance_name>.ldc	Sets the I/O type for each of the ports necessary to interface with DDR4/LPDDR4 SDRAM	No
Clock Constraint SDC file: eval/clock_constraint.sdc	Contains an example constraint for the input PLL reference clock	Yes – user needs to include a create_clock constraint based on the frequency for the input PLL reference clock. This can be placed in a user-created SDC or PDC file.
Memory Controller IP PDC file: eval/constraint.pdc	Contains generated constraints based on IP configuration	Yes – user needs to copy the constraints listed in this file directly into their top-level PDC file. An explanation for each group of constraints to be copied is included within the eval/constraint.pdc file.

7.2.2.1. Clock

The provided clock_constraint.sdc file contains a single create_clock constraint for the PLL reference clock (pll_refclk_i). It is recommended that users copy this constraint into their own SDC or PDC file since the provided clock_constraint.sdc file will be overwritten every time the Memory Controller IP Core is regenerated.

For clocks that are generated from the user's design, external to the IP, create_generated_clock constraints may be needed. In some cases, clocks or generated clocks don't need to be defined/constrained since they are automatically-generated (i.e. for output of PLL or OSC). For additional information on how to implement constraints, refer to the Lattice Radiant Timing Constraints Methodology User Guide.

7.2.2.2. Memory Controller IP

The provided constraint.pdc file contains two sets of constraints:

- IP constraints – specific to the Memory Controller IP Core
- Eval constraints – specific to the Memory Controller Example Design

For implementation of the generated Memory Controller Example Design, users need to copy the IP and Eval constraints into their top-level user PDC file. However, if users are implementing their own Memory Controller design, only the IP constraints need to be copied into the top-level user PDC file. It is recommended that users copy these constraints into their own PDC file since the provided constraint.pdc file will be overwritten everytime the Memory Controller IP Core is regenerated.

The IP constraints are composed of create_generated_clock, set_false_path, ldc_create_group, and set_max_delay constraints. The eval constraints are composed of set_false_path, set_max_delay, and ldc_create_group constraints and should only be copied if running the provided Memory Controller Example Design. Eval constraints are located below the following comment in the provided constraint.pdc file:

```
 ##############################################################################
# Below are the constraints for eval design, you dont need these if you are not using the
eval
```

Refer to the Lattice Radiant Timing Constraints Methodology User Guide for details regarding the implementation of constraints.

7.3. Example Design Hardware Evaluation

After successfully configuring and generating the Memory Controller IP Core, the included synthesis example design can be used for hardware evaluation of the Memory Controller. For a detailed description of the Memory Controller Example Design, refer to the Synthesis Example Design section of this User Guide. The traffic generator fileset is located under the eval/traffic_gen directory and are described in the following table.

Table 7.4. Contents of eval/traffic_gen

File List	Description
ahbl0.v	AHBL_1x2. It routes CPU data access to SYS_MEM or AHBL2APB
ahbl2apb0.v	AHBL to APB bridge
apb0.v	APB_1x4. It routes CPU data access via AHBL2APB going to each module's CSR
cpu0.v	RISC-V CPU
gpio0.v	GPIO module
ctrl_fifo.v	RTL files for AXI4 traffic generator
lscc_axi4_traffic_gen.sv	
lscc_axi4_m_csr.sv	
lscc_axi4_m_rd.sv	
lscc_axi4_m_wr.sv	
lscc_axi4_perf_calc.sv	
lscc_lfsr.v	
mc_axi4_traffic_gen.v	
lscc_osc.v	RTL files for OSC module
osc0.v	
lscc_ram_dp_true.v	Copy of Lattice Radiant RAM_DP_True Foundational IP (needed by SYS_MEM)
memc_apb.v	RTL file for APB configuration interface
sysmem0.v	The SYS_MEM for hardware validation, enabled when eval_top.SIM=0 (Implementation)
uart0.v	The UART module

7.3.1. Preparing the Bitstream

After configuring and generating the Memory Controller IP Core, all associated example design files would have been created under the eval directory. Refer to Table 7.2 for more details. The following steps illustrate how to prepare the Memory Controller Example Design project and generate the associated bitstream.

1. After generating the Memory Controller IP Core, the Radiant project should contain the <instance_name>.ipx under the project's input files. If not, right-click on **Input Files** and select **Add > Existing File** under the **File List** tab in the lower-left corner of the Radiant window. This will open an **Add Existing File** dialog box. Navigate to the <instance_directory>/<instance_name> directory and select the <instance_name>.ipx file. Click **Add**.
2. To add the top-level example design file to the project, right-click on **Input Files** and select **Add > Existing File**. This will open an **Add Existing File** dialog box. Navigate to the eval directory and select the eval_top.sv file. Click **Add**.

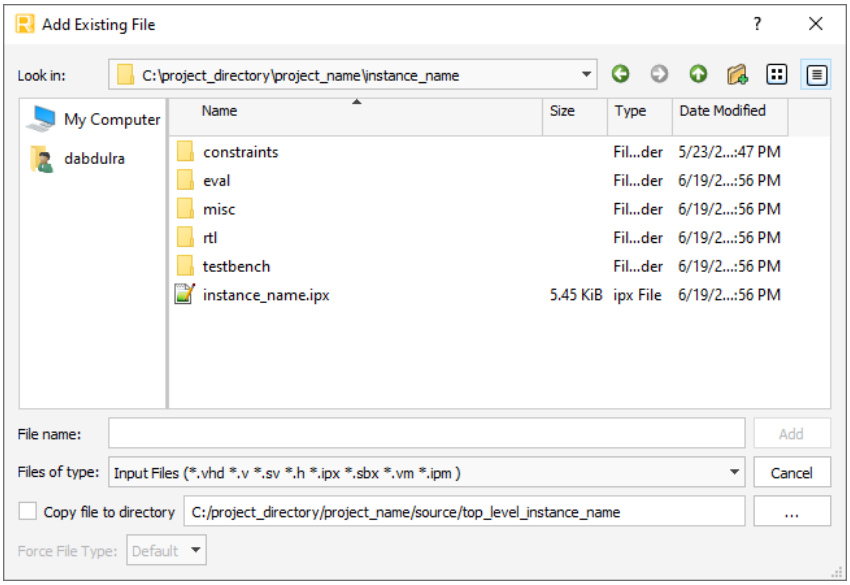

Figure 7.7. Add Existing File Dialog Box

3. To add the pre-synthesis constraint file to the project, right-click on **Pre-Synthesis Constraint Files** and select **Add > Existing File**. In the **Add Existing File** dialog box, check the **Copy file to directory** option. This ensures any user modifications is not overwritten when the Memory Controller IP Core is regenerated. Navigate to the eval directory and select the clock_constraint.sdc file. Click **Add**.
4. To add the post-synthesis constraint file to the project, right-click on **Post-Synthesis Constraint Files** and select **Add > Existing File**. In the **Add Existing File** dialog box, check the **Copy file to directory** option. Navigate to the eval directory and select the constraint.pdc file. Click **Add**.
5. Modify the constraint.pdc to add the pin assignment for the Avant-AT-E/G/X board. Users can accomplish this by either modifying the constraint.pdc file directly or first synthesizing the Radiant project by clicking on the Synthesize Design button, and then adding pinouts via the Device Constraint Editor under **Tools > Device Constraint Editor**. Note that when assigning the UART pins, the UART TX signal is connected to the UART RX on the FPGA side and that the UART RX signal is connected to the UART TX signal on the FPGA side.
6. Before running the example design on hardware, a bitstream needs to be generated. This can be accomplished by clicking on the button. This will generate a <project_name>_<top_level_instance_name>.bit file under the <project_directory>/<project_name>/<top_level_instance_name> directory specified in Step 2.

Users may sometimes encounter timing failures during Place & Route due to unconstrained paths specific to their design. For details on implementing constraints, refer to the Constraints section of this User Guide.

7.3.2. Running on Hardware

To perform hardware evaluation of the Memory Controller Example Design, the following are needed:

- Avant-AT-E/G/X FPGA board with UART connection
- Associated power supply and programming cable
- Personal computer running Lattice Radiant software 2023.1 or later
- Lattice Propel™ software 1.0 or later, or any terminal that supports serial communication

To run the example design on hardware, a bitstream file is required. To generate the .bit file, refer to the Preparing the Bitstream section of this User Guide. The following steps illustrate how to program the FPGA board with the example design.

1. Connect the FPGA board to the computer and power on the board.
2. Run the Lattice Radiant Programmer by clicking on the button. This will launch the Lattice Radiant Programmer which will scan for devices and configure the programmer automatically.

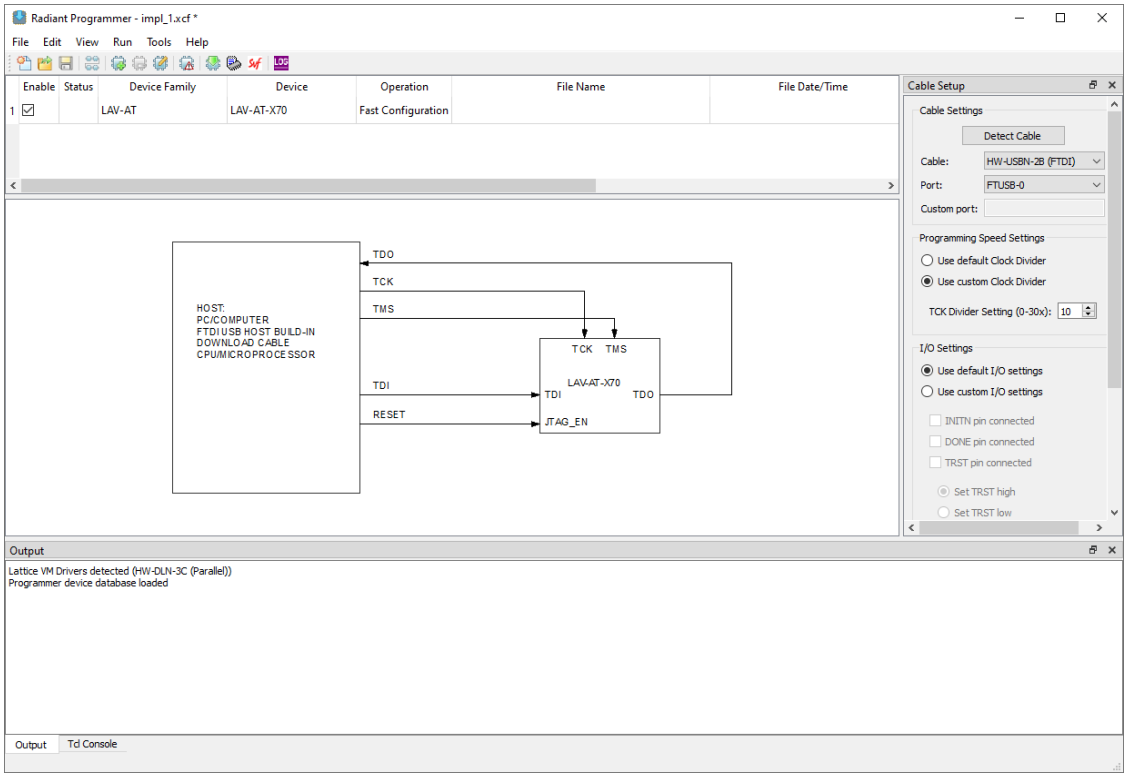

Figure 7.8. Radiant Programmer

3. Click under the **File Name** field and then click on **…** to the right of the field in order to launch the **Open File** dialog box. Navigate to the bitstream file generated in Step 15 and click **Open**.
4. Program the Lattice FPGA device by clicking on the button. Upon successful programming, the **Output** pane at the bottom of the Programmer window will display the following message:
   - After programming the Lattice FPGA with the example design bitstream, a serial terminal needs to be launched. For users wishing to use their own serial communication terminal, skip to Step 25. For users wishing to use the Lattice Propel terminal, continue with Step 23.
5. Launch the Lattice Propel software and select **Launch**. This will open the default workspace.
6. To open a terminal, click on the button.
7. Configure the terminal settings to be a **Serial Terminal** with the appropriate **Baud rate, Data size, Parity, Stop bits, and Encoding**. Click **OK** to launch the **Terminal** pane at the bottom of the Propel window. Note that the **Serial port** will vary depending on the computer setup.

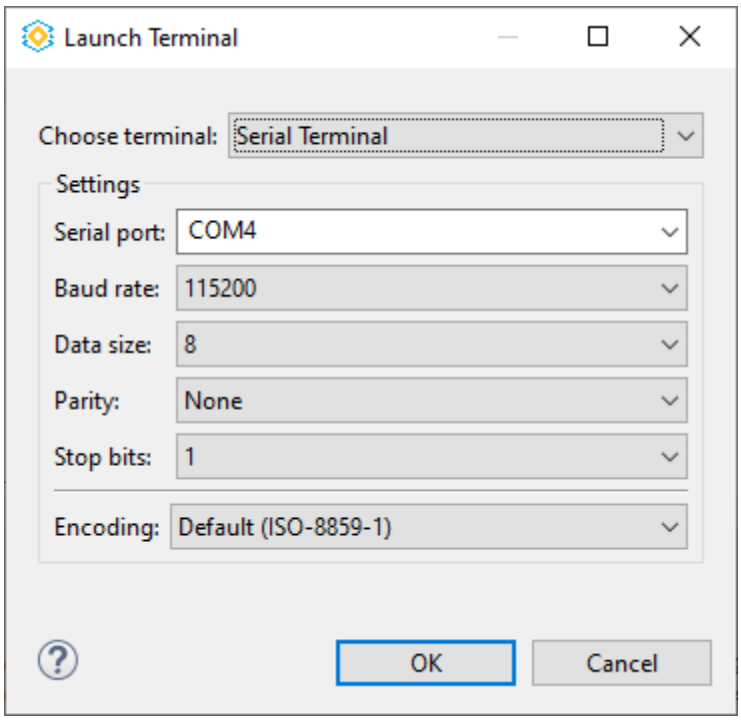

Figure 7.9. Serial Terminal Settings

To run the example design, assert the rstn_i signal. This will prompt the following message to appear in the terminal. If no message is received, close the current serial terminal and open a new one with a different **Serial port**.

```
================================================================
Memory Controller for Avant Devices LPDDR4 Example Design
================================================================
Press any key to proceed training
```

After the user provides input over the serial terminal, training of the DDR4/LPDDR4 SDRAM will begin:

- I: initialization of the DDR4/LPDDR4 SDRAM
- C: command bus training of the DDR4/LPDDR4 SDRAM
- L: write leveling of the DDR4/LPDDR4 SDRAM
- R: read DQ-bit leveling of the DDR4/LPDDR4 SDRAM
- W: write DQ-bit leveling of the DDR4/LPDDR4 SDRAM
- S: self-calibrating logic for read gate training of the DDR4/LPDDR4 SDRAM

Once training completes successfully, 7–10 different data access checks will be executed, depending on the *Maximum Burst Length* attribute:

- Test 1: 2-beat incrementing burst write followed by 10 iterations of burst read
- Test 2: 10 iterations of 2-beat incrementing burst write followed by 10 iterations of burst read
- Test 3: 4-beat incrementing burst write followed by 10 iterations of burst read
- Test 4: 10 iterations of 4-beat incrementing burst write followed by 10 iterations of burst read
- Test 5: 10 iterations of 8-beat incrementing burst write followed by 10 iterations of burst read
- Test 6: 64-beat incrementing parallel burst write and burst read
- Test 7: 128-beat incrementing parallel burst write and burst read
- Test 8: 192-beat incrementing parallel burst write and burst read
- Test 9: 256-beat incrementing parallel burst write and burst read
- Test p: 20k iterations of (64-beat incrementing parallel burst write and burst read) to measure performance

The results from the data access checks and performance measurement are then printed over the serial connection.

```
-----------------------------------------------
        Starting Memory Training
-----------------------------------------------

I
 C
  L
   R
    W
     S
RESULT: Training passed with STATUS_REG_ADDR value: 127
-----------------------------------------------
Starting data access check
-----------------------------------------------
1
 2
  3
   4
    5
     6
      7
       p

The Performance Test measures the throughput of the MC and calculates efficiency via the
calculation as
        Total number of wr_rd transactions  /  Duration of the MC clock (sclk)

-----------------------------------------------
        Starting Performance Test
-----------------------------------------------

BUS EFFICIENCY in %: 79
Performance in Mbps : 31024
Ran : 20000 transactions across fixed address

RESULT : All transaction types have PASSED.
```

The bus efficiency value represents the efficiency percentage of the DDR4/LPDDR4 bus utilization, whereas the performance value represents the bandwidth of the DDR4/LPDDR4 interface.

In the case that a failure is encountered during training, a message will be sent over the serial connection notifying the user of the particular stage that has failed. This will also abort the loop-back data access checks.

```
-------------------------------------------

        Starting Memory Training

-------------------------------------------


I

Command Bus Training Failed
```

7.4. Example Design Simulation

After successfully configuring and generating the Memory Controller IP Core, the included example design can be used to simulate the Memory Controller. All associated simulation files are located under the testbench directory. Refer to Table 7.2 for more details. The following steps illustrate how to prepare the Memory Controller Example Design project for simulation.

1. Before simulating the example design, steps 13-14 under the Preparing the Bitstream section of this User Guide must be completed. To add the top-level testbench file to the project, select **File > Add > Existing Simulation File**. This will open an **Add Existing Simulation File** dialog box. Navigate to the testbench directory and select the tb_top.sv file. Click **Add**.
2. Before creating the simulation environment, it is recommended to set the SIM parameter in eval_top.sv to 1. This parameter shortens the initialization sequence of the DDR4/LPDDR4 interface and disables the UART interface for simulation. Users should not modify the SIM parameter for hardware implementation.

When SIM is set to 1, it programs 0x1E to the Training Operation Register (TRN_OP_REG) to speed up the simulation runtime by reducing the reset and CKE initialization time. Users can configure the simulation of reset and the initialization and training sequences by forcing the value of TRN_OP_REG by locating the following line in tb_top.sv:

```
force `DUT_HIER_PATH.lscc_mc_avant_inst.u_ddrphy.i_csr.trn_operation_reg = 8'h1E;
```

It is also recommended to skip the training sequences (including command bus training) by writing 9’h01C to TRN_OP_REG/trn_opr_i. This will reduce simulation time by programming the verified trained values to the PHY. Refer to the Simulation Example Design section of this User Guide for more details.

To create the simulation environment to simulate the Memory Controller Example Design, the following steps should be taken:

1. Launch the simulation wizard in Radiant by selecting **Tools > Simulation Wizard**. This will open the **Simulation Wizard** dialog box. Click **Next** and provide a name (<sim_name>) and directory (<sim_directory>) for the simulation project, where the default directory is set to <project_directory>/<project_name>. Click **Next**.

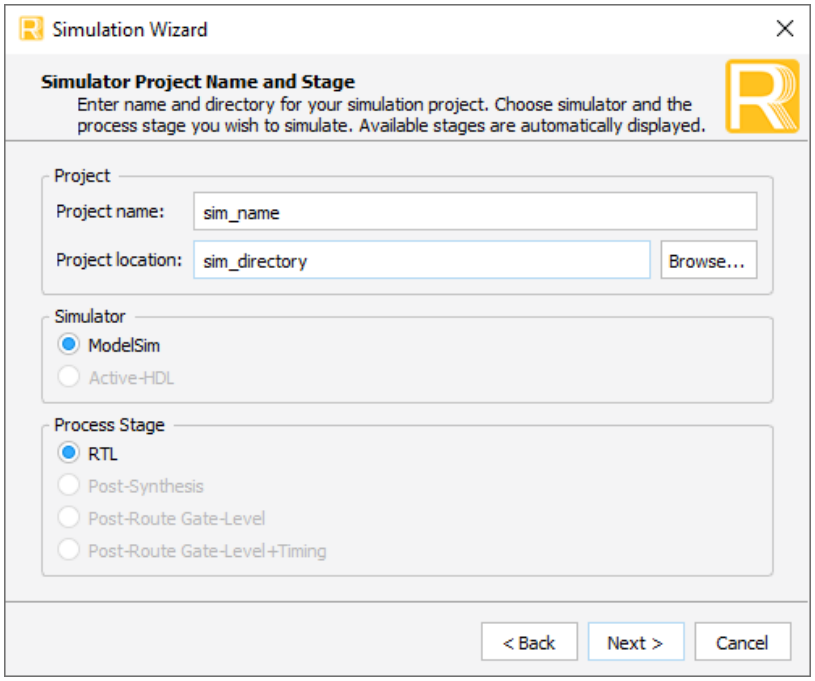

Figure 7.10. Simulation Wizard

2. Under the **Add and Reorder Source** window, notice that the **Source Files** only contains the top-level evaluation (eval_top.sv) and top-level testbench (tb_top.sv) files. Click **Next**.

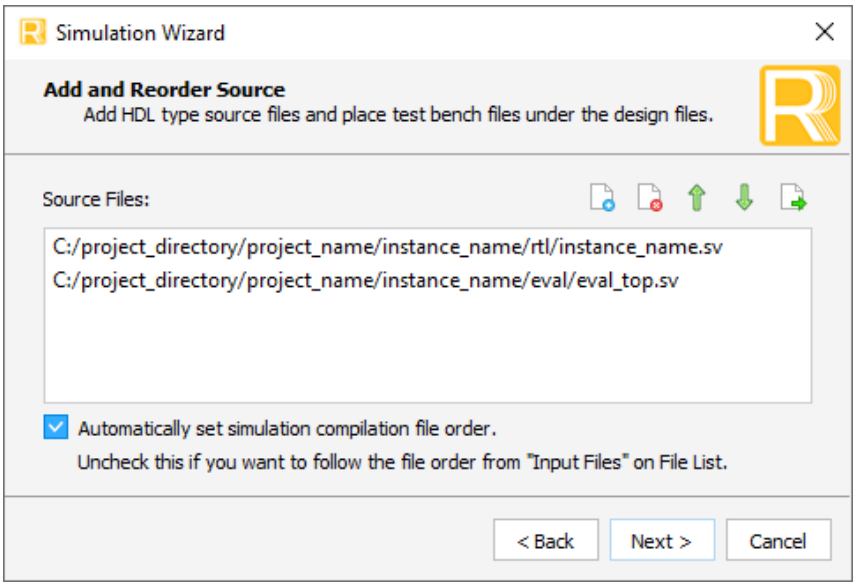

Figure 7.11. Adding and Reordering Simulation Source Files

3. Under the **Parse HDL files for simulation** window, notice that the **Simulation Top Module** is set to eval_top. Click **Next**.

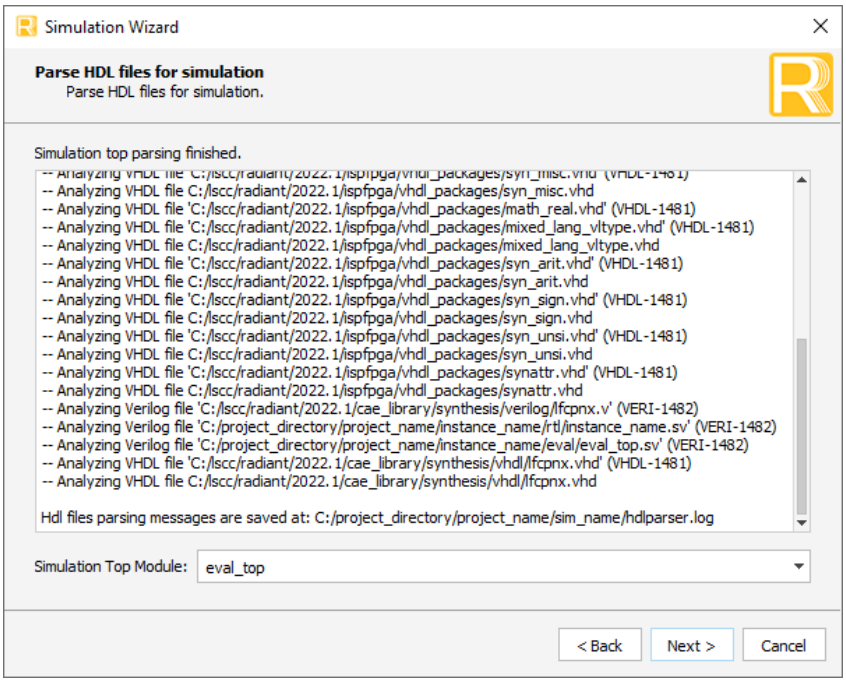

Figure 7.12. Parsing Simulation HDL Files

4. This opens the **Summary** window. By default the simulation will run for 100 µs, which allows users to configure the waveform to log signals of interest in the Modelsim simulator before continuing. Users can then enter the following TCL command in Modelsim to run the simulation until completion: **run -all**. Alternatively, if users wish to run the simulation with the default top-level signals, users can change the 100 µs value to 0 µs in order to execute the simulation completely.

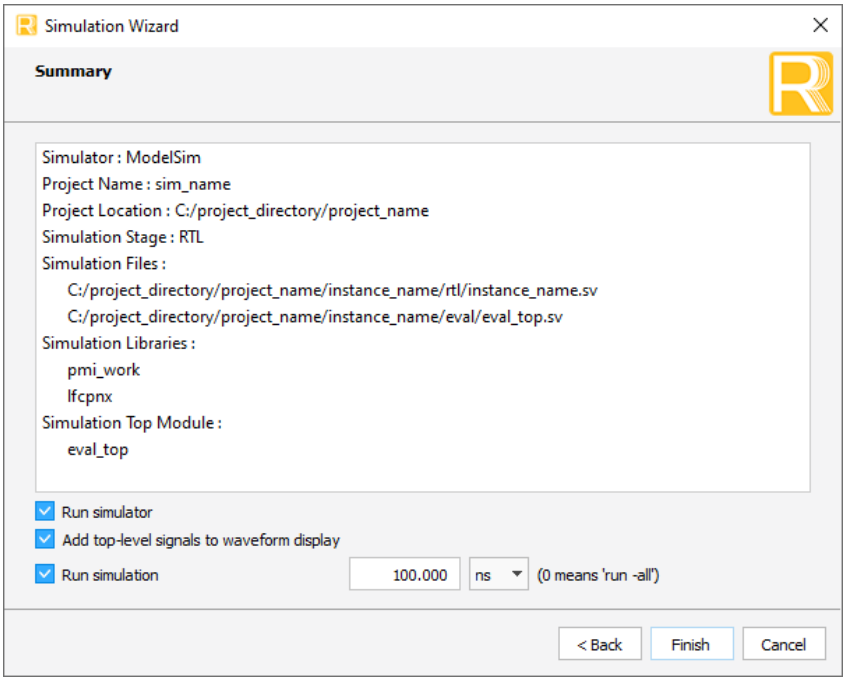

Figure 7.13. Simulation Summary

The results of the Memory Controller IP simulation design are shown in the following figure.

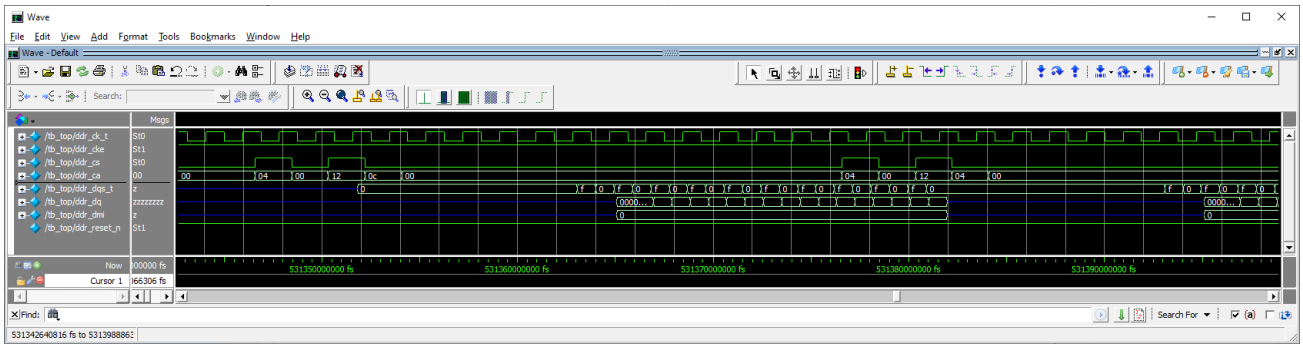

Figure 7.14. Simulation Result Waveform

The following error messages are expected in the Modelsim simulation log and should be disregarded. These messages are due to the violation of timing requirements regarding the DDR4/LPDDR4 simulation model as a consequence of shortening the reset and CKE initialization:

```
# tb_top.LP4MEM_00.mem_x16_00.ins_1ch.<protected> 26083125000 : ###  lpddr4_debug
RESET_n high input
# tb_top.LP4MEM_01.mem_x16_01.ins_1ch.<protected> 26083125000 : ###  lpddr4_debug
RESET_n high input
# Error: tb_top.LP4MEM_01.mem_x16_01.ins_1ch.<protected>.<protected> 26083125000  tINIT1
Error.
# Error: tb_top.LP4MEM_00.mem_x16_00.ins_1ch.<protected>.<protected> 26083125000  tINIT1
Error.
# tb_top.LP4MEM_00.mem_x16_00.ins_1ch.<protected> 32804075000 : ###  lpddr4_debug CKE
high input
# tb_top.LP4MEM_01.mem_x16_01.ins_1ch.<protected> 32804075000 : ###  lpddr4_debug CKE
high input
# Error: tb_top.LP4MEM_01.mem_x16_01.ins_1ch.<protected>.<protected> 32804075000  tINIT3
Error.
# Error: tb_top.LP4MEM_00.mem_x16_00.ins_1ch.<protected>.<protected> 32804075000  tINIT3
Error.
```

Appendix A. Resource Utilization

The following table shows the configuration and resource utilization for LAV-AT-E70-3LFG1156C using Synplify Pro of Lattice Radiant software 2023.2.

Table A.1 DDR4 Resource Utilization for IP Core v2.0.0

Configuration	aclk_i Fmax (MHz)	sclk_o Fmax[1] (MHz)	Registers	LUTs	EBR	DSP
DDR Command Frequency = 1200, Others = Default	426.026	300.120	6529	5392	25	0
DDR Command Frequency = 1200, DDR Bus Width = 16, Others = Default	365.764	300.120	5251	5262	21	0
DDR Command Frequency = 1200, DDR Bus Width = 64, Others = Default	329.381	300.120	9075	5732	33	0
DDR Command Frequency = 1200, DDR Bus Width = 64, Enable Power Down = Checked, Others = Default	369.004	300.120	9185	6346	33	0

Notes:

1. The sclk_o Fmax is generated using the top-level example design wrapper file, eval_top.sv, that is described in the Synthesis Example Design section of this User Guide. These values may increase when the IP Core is used with the user logic.

Table A.2 LPDDR4 Resource Utilization for IP Core v1.3.0

Configuration	aclk_i Fmax (MHz)	sclk_o Fmax[1] (MHz)	Registers	LUTs	EBR	DSP
DDR Command Frequency = 1200, Others = Default	379.219	300.120	7391	5412	25	0
DDR Command Frequency = 1200, DDR Bus Width = 16, Others = Default	378.358	300.120	5723	5180	21	0
DDR Command Frequency = 1200, DDR Bus Width = 64, Others = Default	335.121	300.120	10605	5701	33	0
DDR Command Frequency = 1200, DDR Bus Width = 64, Enable Power Down = Checked, Others = Default	370.508	300.120	10672	5803	33	0

Notes:

1. The sclk_o Fmax is generated using the top-level example design wrapper file, eval_top.sv, that is described in the Synthesis Example Design section of this User Guide. These values may increase when the IP Core is used with the user logic.

References

For more information refer to:

- Avant-E web page
- Avant-G web page
- Avant-X web page
- Lattice Radiant Timing Constraints Methodology User Guide
- Avant DDR Memory PHY Module User Guide
- AMBA AXI Protocol Specification
- AMBA APB Protocol Specification
- DDR4 JEDEC Standard
- LPDDR4 JEDEC Standard
- Lattice Radiant FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.2, December 2023

Section	Change Summary
All	• Changed the document title from *Lattice Avant Memory Controller IP Core - Lattice Radiant Software* to *Memory Controller IP for Avant Devices*. • Reworked document content and structure for clarity.
Acronyms in this document	• Reworked section contents.
Introduction	• Reworked section contents. • Reworked *section 4 Ordering Part Number* and renamed to *subsection* 1.3 Licensing and Ordering Information. • Added IP Validation Summary and Minimum Device Requirements subsection. • Reworked *subsection 1.3 Naming Conventions* and renamed to *subsection* 1.6 Naming Conventions.
Functional Description	• Reworked *subsection 2.1. Overview* and renamed to *subsection* 2.1 IP Architecture. • Added subsection 2.2 Clocking and Reset. • Reworked *subsection 2.2.1 AXI4 Interface* and moved under added *subsection* 2.3 User Interfaces. • Reworked *subsection 2.5. Initialization and Training* and renamed to *subsection* 2.4 Calibration. • Reworked *subsection 2.6. Operations Details* and renamed to *subsection* 2.5 Operation Descriptions.
IP Parameter Description	Reworked *subsection 2.3 Attributes Summary* and moved this under IP Parameter Description section.
Signal Description	Reworked *subsection 2.2 Signal Description* and converted it to Signal Description section.
Register Description	Reworked *subsection 2.4 Register Description* and converted it to Register Description section.
Memory Controller Example Design	Added this section.
Designing and Simulating the IP	Reworked *section 3 IP Generation, Simulation, and Verification* and renamed to this main section.
Appendix A. Resource Utilization	Reworked section contents.
References	Reworked section contents.

Revision 1.1, September 2023

Section	Change Summary
All	• Changed the document title from 'Avant Memory Controller IP Core - Lattice Radiant Software' to 'Lattice Avant Memory Controller IP Core - Lattice Radiant Software'. • Updated the document to JESD209-4C
Introduction	• Updated Lattice Radiant Version to 2023.1 in Table 1.1. Quick Facts. • Removed 933 MHz and BL32 from the Features section.
Functional Description	• Added AXI4 Interface section under Signal Description. • Updated Table 2.2. Supported AXI4 Transactions, Table 2.3. Attributes Table, and Table 2.4. Attributes Descriptions.
IP Generation, Simulation, and Validation	• Added Creating a Radiant Project section. • Updated Configuring and Generating the IP section for the new IP GUI. • Added Figure 3.7 in the IP Evaluation section. • Updated the Hardware Validation section.
Ordering Part Number	Updated this section.
Appendix A. Resource Utilization	Updated this section.

Section	Change Summary
References	Updated this section.
Technical Support Assistance	Added reference link to the Lattice Answer Database.

Revision 1.0, November 2022

Section	Change Summary
All	Changed document title to Avant Memory Controller IP Core - Lattice Radiant Software.
Introduction	• Updated Table 1.1. Quick Facts. • Added 266 and 933 MHz in the Features section.

Functional Description	• Updated rst_n_i description and added Note 6 in Table 2.1. Memory Controller IP Core Signal Description.
	• Updated Table 2.3 Attributes Table.
	  • Updated DDR Command Frequency and Write/Read Ordering Queue.
	  • Added note on supporter frequency per speed grade.
	• Improved Enable DBI description in Table 2.4. Attributes Descriptions.
	• Updated Initialization and Training section.

IP Generation, Simulation, and Validation	• Updated subsections in the IP Generation, Simulation, and Validation section. • Updated the IP Evaluation section. • Updated the Hardware Validation section.
Ordering Part Number	Updated this section.
Appendix A. Resource Utilization	Updated this section.
References	Updated this section.

Revision 0.80, September 2022

Section	Change Summary
All	Preliminary release

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