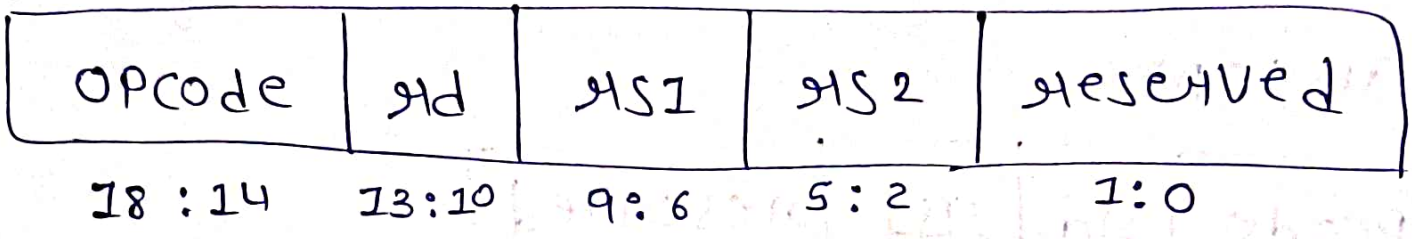
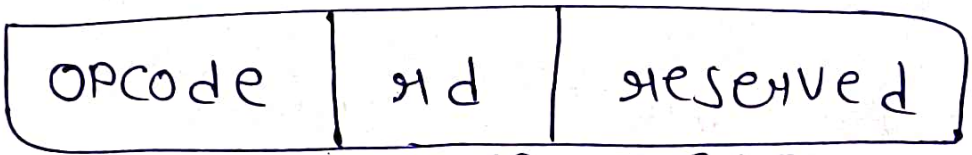
1) Data Processing (R-type)

ADD, SUB, MUL, DIV, AND, OR, XOR

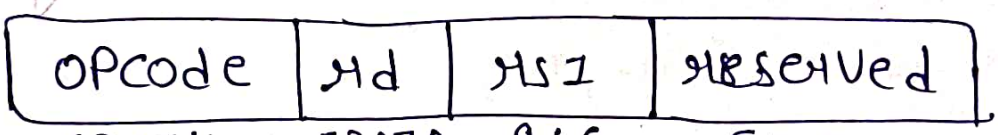


2) Single Register

INC
DEC

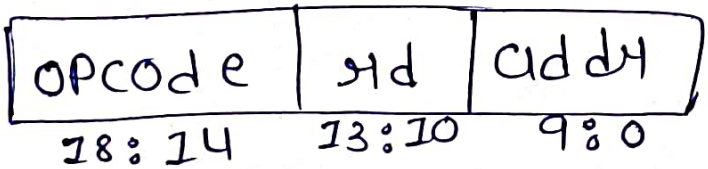


NOT

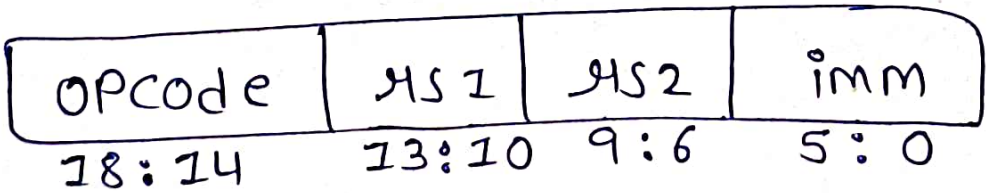


3) Memory (I-type)

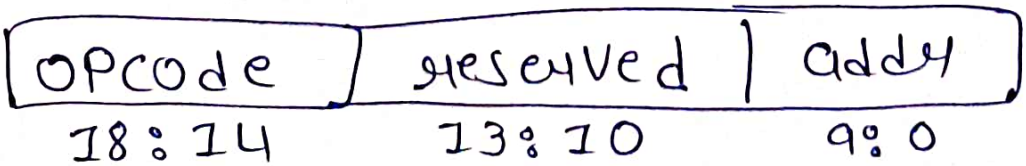
LD Rd, addr Rd = mem(addr)
ST addr, Rd



4) Branch BEQ, BNE, ~~JMP~~



JMP



YASH SIDDHAPURA

Conclusion:

Rubric wise marks obtained:

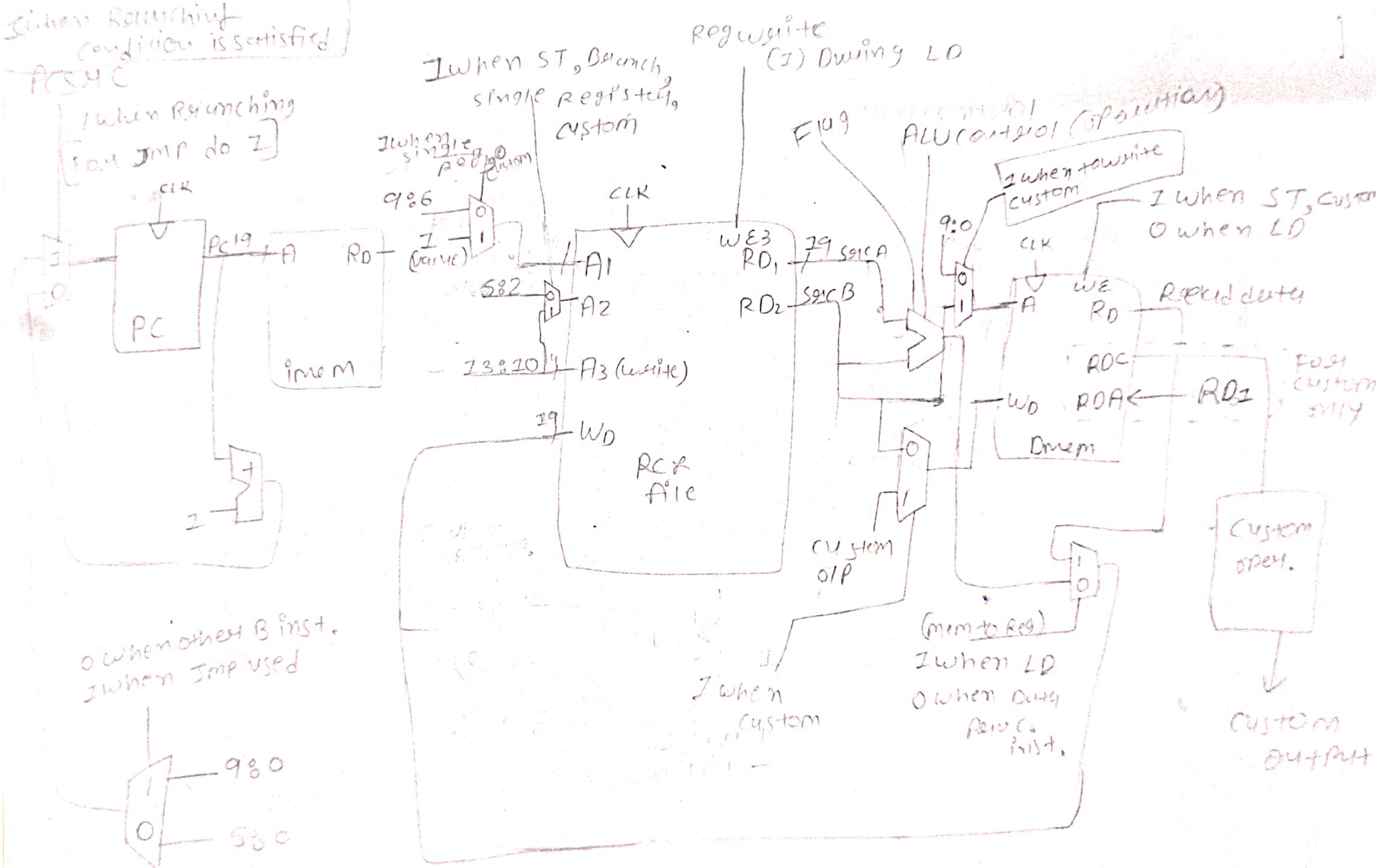
Rubrics	Presence and efforts	Safety in Laboratory	Preparedness	Quality of Lab. Manual	Ability to Use Laboratory Apparatus	Total
Marks						

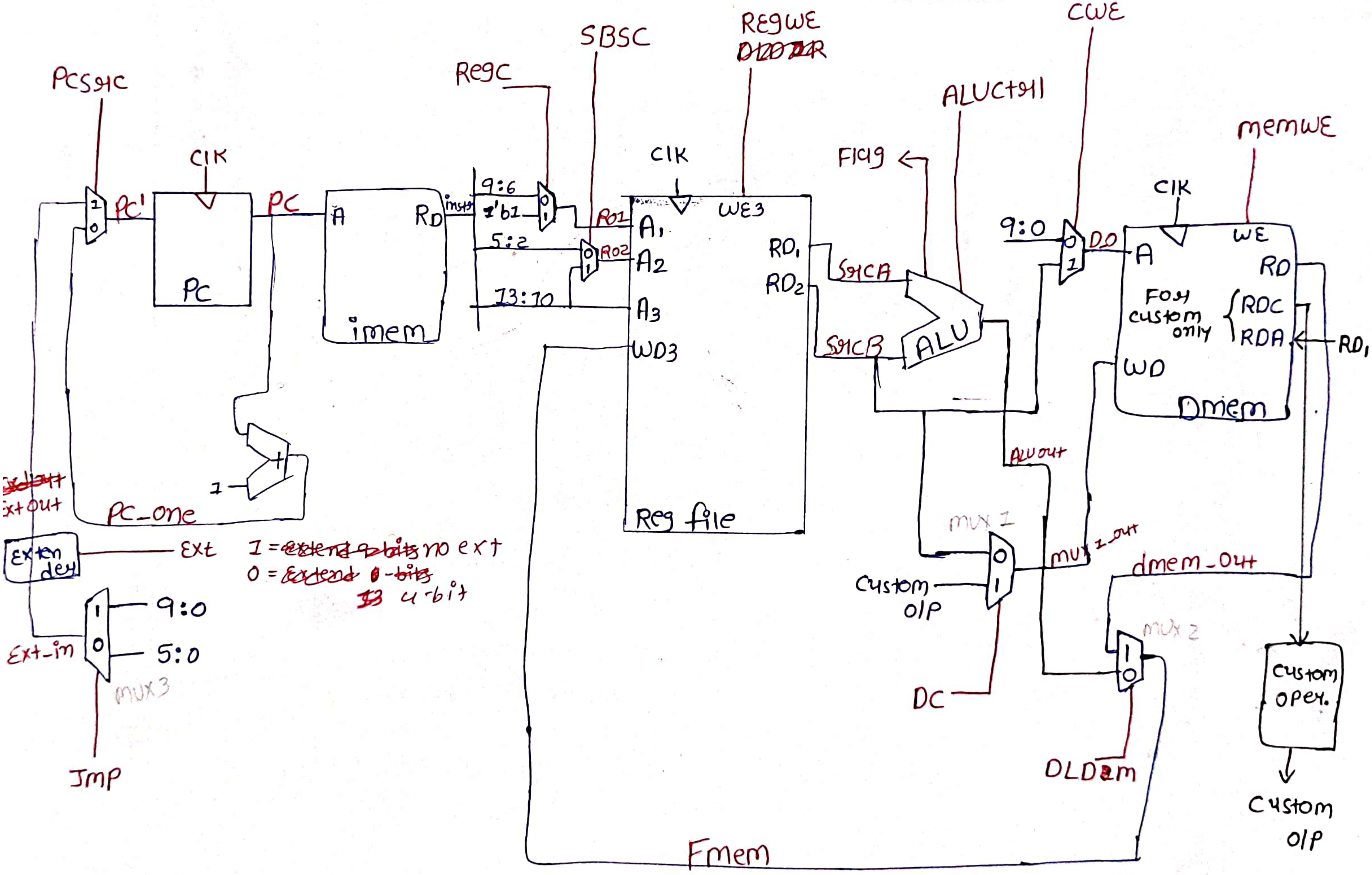
Lab Manual Modified By:

Prof. H.L.Desai

AP, EC

LDCE, Ahmedabad.

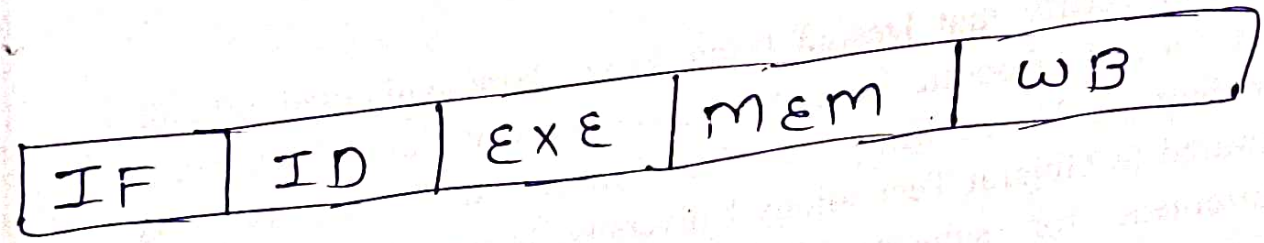

1 when Branching condition is satisfied
ACSHC
1 when Branching
[for JMP do 1]
CLK
PC
PC 19
A
RD
imem
1
9:6
1 (value)
1 when single reg @ custom
5:2
13:10
1 when ST, Branch, single register, custom
CLK
A1
A2
A3 (write)
WD
19
RC file
WE3
RD1
RD2
RegWrite (1) During LD
19 SrcA
SrcB
Flag
ALU control (operation)
9:0
1 when to write custom
CLK
A
WE
RD
RDC
RDA
WD
Dmem
1 when ST, Custom
0 when LD
Read data
RD1
For custom only
Custom oper.
Custom output
Custom O/P
1 when custom
(mem to Reg)
1 when LD
0 when Data Proc. inst.
0 when other B inst.
1 when Jmp used
9:0
5:0

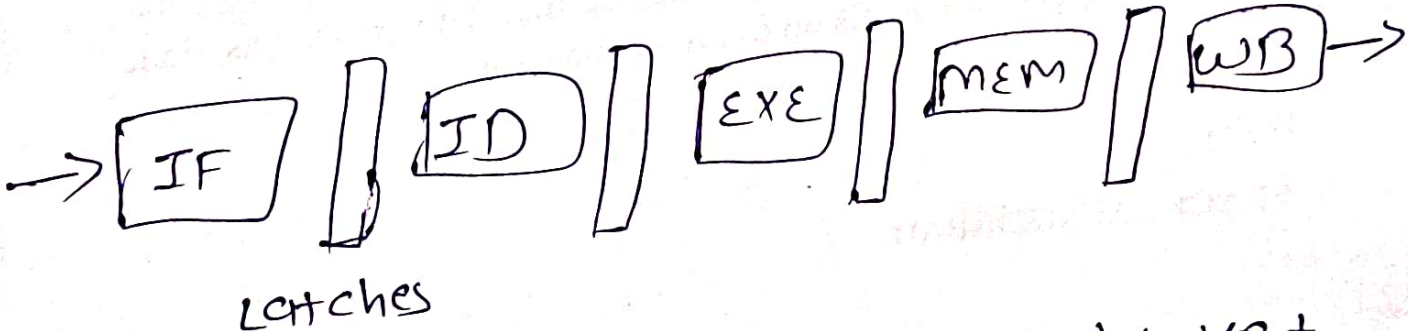


PCSrc
PC'
clk
PC
PC
A
imem
RD
instr
9:6
1'b1
5:2
13:10
RegC
SBSC
RO1
RO2
A1
A2
A3
WD3
clk
WE3
RegWE
RD1
RD2
Reg file
SrcA
SrcB
ALU
Flag
ALUCtrl
ALUout
CWE
9:0
DO
clk
A
WE
memWE
RD
For custom only
RDC
RDA
RD1
WD
Dmem
mux 1
mux1_out
Custom o/p
DC
dmem_out
mux 2
OLDRm
Custom oper.
Custom o/p
Fmem
PC_one
1
+
Ext_out
Extender
Ext
1 = no ext
0 = 4-bit
9:0
5:0
Ext_in
mux3
Jmp

5-Stage pipelining

1) Inst. fetch (IF)
2) Inst. Decode (ID)
3) Inst. exe (EXE)
4) (MEM) - Access memory to write
5) Write back to Reg or Memory (WB)

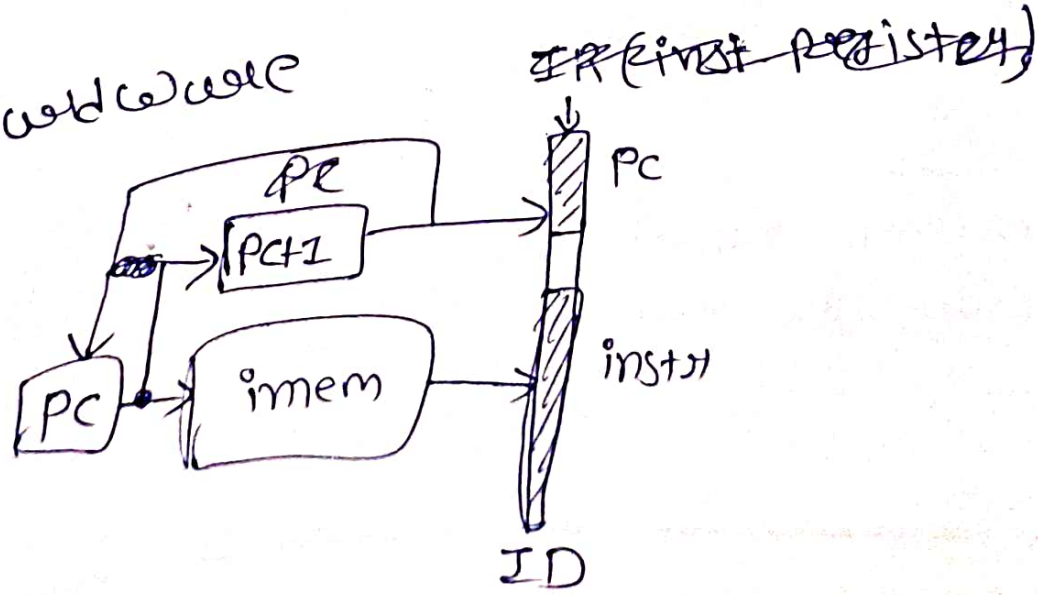




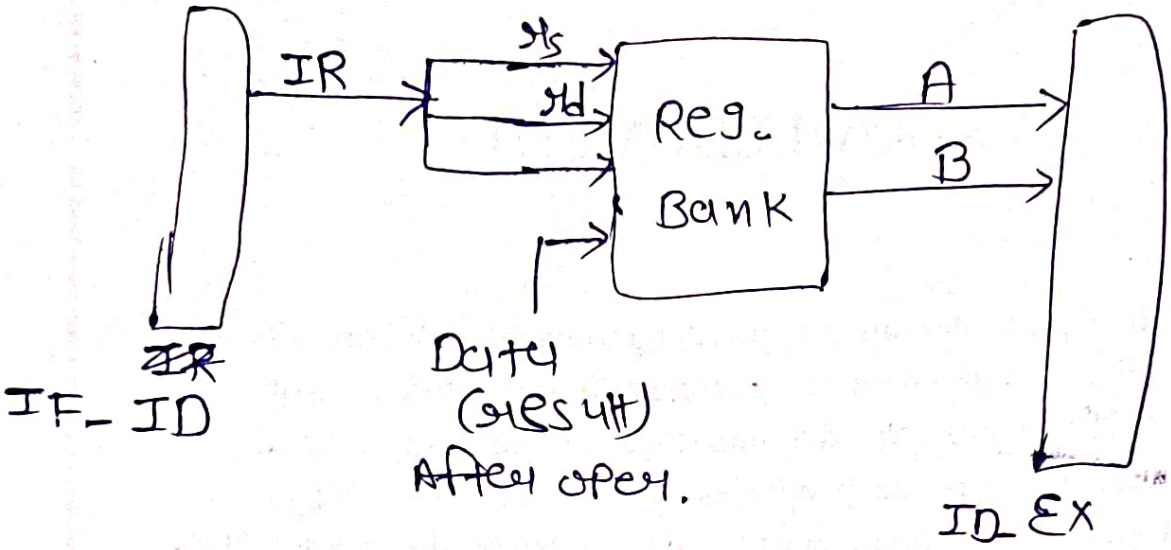
Latches

→ Latches used cuz if block is not ready yet to process data so data should not change.

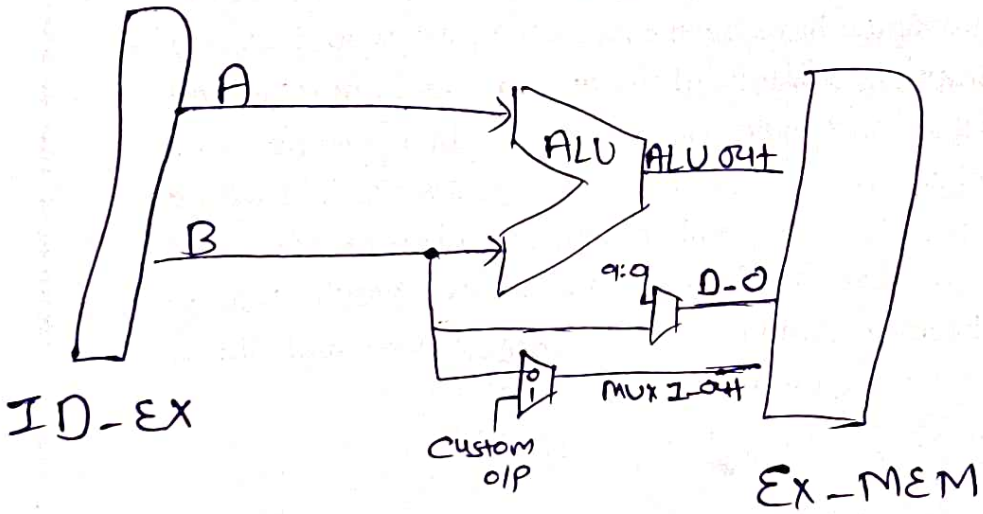
1) IF Hardware



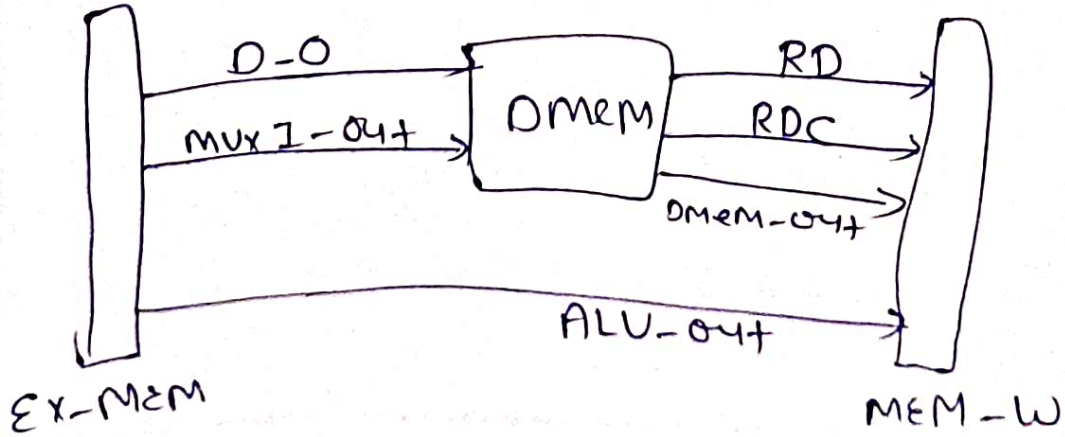
2) ID


IR
Reg.
Bank
A
B
IF-ID
Data
(Result)
After oper.
ID-EX

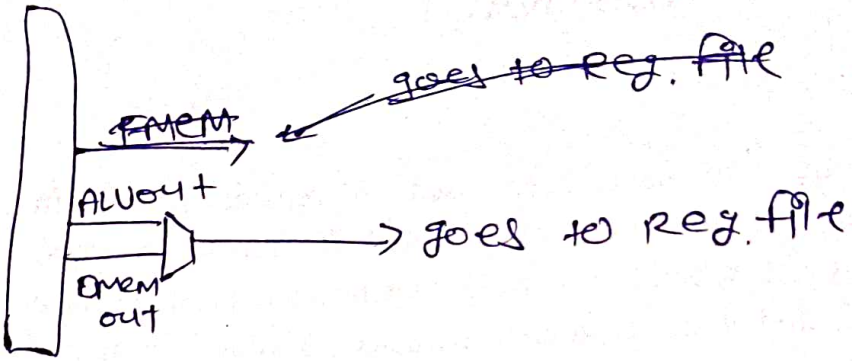
3) EX


A
B
ALU
ALU out
2:1
D-O
MUX I-out
Custom
O/P
ID-EX
EX-MEM

4) MEM


D-O
MUX I-out
DMEM
RD
RDC
DMEM-out
ALU-out
EX-MEM
MEM-W

5) WB



MEM_W