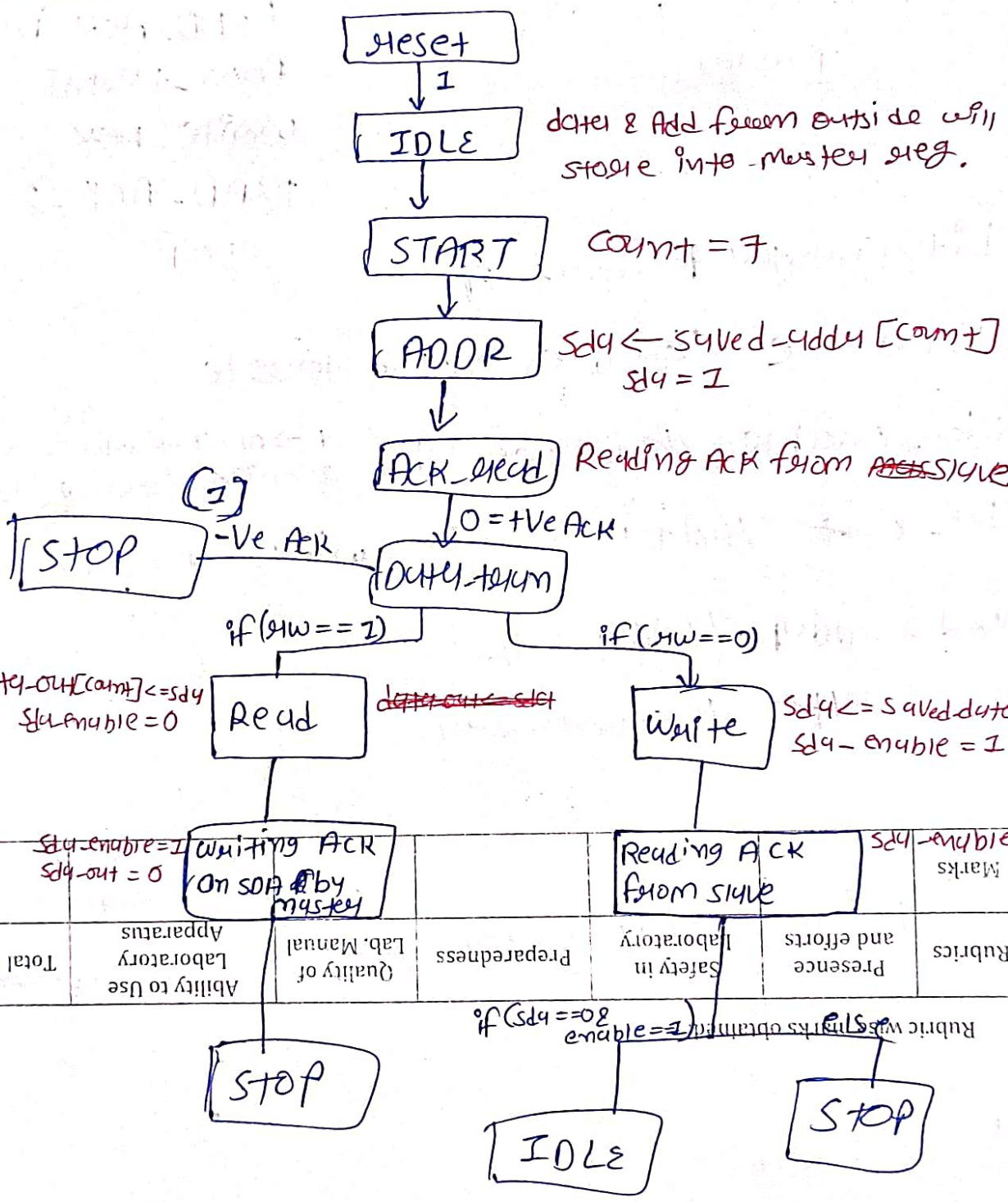
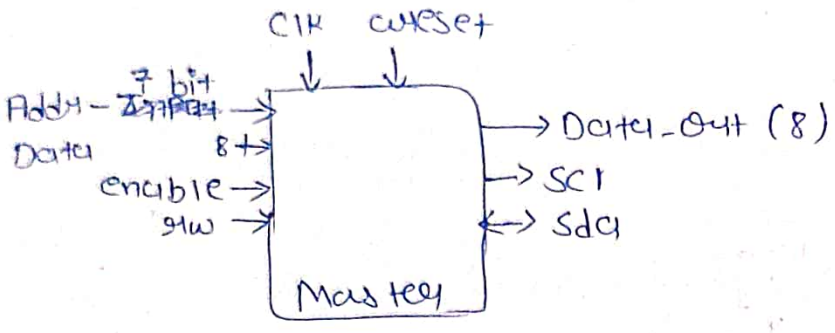
Mestrey



Conclusion:

SCL toggles when scl_enable is 1



IDLE
START
ADDR (Actually reaches at 9th clock)
READ_ACK (from slave)
Data_transmit
Write_ACK
READ_ACK_2
STOP

3-bit counter ~~down~~ count ~~7~~

scl_enable //enables scl to toggle

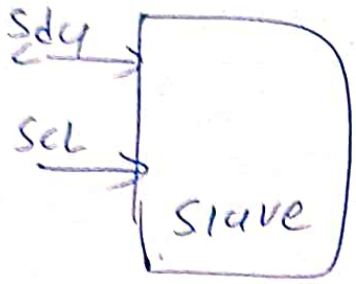
sda_enable //enables sda (1 -> master drives sda, 0 -> master releases sda for slave)

sda_out //Assigns ~~out~~ to sda pin

saved_addr //Addr + rw

saved_data //saved data

During idle, start & stop scl should not toggle ~~should~~



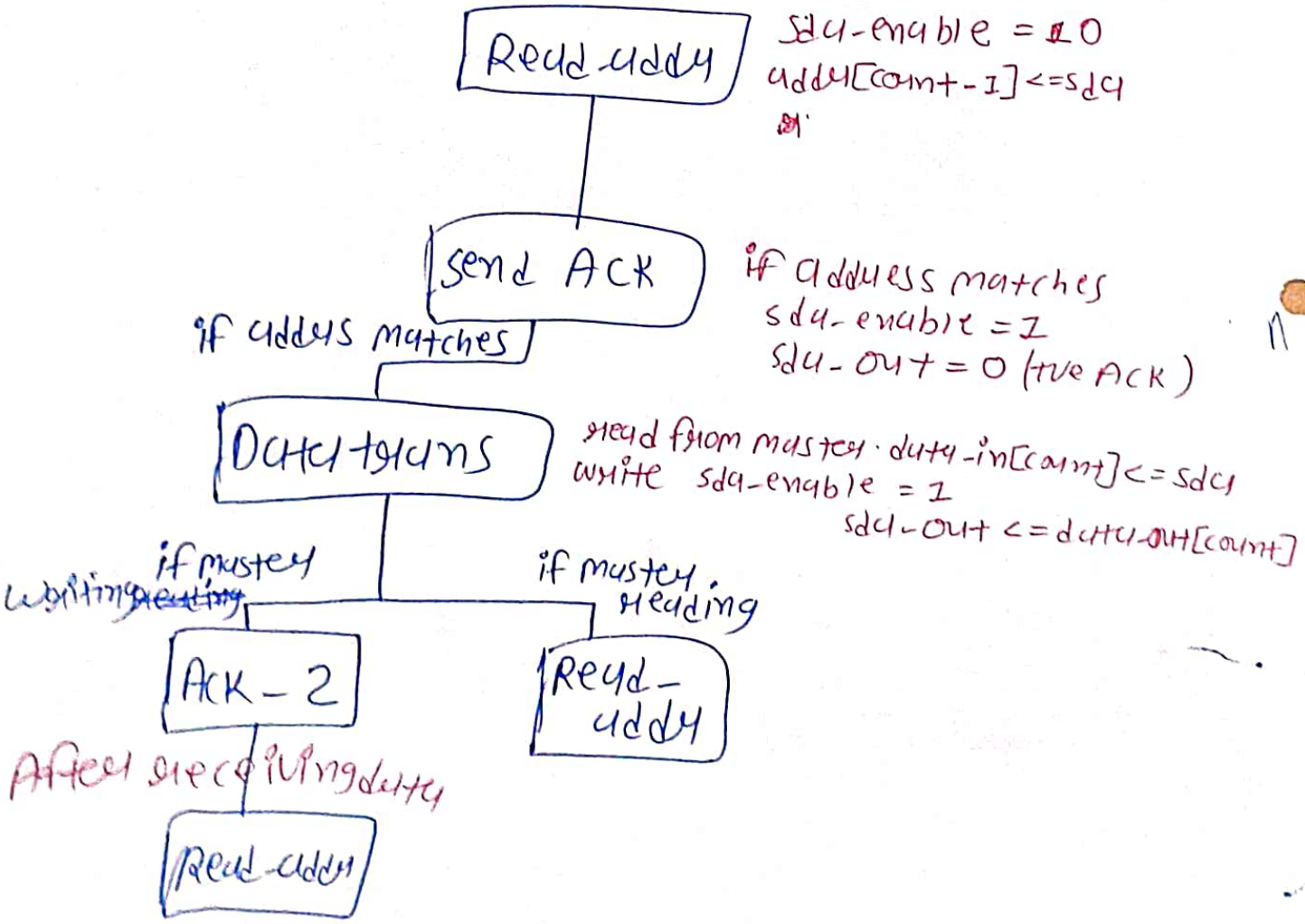
Read-addr
send-ACK
Data-trans
Send-ACK-2

has 7-bit physical Address

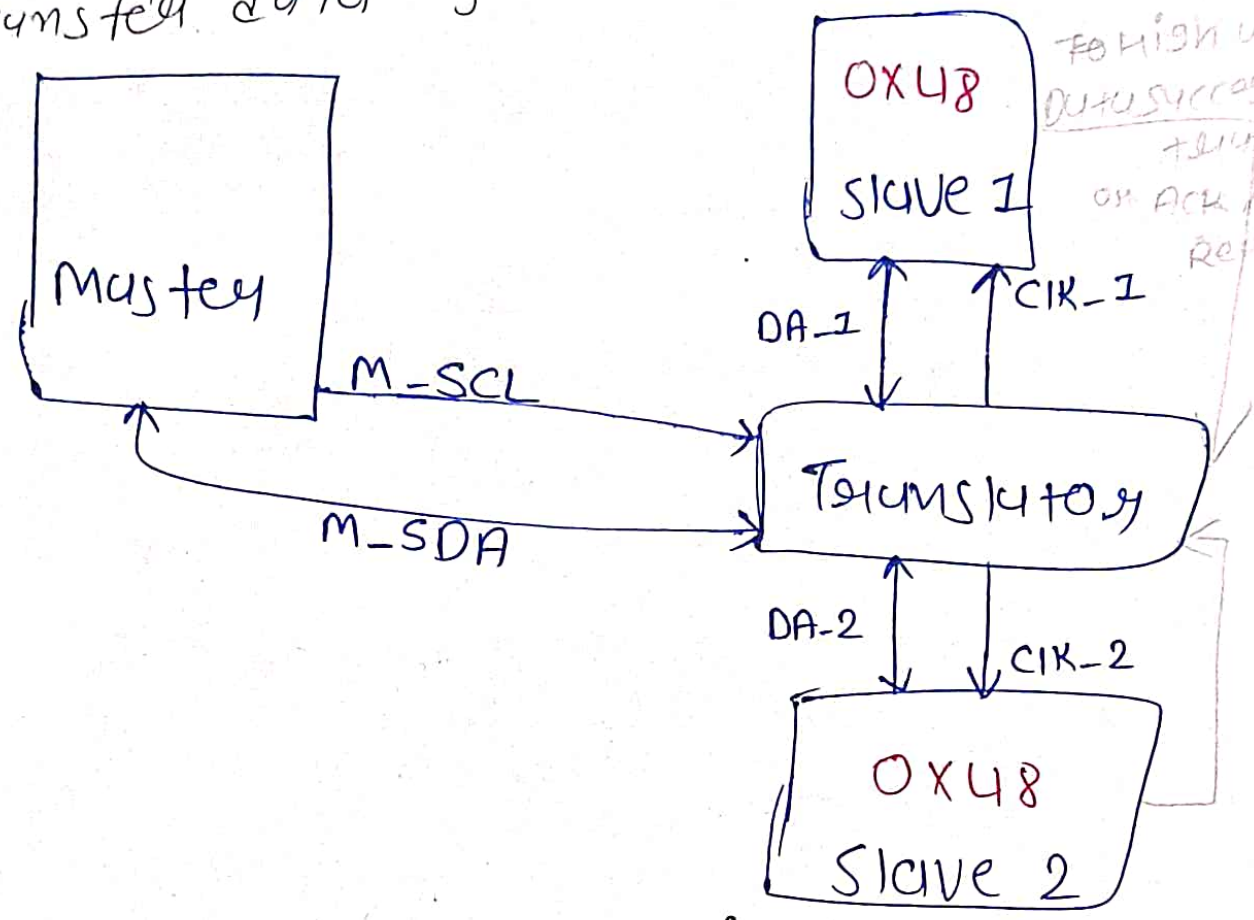
if (sda == 0 && scl == 1) start condition
if (sda == 1 && scl == 1) stop condition

ideally both will be high

SLAVE



After receiving data & transfer data } done = 1

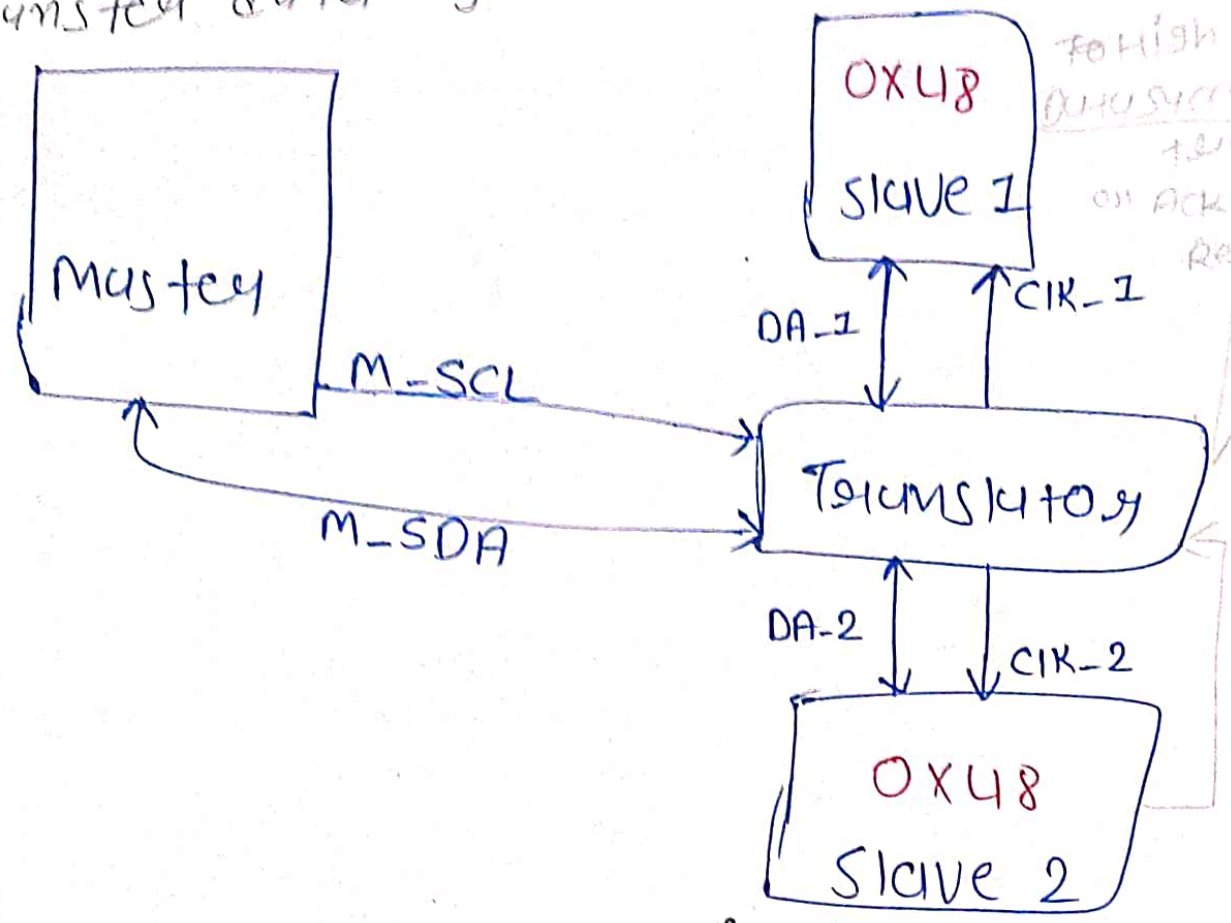


Master sends add. → Translator checks all add. with incoming if it hes then +ve ACK & stores data normally

↓

After comm. Translator behaves as master

After receiving data & transfer data } done = 1

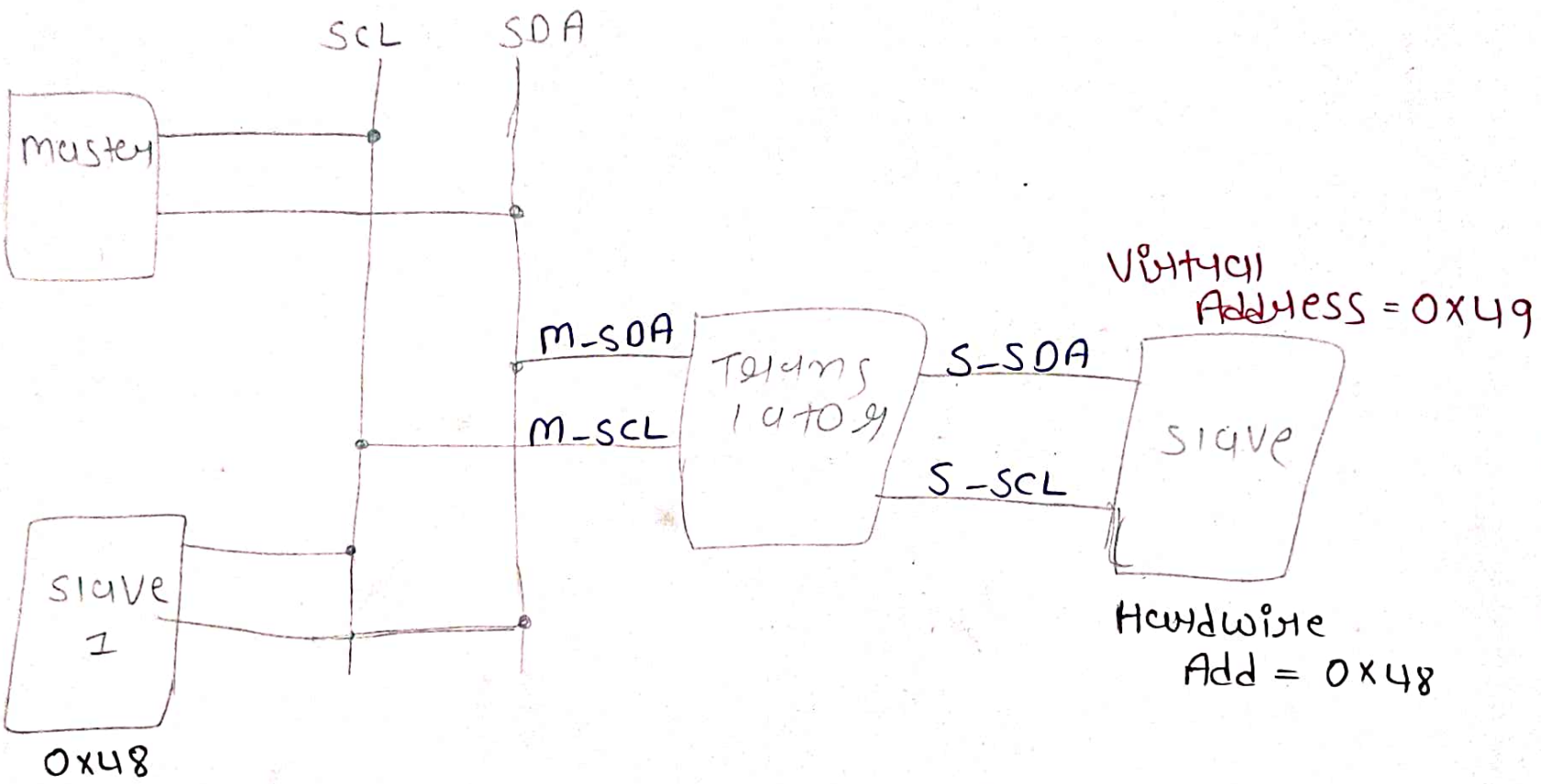


Virtual = 0X49

Master sends add. → Translator checks all add. with incoming if it hey then +ve ACK & stores data normally

↓

After comm. Translator behaves as master



Translator acts slave toward master

Translator acts master toward slave