Coláiste na Tríonóide, Baile Átha Cliath
Trinity College Dublin
Ollscoil Átha Cliath | The University of Dublin

FACULTY OF ENGINEERING, MATHEMATICS & SCIENCE

SCHOOL OF ENGINEERING

Electronic & Electrical Engineering

Engineering **Michaelmas Term, 2020**

Junior Sophister

Annual Examinations

EXAM PAPER

Digital Systems Design (3C7)

11th January 2021 **Online** **12:00- 02:00**

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Instructions to Candidates:

Answer ALL questions.

Materials Permitted for this Examination:

Non-programmable calculators are permitted for this examination. Please indicate the make and model of your calculator on each answer book used.

Acronyms and notation possible used in this paper:

ASIC: Application Specific Integrated Circuit

FPGA: Field Programmable Gate Array

FSM: Finite State Machine

XDC: Xilinx Design Constraint

All symbols have their usual meaning.

Q.1 Multiple Choice Questions

Q.2 Long answer questions: Upload the answer sheet including all questions below. Remember to write your name and ID at the top of each sheet.

(a) A wired network controller within a car operates in a dual channel mode for redundancy, with quick switching between channels P and R based on a pattern observed on the serial synchronous data. By default, the prime channel P is active and the transceivers use this channel to transmit and receive sensor data. When a specific pattern "10101101" is received on the P channel, the system must switch to the redundant channel R for active transmission and reception. When the error is rectified, the system will receive the reverse pattern on channel R (i.e., "10110101"), on which the system switches back to the primary channel P.

Design a Moore FSM to implement this data-path controller, which **generates a pulse of 1 clock cycle** on the appropriate output enable, when the pattern is detected. Clearly mark the inputs, outputs and transition conditions, using legends, if appropriate.

[10 marks]

(b) Provide a Verilog outline (note, only an outline, entire code is not required) for this module

[5 marks]

(c) Specify a test plan to verify the functionality of the design.

[7 marks]

(d) Consider a 5-input combinational logic function

$$f(A, B, C, D, E) = (A \oplus D) \cdot (B' + (D \odot E)) + C'E$$

Build the truth table for the function and hence determine the contents of the LUT when this function is mapped on to a 6-input LUT by the implementation tools.

[7 marks]

(e) Write a behavioural Verilog code for a parameterised synchronous 10-bit Up/Down counter, where the parameter **`INC`** specifies the increment steps to be used in the Up/Down counts. The module has an active high synchronous **`reset`** input to reset the count to 0, and a **`down`** input signal which, when high, causes the counter to count down. The module also has a **`load`** input which when set to 1, loads the value on the input pins **`start_val`** to the counter. Finally, the counter also has an **`overflow`** output bit, which is set to 1 for **one clock cycle**, when the counter reaches its maximum value in either direction.

[7 marks]

(f). What are IP Blocks? Describe how they can be incorporated into a Verilog design you are building.

[4 marks]