Coláiste na Tríonóide, Baile Átha Cliath
Trinity College Dublin
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EEU33C07-1

FACULTY OF SCIENCE, TECHNOLOGY, ENGINEERING AND MATHEMATICS

SCHOOL OF ENGINEERING

Electronic and Electrical Engineering

Engineering **Semester 1, 2021**

Junior Sophister

Digital Systems Design

17/12/2021 **RDS Simmonscourt** **09:30–11:30**

Asst. Prof. S. Shanker

Instructions to candidates:

Answer all questions.

Acronyms used in this paper:

ASIC	Application Specific Integrated Circuits
FPGA	Field Programmable Gate Arrays
FSM	Finite State Machine
XDC	Xilinx Design Constraint

All symbols have usual meanings

Q.1 **[Total: 25 marks]**

(a) You are designing an audio filter module that takes digitised audio samples as inputs to perform a multiply-accumulate operation over 32 samples (i.e., a 32-tap filter). Given that the audio input is in the range of $2000\,\text{mV}$ and the filter coefficients (internal registers) are in the range of ± 128, determine the specification of the inputs and outputs of this module. Assume that all inputs (audio signal and coefficients) are integers. **[5 marks]**

(b) What are the potential issues of using positional association method when instantiating moules in Verilog? **[5 marks]**

(c) Why is it important to observe timing parameters of your clock (jitter and delay) in your synchronous design? **[5 marks]**

(d) You are tasked with designing a functionality for a low-volume energy-efficient Interet of Things application. Which platform among Processors, FPGAs or ASICs would you choose and why? **[5 marks]**

(e) With respect to the synchronous always block below, explain the use of non-blocking and blocking assignments in Verilog **[5 marks]**

```
1   always @ (posedge clk) begin
2     if (!reset_n)
3       count <= 0;
4     else
5       count <= count + 1;
6   end
```

Q.2 **[Total: 25 marks]**

(a) You are designing a pattern detector for a radiation monitoring equipment, that produces a 1-bit output every second corresponding to the intensity of radiation it observes. The patten detector you are designing observes the output bit of the radiation montior to detect a sequence ['101001011101'] indicating high radiation presence. Since radiation output is a continuous function, subsequent sequences may overlap in the case of high radiation and thus the pattern detection logic should cater to them.

You are to design an FSM to implement this detector, which sets an 'alert' signal to high whenever this squence is detected at the output of the radiation monitor. Show the design of the FSM using a state machine, clearly marking the inputs, outputs, transition conditions and legends, as appropriate. **[10 marks]**

(b) Complete the state transition table for your FSM design above. Is it a Mealy or a Moore machine? **[7 marks]**

(c) Sketch a timing diagram showing the operation of your FSM, assuming all outputs and internal state as registered. Use ['10100'] as the input sequence to show the working. **[8 marks]**

Q.3 **[Total: 25 marks]**

(a) What type of circuit will the following code snippet generate? Is it recommended to use the code below to target FPGA devices? Explain your answer and how you will need to alter it for an FPGA device, if needed. **[6 marks]**

```
1   always @ * begin
2   case (sel)
3     2'b00: begin
4       y = a;
5       z = b;
6     end
7     2'b01: begin
8       y = b;
9       x = c;
10    end
11    2'b10: begin
12      x = c;
13      z = a;
14    end
15    default: begin
16      y = 4'hA;
17    end
18  endcase
19  end
```

(b) Consider a 5-input combinational logic function
$f(P,Q,R,S,T) = (R \oplus Q \oplus T) + (Q' \cdot S \cdot T)' + (P+Q)'$
Build the truth table for the function and hence determine the contents of the LUT when this function is mapped on to a 6-input LUT by the implementation tools. **[9 marks]**

(c) Using example code snippets, explain the different reset strategies that can be used in synchronous design. Why is one of them preferred over the others when targeting an FPGA device? **[10 marks]**

Q.4 **[Total: 25 marks]**

(a) Explain the specific steps performed by the implementation phase in a Vivado design flow, describing the importance, output and complexity of each step. **[8 marks]**

(b) What is the importance of timing simulation? How does it compare to behavioural simulation? **[5 marks]**

(c) Explain the operation of a positive edge triggered D flip-flop (D-FF) built using a master-slave D latch arrangement. A specific use case of the D-FF is shown below, where the output Q of the slave latch is connected back to the D input of the master through an inverter. With the help of a timing diagram, explain the operation of this circuit. **[12 marks]**