IIT GUWAHATI, DEPT OF CSE

CS221: Digital Design: Examination of Module 7 (Lec 27-29)
Date: 06th November 2020, Timing: 9.00AM to 9.45AM
Total Mark: 25 (will be scaled to 10 Marks)

Submission Procedure: Submit PDF scan copy of handwritten answer sheet (mention your name and roll no in the sheet) to MS Team course examination link before 9.50AM of 06th November 2020. Submission after 10.00AM of 06th Nov 2020 will not be accepted.

1. [**12 Marks**] Design a Moore type FSM that has an input X and an output Y. Whenever X changes from 0 to 1, Y should become 1 for five clock cycles and then return to 0 even if X is still 1.
   a) [3] Draw a neat FSM diagram for the said problem.
   b) [3] Verify the completeness properties of the FSM.
   c) [2] State FSM using tabular form
   d) [4] Implement a controller the designed FSM (or implement the design).

2. [**8 Marks**] Design a Mealy type FSM for counter which count 55, 26, 37, 12 and repeat, when external control signal is X=1, otherwise hold the counter value to present state.
   a) [3] Draw a neat FSM diagram for the said problem.
   b) [2] State FSM using tabular form
   c) [3] Implement a controller the designed FSM (or implement the design) using JK Flip Flops.

3. [**5 Marks=2.5+2.5**] Draw Mealy FSM and Moore FSM for serial binary adder, where serial binary adder has two primary inputs: X and Y, two outputs: S and C, and the carry output is feedback to input of the full adder through a D-flip flop as shown in the diagram.