SIDDHARTH CHARAN
19010105

Q. (1) Given; for a XY flip flop :-

(a)

X	Y	Q(t+1)
0	0	1
0	1	Qt
1	0	Qt'
1	1	0

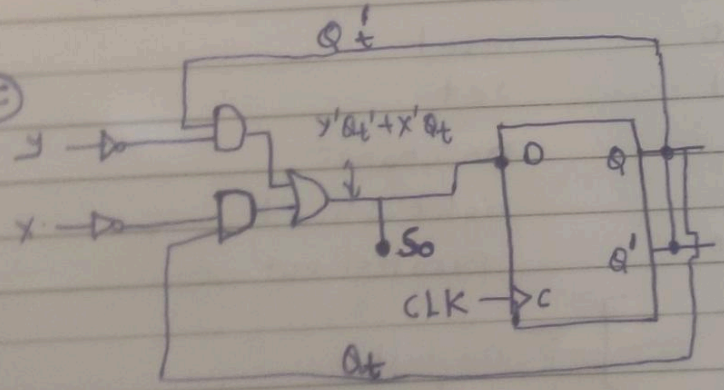
[This table is generated as per characteristics given in question]

(b) From Table :-

$Q_{t+1} = \bar{X}\bar{Y}Q_t + X\bar{Y}\bar{Q}_t + \bar{X}\bar{Y}$

$\boxed{Q_{t+1} = Y'Q_t' + X'Q_t}$

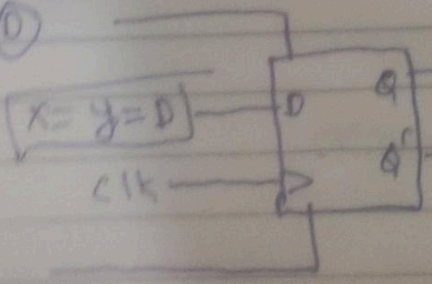
(c)



We will use output of D-FF again with two 'and' and 'one or gates to design our circuit.
[As, we can see in dy gram]

$\boxed{S_0 = Y'Q_t' + X'Q_t}$

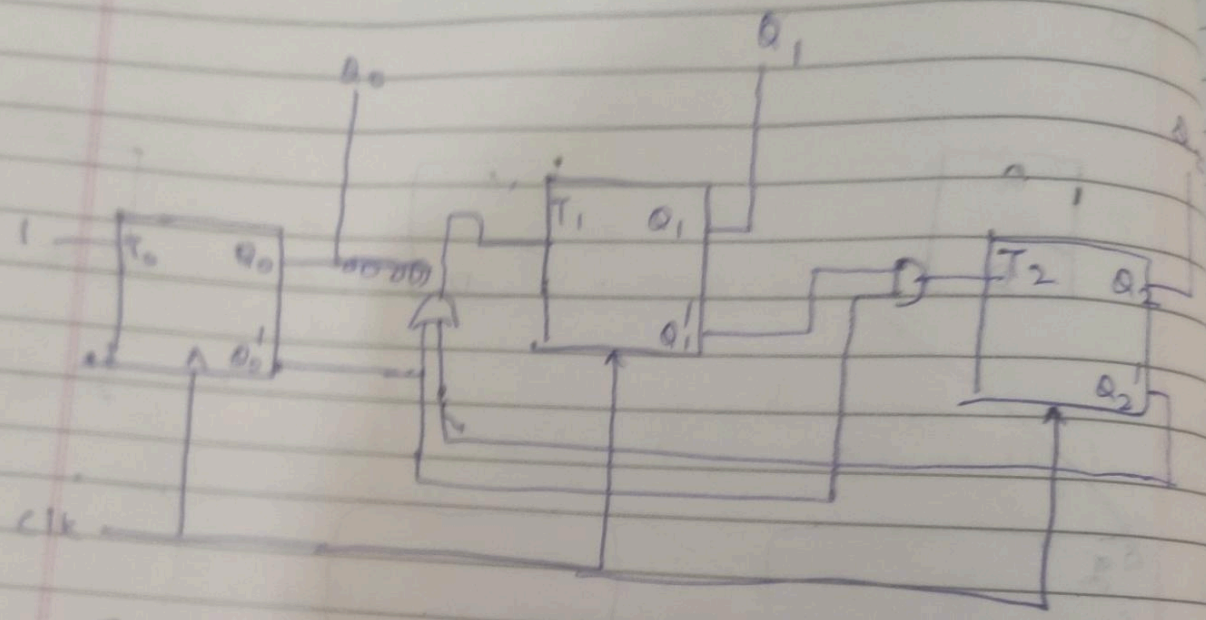
(d)



$Q = D\bar{Q} + DQ$

$\boxed{Q = D}$

SIDDHARTH CHARAN
1961010185



[Design of counter]

19010108S
SIDDHARTH CHARAN

Q.① Given;
we need to design a counter with 3 flip flops, which count.
7, 6, 5, 4, 3, 0 and repeat.

	Present state	T_2	T_1	T_0	Next state
7	1 1 1	0	0	1	1 1 0
6	1 1 0	0	1	1	1 0 1
5	1 0 1	0	0	1	1 0 0
4	1 0 0	1	1	1	0 1 1
3	0 1 1	0	1	1	0 0 0
0	0 0 0	1	1	1	1 1 1

(i) $T_2 = \Sigma M(4,0) + [d(1,2)]$ → (don't care)

Q_0 \ Q_2Q_1	00	01	11	10
0	1	X		1
0	X			

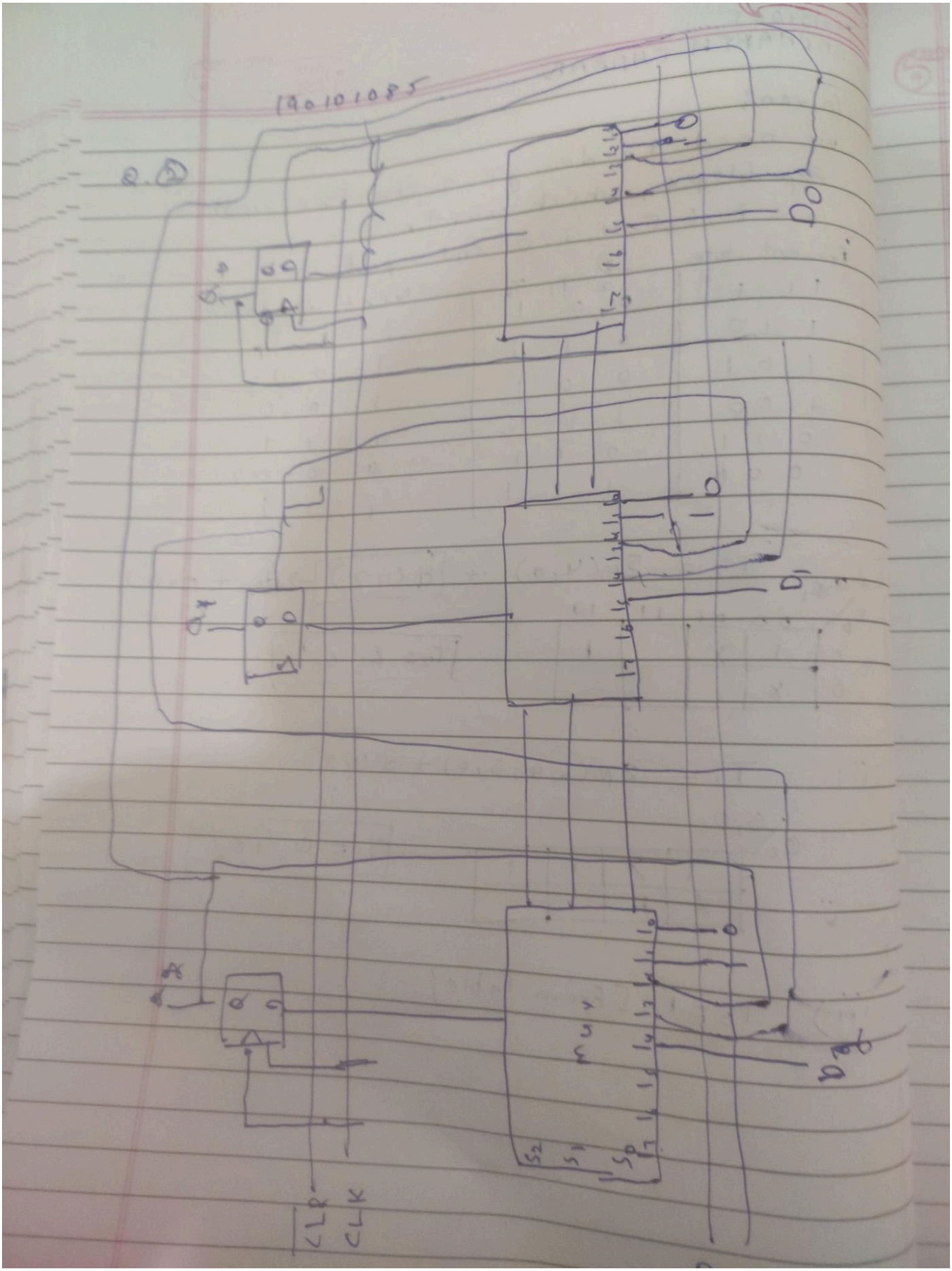
$T_2 = Q_1' Q_0'$

(ii) $T_1 = \Sigma m(6,4,3,0) + d(1,2)$

Q_0 \ Q_2Q_1				
	1	X	1	1
	X	1		

$T_1 = Q_0' + Q_2'$

(iii) $T_0 = 1$ [From Table]


190101085
Q.2
D0
D1
D2
S2
S1
S0
CLR
CLK

SIDDHARTH CHARAN
19010108S

Q. We are asked to design a circuit such that it supports:-

(a) reset to 000
(b) set to 111
(c) retain the older value
(d) right shift with rotate bit
(e) parallel out

⇒ We will use D flip flops and multiplexers to do our task.

For 5 tasks; we need 3x8 mux.

In mux

S_0	S_1	S_2	
0	0	0	reset
0	0	1	set
0	1	0	no change
0	1	1	right shift
1	0	0	parallel out
1	0	1	→ no tasks
1	1	0	
1	1	1	

So, design is :-