IIT GUWAHATI, DEPT OF CSE

CS221 (Digital Design) Examination Module 9 (Based on ASM/Lec 33, 34, 35)

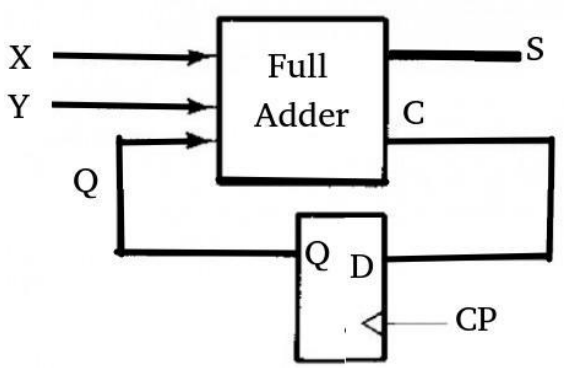
Date: 20th November 2020, Timing: 9.00AM to 9.45AM

Total Mark: 20

Submission Procedure: Submit PDF scan copy of handwritten answer sheet (mention your name and roll no in the sheet) to MS Team course examination link before 9.50AM of 20th November 2020.

- **Submission after 10.00AM of 20th Nov 2020 will not be accepted.**
- **If you have any issue with MS team upload then send email to me quickly (mentioning your Roll No, Exam 9 and attach the solution) before 10.15AM of 20th Nov 2020.**

1. [2+3+2+3 **Marks**] Given Serial Binary Adder as shown below.
   a) Draw Mealy type FSM for serial binary adder, where serial binary adder has two primary inputs: X and Y, two outputs: S and C, and the carry output is feedback to input of the full adder through a D-flip flop as shown in the diagram.



   b) [2+2] Draw ASM chart for the corresponding to the Mealy FSM for the above serial binary adder. Identify all the ASM blocks of your ASM.
   c) Infer the data path required for the drawn ASM
   d) Design an ASM controller (mentioning all required control signals, input signals) for the same using a decoder (to identify all the different states) and other logic.

2. [4+2+4 **Marks**] Design a digital system which calculate sum of first N odd number. Your designed digital system should have input two input (a) go signal (1 bit) and (b) the value N (8-bit number). Outputs are ready/done signal and the sum (a 16-bit number).

   a) [2+2] Draw ASM chart for the above problem. Identify all the ASM blocks of your ASM.
   b) Infer the data path required for the drawn ASM.
   c) Design an ASM controller (mentioning all required control signals, input signals) for the same using a decoder (to identify all the different states) and other logic.