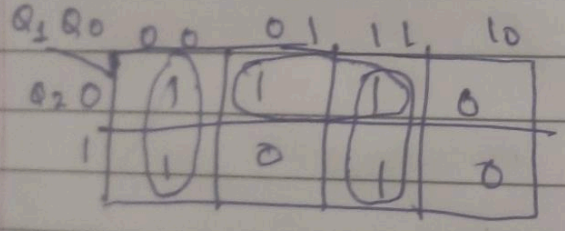
19010108S
SIDDHARTH CHARAN

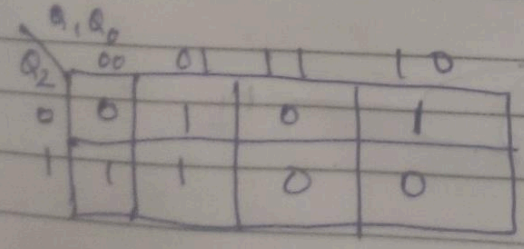
Q.① We need to design counter which count the following sequence & repeat :-

⇒ (5, 7, 2, 5, 6, 3, 1, 4) & repeat it.

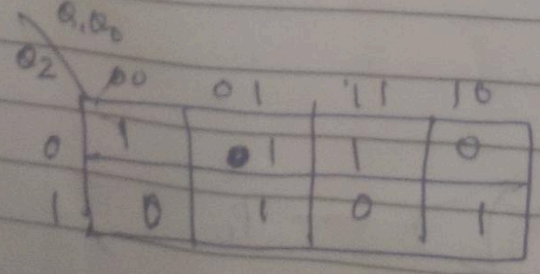
Q_2	Q_1	Q_0	P_2	P_1	P_0
0	0	0	1	0	1
0	0	1	1	1	1
0	1	0	0	1	0
0	1	1	1	0	1
1	0	0	1	1	0
1	0	1	0	1	1
1	1	0	0	0	1
1	1	1	1	0	0



$P_2 = \bar{Q}_1 \bar{Q}_0 + \bar{Q}_2 Q_0 + Q_1 Q_0$

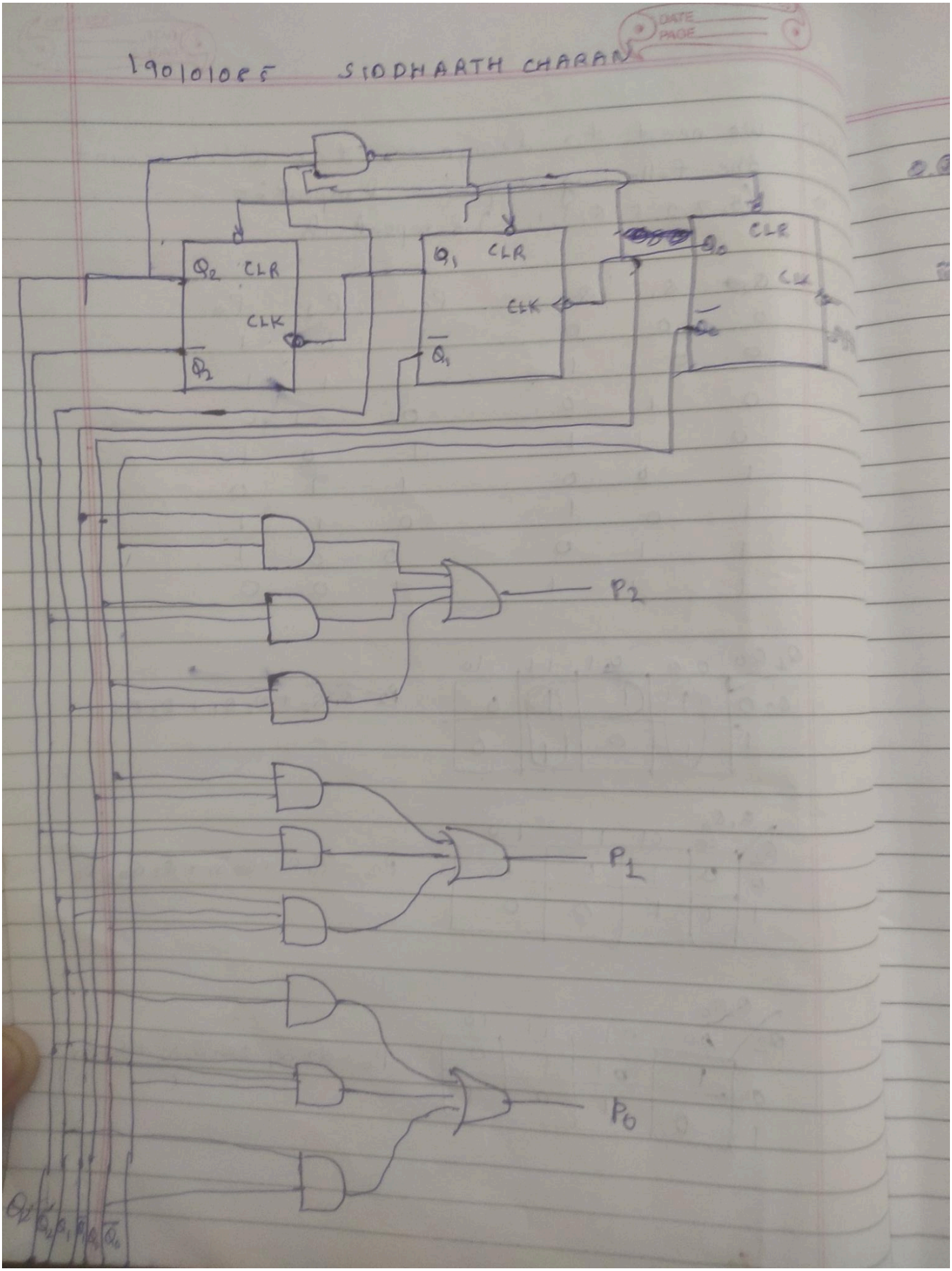


$P_2 = \bar{Q}_1 Q_0 + Q_2 \bar{Q}_1 + \bar{Q}_2 Q_0 + \bar{Q}_0$



$P_0 = \bar{Q}_2 \bar{Q}_1 + Q_2 Q_1 \bar{Q}_0 + \bar{Q}_2 Q_0$

19010108 SIDDHARTH CHARAN



19010108
SIDDHARTH CHARAN

class notes
DATE
PAGE

2. We need to design a 4-bit register to support following eight functions :-

i. Parallel input
ii. Parallel output
iii Left shift with rotate.
iv Right shift with rotate
v left shift with left serial in, serial out
vi Right shift with right serial in, serial out
vii Complement the bits
viii Swap bits

⇒ As ; there are 8 tasks ; we need to use a 3x8 MUX.

⇒ We will use 4-D Flip flops, As ; there are 4 bits.

S_2	S_1	S_0	
0	0	0	Parallel Input
0	0	1	Parallel Output
0	1	0	Left rotation
0	1	1	Right rotation
1	0	0	left shift with l serial in
1	0	1	right shift with r serial in, serial out
1	1	0	Complement the bits
1	1	1	swap bits.

19010 1085 SIDDHARTH CHARAN