EE5331-DSP Architectures and Embedded Systems Programming Assignment 2: A Wallace Multiplier on FPGA

1 Introduction

In this assignment, the objective is to implement a 4-bit unsigned Wallace multiplier on the FPGA board. The numbers can be hard-coded in your program. The result should appear on the LCD on the FPGA board.

2 The Wallace Multiplier

A Wallace multiplier for a pair of 4-bit unsigned numbers is depicted in Figure 1. The elements in the partial product are shown in the upper half of the figure (labelled (a)). Note that the partial product elements are shown only to indicate what portions of the "multiplicand" are inputs to half-adders. The lower half (labelled (b)) shows which elements would become inputs to various full-adders (that add 3 bits at a time). The addition of (P3[3] S4 S3 S2 S1) to (C4 C3 C2 C1 C0) can be done by a 'dedicated' 5-bit adder or handled separately using one half-adder for S1 and C0 and 4 full-adders (each taking also the output carry bits from the stage on the 'right': for eg. a full-adder that takes S2 and C1 along with carry output of addition of S1 and C0).

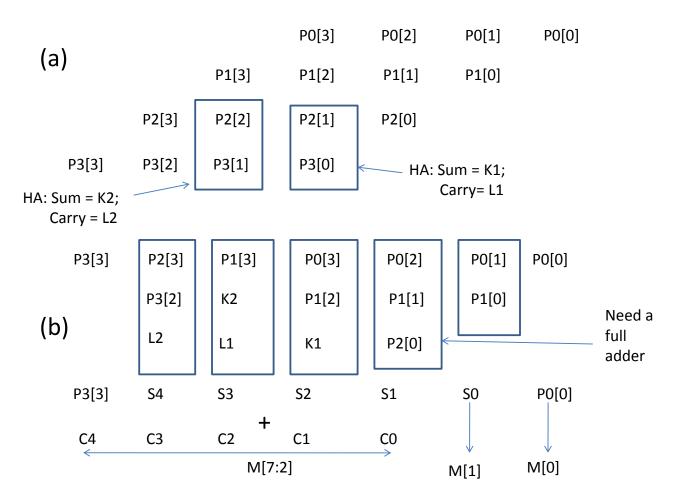


Figure 1: Wallace Multiplier

3 Tasks to be Performed

Task 1: Complete the Verilog module below to describe the functionality of the Wallace multiplier.

Task 2: Write a Verilog testbench and simulate the Wallace multiplier.

Task 3: Write a ".ucf" file, implement the design of the Wallace multiplier (for different input sets) on the FPGA board and show the output on the LCD. Use the LCD code given for the first assignment.

Optional Task 4: Extend the code to an 8-bit Wallace multiplier.