EE5331-DSP Architectures and Embedded Systems

Programming Assignment 4

1 Introduction

In this assignment, the objective is to complete a partially-filled (Verilog) design of conventional CORDIC operating in vectoring mode (to find arctan). You also need to write a testbench file (in Verilog) and do a simulation. Your program should handle a vector in any of the four quadrants in the plane.

2 Tasks to be Performed

Task 1: Complete the Verilog module below to describe the vectoring mode CORDIC.

```
module cordic
(input        clk,
 input ..... x_in, y_in,
 output reg  r, phi);


  // fill in reg declarations suitably
  reg ......


// if vector is in first or fourth quadrant, can
// proceed to do rotations by 45 (-45), 26.5 (-26.5) etc.
// else need to rotate by 90 or -90 depending
// the location (second/third quadrant)
  always @(posedge clk) begin
    if (x_in >= 0)             // Test for x_in
      begin
      x[0] <= x_in;
      y[0] <= y_in;
      z[0] <= 0;
      end
    else if (y_in >= 0) // if x_in < 0, check y ...
      begin
      ......
      ......
      ......
      end
    else
      begin
      ..........
      ...........
      ..........
      end
```

```
//rotate by plusorminus 45
// accordingly assign to x, y and z


if (y[0] >= 0)
  begin
  x[1] <= ...........
  y[1] <= ............
  z[1] <= ............
  end
else
  begin
  x[1] <= ............
  y[1] <= ............
  z[1] <= ..............
  end


 //rotate by plusorminus 26.5
// accordingly assign to x, y and z

if (y[1] >= 0)
  begin
  x[2] <= ................................
  y[2] <= ..................................
  z[2] <= ..................
  end
else
  begin
  ........................
  ......................
  ................
  end

 //rotate by plusorminus 14.1 (or approx 14 degrees)
// accordingly assign to x, y and z
if (y[2] >= 0)
  begin
    ......................
     ..............
    ..............
  end
else
  begin
    ..............................
    ..................
    ................
  end
```

```
     // continue to make small rotations by plusorminus 7 deg
     .......


    // fill code for still smaller rotations
        ......................

    // make assignments to r, phi suitably
    ...................
    ...................

  end

endmodule
```

Note: Angles can be output in degrees. Also, fractional parts can be handled by multiplying by a factor of 100 for instance. As an example, an angle like 26.56 can be displayed as 2656.

Task 2: Write a testbench for conventional CORDIC in vectoring mode and do a simulation. Explain the results of the simulation.