Ippili Sidhartha Kumar

Masters in Electronic Systems, Electrical Engineering, IIT Bombay

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AREAS OF INTEREST

Digital VLSI design, Computer Architecture, Domain-specific accelerated computing, Embedded Systems

EDUCATION

Examination	University	Institute	Year	CPI/%
Post Graduation	IIT Bombay	IIT Bombay	2022	9.84
Post Graduate Specialization: *Electronic Systems*				
Graduation	NIT Rourkela	NIT Rourkela	2019	8.86
Graduation Specialization: *Electronics & Instrumentation Engineering*				
Intermediate	CBSE	K. V. No. 1, Bhubaneswar	2015	92 %
Matriculation	CBSE	K. V. No. 1, Bhubaneswar	2013	10

MAJOR PROJECT AND SEMINAR

Guide: *Prof. Sachin B. Patkar, Department of Electrical Engineering, IIT Bombay*

- **M.Tech. Project: Acceleration of Cryptographic algorithms using custom hardware** *Jun '21 - July '22*
  - Objective - To design specialized hardware systems for acceleration of post-quantum cryptographic algorithms using hardware/software co-design
  - Reviewed literature on various post-quantum cryptographic algorithms like **lattice based Ring-LWE**
  - Developing hardware accelerators for polynomial multiplication which are highly parallelizable and can be configured to handle variable dimensions for **post-quantum cryptographic** applications
  - Developing scalable **post-quantum cryptoprocessors**, Integration of the developed accelerators with **RISC-V cores** in the form of off-load engine
  - Development of accelerators for large scale primitives of Zero Knowledge Proofs like NTT and MSM
- **M.Tech. Seminar: Custom hardware based acceleration of algorithms** *Aug - Dec '20*
  - Reviewed literature on Xilinx **Vivado HLS** and high-speed data transfer mechanisms like **AXI** BUS protocol
  - Case study: hardware based acceleration of stereo-depth estimation which uses custom logic based disparity estimation unit along with software running on ARM SoCs.

KEY COURSE PROJECTS

- **32×32 Matrix-vector Product Accelerator** *Jul - Dec '20*
  Instructor: *Prof. Madhav Desai, Dept. of EE, IIT Bombay* *(Algorithmic Design of Digital Systems)*
  - Designed a **hardware accelerator** for matrix-vector product calculation in **Aa language**
  - Performance was improved using **pipeline parallel** architecture and **memory banking**
- **FPGA based image compression and encryption system** *Jan - May '20*
  Instructor: *Prof. Sachin Patkar, Dept. of EE, IIT Bombay* *(VLSI Design Lab)*
  - **DWT** based compression (**BSV**) and AES-128 encryption (**Verilog**) was implemented as a **co-processor** unit
  - Tested the design using **NIOS II soft-core** and Nios II Software Build Tools on Intel DE0-Nano
- **4-input/4-output Packet switch** *Jul - Dec '20*
  Instructor: *Prof. Madhav Desai, Dept. of EE, IIT Bombay* *(Algorithmic Design of Digital Systems)*
  - Designed a packet switch for routing data packets in Aa language which generated **VHDL** model
  - **C/RTL co-simulation** was done using GHDL and **AHIR toolchain** that covered various port scenarios
- **32-bit Dadda Multiplier RTL design** *Jul - Dec '19*
  Instructor: *Prof. Dinesh Sharma, Dept. of EE, IIT Bombay* *(VLSI Design)*
  - Designed a parameterized PHP script to generate **VHDL** code for all reduction stages of Dadda multiplier which supports variable data-width multiplication and used Brent-Kung adder for final addition
- **16-bit Brent Kung adder ASIC design** *Jul - Dec '19*
  Instructor: *Prof. Dinesh Sharma, Dept. of EE, IIT Bombay* *(VLSI Design)*
  - Designed 32-bit logarithmic (Brent Kung) adder in VHDL and determined the critical path delay
  - Designed layout of 16-bit Brent Kung Adder using **Cadence Virtuoso** and extracted the delays
- **16-bit 8-point FFT processor RTL Design** *Feb - Mar '19*
  Guide: *Prof. Debiprasad P Acharya, Dept. of ECE, NIT Rourkela* *(Reconfigurable Systems Design Lab)*
  - Implemented **pipelined FFT processor** in Verilog that calculates the DFT sequence of 16-bit fixed point input sequence using decimation-in-time algorithm
- **CNF builder framework for use in verification** *Jan - May '21*
  Instructor: *Prof. Madhav Desai, Dept. of EE, IIT Bombay* *(Testing and Verification of VLSI Circuits)*
  - Designed light-weight C++ library for manipulation of logical expressions in conjuctive normal form (CNF)
  - Used the framework for generating fault test patterns and verifying FSM equivalence

RELEVANT COURSES

• Hardware Description • VLSI Design • VLSI Design Lab • Advanced Computer Architecture • Processor Design
• Embedded Systems Design • Testing & Verification of VLSI Circuits • Algorithmic Design of Digital Systems

RESEARCH & DEVELOPMENT PROJECTS

- **Zero-based timetabling for Indian Railways** *Apr - Oct '20*
  Guide: *Prof. Madhu N Belur, Department of Electrical Engineering, IIT Bombay*
  - Added network simulation and multi-train linking functionality to a single-section train simulator which enabled efficient simultaneous multi-route simulation
  - Implemented various optimization techniques in the simulator which reduced simulation time significantly

WORK EXPERIENCE

- **Cyber Physical Systems Lab, IIIT Delhi** | Research Intern *May - Jul 18*
  Guide: *Dr. P. B. Sujit, Dept. of ECE*
  Topic: Implementation of Model Predictive Control based cooperative target defence using ground-rovers
  - Interfaced a MATLAB based 3-agent control algorithm with remotely controlled ground rovers using ROS
  - Optimized the reaction delay by modifying the rovers' on-board controller firmware and developed browser-based visualization tool for realtime GPS data collection
- **Drubus Technologies Pvt. Limited** | Summer Intern *May - Jul '17*
  Advisor: *Sanjay Kumar Mitra, Co-founder and CTO*
  - **Multi-tenancy Infrastructure development for Cloud Applications** - facilitated deployment of web applications in a distributed system for multiple clients while ensuring high availability.
  - **Multi-threaded Pooling Mechanism** - Implemented various scheduling algorithms to share resources among multiple web clients to ensure fair service access.

TECHNICAL SKILLS

- **Languages**: Verilog, VHDL, Bluespec System Verilog (BSV), C, C++, PHP, Python
- **Software Tools**: Intel Quartus, Xilinx Vivado HLS, Modelsim, GHDL, Git
- **Hardware Platforms**: Intel DE0-Nano, TUL Pynq-Z2, Xilinx Zynq-7000, Xilinx Kintex-7, Raspberry Pi 3B+

PUBLICATION

- A. Manoharan et al., "NMPC Based Approach for Cooperative Target Defence," 2019 American Control Conference (ACC), 2019, pp. 5292-5297, doi: 10.23919/ACC.2019.8815386.

SELF PROJECTS

- **Pipelined RISC processor** *Mar - May '21*
  - Designed a 6-stage **pipelined** RISC processor based on IITB-RISC ISA in **VHDL** and **Verilog**
  - Implemented **data forwarding** and **branch prediction** units for improving performance
  - Designed a PHP based **instruction simulator** for ISA verification of the RTL design
- **4-way Out-of-order RISC processor** *Jul - Aug '21*
  - Designed a 4-way fetch, pipelined **superscalar** processor which supports a subset of **RISC-V 32-bit Base Integer Instruction Set** using **Bluespec System Verilog**
- **Design of Hack processor ecosystem (Nand2Tetris)** *Mar - May '21*
  - Implemented multi-cycle processor based on the Hack ISA (part of Nand2Tetris course) in Verilog
  - Implemented two-stage (high level and stack based virtual machine) compiler for Hack ISA in PHP
- **Raspberry Pi based bare metal digital oscilloscope framework** *May '19 - Present*
  - Designed a bare metal C++ based light-weight oscilloscope environment using open source frameworks

POSITION OF RESPONSIBILITIES

- **System Administrator** | Electrical Engineering Department, IIT Bombay *Jul '19 - Present*
  - Responsible for development of EE department website and maintaining web servers
  - **Automated** handling of various administrative tasks by designing web portals to reduce manual efforts
  - **Digitized** and automated M.Tech RA admission process through design of portals for online admissions
- **Student Companion** | Institute Student Companion Programme, IIT Bombay *Jul '20 - Jun '21*
  - **Mentored** 7 students, helping them on academic and non-academic fronts during Covid-19 pandemic.
  - Helped the Department Coordinator in compiling and developing the department's Master's handbook that serves as an informative manual to PG freshmen.

SCHOLASTIC ACHIEVEMENTS AND EXTRACURRICULAR ACTIVITIES

- Currently ranked **6th** among **131 M.Tech. students** of Electrical Engineering department
- Achieved **98.99 percentile** in **GATE** 2019 (Computer Science) among **99,932 candidates**
- Received Medhabruti State Scholarship 2015-19 (Merit-cum-means) for Technical Studies (Govt. of Odisha)
- Received **Academic Excellence Award** for securing **first** position in the department in 2015-16 (B.Tech)
- Interests and hobbies - Badminton, Movies, Swimming