Sidhartha Kumar Ippili

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Education

Indian Institute of Technology — Mumbai, India

Masters in Electronic Systems; ***GPA: 9.84/10*** — July 2019 - June 2022

National Institute of Technology — Rourkela, India

Bachelors in Electronics and Instrumentation Engineering; ***GPA: 8.86/10*** — July 2015 - May 2019

Work Experience

Texas Instruments Pvt. Ltd. (Full-time) — Bengaluru, India

Digital Design Engineer, Radar R&D — August 2022 - Present

- Working on pre-Silicon validation of Radar SoCs using in-circuit emulation on Cadence Palladium hardware
- Owned emulation setup for one product which involves building emulation image from design RTL and made significant enhancements in the build flow, feature-set e.g. **integration of UPF power intent onto Cadence emulation platform**, resulting in enhanced validation quality and reduction of turnaround time when migrating to newer design RTL release
- Developed **Python based framework to generate synthesizable RTL** of testbench for emulation platform to expose the design to various complex use-cases in pre-Si stage
- Worked on validation of **ethernet IP** by implementing various complex software datapaths while meeting system performance in memory-constrained devices. This included generation of UDP and PTP packets and transmitting them over 1 Gbps interface which was implemented in bare-metal C code
- Developed system level test scenarios and implemented them in Embedded C to uncover RTL bugs/corner-case misses
- Mentored several interns working on range of activities including development of product agnostic automation flows for better reuse, power aware emulation, cache architecture exploration using processor benchmarks

Cyber-Physical Systems Lab (Research Intern) — IIIT Delhi

Guide: Dr. P. B. Sujit, Dept. of ECE — May - Jul 18

- Topic: Implementation of Model Predictive Control based cooperative target defence using ground-rovers
- Interfaced a MATLAB based 3-agent control algorithm with remotely controlled ground rovers using ROS
- Optimized the reaction delay by modifying the rovers' on-board controller firmware and developed browser-based visualization tool for realtime GPS data collection

Drubus Technologies Pvt. Limited (Summer Intern) — Bhubaneswar, India

Advisor: Sanjay Kumar Mitra, Co-founder and CTO — May - Jul '17

- Multi-tenancy Infrastructure development for Cloud Applications - facilitated deployment of web applications in a distributed system for multiple clients while ensuring high availability
- Multi-threaded Pooling Mechanism - Implemented various scheduling algorithms to share resources among multiple web clients to ensure fair service access

Research and Academic Projects

HW/SW co-design based acceleration of post-quantum cryptographic algorithms — IIT Bombay

M.Tech. Project, Guide: Prof. Sachin Patkar, Dept. of EE — Jun '21 - July '22

- Developed hardware accelerators for polynomial multiplication which are highly parallel and can be configured to handle variable dimensions for post-quantum cryptographic applications
- Development of accelerators for large scale primitives of Zero Knowledge Proofs like high order Number Theoretic Transform and Multi-Scalar Multiplication
- Integration of the developed accelerators with Xilinx Micro-blaze core in the form of off-load engine

Cache conflict based attack on randomized cache — Jun '21 - July '22

Instructor: Prof. Biswabandan Panda, Dept. of CSE, IIT Bombay (Comp. Arch. for Performance & Security)

- Attempted to exploit the knowledge of replacement policy used to mount side-channel attack on last level randomized cache
- Analysed the extent to which prime+probe attack can affect randomized cache using a trace based architecture simulator (ChampSim)

32×32 Matrix-vector Product Accelerator — Jul - Dec '20

Instructor: Prof. Madhav Desai, Dept. of EE, IT Bombay (Algorithmic Design of Digital Systems)

- Designed a **hardware accelerator** for matrix-vector product calculation in **Aa language**

- Performance was improved using **pipeline parallel** architecture and **memory banking**

FPGA based image compression and encryption system Jan - May '20

Instructor: Prof. Sachin Patkar, Dept. of EE, IIT Bombay (VLSI Design Lab)

- **DWT** based compression implemented in BSV and AES-128 encryption implemented in Verilog was implemented as a **co-processor** unit
- Tested the design using **NIOS II soft-core** and Nios II Software Build Tools on Intel DE0-Nano

4-input/4-output Packet switch Jul - Dec '20

Instructor: Prof. Madhav Desai, Dept. of EE, IIT Bombay (Algorithmic Design of Digital Systems)

- Designed a packet switch for routing data packets in Aa language which generated **VHDL** model
- **C/RTL co-simulation** was done using GHDL and **AHIR toolchain** that covered various port scenarios

32-bit Dadda Multiplier RTL design Jul - Dec '19

Instructor: Prof. Dinesh Sharma, Dept. of EE, IIT Bombay (VLSI Design)

- Designed a parameterized PHP script to generate **VHDL** code for all reduction stages of Dadda multiplier which supports variable data-width multiplication and used Brent-Kung adder for final addition

16-bit Brent Kung adder ASIC design Jul - Dec '19

Instructor: Prof. Dinesh Sharma, Dept. of EE, IIT Bombay (VLSI Design)

- Designed 32-bit logarithmic (Brent Kung) adder in VHDL and determined the critical path delay
- Designed layout of 16-bit Brent Kung Adder using **Cadence Virtuoso** and extracted the delays

16-bit 8-point FFT processor RTL Design Feb - Mar '19

Guide: Prof. Debiprasad P Acharya, Dept. of ECE, NIT Rourkela (Reconfigurable Systems Design Lab)

- Implemented **pipelined FFT processor** in Verilog that calculates the DFT sequence of 16-bit fixed point input sequence using decimation-in-time algorithm

CNF builder framework for use in verification Jan - May '21

Instructor: Prof. Madhav Desai, Dept. of EE, IIT Bombay (Testing and Verification of VLSI Circuits)

- Designed light-weight C++ library for manipulation of logical expressions in conjunctive normal form (CNF)
- Used the framework for generating fault test patterns and verifying FSM equivalence

Awards and Achievements

- Achieved 98.99 percentile in GATE 2019 (Computer Science) among 99,932 candidates
- Received Medhabruti State Scholarship 2015-19 (Merit-cum-means) for Technical Studies (Govt. of Odisha)
- Received Academic Excellence Award for securing first position in the department in 2015-16 (B.Tech)

Publications

- **Unified Design Verification Flow for Pre-Silicon SoC Power Estimation And Achieving Post-Silicon Correlation to Customer Sampling**, *Poster presentation in 60th Design Automation Conference (DAC 2023), link*
- **NMPC Based Approach for Cooperative Target Defence**, *American Control Conference (ACC), 2019, pp. 5292-5297, doi: 10.23919/ACC.2019.8815386.*

Key Courses

Courses: Hardware Description, VLSI Design, VLSI Design Lab, Advanced Computer Architecture, Processor Design, Embedded Systems Design, Testing & Verification of VLSI Circuits, Algorithmic Design of Digital Systems

Skills Summary

Languages: Verilog, VHDL, Embedded C, Python, Assembly, System Verilog

Platforms: Linux, Windows, Git