

## **IV<sup>th</sup> Semester Computer Science and Engineering & Information Technology**

1. To implement Amplitude Modulation (AM), Demodulation and calculate the modulation index.
2. To implement Frequency Modulation (FM), using IC-2206 and demodulation using IC-565.
3. To implement Pulse Amplitude Modulation (PAM), and demodulation.
4. To implement Pulse Width Modulation (PWM).
5. To implement Pulse Position Modulation (PPM).
6. To perform Amplitude Shift Keying (ASK) modulation and Demodulation.
7. To perform Frequency Shift Keying (FSK) modulation and demodulation.
8. To implement Phase Lock Lock (PLL) and find out the look range capture range.
9. To design and test the circuit of voltage to Frequency Converter (VCO) using IC-555.
10. To study Digital Phase Detector (DPD) and to detect the phase difference between two sinusoidal waves.

# EXPERIMENT NUMBER 1

## Amplitude Modulation & Demodulation

**AIM:** To perform amplitude modulation and demodulation and calculate the modulation index for various modulating voltages and plot the relevant waveforms.

### LEARNING OBJECTIVE:

- To provide a familiarization to generate an amplitude-modulated (AM) signal, with an adjustable modulation factor ( $m$ ).
- To examine both time & frequency displays of an AM signal.
- To measure the percentage modulation ( $m\%$ ), and the percentage of total power in both sidebands and in the carrier versus the modulation index ( $m$ ).
- To investigate the use (& limitation) of envelope detection in demodulating AM signals.

**PRIOR CONCEPTS:** Modulation and its types, Frequency and Amplitude variance, Sampling Theorem.

### EQUIPMENT REQUIRED

Equipment	Range	Quantity
CRO	(0-20)MHz	1
Function Generator	(0-1)MHz	2
Experiment Kit		1
Power Supply	(0-30)V	1

### COMPONENTS REQUIRED

Components	Value	Quantity
Transistor	BC307	1
Capacitor	0.01μF	2
	0.1μF	1
	10μF	1
Resistor	10kΩ	1
	1kΩ	1
	22kΩ	1
	1.2KΩ	3
Diode	IN4001	1

**THEORY:** Modulation is defined as the process by which some characteristics of a carrier signal is varied in accordance with a modulating signal. The base band signal is referred to as the modulating signal and the output of the modulation process is called as the modulated signal. Amplitude modulation is defined as the process in which the amplitude of the sinusoidal carrier wave is varied in accordance with the base band signal. The envelope of the modulating wave has the same shape as the base band signal provided the following two requirements are satisfied.

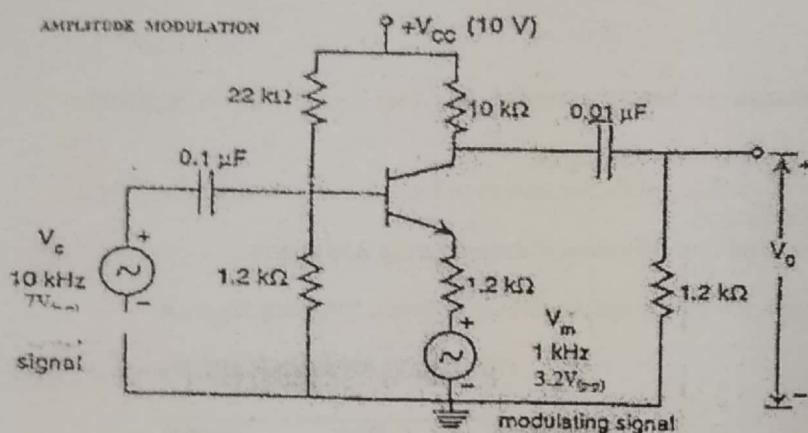
1. The carrier frequency  $f_c$  must be much greater than the highest frequency components  $f_m$  of the message signal  $m(t)$  i.e.  $f_c \gg f_m$ .
2. The modulation index must be less than unity. If the modulation index is greater than unity, the carrier wave becomes over modulated.

### PROCEDURE

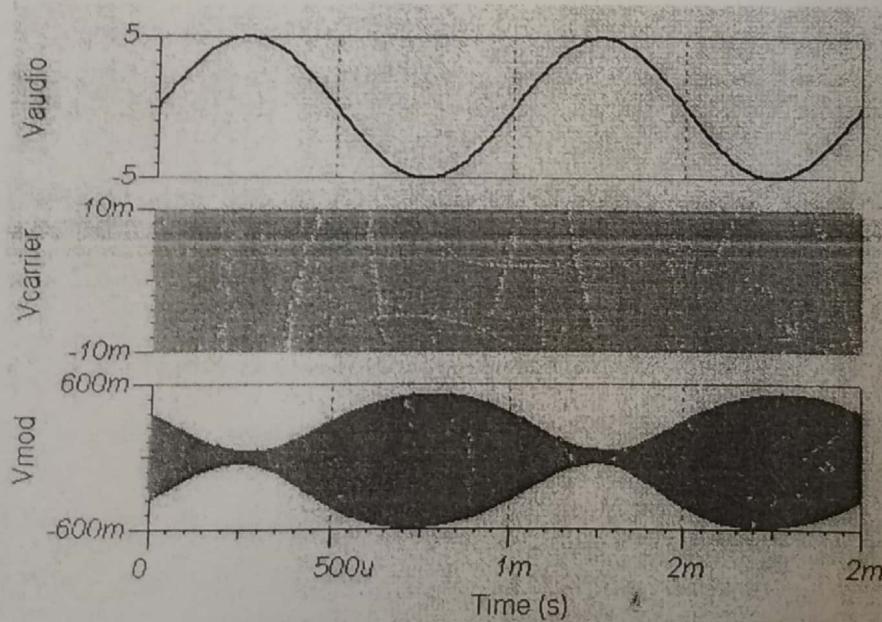
1. Connections are made as shown in the circuit diagram.
2. The power supply is connected to the collector of the transistor.
3. Modulated Output is taken from the collector of the transistor.
4. Carrier signal is set to 3.2V<sub>(p-p)</sub>, 10 KHz using function generator.
5. Modulating signal is set to around 3.2V<sub>(p-p)</sub>, 1 KHz (with a +2V dc - offset) and amplitude is varied around the carrier voltage.
6. Calculate  $F_{max}$  and  $F_{min}$  from the output waveform.
7. Calculate the modulation index using the formula

$$f_{\text{pulsed}} = \frac{F_{\text{max}} - F_{\text{min}}}{F_{\text{max}} + F_{\text{min}}} ,$$

### CIRCUIT DIAGRAM



### WAVEFORM



### Lab Report

The AM Broadcast station technical standards specify that the % modulation be maintained @ 85 - 95%; comment on any possible disadvantages [based on your experimental results] that will occur by ignoring this specification.

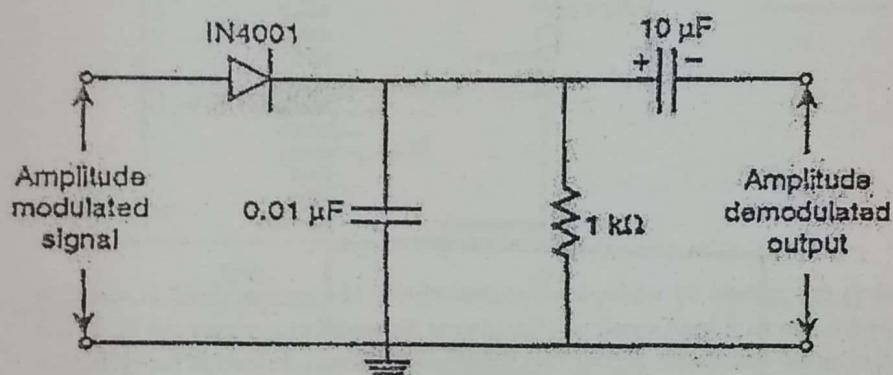
## Amplitude Demodulation

The process of detection provides a means of recovering the modulating Signal from demodulating signal. Demodulation is the reverse process of modulation. The detector circuit is employed to separate the carrier wave and eliminate the side bands. Since the envelope of an AM wave has the same shape as the message, independent of the carrier frequency and phase, demodulation can be accomplished by extracting envelope.

### PROCEDURE

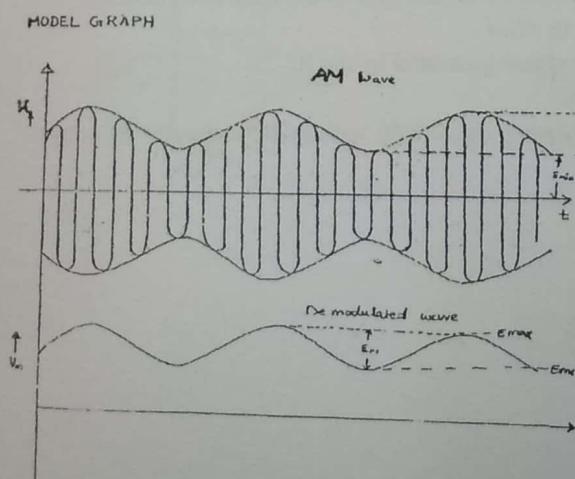
1. Connections are made as shown in the circuit diagram.
2. The amplitude modulated signal from AM generator is given as input to the circuit
3. The demodulated output is observed on the CRO.
4. Various values of modulating voltage signal frequency corresponding to demodulated voltage and frequency are noted and the readings are compared (both must be same in all parameters).

### CIRCUIT DIAGRAM AND OPERATING PRINCIPLE



The detection of AM signals is accomplished by means of a diode rectifier which may be either a vacuum tube or a semiconductor diode. The demodulator must meet three requirements: (1) It must be sensitive to the type of modulation applied at the input, (2) it must be nonlinear, and (3) it must provide filtering. Because the semiconductor is a nonlinear device, it conducts in only one direction. This eliminates the negative portion of the RF carrier and reproduces the signal.

### WAVEFORM



## EXPERIMENT NUMBER 2

### Frequency Modulation & Demodulation

**AIM:** To perform frequency modulation and demodulation and for various modulating voltages and plot the relevant waveforms.

#### EQUIPMENT REQUIRED

Equipment	Range	Quantity
CRO	(0-20)MHz	1
Function Generator	(0-1)MHz	2
Experiment Kit		1
Power Supply	+12V	1
Multimeter		

#### COMPONENTS REQUIRED

Components	Value	Quantity
IC	IC2206	1
IC	IC565	1
Capacitor	0.01μF	2
	1μF	2
	10μF	2
	100μF	2
	470μF	1
Resistor	-10kΩ	1
	1kΩ	1
	-10kΩ	1
	4.7kΩ	2
	47kΩ	1
	200Ω	1
	560Ω	2
Potentiometer	0-470kΩ	1

**THEORY:** Modulation is defined as the process by which some characteristics of a carrier signal is varied in accordance with a modulating signal. The base band signal is referred to as the modulating signal and the output of the modulation process is called as the modulation signal. Amplitude modulation is defined as the process in which the amplitude of the carrier wave is varied about a mean value linearly with the base band signal. The envelope of the modulating wave has the same shape as the base band signal provided the following two requirements are satisfied.

1. The carrier frequency  $f_c$  must be much greater than the highest frequency components  $f_m$  of the message signal  $m(t)$  i.e.  $f_c \gg f_m$ .
2. The modulation index must be less than unity. If the modulation index is greater than unity, the carrier wave becomes over modulated.

#### PROCEDURE:

1. Connections are made as shown in the circuit diagram; only potentiometer is not connected initially.
2. Another end of 1K resistor is grounded and  $V_{cc}$  is set to +12V.
3. Output is observed on the display which is the carrier signal generated by the IC.
4. Note down the carrier sine wave frequency  $f_c$  of the IC.
5. Now connect the potentiometer and apply the modulating signal  $m(t)$  with suitable amplitude to get undistorted FM signal.

#### DESIGN PROCEDURE

##### Design 1:

###### 1. FM Modulator Circuit

Let carrier frequency  $f_c = 3\text{ KHz}$ ,  $f_c = 0.3/\text{RC}_t$   
 Choose  $R = 10\text{K}\Omega = R_a = R_b$ , then  $C_t = 0.01\mu\text{f}$   
 Take  $R_L = 10\text{K}\Omega$ ,  $C_C = 0.01\mu\text{f}$

###### 2. Demodulator using PLL

Let  $f_o = f_c = 3\text{ KHz}$ ,  $f_o = 1.2/4R_1C_1$   
 Choose  $C_1 = 0.01\mu\text{f}$ , then  $R_1 = 100\text{ K}\Omega$   
 Filter Design: Let  $f_m = 1\text{ KHz} = 1/2\pi RC$   
 Choose  $C = 0.1\mu\text{f}$ , then  $R = 1.59\text{ K}\Omega$

Design 2:

1. FM Modulator Circuit

Let carrier frequency  $f_c = 5 \text{ KHz}$

Choose  $R = 10\text{K}\Omega = R_a = R_b$ , then  $C_t = 0.001\mu\text{F}$

Take  $R_L = 10\text{K}\Omega$ ,  $C_C = 0.01\mu\text{F}$

2. Demodulator using PLL

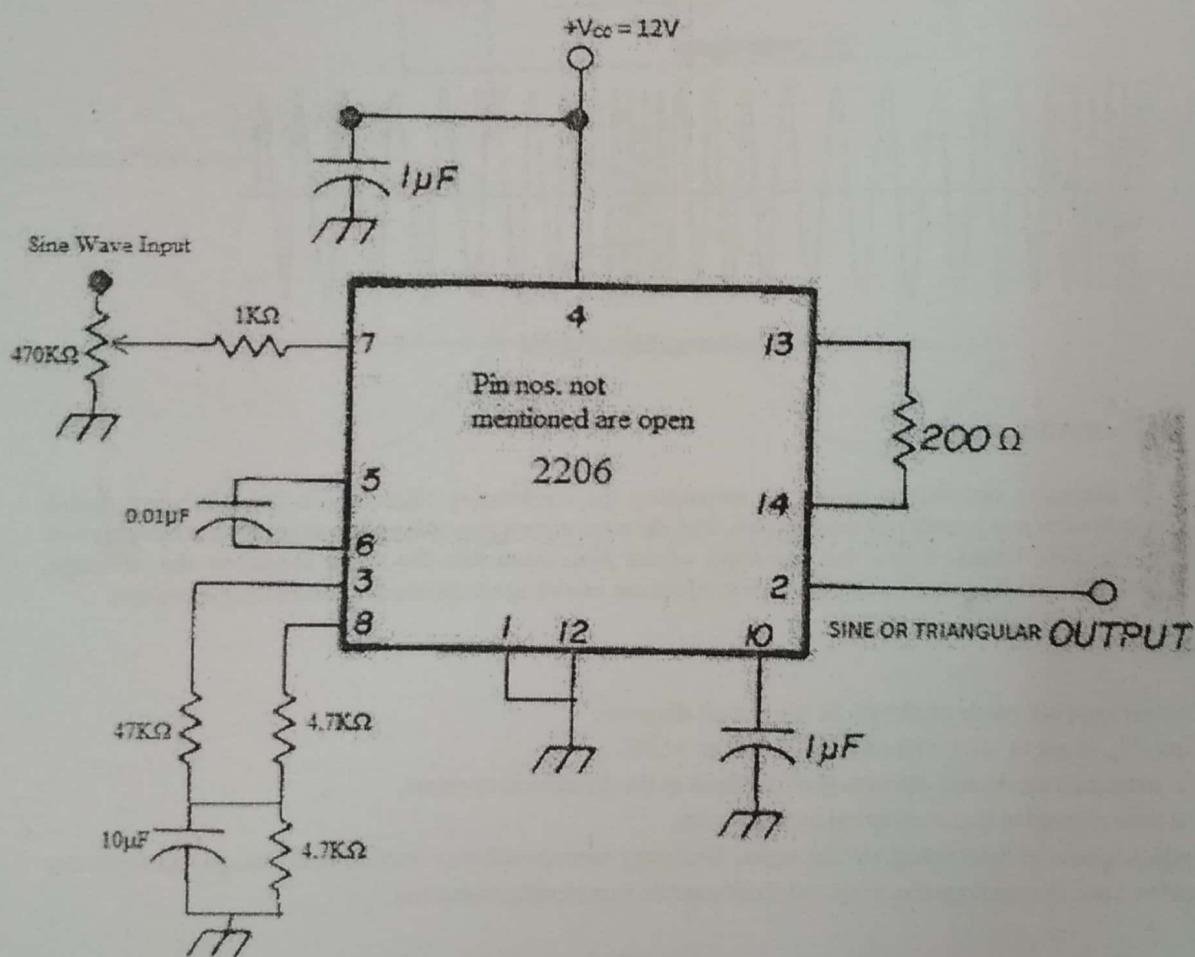
Let  $f_o = f_c = 3\text{ KHz}$ ,  $f_o = 1.2/4R_1C_1$

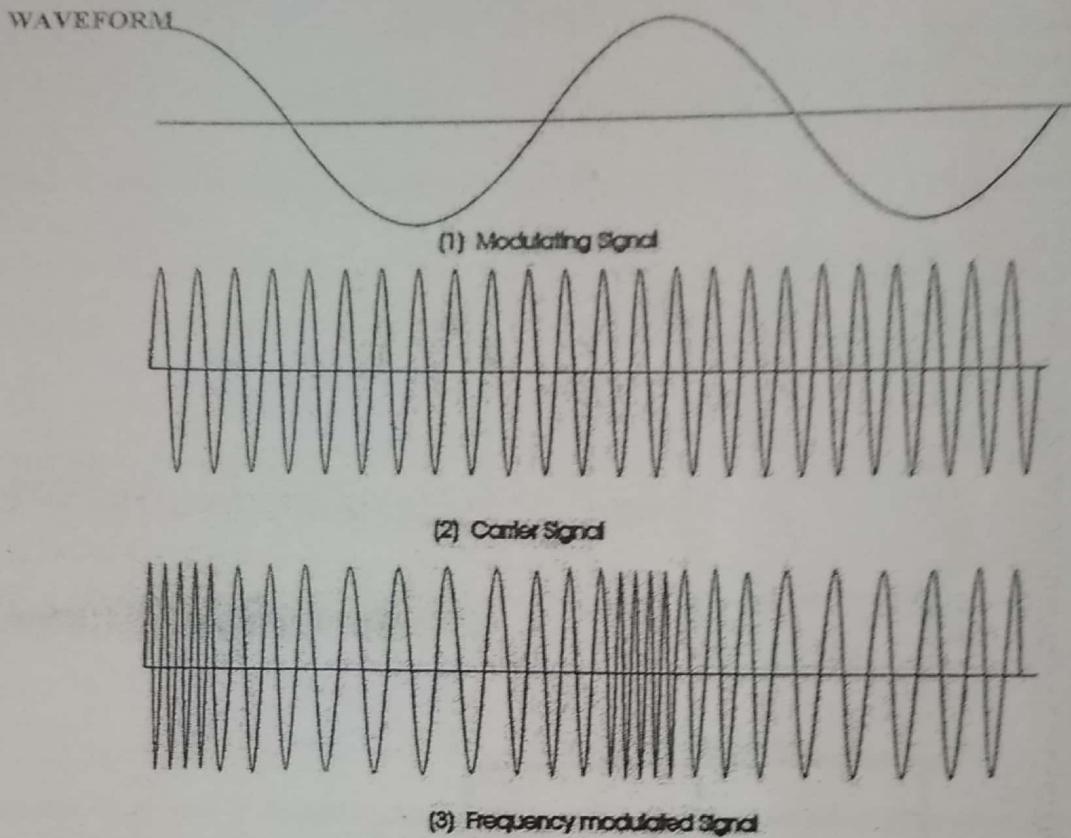
Choose  $C_1 = 0.001\mu\text{F}$ , then  $R_1 = 100 \text{ K}\Omega$

Filter Design: Let  $f_m = 1 \text{ KHz} = 1/2\pi RC$

Choose  $C = 0.1\mu\text{F}$ , then  $R = 1.59 \text{ K}\Omega$

CIRCUIT DIAGRAM





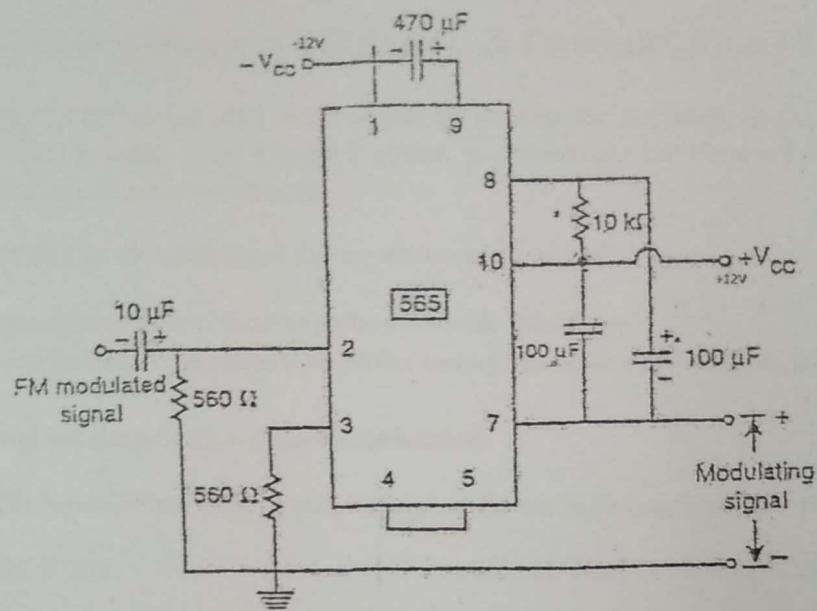
## Frequency Demodulation

The process of detection provides a means of recovering the modulating Signal from demodulating signal. Demodulation is the reverse process of modulation. The detector circuit is employed to separate the carrier wave and eliminate the side bands. Since the envelope of an AM wave has the same shape as the message, independent of the carrier frequency and phase, demodulation can be accomplished by extracting envelope.

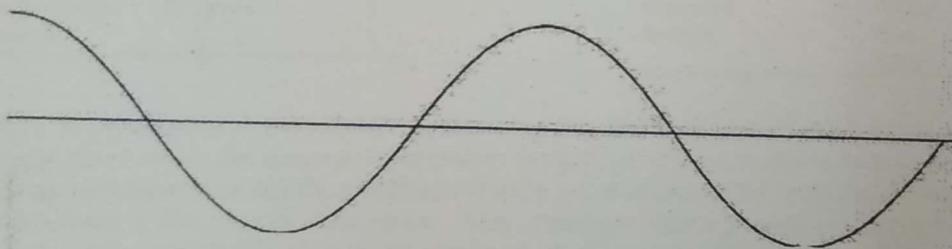
## PROCEDURE

1. Connections are made as shown in the circuit diagram.
2. Now  $-V_{cc}$  is set to -12V and  $+V_{cc}$  is set to +12V.
3. The frequency modulated signal is given as input to the demodulation circuit.
4. The demodulated output is observed on the display.
5. Various values of modulating voltage signal frequency corresponding to demodulated voltage and frequency are noted and the readings are compared (both must be same in all parameters).

## CIRCUIT DIAGRAM



Demodulated Waveform



## EXPERIMENT NUMBER 3

### Pulse Amplitude Modulation & Demodulation (PAM)

**AIM:** Conduct an experiment to generate PAM signal by varying the amplitude of the modulating signal and frequency of the sampling signal. Also design a circuit to demodulate the obtained PAM signal and verify sampling theorem. Plot the relevant waveforms.

**LEARNING OBJECTIVE:** To understand the waveform of PAM and:

- To understand the use of transistor as pulse amplitude modulator.
- To understand the use of operational amplifier and switching device (FET) as pulse amplitude modulator.
- To understand the classification of pulse modulation.

**PRIOR CONCEPTS:** Modulation and its types, Pulse modulation, Sampling Theorem, Nyquist Rate.

#### EQUIPMENT REQUIRED

Equipment	Range	Quantity
CRO	(0-20)MHz	1
Function Generator	(0-1)MHz	2
Experiment Kit		1

#### COMPONENTS REQUIRED

Components	Value	Quantity
Transistor	BC107	1
Capacitor	0.01μF	1
Resistor	10kΩ	2
	22kΩ	1

**THEORY:** Pulse-amplitude modulation is the simplest form of signal modulation and analog to digital conversion method where the message information is encoded in the amplitude of a series of signal pulses. It is a modulation technique in which the amplitude of each pulse is controlled by the instantaneous amplitude of the modulation signal at the time of each pulse. This technique transmits data by varying the voltage or power amplitudes of individual pulses in a timed sequence of electromagnetic pulses. In other words, the data to be transmitted is encoded in the amplitude of a series of signal pulses. Modulating a sine-wave carrier makes it possible to keep the frequency content of the transferred signal as close as possible to the centre frequency (typically the carrier frequency) of the pass band. There are two operations involved in the generation of PAM signal.

- i. Instantaneous sampling of modulating signal  $m(t)$  every  $T_s$  seconds where the sampling rate  $f_s = 1/T_s$  is chosen in accordance with the sampling theorem.
- ii. Lengthening the duration of each sample so obtained to some constant value  $T$ .

These two operations are jointly referred to as SAMPLE and HOLD.

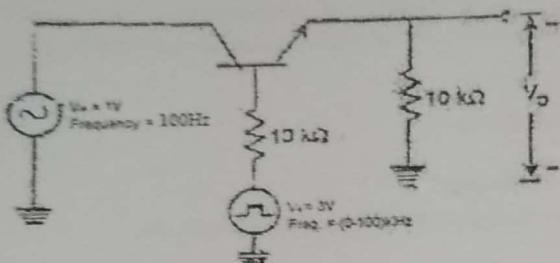
Demodulation is performed by detecting the amplitude level of the carrier at every symbol period.

#### PROCEDURE

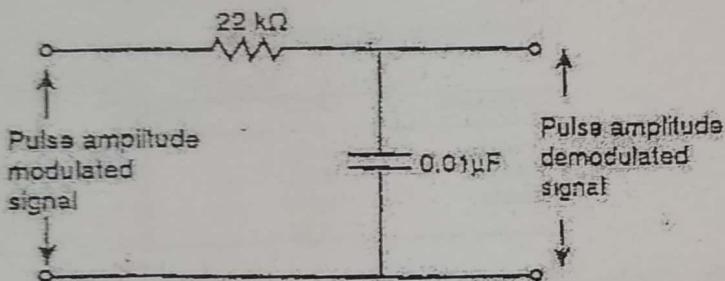
1. Connections are made as shown in the circuit diagram.
2. Apply the square wave carrier signal of around  $5V_{(p-p)}$  amplitude with frequency  $f_c = 5\text{ KHz}$  at the base.
3. Apply sine wave modulating signal with frequency  $f_m = 100\text{Hz}$  with  $2V_{(p-p)}$  amplitude (use function generator) at the collector of the transistor.  
*Note: frequency ranges mentioned above may vary from kit to kit. These values are just for your guidance.*
4. Output is taken at the emitter.
5. Observe the PAM output.
6. Modulated signal is fed to the input of demodulation circuit.
7. Observe the demodulated signal at the output.
8. Repeat the steps 2 to 5 for  $f_c = 2f_m$  and  $f_c < 2f_m$ .

## CIRCUIT DIAGRAM

### Pulse Amplitude Modulation



### Pulse Amplitude Demodulation

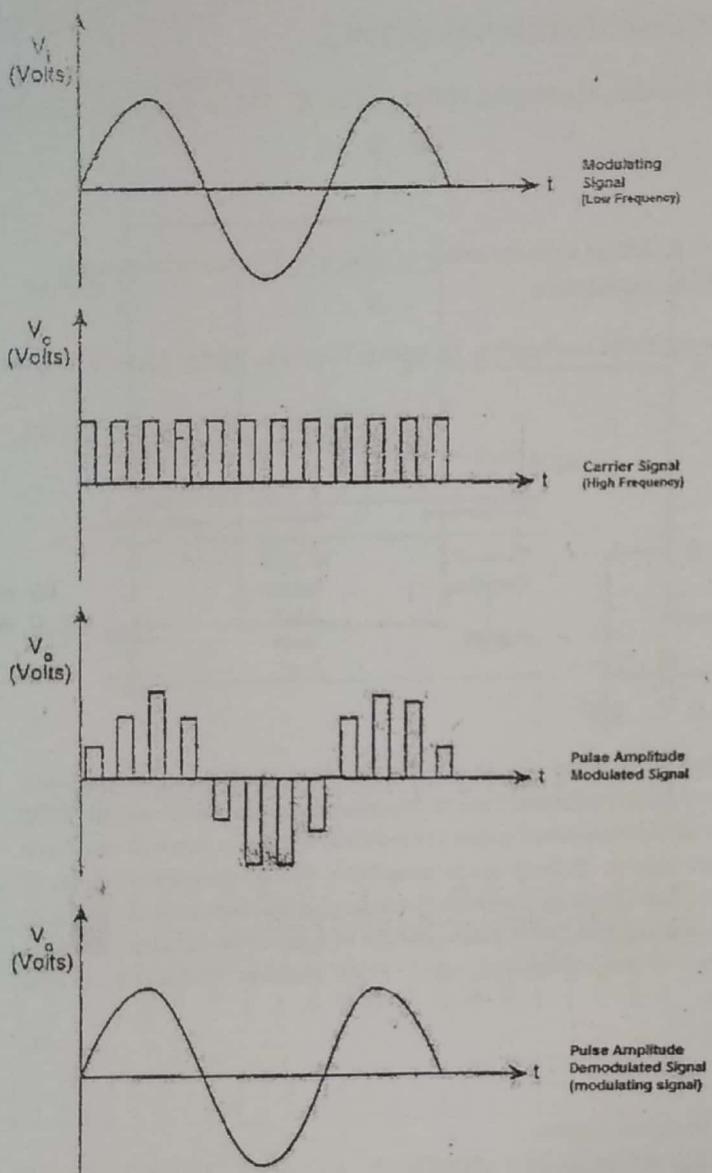


### OBSERVATIONS:

- Number of pulses obtained in one cycle of the modulating signal =
- Measure of the amplitude of each pulse =

**CONCLUSION:** Thus, in PAM, (amplitude/time/position) of carrier changes in accordance to the \_\_\_\_\_ of the modulating signal. Write the conclusion based on the amplitude (volts) of pulse count.

## WAVEFORMS:



## Lab Report

Write a paragraph about questions and confusions that you experienced while performing the experiment in this lab.

## EXPERIMENT NUMBER 4

### Pulse Position Modulation (PPM)

**AIM:** To understand and implement Pulse Position Modulation (PPM) using IC 555 and plot the relevant waveforms.

#### LEARNING OBJECTIVE:

- To understand the operation of Timer IC 555 as a multivibrator in astable and monostable mode.
- To understand the classification of Pulse modulation.

**PRIOR CONCEPTS:** Modulation and its types, Pulse modulation, Sampling Theorem, PWM, Timer IC 555 in monostable mode of operation.

#### EQUIPMENT REQUIRED

Equipment	Range	Quantity
CRO	[0-20]MHz	1
Function Generator	[0-1]MHz	2
Experiment Kit		1

#### COMPONENTS REQUIRED

Components	Value	Quantity	
Timer IC	IC 555	2	
Capacitor	0.01μF	1	10 μF
	0.1μF	2	100 μF
Resistor	10kΩ	2	
	1 kΩ	1	

**THEORY:** Modulation of a pulse carrier wherein the value of each instantaneous sample of a modulating wave varies the position in time of a pulse relative to its unmodulated time of occurrence. As the name implies, PPM is a data-encoding scheme where the position of the transmitted pulses is modified. Typically this will result in a long stream of pulses that are unevenly spaced in time. Pulse position modulation (PPM) uses pulses that are of uniform height and width but displaced in time from some base position according to the amplitude of the signal at the instant of sampling. The position of each pulse, in relation to the position of a recurrent reference pulse, is varied by each instantaneous sampled value of the modulating wave. Pulse position modulation is also sometimes known as pulse-phase modulation.

#### PROCEDURE

1. Connections are made as shown in the circuit diagram.
2. Vary the input (sine wave) between 5 to 15V at pin no. 5 of first IC.
3. Check the working of 555 timer as a monostable multivibrator by giving an unmodulated PWM signal. Verify the pulse width of output signal for the designed value.
4. By applying the PWM signal note the change in the position of the pulses i.e. PPM signal.
5. Plot the observed waveform for any one reading.

#### OBSERVATIONS:

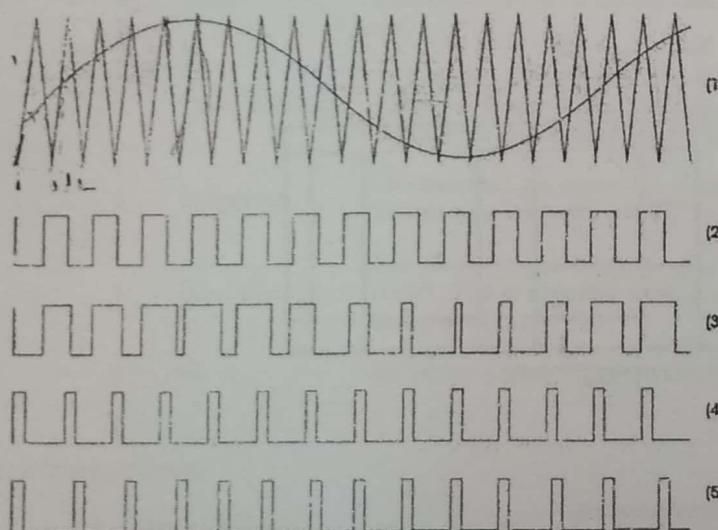
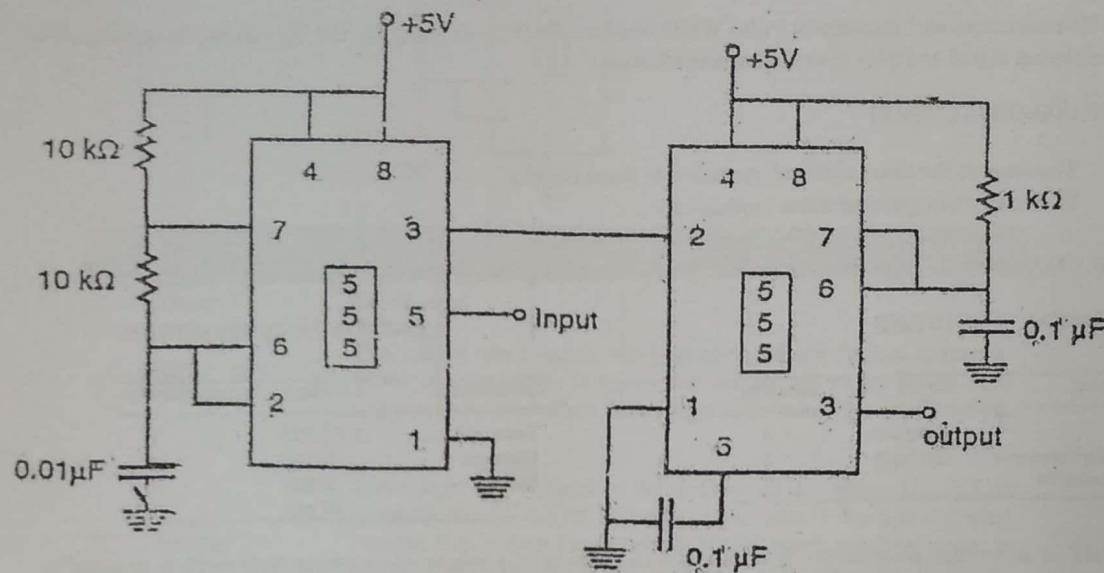
##### Measurement of Amplitude and Frequency of Various Waveforms

S.No.	Type of Signal	Amplitude	Frequency
1.	Modulating		
2.	Carrier		
3.	PWM		
4.	PPM		

**CONCLUSION:** Thus, in PPM, (amplitude/time/position) of carrier changes in accordance to the instantaneous \_\_\_\_\_ of the modulating signal. Write the conclusion based on the amplitude and position of pulses.

#### CIRCUIT DIAGRAM

Pulse Position Modulation



- (1) Modulating Signal & Triangular Signal
- (2) Comparator O/P (With zero Modulating Signal)
- (3) PWM
- (4) Monostable Multivibrator O/P (With zero Modulating Signal)
- (5) PPM

## EXPERIMENT NUMBER 5

### Pulse Width Modulation (PWM)

**AIM:** To understand and implement Pulse Width Modulation (PWM) using IC 555 by varying the amplitude of the modulating signal and plot the relevant waveforms.

**LEARNING OBJECTIVE:**

- To compare the two modes of operation of timer IC 555.
- To classify the types of pulse modulation.

**PRIOR CONCEPTS:** Types of Modulation, Amplitude modulation, Pulse modulation and Sampling Theorem.

**EQUIPMENT REQUIRED**

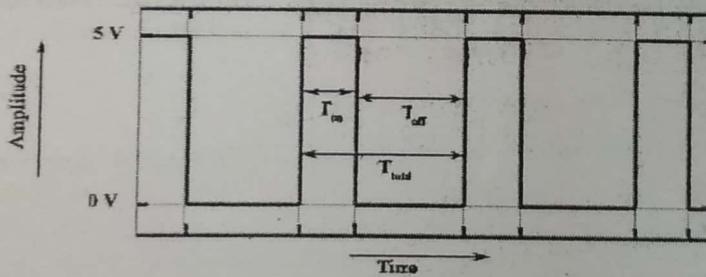
Equipment	Range	Quantity
CRO	(0-20)MHz	1
Function Generator	(0-1)MHz	2
Experiment Kit		1

**COMPONENTS REQUIRED**

Components	Value	Quantity
Timer IC	IC 555	1
Capacitor	0.01μF	1
Resistor	10kΩ	1
	47 kΩ	1

**THEORY:** Pulse-width Modulation is achieved with the help of a square wave whose duty cycle is changed to get a varying voltage output as a result of average value of waveform. The duty cycle is defined as the percentage of digital 'high' to digital 'low' signals present during a PWM period. Consider a square wave shown in the figure below.  $T_{on}$  is the time for which the output is high and  $T_{off}$  is time for which output is low. Let  $T_{total}$  be time period of the wave such that,

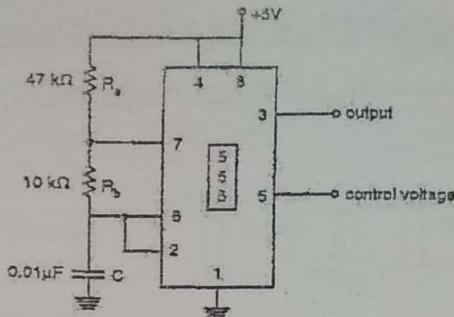
$$T_{total} = T_{on} + T_{off}$$



**PROCEDURE**

1. Connections are made as shown in the circuit diagram.
2. Vary the control voltage (0-5) V and observe the corresponding waveform.
3. Change in the control voltage changes the width of the square wave generated by the IC.
4. Note down  $T_{ON}$  and  $T_{OFF}$ .
5. Plot the observed waveform.

## CIRCUIT DIAGRAM OF PULSE WIDTH MODULATION



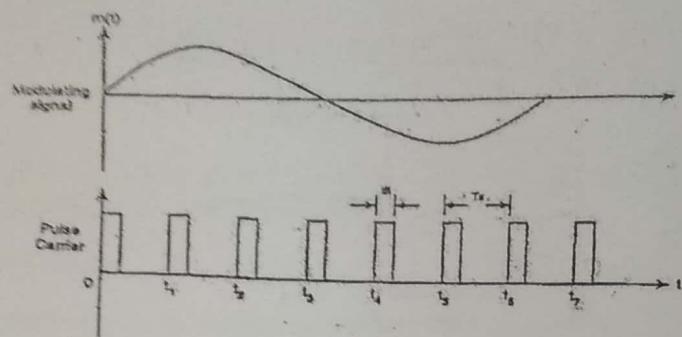
PIN	DESCRIPTION	PURPOSE
1	Ground	DC Ground
2	Trigger	The trigger pin triggers the beginning of the timing sequence. When it goes LOW, it causes the output pin to go HIGH. The trigger is activated when the voltage falls below 1/3 of +V on pin 8.
3	Output	The output pin is used to drive external circuitry. The HIGH output is usually about 1.7 volts lower than +V when sourcing current. The output pin is driven HIGH when the trigger pin is taken LOW. The output pin is driven LOW when the threshold pin is taken HIGH, or the reset pin is taken LOW.
4	Reset	The reset pin is used to drive the output LOW, regardless of the state of the circuit. When not used, the reset pin should be tied to +V.
5	Control Voltage	The control voltage pin allows the input of external voltages to affect the timing of the 555 chip. When not used, it should be bypassed to ground through an 0.01μF capacitor.
6	Threshold	The threshold pin causes the output to be driven LOW when its voltage rises above 2/3 of +V.
7	Discharge	The discharge pin shorts to ground when the output pin goes HIGH. This is normally used to discharge the timing capacitor during oscillation.
8	+V	DC Power - Apply +3 to +18VDC here.

### OBSERVATIONS:

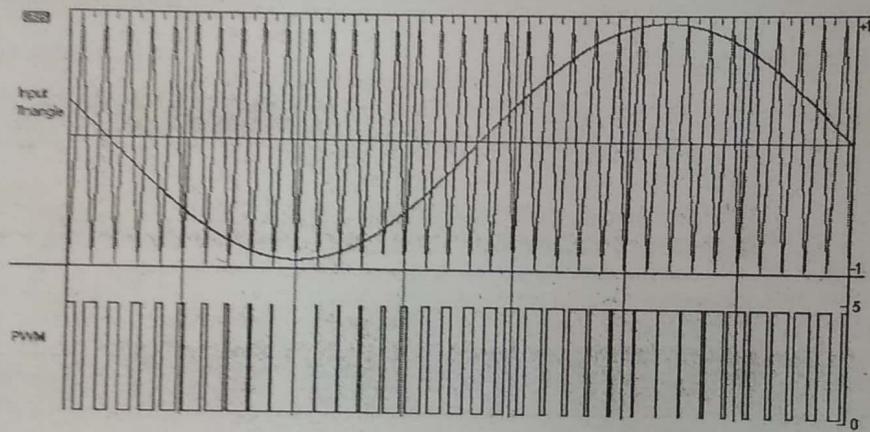
- $T_{ON}$  period of carrier signal (Output of  $IC_1$ ) =
- Total Period =  $T_{ON} + T_{OFF}$
- Amplitude of the carrier signal =
- Amplitude of the modulating signal =
- Frequency of the modulating signal =

**CONCLUSION:** Thus, in PWM, (width/amplitude//position) of carrier changes in accordance to the instantaneous \_\_\_\_\_ of the modulating signal. Write the conclusion based on the duty cycle

WAVEFORMS:



Sample Input-Output:



## EXPERIMENT NUMBER 4(a)

### Binary Frequency Shift Keying Modulator (B-FSK)

AIM: To study and implement Binary FSK modulation and demodulation schemes and to observe the waveform.

#### EQUIPMENT REQUIRED:

Equipment	Range	Quantity
CRO	(0-20) MHz	1
Function Generator	(0-1) MHz	1
Power Supply	(0-30) V +12V	1

#### COMPONENTS REQUIRED:

Component	Value	Quantity
IC	XR2206	1
Timer IC	555	1
PLL IC	565	1
Transistor	BC107	1
Op-amp	IC741	1
Diode		
Resistors	1K 10K 4.7K 100K	3 3 2 1
Capacitors	1nF 22uF .01uF 1uF	1 1 2 1

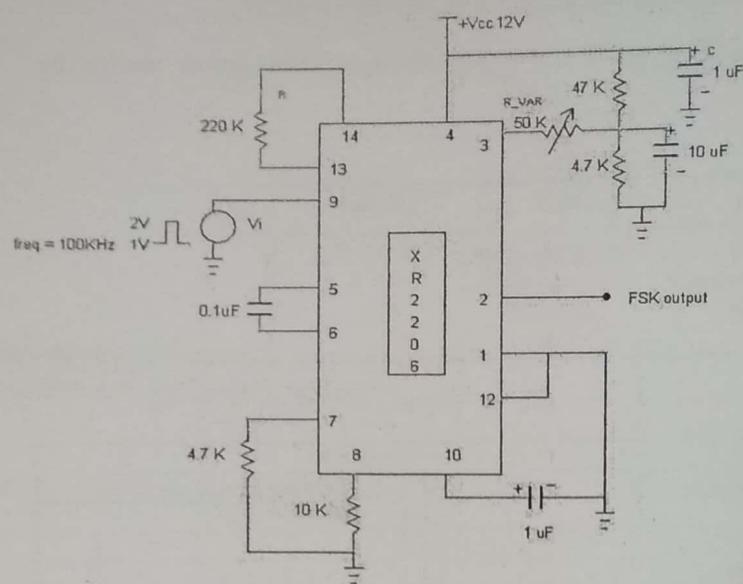
#### THEORY:

Frequency-shift keying (FSK) is a frequency modulation scheme in which digital information is transmitted through discrete frequency changes of a carrier wave. The two binary states logic 0 (low) and 1 (high) are represented by an analog waveform. Logic 0 is represented by a wave at a specific frequency, and logic 1 is represented by a wave at a different frequency. One frequency is designated as the "mark" frequency and the other as the "space" frequency. The mark and space frequency are corresponding to binary one and zero, respectively. FSK finds a wide range of application in low-speed digital data transmission systems. Their appeal is mainly due to the hardware advantages that result principally from the use of non-coherent demodulation process and the relative ease of signal generation.

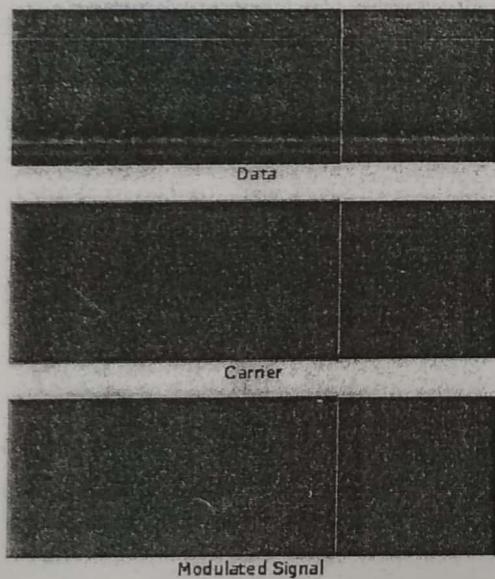
#### PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Set the AF input (say 1Vpp, 150Hz) using function generator.
3. Observe the output waveform on the CRO.
4. Plot the observed waveform on the CRO.
5. Identify the mark and space frequency.
6. Find the mark frequency ( $F_m$ ) and space frequency ( $F_s$ ).
7. Calculate the modulation index  $MI = |F_m - F_s|/(F_0/2)$  where  $F_0$  is the fundamental frequency of the input signal.

CIRCUIT DIAGRAM:



WAVEFORM:



## EXPERIMENT NUMBER 4(b)

### Binary Frequency Shift Keying Demodulator

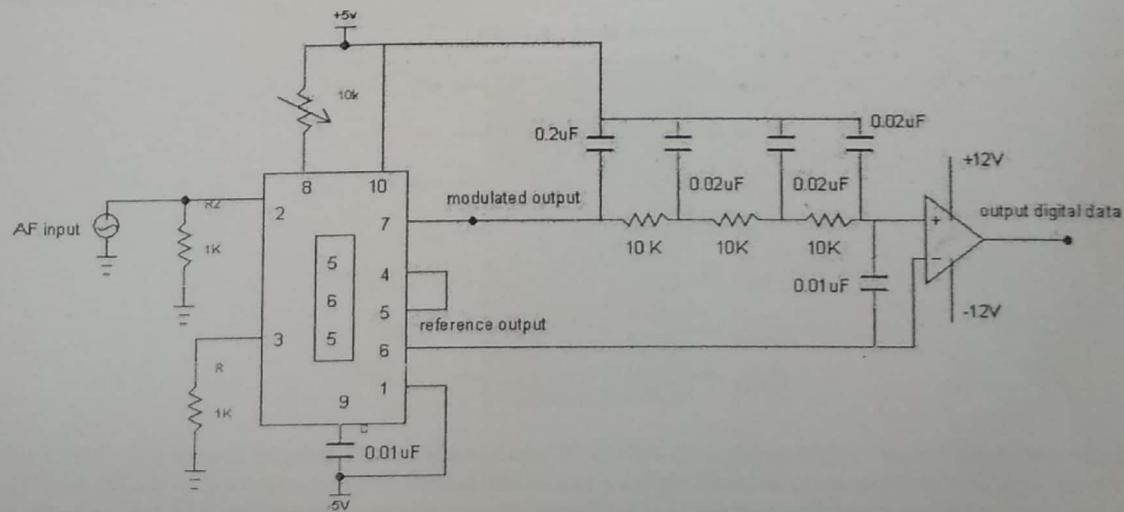
EQUIPMENT REQUIRED:

Equipment	Range	Quantity
CRO	(0-20) MHz	1
Function Generator	(0-1) MHz	1
Power Supply	(0-30) V +12V	1

COMPONENTS REQUIRED:

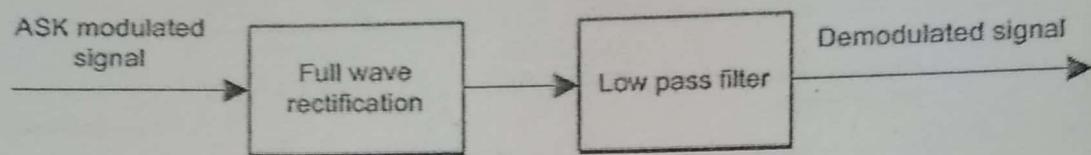
Component	Value	Quantity
IC 565 (PLL-IC)	565	1
IC-741 (OP-AMP)	Ic 741	1
Potentiometer	10K	1
Resistors	1K	2
	10K	3
	33K	1
Capacitors	0.02uF	3
	0.01uF	2
	0.2uF	1

CIRCUIT DIAGRAM:



#### **THEORY:**

The demodulation methods for FSK can be divided into two major categories: FM detector demodulator and filter-type demodulator. The FM detector demodulator treats the FSK signal as a simple FM signal with binary modulation.



#### **PROCEDURE:**

1. Connections are made as per the circuit diagram.
2. Give the FSK modulated signal as input to pin no. 2.
3. Observe the output waveform on the CRO.

## EXPERIMENT NUMBER 8

### Phase Locked Loop (PLL)

**AIM:** To study IC 565 PLL and find the following parameters.

1. Lock Range
2. Capture Range.

#### LEARNING OBJECTIVE:

- To compare the two modes of operation of timer IC 555.
- To classify the types of pulse modulation.

**PRIOR CONCEPTS:** Types of Modulation, Amplitude modulation, Pulse modulation and Sampling Theorem.

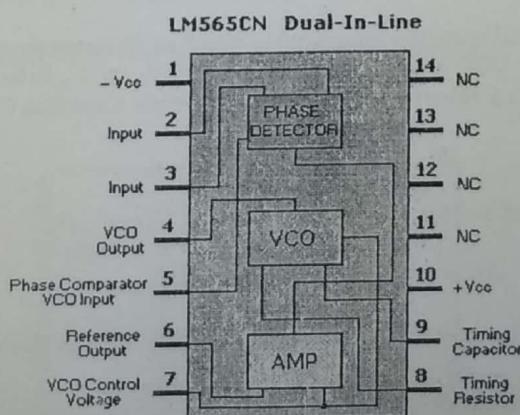
#### EQUIPMENT REQUIRED

Equipment	Range	Quantity
CRO	(0-20)MHz	1
Function Generator	(0-1)MHz	1
Experiment Kit		1
Dual Power Supply	(0-30)V	1

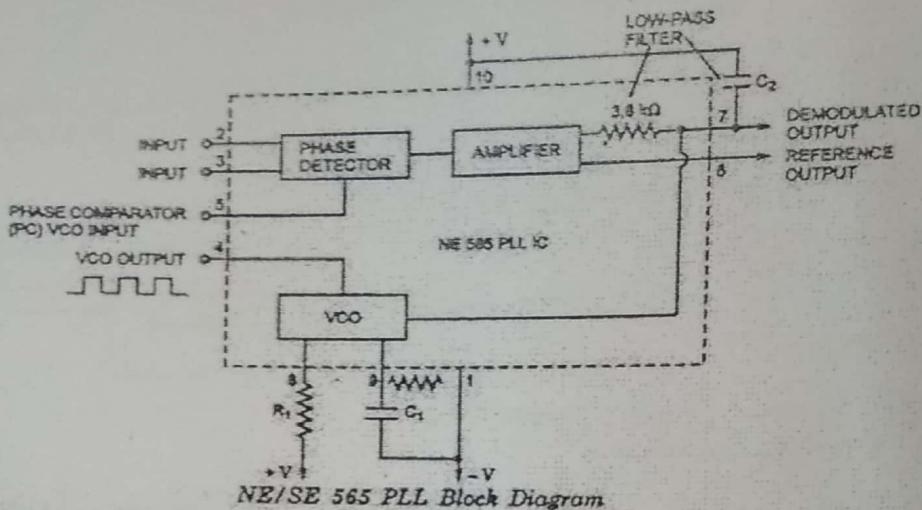
#### COMPONENTS REQUIRED

Components	Value	Quantity
IC	IC 565	1
Capacitor	0.01μF	3
	1μF	1
Resistor	6.8KΩ	1

**THEORY:** Phase-locked loop (PLL) is a feedback loop which locks two waveforms with same frequency but shifted in phase. The fundamental use of this loop is in comparing frequencies of two waveforms and then adjusting the frequency of the waveform in the loop to equal the input waveform frequency. The heart of the PLL is a phase comparator which along with a voltage controlled oscillator (VCO), a filter and an amplifier forms the loop. If the two frequencies are different the output of the phase comparator varies and changes the input to the VCO to make its output frequency equal to the input waveform frequency. The locking of the two frequencies is a nonlinear process but linear approximation can be used to analyse PLL dynamics. The range over which the loop system will follow changes in the input frequency is called the *lock range*. On the other hand, the frequency range in which the loop acquires phase-lock is the *capture range*, and is never greater than the lock range.



The LM565 is a general purpose Phase-Locked Loop IC containing a stable, highly linear voltage controlled oscillator (VCO) for low distortion FM demodulation, and a double balanced phase detector with good carrier suppression. The VCO frequency is set with an external resistor and capacitor, and a tuning range of 10:1 can be obtained with the same capacitor. The characteristics of the closed loop system--bandwidth, response speed, capture and pull in range--may be adjusted over a wide range with an external resistor and capacitor. The loop



#### CIRCUIT DESCRIPTION:

- Operating frequency range of the IC: 0.001 Hz to 500 kHz.
- Operating voltage range:  $\pm 6$  to  $\pm 12$  V.
- Input level required for tracking: 10 mV<sub>ms</sub> minimum to 3 V peak-to-peak maximum.

As shown in the figure, the PLL system consists of a phase detector or comparator (PC), a voltage-controlled oscillator (VCO), an amplifier and R-C combination forming low-pass filter circuit. The input signals are fed to the phase detector through pins 2 and 3 in differential mode. The input signals can be direct-coupled provided that the dc level at these two pins is made same and dc resistances seen from pins 2 and 3 are equal. By shorting pins 4 and 5 output of VCO is supplied back to the phase comparator (PC). The output of PC is internally connected to amplifier, the output of which is available at pins 6 and 7 through a resistor of 3.6 k Ω connected internally. A capacitor C<sub>2</sub> connected between pins 7 and 10 forms a low-pass filter with 3.6 k Ω resistor. The filter capacitor C<sub>2</sub> should be large enough so as to eliminate the variations in demodulated output and stabilize the VCO frequency. Voltage available at pin 7 is connected internally to VCO as a control signal. At pin 6 a reference voltage nominally equal to voltage at pin 7 is available allowing both the differential stages to be biased. Pins 1 and 10 are supply pins.

The centre frequency of the PLL is determined by the free-running frequency of the VCO which is given as

$$f_{\text{OUT}} = 1.2/4R_t C_t \text{ Hertz}$$

where R<sub>t</sub> and C<sub>t</sub> are external resistor and capacitor connected to pins 8 and 9 respectively, as illustrated in figure. The free-running frequency F<sub>out</sub> of the VCO is adjusted, externally with R<sub>t</sub> and C<sub>t</sub>, to be at the centre of the input frequency range. Resistor R<sub>t</sub> must have a value between 2 and 20 kilo ohm. Capacitor C<sub>t</sub> may have any value. The lock-range of PLL is given as

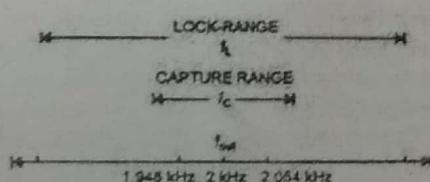
$$\Delta f_L = \pm 8f_{\text{OUT}} / V \text{ Hertz}$$

where f<sub>OUT</sub> is free-running frequency of VCO in Hz and V = (+ V) - (- V) and  
The capture range is given as

$$\Delta f_C = \pm [\Delta f_L / 2\pi (3.6) (10)^3 C]^{1/2}$$

The lock range usually increases with an increase in input voltage but falls with an increase in supply voltages.

#### Graphical Relationship between f<sub>OUT</sub>, f<sub>C</sub> and f<sub>L</sub>



## EXPERIMENT NUMBER 9

### Voltage Controlled Oscillator (VCO)

**AIM:** To design and test the circuit of Voltage to Frequency Converter (VCO) using IC 555.

#### LEARNING OBJECTIVE:

- To study the modes of operation of timer IC 555.
- To classify the types converters.

#### EQUIPMENT REQUIRED

Equipment	Range	Quantity
CRO	(0-20)MHz	1
Function Generator	(0-1)MHz	1
Experiment Kit		1
Power Supply	(0-30)V	1

#### COMPONENTS REQUIRED

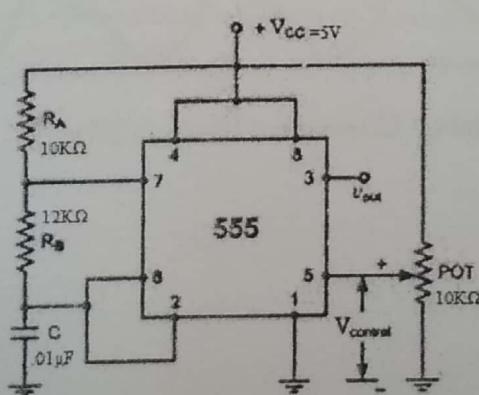
Components	Value	Quantity
Timer IC	IC 555	1
Capacitor	0.01μF	1
Resistor	10kΩ	1
	12 kΩ	1
Potentiometer	22 kΩ	1

**THEORY:** A voltage-controlled oscillator or VCO is an electronic oscillator designed to be controlled in oscillation frequency by a voltage input. The frequency of oscillation is varied by the applied DC voltage, while modulating signals may also be fed into the VCO to cause frequency modulation (FM) or phase modulation (PM). The circuit is sometimes called a **voltage-to-frequency converter** because the output frequency can be changed by changing the input voltage.

#### PROCEDURE

1. Connections are made as shown in the circuit diagram.
2. Set the input voltage at +5V and observe the corresponding waveform at pin no. 3 for various voltages at pin no. 5.
3. Change in the control voltage changes the frequency of the output waveform. Determine this frequency.
4. Repeat the above procedure for different voltages.

#### CIRCUIT DIAGRAM OF VOLTAGE CONTROLLED OSCILLATOR



**Description:** Pin 5 terminal is voltage control terminal and its function is to control the threshold and trigger levels. Normally, the control voltage is  $+4-5V_{CC}$  because of the internal voltage divider. However, an external

voltage can be applied to this terminal directly or through a pot, as illustrated in figure, and by adjusting the pot, control voltage can be varied. Voltage across the timing capacitor is depicted in figure, which varies between  $+V_{control}$  and  $\frac{1}{2} V_{control}$ . If control voltage is increased, the capacitor takes a longer time to charge and discharge; the frequency, therefore, decreases. Thus the frequency can be changed by changing the control voltage. Incidentally, the control voltage may be made available through a pot, or it may be output of a transistor circuit, op-amp, or some other device.

#### OBSERVATIONS:

Given,  $f = 4\text{KHz}$

Duty Cycle = 65%

$C = 0.01\mu\text{F}$

$$\begin{aligned} \text{Total Period} &= T_{ON} + T_{OFF} = 1/f \\ \text{Duty Cycle} &= \frac{T_{ON}}{T_{ON} + T_{OFF}} = 0.65 \end{aligned}$$

$$= 2.5 \times 10^{-4} \text{ sec}$$

$$\begin{aligned} \text{Therefore, } T_{ON} &= 0.65(T_{ON} + T_{OFF}) = 1.625 \times 10^{-4} \text{ sec} \\ T_{OFF} &= T - T_{ON} = (2.5 - 1.625) \times 10^{-4} \text{ sec} = 0.875 \times 10^{-4} \text{ sec} \end{aligned}$$

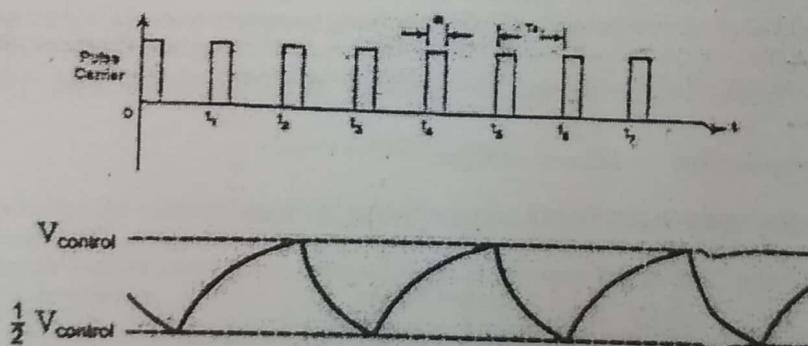
$$\text{We know that, } T_{OFF} = 0.693R_2C$$

$$\text{Therefore, } R_2 = \frac{T_{OFF}}{0.693C} = 12.63\text{K}\Omega$$

$$\text{So, Choose } R_2 = 12 \text{ K}\Omega$$

**CONCLUSION:** Thus, in VCO, (frequency/width/amplitude) of carrier changes in accordance to the instantaneous \_\_\_\_\_.

#### WAVEFORMS:



*Timing Capacitor Voltage Waveform*

## EXPERIMENT NUMBER 6

### Digital Phase Detector

**AIM:** To study and implement Digital Phase Detector and to detect the phase difference between two sinusoidal waves.

#### APPARATUS REQUIRED:

Apparatus	Range	Quantity
Function Generator	(0-100) MHz	1
Ammeter	(0-10) mA	1

#### COMPONENTS REQUIRED:

Components	Range	Quantity
IC 741		2
Resistor	1 K	1
Pot	100K	1
BC 107		1
Capacitor	.01 uF	1
IC 7486		1

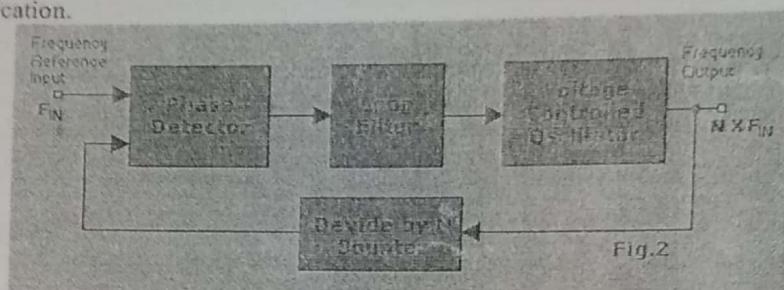
#### THEORY:

The phase detector compares the input frequency and the VCO and generates a dc voltage that is proportional to the phase detector difference between the two frequencies. Depending on the analog or digital phase detector used, the PLL is either called an analog or digital type respectively. For simplicity, digital phase detectors are used. Examples of digital phase detectors are Exclusive-OR phase detector and Edge – triggered phase detector.

#### EX-OR phase detector

The exclusive-OR phase detector uses an exclusive-OR gate such as CMOS type IC 4070. The EX-OR phase detector is preferred when both the inputs are square waves. The output of the EX-OR gate is high only when  $f_{in}$  and  $f_{out}$  are applied at EX-OR inputs and the output is the difference between the two inputs. In the waveforms shown below  $f_{in}$  is lagging  $f_{out}$  by some phase shift where the output is the phase difference between the two signals. These two square waves will be the outputs of the op-amp. R and C will create a phase difference between the inputs of the op-amp. The output of these op-amps will be square waves having some phase difference.

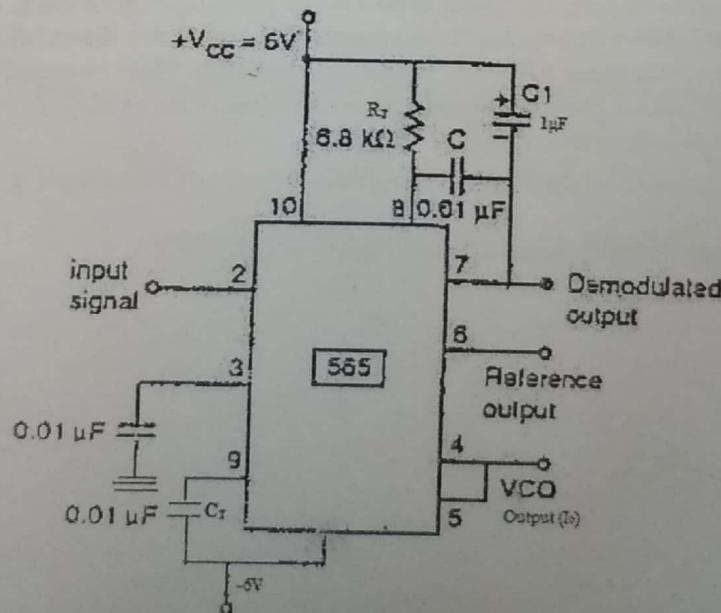
may be broken between the VCO and the phase detector for insertion of a digital frequency divider to obtain frequency multiplication.



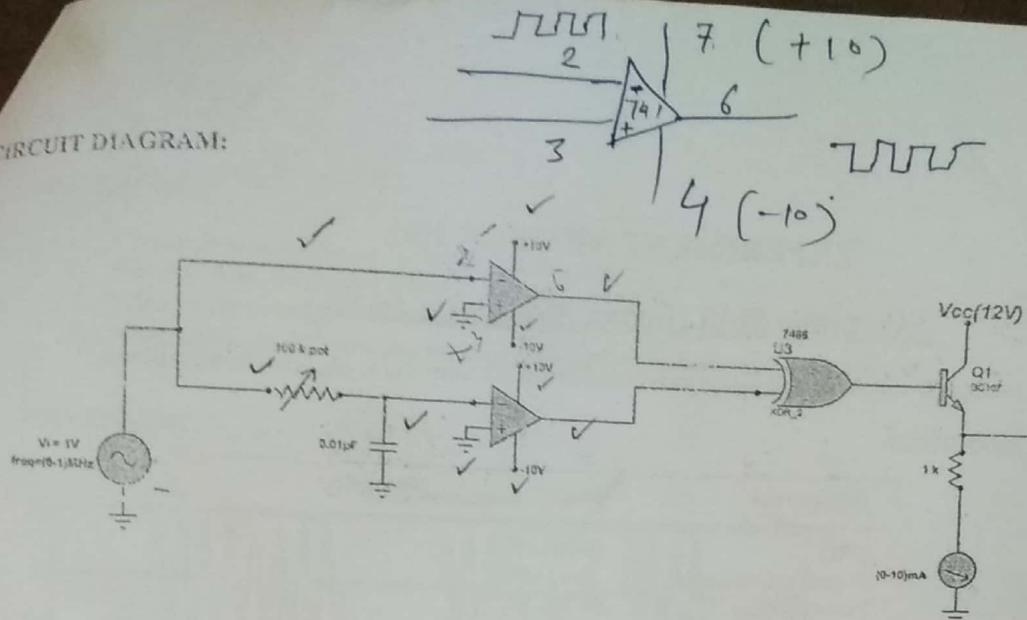
#### PROCEDURE:

1. Connections are made as shown in the circuit diagram.
2. Measure the free running frequency of IC565 at pin 4 using display with the input signal (say 0V) from the function generator or by shorting pin 2 to ground.
3. Set the input signal say 1V, 1 KHz to pin no. 2 using function generator and observe the corresponding waveform.
4. The frequency is varied till the output signal is  $180^\circ$  out of phase with the input. This is the upper end of the lock range.
5. The frequency is reduced till the output is  $90^\circ$  out of phase with the input. This is the upper end of the capture range.
6. The frequency is varied till a  $90^\circ$  phase shift is obtained in the output with reference to the input once again. This is the lower end of the capture range.
7. As the frequency is decreased further, output goes to  $180^\circ$  out of phase with the input once again. This is the lower end of the lock range.
8. The lock range  $\Delta f_L = (f_2 - f_1)$   
The capture range  $\Delta f_C = (f_3 - f_1)$
9. Compare these values with the theoretical values.

#### Circuit Diagram



CIRCUIT DIAGRAM:



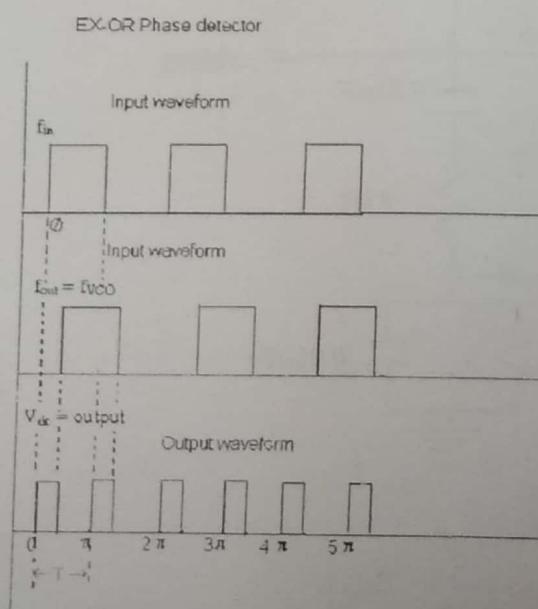
PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Set the input signal to 1 Vpp, 1KHz using function generator.
3. Observe the square waves at the output (pin no. 6) of both Op-Amps.
4. Vary the resistance and note down the corresponding current using DC Ammeter.
5. Also observe the output waveform across the emitter resistance of the transistor.
6. Phase angle can be calculated using the formula  $\alpha = \tan^{-1}(\omega RC)$ .
7. Plot the graph phase vs current (mA).

OBSERVATIONS:

Resistance(kΩ)	Current(mA)	Phase Angle $\alpha = \tan^{-1}(\omega RC)$

WAVEFORMS:



CONCLUSION:

## EXPERIMENT NUMBER 1(a)

### Amplitude Shift Keying Modulator (ASK)

**AIM:** To study and implement ASK modulation and demodulation schemes and to observe the waveform.

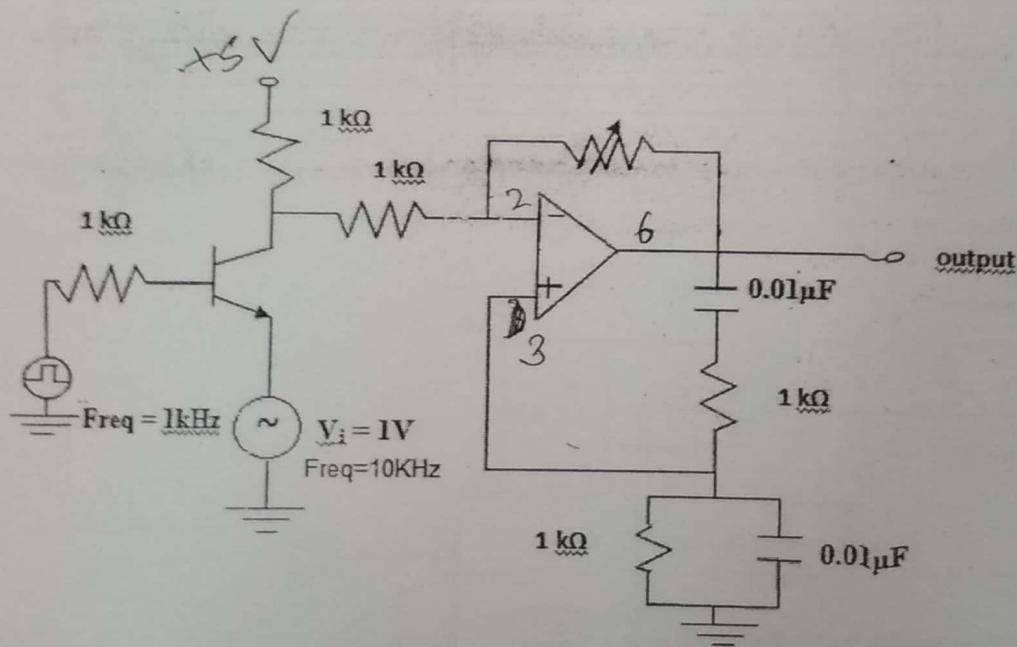
#### EQUIPMENT REQUIRED:

Equipment	Range	Quantity
CRO	(0-20) MHz	1
Function Generator	(0-1) MHz	2
Power Supply	(0-30) V	1
	+5V	1

#### COMPONENTS REQUIRED:

Component	Value	Quantity
Op-amp	741	1
Transistor	BC107	1
Resistor	1 kΩ	5
	10 kΩ (pot)	1
Capacitor	0.01 μF	2

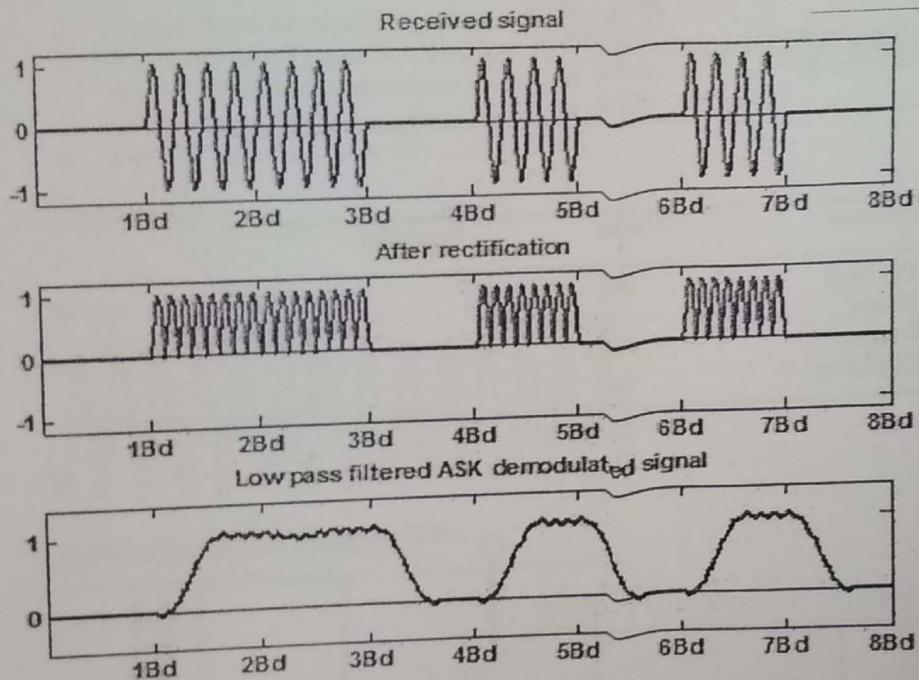
#### CIRCUIT DIAGRAM:



**PROCEDURE:**

1. Connections are made as per the circuit diagram.
2. Give the ASK modulated signal as input to the circuit.
3. Observe the output waveform on the CRO.
4. Vary the  $V_{ref}$  (0-5V) and observe the corresponding waveform on the CRO.

**WAVEFORM:**



## EXPERIMENT NUMBER 1(b)

### Amplitude Shift Keying Demodulator

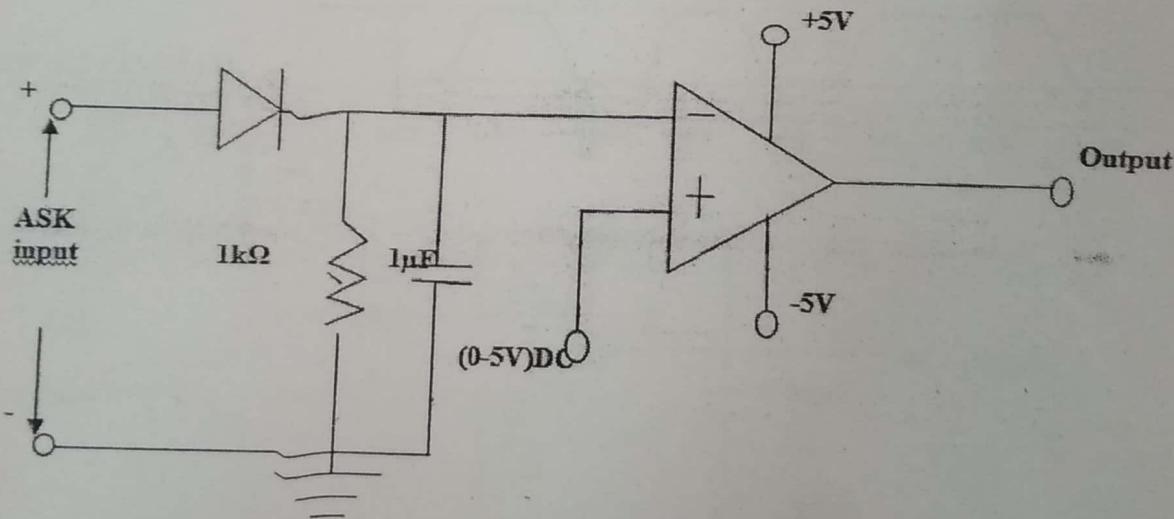
#### EQUIPMENT REQUIRED:

Equipment	Range	Quantity
CRO	(0-20) MHz	1
Function Generator	(0-1) MHz	1
Power Supply	(0-30) V +12V	1

#### COMPONENTS REQUIRED:

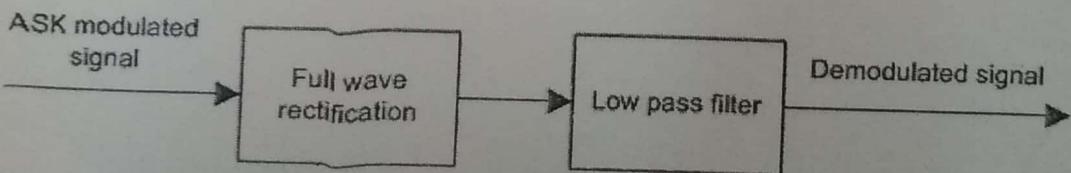
Component	Value	Quantity
Op-amp	741	1
Diode	IN4001	1
Resistor	1 kΩ	1
Capacitor	1 μF	1

#### CIRCUIT DIAGRAM:



#### THEORY:

The demodulator which is designed specifically for the symbol-set used by the modulator determines the amplitude of the received signal and maps it back to the symbol it represents, thus recovering the original data.



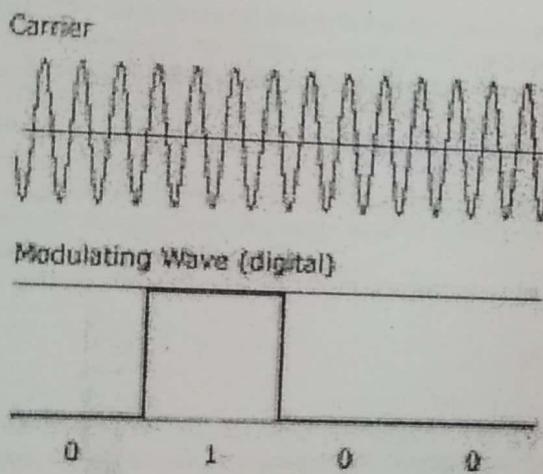
### **THEORY:**

To represent a digital data, finite number of distinct signals is used. ASK uses a finite number of amplitudes, each assigned a unique pattern of binary digit. Each amplitude signal encodes an equal number of bits. Each pattern of bits forms the symbol that is represented by the particular amplitude. In digital communications ASK is a modulation process, which imparts to a sinusoid two or more discrete amplitude levels. These are related to the number of levels adopted by the digital message.

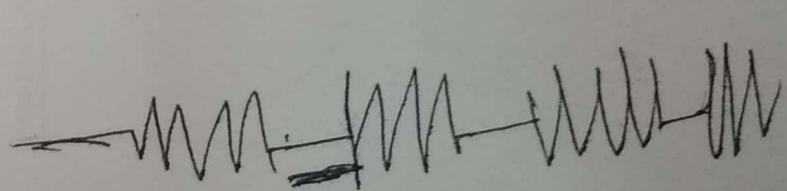
### **PROCEDURE:**

1. Connections are made as per the circuit diagram.
2. Set input signal (square wave) say 1V, 1 kHz using a function generator and carrier signal (sine wave) say 1V, 10 kHz using another generator.
3. Observe the output waveform on the CRO.
4. Plot the observed waveform on the CRO.

### **WAVEFORM:**



Modulated Result



## Pre-emphasis and De-emphasis Networks

**AIM:** To design and conduct an experiment to test a pre-emphasis and de-emphasis circuit for  $75\mu s$  between 2.1KHz to 15KHz and plot the waveform according to the recorded results.

### EQUIPMENT REQUIRED

Equipment	Range	Quantity
CRO	(0-20)MHz	1
Function Generator	(0-1)MHz	2
Experiment Kit		1
Power Supply	(0-30)V	1

### COMPONENTS REQUIRED

Components	Value	Quantity
Capacitor	1000pF	1
	100pF	1
Resistor	$75\Omega$	4

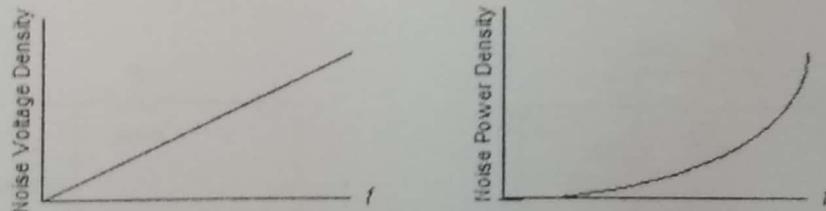
**THEORY:** In processing electronic audio signals, pre-emphasis refers to a system process designed to increase (within a frequency band) the magnitude of some (usually higher) frequencies with respect to the magnitude of other (usually lower) frequencies in order to improve the overall signal-to-noise ratio by minimizing the adverse effects of such phenomena as attenuation distortion or saturation of recording media. The whole system is called emphasis. The frequency curve is decided by special time constants. The cutoff frequency can be calculated from that value.

De-emphasis is the complement of pre-emphasis. De-emphasis is a system process designed to decrease, (within a band of frequencies), the magnitude of some (usually higher) frequencies with respect to the magnitude of other (usually lower) frequencies.

The fact that the carrier deviation in the presence of noise is given by:

$$\delta = \theta f_m$$

implies that noise voltage density increases linearly with frequency. Since power increases as the square of voltage, we obtain the following noise characteristics:



In order to keep a constant S/N ratio over the entire broadcast band, it is necessary to pre-emphasize or boost high frequency signals. This naturally requires performing the opposite function at the receiver, otherwise the signal would sound quite tinny.

In commercial FM broadcast, the pre-emphasis and de-emphasis circuits consist of a simple RC network. The RC time constant is  $75\mu s$ , and the corner frequency is 2125 Hz.

The magnitude of the pre-emphasis response is defined by

$$\left| \frac{V_o}{V_{in}} \right| = 20 \log \left[ \frac{R_2}{R_1 + R_2} \sqrt{1 + \left( \frac{f}{f_c} \right)^2} \right]$$

$$f_c = 2125 \text{ Hz}$$

#### PROCEDURE

1. Connections are made as shown in the circuit diagram.
2. Apply a sine wave of 1Vpp amplitude, vary the frequency in regular steps between 0-100KHz and note down the corresponding output voltage.
3. Plot a graph of gain (dB) Vs frequency.

#### Circuit Design:

##### 1. Pre-emphasis circuit

$$\text{Given } f_l = 15 \text{ KHz}, f_2 = 21 \text{ KHz}$$

$$f_l = 1/2\pi rC \text{ and } f_2 = 1/2\pi RC$$

$$\text{Choose } C_1 = 0.1 \mu\text{F}, \text{ then } r = 820\Omega \text{ and } R = 100\Omega$$

$$\text{Also, } r/R = R_f/R_1, \text{ then } R_1 = 2.2\text{K}\Omega \text{ and } R_f = 15\text{K}\Omega$$

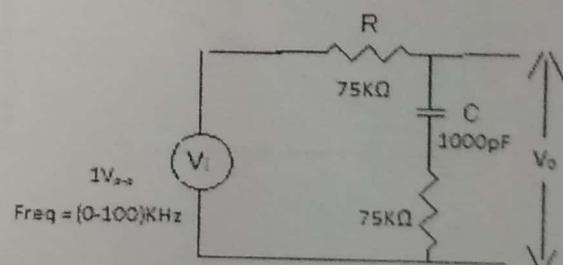
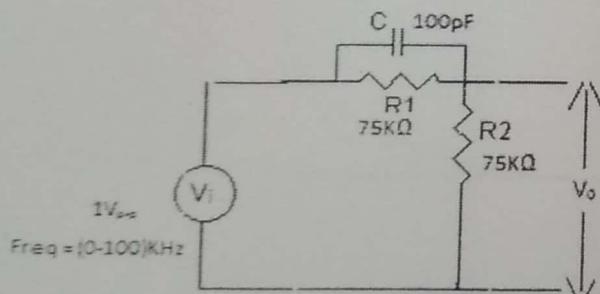
##### 2. De-emphasis circuit

$$f_c = 1/2\pi R_d C_d$$

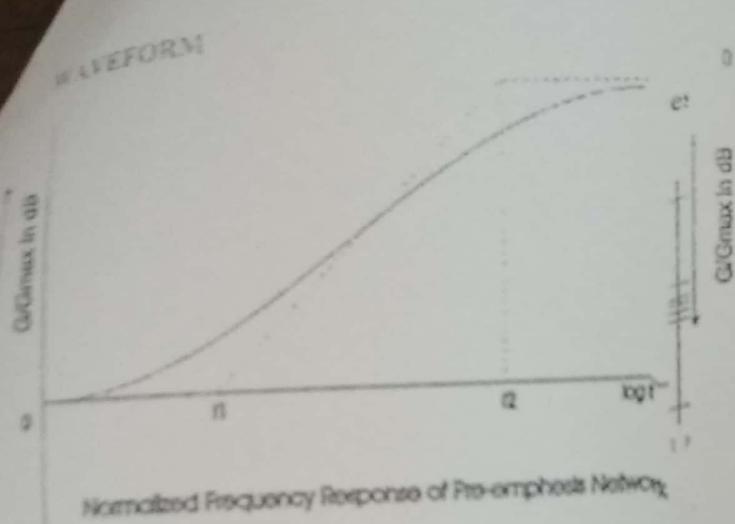
$$\text{Choose } C_d = 0.1 \mu\text{F}, \text{ and } f_c = f_l = 2.1 \text{ KHz}$$

$$\text{Then } R_d = 820\Omega$$

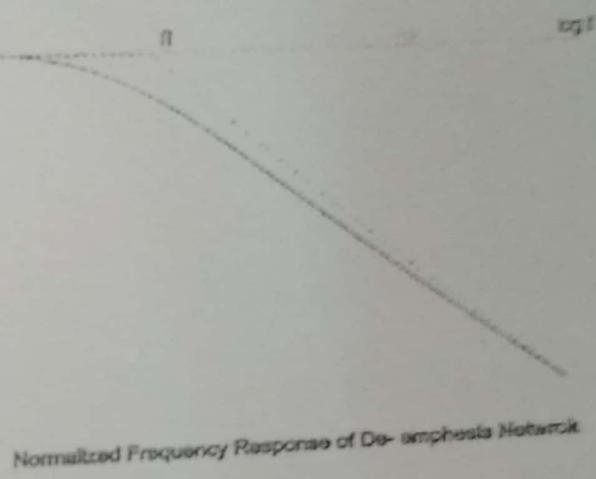
#### CIRCUIT DIAGRAM



WAVEFORM



Normalized Frequency Response of Pre-emphasis Network



Normalized Frequency Response of De-emphasis Network