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| **Course Title and Code:** Computer Organization and Architecture (CS 1134) | | | |
| Hours per Week | | **L-T-P: 3-0-2** | |
| Credits | | **4** | |
| Students who can take | | B. Tech. CSEIII Semester | |
| Prerequisite: Basics of Digital circuits and systems | | | |
| **Weightage: Theory -65%, Practical and Assignments – 35%** | | | |
| **Course Objectives**: To study the basic organization and architecture of digital computers (CPU, memory, I/O, software). Such knowledge leads to a better understanding and utilization of digital computers and can be used in the design and application of computer systems or as the foundation for more advanced computer-related studies. | | | |
| **Course Outcome:**  On successful completion of this course, the students should be able to:   1. Draw the functional block diagram of the single bus architecture of a computer and describe the function of the instruction execution cycle, RTL interpretation of instructions, addressing modes, and instruction set. 2. Design components of Arithmetic Logic Units, functional components for Computer Arithmetic and Logical operations, Familiarization of Fixed- and Floating-point representation. 3. Develop assembly language programs for multiplication, division, and I/O interface using 8086. Develop RTL description of functional components of CPU using HDL. 4. Given a CPU organization and instruction, design a memory module and analyze its operation by interfacing with the CPU. 5. Given a CPU organization, assess its performance, and apply design techniques to enhance performance using pipelining, parallelism, and RISC methodology. 6. Analyze the performance of cache-based systems and pipelining. | | | |
| **Sr. No** | **Specifications** | | **Marks** |
| 1 | Attendance | | **5** |
| 2 | Assignment | | **10** |
| 3 | Class Participation | | **0** |
| 4 | Quiz | | **10** |
| 5 | Theory Exam-I | | Nil |
| 6 | Theory Exam-II | | **20** |
| 7 | Theory Exam-III | | **30** |
| 8 | Report-I | | Nil |
| 9 | Report-II | | Nil |
| 10 | Report-III | | Nil |
| 11 | Project-I | | Nil |
| 12 | Project-II | | Nil |
| 13 | Project-III | | Nil |
| 14 | Lab Evaluation-I | | 15 |
| 15 | Lab Evaluation-II | | 10 |
| 16 | Viva | | Nil |
| 17 | Course Portfolio | | Nil |
|  | **Total (100)** | | **100** |
|  |  | |  |
| **Re-Test Evaluation** | | | |
|  | **Theory Exam-III** | | **30** |
|  | **Total:** | | **30** |

**Course Syllabi (Theory):**

**Unit I:** BASIC STRUCTURE OF COMPUTERS: Review of Digital Logic and Systems, Functional units, Von Neuman and Harvard Architecture Basic operational concepts, Bus structures, PCI, Multiple bus organization, Performance, and metrics,

**Unit II**: BASIC PROCESSING UNIT: Fundamental concepts, Execution of a complete instruction, The Arithmetic and Logic Unit (ALU), Number Systems, Fixed point representation, and Arithmetic, Floating Point Representation and Arithmetic, Hardwired control, Micro programmed control.

**Unit III**: INSTRUCTION SETS: Characteristics and functions, x86 Architecture, Instruction set architecture, Addressing modes and formats, RISC and CISC.

**Unit IV:** PIPELINING: Basic concepts, Data hazards, Instruction hazards, Influence on instruction sets, Data path, and control path, Performance considerations, Exception handling.

**Unit V:** MEMORY SYSTEM: Basic concepts, Memory Hierarchy, Semiconductor RAM, ROM, Speed, Size and cost, Cache memories, Improving cache performance, Virtual memory, Memory management requirements, Associative memories, and Secondary storage devices.

**Unit VI:** I/O ORGANIZATION: Accessing I/O devices, Programmed Input/Output, Interrupts, Direct Memory Access, I/O devices, and processors.

**Unit VII**: PARALLEL PROCESSING: The use of multiple processors, Symmetric Multiprocessors, Cache coherence, UMA, and NUMA.

**Text Books:**

* Mano, M. Morris. "Computer system architecture, 1993." Prentice Hall 3: 299.
* Patterson, David A., and John L. Hennessy. Computer Organization and Design MIPS Edition: The Hardware/Software Interface. Newnes, 2013.

**Reference Books:**

* Hayes, John P. Computer architecture and organization. McGraw-Hill, Inc., 2002.
* Heuring, Vincent P., Harry Frederick Jordan, and Miles Murdocca. Computer systems design and architecture. Addison-Wesley, 1997.

# [Kai Hwang](https://www.pdfdrive.com/search?q=Kai+Hwang) & [Naresh Jotwani](https://www.pdfdrive.com/search?q=Naresh+Jotwani) - Advanced Computer Architecture: Parallelism, Scalability, Programmability, Tata McGraw Hill, 2003

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| Course Outcome | Correlation with program outcomes | | | | | | | | | | | | | | | | Correlation with program-specific outcomes | |
| PO 1 | PO 2a | PO 2b | PO 2c | PO 3a | PO 3b | PO 3c | PO 4a | PO 4b | PO 4c | PO 5a | PO 5b | PO 6 | PO 7a | PO 7b | PSO-1 | | PSO-2 |
| **CS1107.1** |  | 1 |  | 1 |  |  |  | 1 |  |  |  | 1 |  |  |  | 2 | |  |
| **CS1107.2** |  | 1 |  |  |  |  | 1 |  |  |  | 2 |  |  |  |  |  | |  |
| **CS1107.3** |  |  | 1 |  | 1 |  |  |  | 1 | 1 |  |  | 1 |  |  | 2 | | 2 |
| **CS1107.4** | 1 |  |  |  |  |  |  | 1 |  |  |  | 1 |  | 1 |  | 2 | |  |
| **CS1107.5** | 1 |  | 1 |  | 1 |  |  |  | 1 |  |  | 1 |  |  |  |  | | 2 |
| **CS1107.6** | 1 | 2 |  |  |  | 2 |  |  |  | 2 |  |  |  | 1 |  | 2 | | 2 |

**Course Articulation Matrix: (Mapping of COs with POs)**

**1- Low Correlation; 2- Moderate Correlation; 3- Substantial Correlation**

**Learning Activities**

|  |  |  |  |
| --- | --- | --- | --- |
| **Sl. No** | **Learning Activities** | **Evaluation**  **Components**  **Used** | **CO** |
| LA1 | Installation of ISE 14.7 and environment setup | Assignment | CS1107.1 |
| LA2 | Developing simple VHDL models for ALU components | Lab Evaluation  Theory Exam I  Theory Exam II | CS1107.5  CS1107.6 |
| LA3 | Synthesis and simulation of digital systems basic circuits | Lab Evaluation | CS1107.1  CS1107.5 |
| LA4 | Design and simulation of combinational and sequential components for ALU and memory using VHDL | Assignment Theory Exam I  Theory Exam II | CS1107.7  CS1107.8 |
| LA5 | Designing memory and cache organization and perform mapping of cache using various mapping strategies | Assignment  Theory Exam II | CS1107.4  CS1107.6 |
| LA6 | Developing assembly language programs for multiplication, division, and I/O interface using 8086 | Lab evaluation  Assignments Theory Exam I  Theory Exam II | CS1107.3  CS1107.4 |
| LA7 | Developing assembly language programs using RISC followed by simulation | Lab Evaluation  Assignments  Theory Exam II | CS1107.4  CS1107.6 |
| LA8 | Developing functional components using Verilog for ALU and memory design | Lab Evaluation  Assignment  Theory Exam II | CS1107.5  CS1107.6 |

**Course Articulation Matrix: (Mapping of Activities with COs)**

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| --- |
| **Activities** |
|  | CS1107.1 | CS1107.2 | CS1107.3 | CS1107.4 | CS1107.5 | CS1107.6 |
| LA1 | 1 | 1 |  |  |  |  |
| LA2 |  |  |  | 2 |  |  |
| LA3 | 2 |  |  | 3 |  |  |
| LA4 |  |  |  | 2 | 1 |  |
| LA5 |  |  |  |  |  | 2 |
| LA6 |  | 2 | 3 |  |  |  |
| LA7 |  |  | 2 |  | 3 |  |
| LA8 |  |  |  | 1 |  |  |

**1- Low Correlation; 2- Moderate Correlation; 3- Substantial Correlation**

**Correlation of Course Objectives with learning activities**