

Semiconductor physics

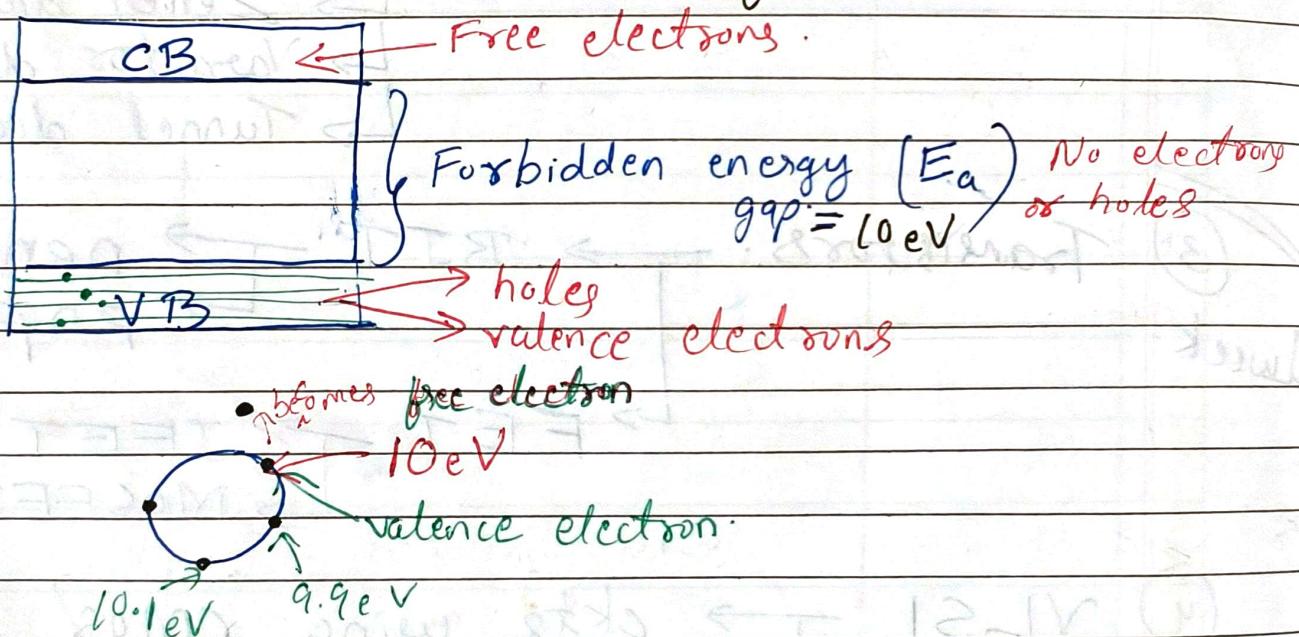
Based on the conductivity, all the materials are classified into three categories

- (1) Insulators
- (2) Conductors
- (3) Semiconductors

① Insulators

The materials that do not conduct electricity are called insulators. eg plastic, wood, rubber

The energy band diagram of insulator is.



No two electrons have same energy but they are near each other.

The forbidden energy gap of insulator is around 10 eV .

If we give 10 eV energy to an electron in the

Energy

~~unit Joules~~ but Joules is every big quantity for EDC
 for electrons.

$$1 \text{ eV} = 1.6 \times 10^{-19} \text{ Joules}$$

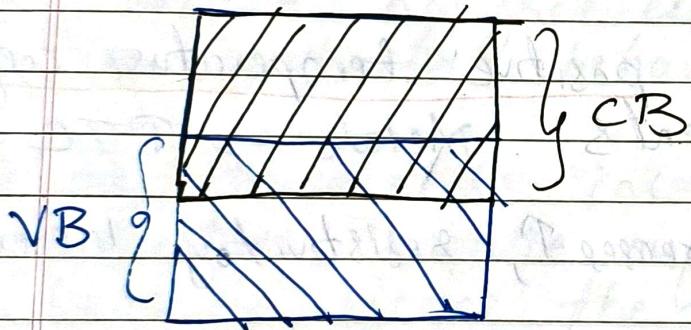
valence band then it becomes free electron.
 - But insulators cannot withstand that high energy. [If that high energy is applied to them then they loose their physical appearance i.e. (burn or deformed)]

- Hence insulators never become conductors.

(2) Conductor

A good conductor of electricity is called conductor eg: all metals, copper, silver.

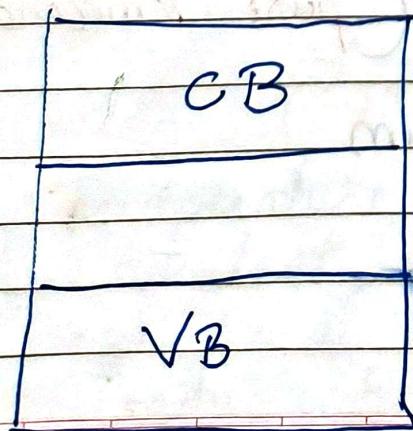
Energy band diagram.



All electrons are free electrons.

(3) Semiconductors

The conductivity of semiconductors lies between conductors & insulators eg: silicon & germanium.



$$\left. \begin{array}{l} \text{CB} \\ \text{VB} \end{array} \right\} E_a \approx 1 \text{ eV} \rightarrow \begin{array}{l} \text{for silicon} \\ E_a(\text{Si}) = 1.21 - 3.6 \times 10^{-4} T \end{array}$$

$$\rightarrow \begin{array}{l} \text{for germanium} \\ E_a(\text{Ge}) = 0.785 - 2.23 \times 10^{-4} T \end{array}$$

where $T \leftarrow$ temp in Kelvin

Metals do not have holes.

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* Forbidden energy gap (0°K)

$$E_a(\text{Si}) = 1.21 \text{ eV} \quad \begin{matrix} \downarrow \\ \text{semiconductor} \end{matrix}$$

$$E_a(\text{Ge}) = 0.785 \text{ eV} \quad \begin{matrix} \downarrow \\ \text{behaves as an insulator.} \end{matrix}$$

* Forbidden energy gap (300°K) \leftarrow room temperature

$$E_a(\text{Si}) = 1.1 \text{ eV} \quad \begin{matrix} \downarrow \\ \text{insulator} \end{matrix}$$

$$E_a(\text{Ge}) = 0.72 \text{ eV} \quad \begin{matrix} \downarrow \\ \text{semiconductor} \end{matrix}$$

As temperature \uparrow , resistivity decreases
& this is called (Negative temperature coefficient)
Semiconductors \rightarrow NTC.

Note:- Metals exhibits positive temperature coefficient PTC of coefficients Metals \rightarrow PTC

i.e. (as Temp increases T , resistivity increases)

Semiconductor classification

(1) Intrinsic semiconductors

(2) Extrinsic semiconductors

(1) Intrinsic semiconductors (pure semiconductors)

e.g.: - Silicon, germanium

~~DT~~ Any time if a covalent bond is broken, then an electron-hole pair is created.

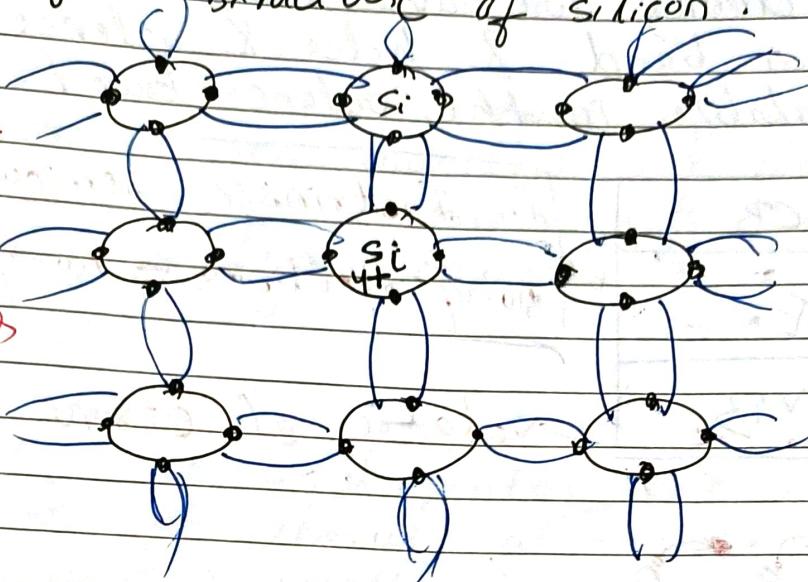
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Crystal structure of silicon.

~~DT~~ 0°K

No free electrons



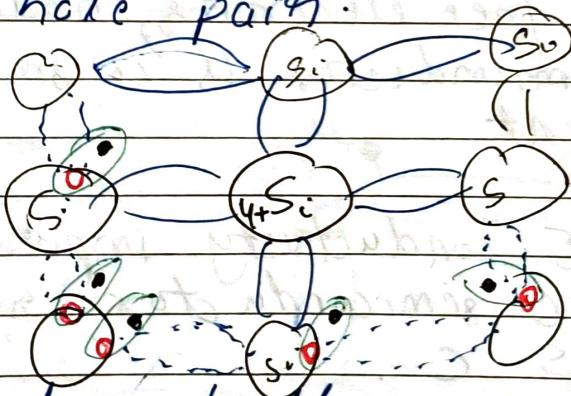
No free electrons available at 0°K

valence electrons

~~DT~~ At 0°K , all the valence electrons (4) forms covalent bonds with neighbouring valence electrons.

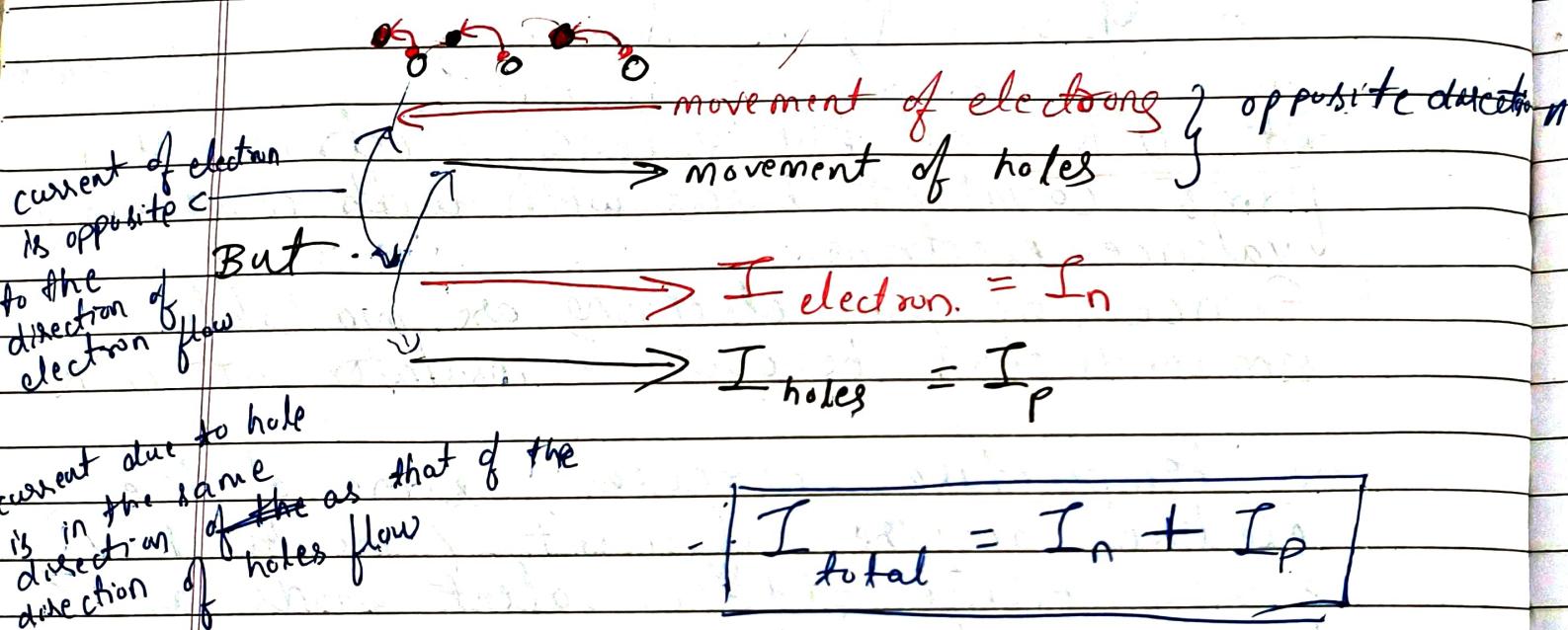
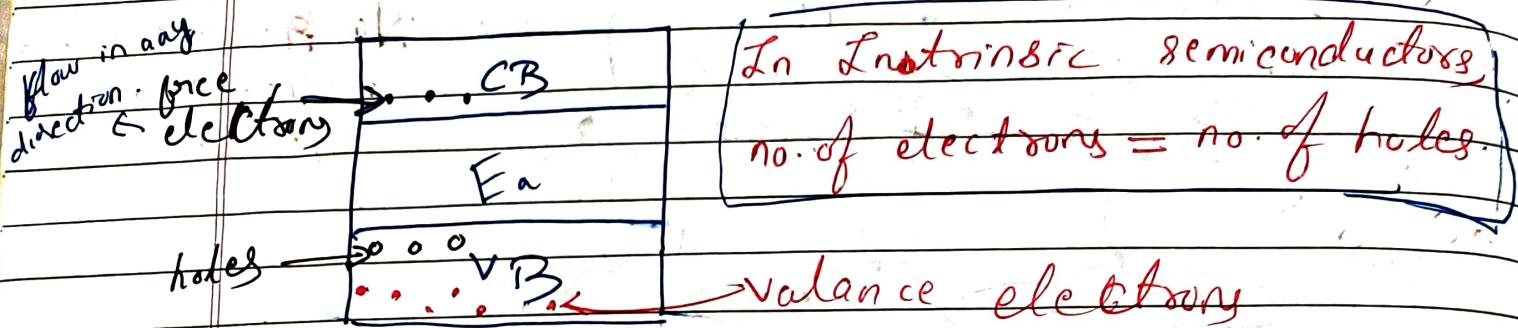
Since, no free electrons are available, semiconductor behaves as insulator at 0°K .

As temperature increases some of the electrons acquire sufficient (around 1 eV) energy. Hence the co-valent bonds are broken resulting the generation of free electron-hole pairs.



As temperature further increases, more number of covalent bonds are broken thereby producing a large no. of electron hole pairs.
∴ Conductivity increases.

Free electrons are available in the conduction band & holes & valence electrons are available in the valence band.



- The no. of free electrons, holes available in intrinsic semiconductor is so small resulting a small current
- To increase conductivity impurities are added to intrinsic semiconductor, resulting into extrinsic S. C.
- Process of adding impurities is called doping. Doping is used to increase conductivity.

donates electrons \rightarrow +ve ion
accepts electrons \rightarrow -ve ion

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(2) Intrinsic Semiconductors

Based on the type of impurity added, extrinsic semiconductors are classified as

- (a) n-type semiconductor
- (b) p-type semiconductor.

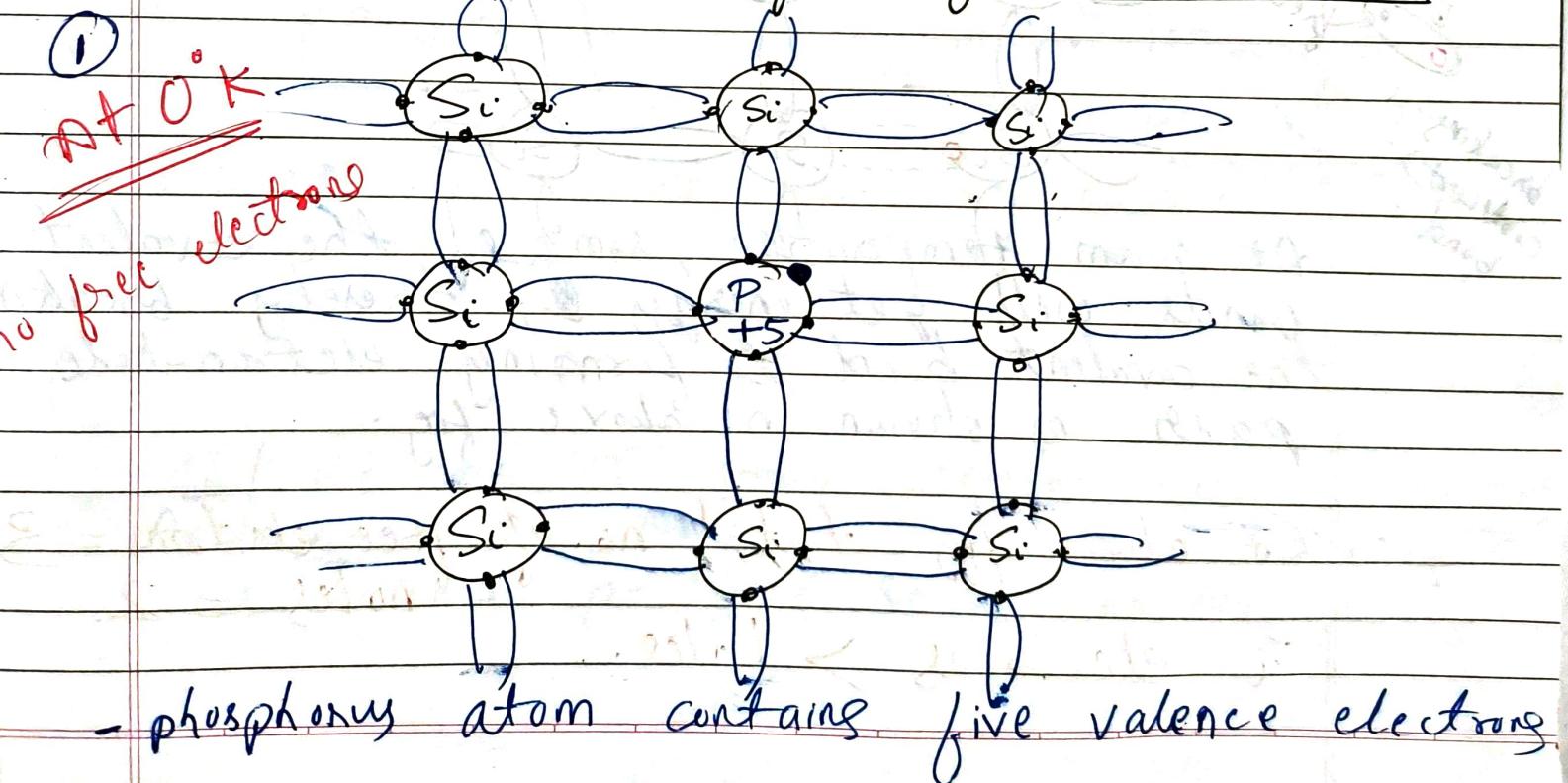
(a) n-type semiconductor

If we add pentavalent impurities such as phosphorus, arsenic, antimony, then the resulting semiconductor is called n-type semiconductor.

The doping concentration is 1 part in 10^8

Add one \downarrow in Silicon atoms
 \downarrow
phosphorus atom

Crystal structure of n-type semiconductor

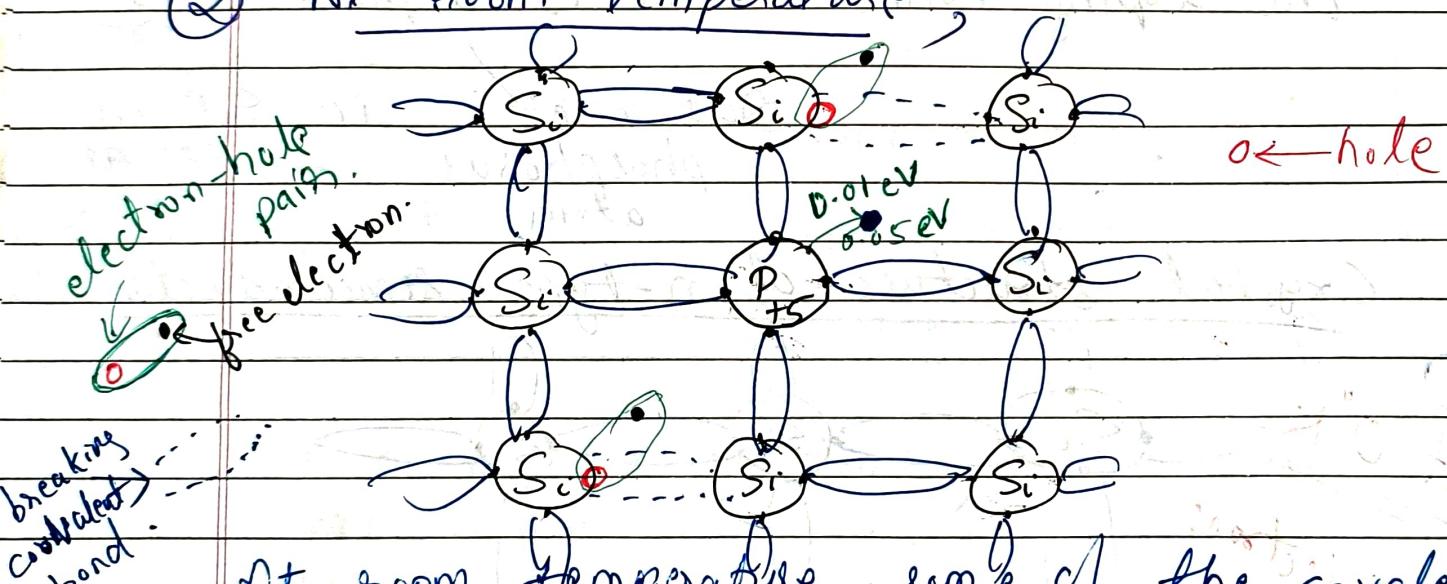


out of which 4 electrons form covalent bonds with neighbouring 4 silicon atom.

- 1 valence electron of phosphorus is not involved in any covalent bonds. The amount of energy required to make this 5th unattached valence electron as a free electron is $\rightarrow 0.01 \text{ eV (P)}$
 0.05 eV (Si)

~~If we give this small energy, the 5th valence electron becomes free electrons & no hole will be created~~

② At room temperature,



At room temperature, some of the covalent bonds will get energy \rightarrow , thereby breaking the covalent bond & forming electron-hole pair as shown in above fig.

In above fig, total no. of free electrons = 3
holes = 2
i.e. electrons $>$ holes.

* In a n-type semiconductors majority charge carriers are electrons & minority charge carriers are holes.

* An n-type semiconductor is always electrically neutral.

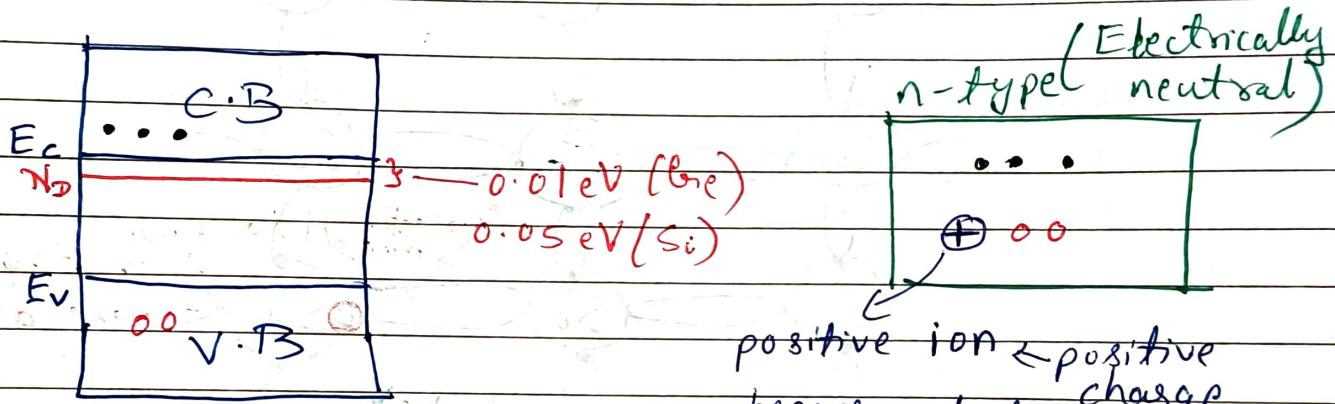
$$\text{Total no. of electrons} = \text{Total no. of } \begin{matrix} \text{mobile} \\ + \end{matrix} \text{ positive holes}$$

~~current~~

not mobile

* Since phosphorus atom donated an electron, it is called donor impurity.

Energy band diagram of n-type semiconductor



Current flows ~~due to~~ due to electrons & holes
Not ions.

(2) P-type Semiconductors.

If we add 3rd group element such as Boron Aluminium to intrinsic S.C., then resulting sc is called p-type semiconductor.

~~① AT 0°K~~

~~AT 0°K~~

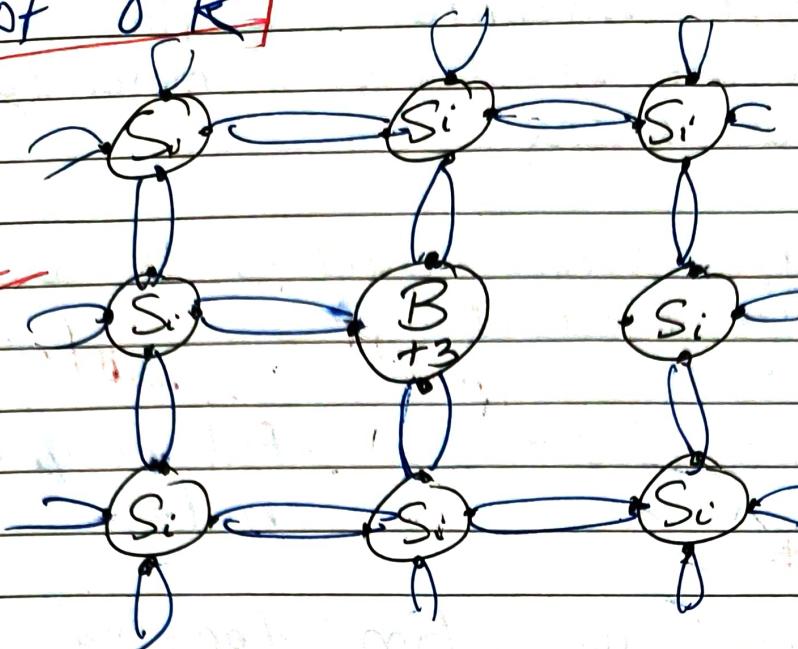


fig 1

~~② AT 1°K or 2°K (little increase in temp)~~

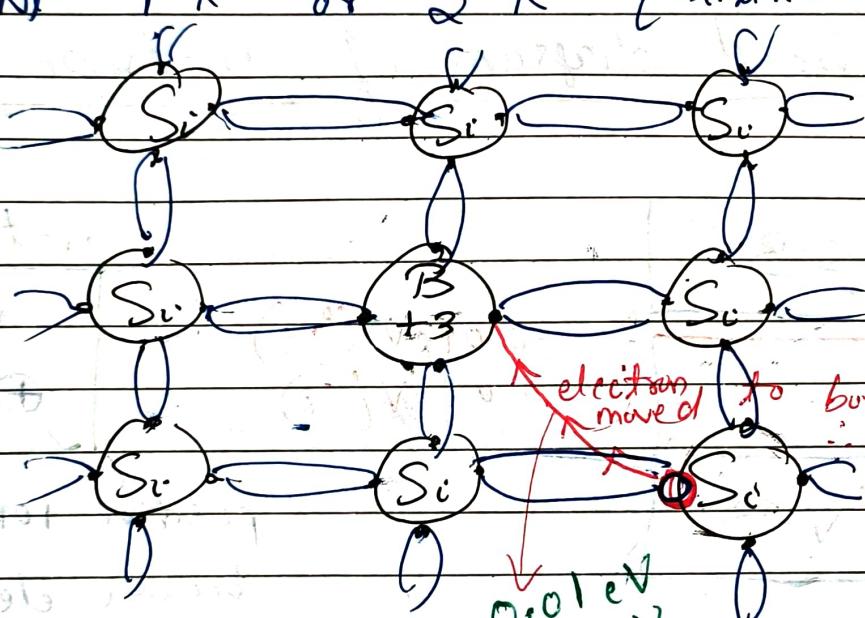


fig 2

~~③ AT 300°K (room temperature)~~

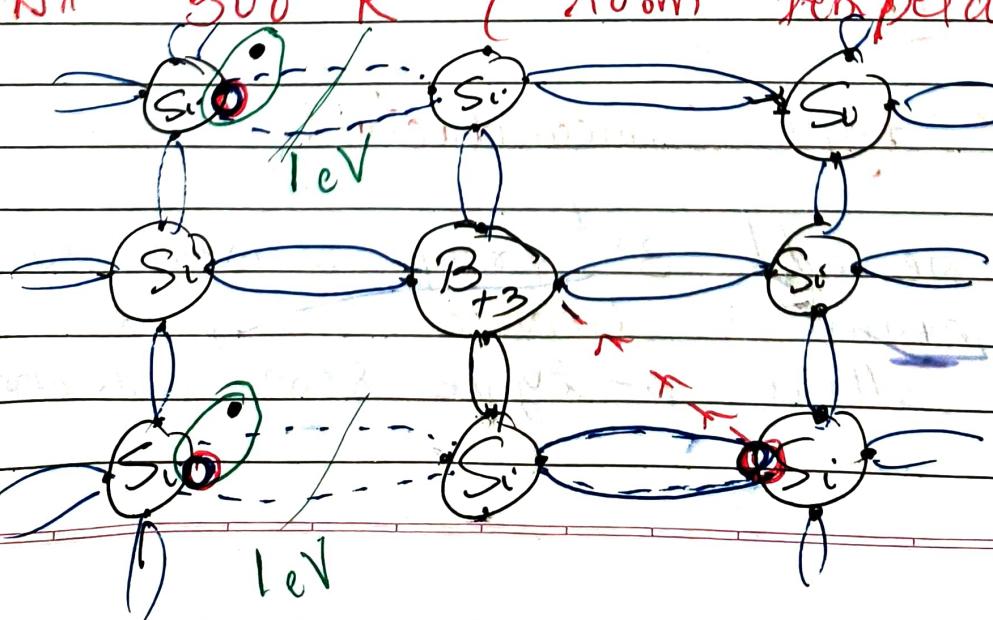
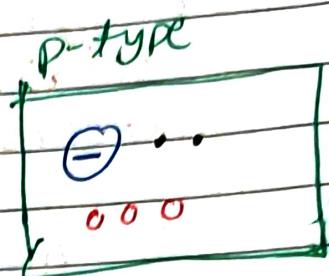
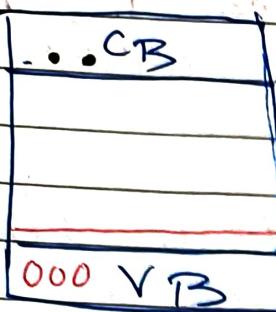


fig 3

1 eV

Energy Band diagram :-



- Boron atom at 0°K has 3 valence electrons out of which all three form covalent bond but to become stable it requires one more electron & due to this the Boron atom has the tendency to attract one electron from neighbouring Si atom & forms covalent bond & becomes stable as shown in fig ①
- Now as electron moves from neighbouring atom of Si, hole is created in that atom.
- In p-type S.C. majority charge carriers are holes & minority charge carriers are electrons
- p-type is also electrically neutral.

Mass Action Law

$$n_p = n_i^2 \quad \leftarrow \text{Applicable for intrinsic} \text{ } \cancel{\text{and}} \text{ } \text{extrinsic} \text{ semiconductors}$$

$n_p \rightarrow$ holes concentration
 $n \rightarrow$ electron concentration
 $n_i \rightarrow$ intrinsic carrier concentration.

for p-type semiconductor, $n_p P_p = n_i^2$

for n-type semiconductor, $n_n P_n = n_i^2$

Compared to intrinsic S.C., in an extrinsic S.C., minority carrier concentration decreases.

At higher temperatures, extrinsic semiconductor becomes intrinsic semiconductors.

N-S.C. \rightarrow 130 electrons 100 holes

Now, temp is increased \rightarrow \therefore elect \uparrow & holes \uparrow

Conductivity of new intrinsic S.C. is larger than older (original intrinsic sc)

Law

Law of Electrical Neutrality

Total +ve charge = Total -ve charge

$\downarrow \quad \downarrow$
Donor ions + holes = Acceptor ions + electrons

$$\therefore N_D + p = N_A + n$$

In Intrinsic S.C., $N_A = 0$, $N_D = 0$

$$\therefore \boxed{n = p}$$

In Extrinsic S.C.,

\rightarrow n-type SC, $N_A = 0$

$$\therefore \boxed{N_D + p_n = n_n}$$

hole is minority carrier \therefore neglect p_n

(5)

P-type S.C (Acceptor)

$\therefore N_D = 0$

$$P = N_A + n$$

$$N_D \approx n_n$$

we know that

$$n_n p_n = n_i^2$$

$$\therefore P_n = \frac{n_i^2}{n_n} = \frac{n_i^2}{N_D}$$

$$P_p = N_A$$

we know that

$$n_p p_p = n_i^2$$

$$\therefore P_p = \frac{n_i^2}{N_A} = \frac{n_i^2}{P_p}$$

neglect electron
it is minority carrier.

In metal, total no. of electrons = ~~total~~ no. of positive ions
Hence, metal is also electrically neutral.

Drift mechanism:

- Consider a metal in which there exists large no. of free electrons but they move randomly. At any point of time, it is assumed that number of electrons travelling in one direction is exactly equal to number of electrons travelling in opposite direction. Hence net current is zero.

- If we externally apply an electric field, all the electrons will be aligned in one particular direction producing current in opposite direction. This mechanism is called drift. & the current due to this mechanism is called drift current.

~~Fermi - Dirac~~ Fermi - Dirac Probability Function

It is a probability of finding an electron at energy level,

$$f(E) = \frac{1}{1 + e^{\frac{E-E_f}{kT}}}$$

$E_f \rightarrow$ fermi energy level, it gives concentration of electrons & holes (i.e. if electrons are more or holes are more)

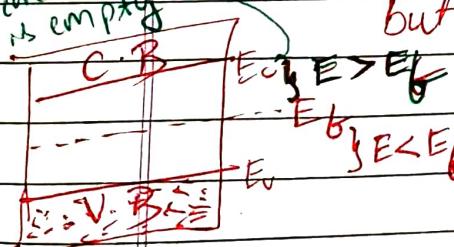
$E \rightarrow$ Energy level.

case 1 \rightarrow ① $T \neq 0$, $E = E_f$, then $f(E) = 0.5$

\rightarrow ② If $T=0$, If $E > E_f$, then $f(E) = 0$

③ If $T=0$, If $E < E_f$ the $f(E) = 1$

no chance of finding electron in conduction band at $T=0$, the valence band has all valence electrons



but the conduction band is empty.

chances of finding electron is maximum, because at $T=0$, the valence band is full with valence electrons

Fermi-Energy level in an intrinsic S.C

For an intrinsic S.C., no. of electrons is equal to no. of holes.

$$\text{i.e. } n = p \rightarrow (1)$$

$$n = N_c e^{-\frac{(E_c - E_F)}{KT}} \rightarrow (2)$$

$$p = N_v e^{-\frac{(E_F - E_V)}{KT}} \rightarrow (3)$$

$$\text{where } N_c = 2 \left[\frac{2\pi m_n}{h^2} \right]^{3/2} K T \rightarrow (4)$$

\rightarrow Planck's constant

$$\& N_v = 2 \left[\frac{2\pi m_p}{h^2} \right]^{3/2} K T \rightarrow (5)$$

effective mass of electron effective mass of hole mass of particle at rest

where ~~$m_p = m_n$~~ $m_p = m_n = 0.5 m_0$

Substitute (2) & (3) in eq (1) -

$$N_c e^{-\frac{(E_c - E_F)}{KT}} = N_v e^{-\frac{(E_F - E_V)}{KT}}$$

$$\therefore \frac{N_c}{N_v} = e^{-\frac{(E_F - E_V) + (E_c - E_F)}{KT}}$$

$$\frac{N_c}{N_v} = e^{-\frac{E_F + E_V - E_c - E_F}{KT}}$$

$$\therefore \frac{N_c}{N_v} = e^{-\frac{E_c + E_V - 2E_F}{KT}}$$

Taking inverse log

$$\ln \left(\frac{N_c}{N_v} \right) = \frac{E_c + E_V - 2E_F}{KT}$$

$$\therefore E_F = \frac{E_c + E_V}{2} - \frac{KT}{2} \ln \left(\frac{N_c}{N_v} \right)$$

If $m_n = m_p$ then, $N_c = N_v$

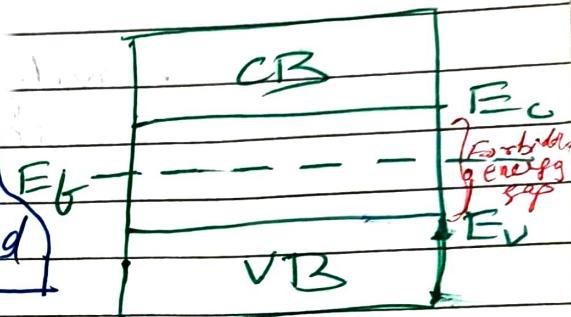
$$\therefore \ln\left(\frac{N_c}{N_v}\right) = 0$$

$$\therefore E_f = \frac{E_c + E_v}{2}$$

For intrinsic S.C., Fermi level lies between (at center) E_c & E_v .
of forbidden energy gap.

This shows that;

$$\boxed{\text{No. of free electrons} = \text{No. of holes in C.B.} - \text{in valence band}}$$

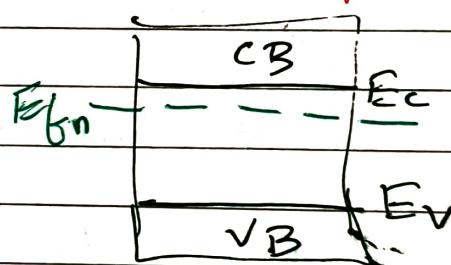


* For n-type Semiconductors (Fermi-energy level)

$$n_n = N_c e^{-\frac{(E_c - E_{fn})}{kT}}$$

(electrons major carrier)

$$\therefore N_D = N_c e^{-\frac{(E_c - E_{fn})}{kT}}$$



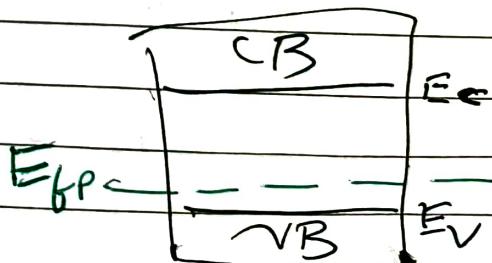
$$\therefore E_{fn} = E_c - kT \ln\left(\frac{N_c}{N_D}\right)$$

* For p-type S.C. (Fermi-energy level)

$$P_P = N_v e^{-\frac{(E_{fp} - E_v)}{kT}}$$

$$N_A = N_v e^{-\frac{(E_{fp} - E_v)}{kT}}$$

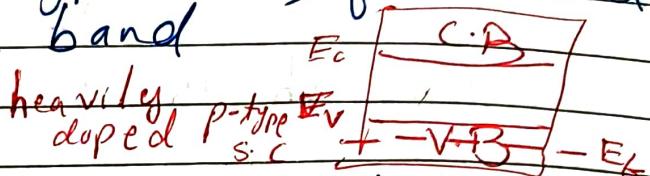
$$e^{\frac{(E_{fp} - E_v)}{kT}} = \frac{N_v}{N_A}$$



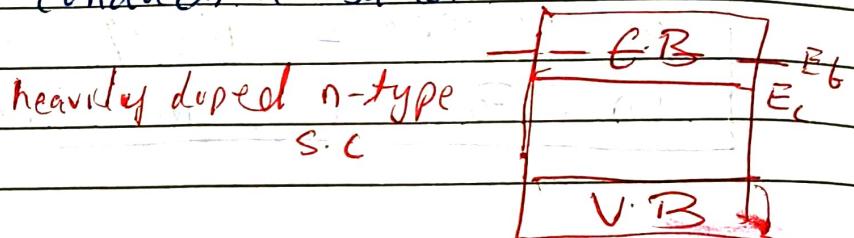
$$E_{fp} = E_v + kT \ln\left(\frac{N_v}{N_A}\right)$$

- As temperature increases, fermi-level moves towards the center.
- At higher temperature, extrinsic S.C become intrinsic S.C

$1 \text{ part in } 10^3$ For heavily doped p-type S.C, fermi-level lies inside the valence band



For heavily doped n-type S.C, fermi-level lies inside the conduction band.



Distance between fermi level of n-type S.C & intrinsic S.C.

$$-(E_C - E_F)$$

we know that, $n = N_c e^{-\frac{(E_C - E_F)}{KT}}$ $\rightarrow \textcircled{1}$.

For n-type S.C, eq $\textcircled{1}$ becomes

$$N_D = N_c e^{-\frac{(E_C - E_F)}{KT}} \rightarrow \textcircled{2}$$

For intrinsic S.C, eq $\textcircled{1}$ becomes

$$n_i = N_c e^{-\frac{(E_C - E_{fi})}{KT}} \rightarrow \textcircled{3}$$

$$\textcircled{2} \div \textcircled{3}$$

$$E_{f^n} - E_{f^i} = KT \ln \left(\frac{N_D}{N_i} \right)$$

~~Distance between fermi level of p-type S.C & intrinsic S.C~~

we know that, $p = N_v e^{-\frac{(E_F - E_V)}{KT}}$ $\rightarrow \textcircled{1}$

For P-type S.C, eq $\textcircled{1}$ becomes:

$$N_A = N_v e^{-\frac{(E_{fP} - E_V)}{KT}} \rightarrow \textcircled{2}$$

For intrinsic S.C, eq $\textcircled{1}$ becomes

$$n_i = N_v e^{-\frac{(E_{fi} - E_V)}{KT}} \rightarrow \textcircled{3}$$

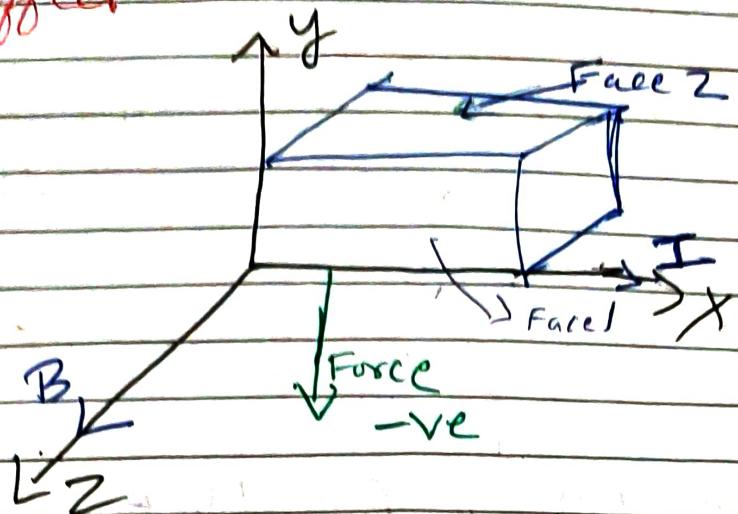
$$\textcircled{2} \div \textcircled{3}$$

$$\therefore \frac{N_A}{n_i} = e^{-\frac{E_{fP} + E_V + E_{fi} - E_V}{KT}}$$

$$\therefore E_{fi} - E_{fP} = KT \ln \left(\frac{N_A}{n_i} \right)$$

$\Rightarrow \left(\frac{N_A}{p_i} \right) \text{ same}$

Hall effect



A semiconductor is placed in a field where magnetic field (B) & current (I) are perpendicular to each other then the Semiconductor experiences force in the direction perpendicular to both B & I .
This is called Hall effect.

- The force experienced by semiconductor is called Lorentz force & is equal to $(q \bar{V} \times \bar{B})$ cross product

By using Hall effect

- ① We can find the type of semiconductors
- ② We can calculate carrier concentration.
- ③ We can calculate conductivity.

Under thermal equilibrium, force due to electric field is equal to force due to magnetic field

$$\text{at thermal equilibrium} \quad \text{Force due to Electric field} = \text{Force due to magnetic field.}$$

$$\therefore E = B \rho v$$

$$\therefore E = B v$$

$$\therefore E = \frac{V_H}{d}$$

$$\therefore \frac{V_H}{d} = B v$$

$$\therefore V_H = B d v$$

$$= B d \frac{J}{S_v}$$

$$J = n e v$$

$$\therefore v = J$$

concentration $\rightarrow n e$

$$\therefore v = \frac{J}{S_v}$$

charge density

$$J = \frac{I}{A}$$

$$= B d \cdot \left(\frac{I}{A} \right) S_v$$

$$= \frac{B d k}{S_v} \frac{I}{W d}$$

$$\therefore V_H = \frac{B I}{W} \frac{1}{S_v}$$

$$V_H = \frac{B I}{W} R_H$$

where

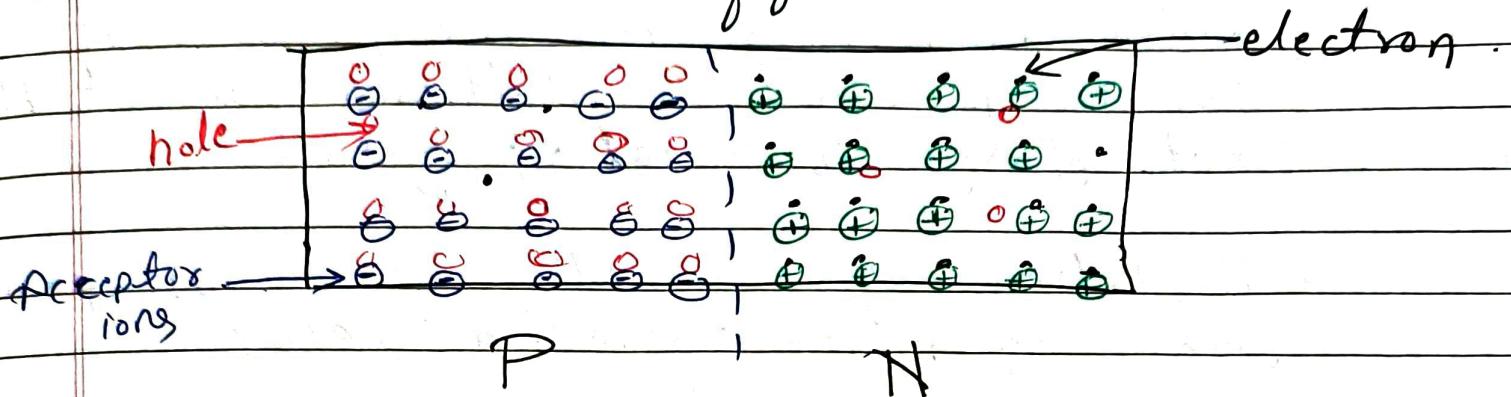
$$R_H = \frac{1}{S_v} = \frac{1}{n e}$$

If half voltage $\Rightarrow V_H = -ve$ then n-type s.c

$V_H = +ve$ then p-type s.c

PN junction Diode

Take a pure intrinsic S.C such as silicon. At one side p-type impurities are added & at the other side n-type impurities are added as shown in figure below:-



Working:

Be'coz of diffusion mechanism, holes will move from $P \rightarrow N$, at the same time electrons will move from $N \rightarrow P$.

- Near the junction, electrons will recombine with the holes leaving the ions.
- After sometime, there exists sufficient charges on either side of the junction to repel the majority charge carriers (movement)
- The region of uncovered ions form depletion layers.
- At room temperature, normally the width of depletion layer is 0.5.
- In the depletion layer, there exist +ve charge & -ve charge thereby creating an

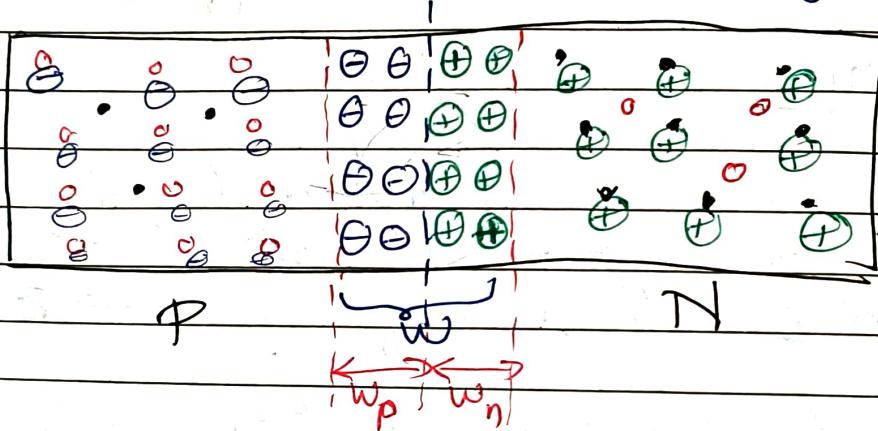
~~drift current~~ →
← diffusion current

internal electric field:

This internal electric field will allow the minority carrier to cross junction resulting to drift current.

Under open ckt condition, this drift current is equal to diffusion current. Hence net charge is equal to zero.

- Depletion region is also known as space charge region or transition region.

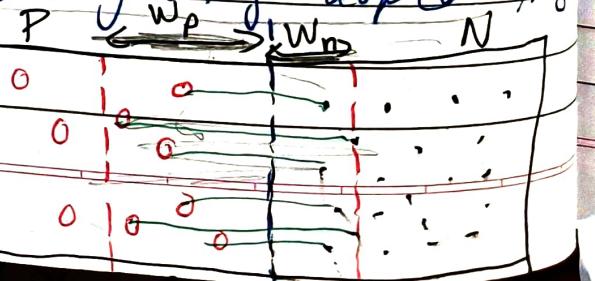


$$\therefore W = W_p + W_n$$

If p-type S.C & n-type S.C are equally doped then the width of the depletion region in n-region & p-region are equal.
i.e $W_n = W_p$.

else the depletion region will penetrate more into the lightly doped region.

P-region
is lightly doped



$$V_B = V_T \ln \left(\frac{N_A N_D}{n_i^2} \right)$$

$$F.B \rightarrow V_B = V_o + V_R$$

$$F.B \rightarrow V_B = V_o - V_F$$

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Forward voltage

* The width of depletion layer W is given as -

$$W = \sqrt{\frac{2\epsilon}{e} V_B \left(\frac{1}{N_A} + \frac{1}{N_D} \right)}$$

where V_B = barrier potential of depletion region.

$$\therefore V_B = V_T \ln \left(\frac{N_A N_D}{n_i^2} \right)$$

at open ckt condition

$$\epsilon = \epsilon_0 \epsilon_r \quad \text{relative permittivity}$$

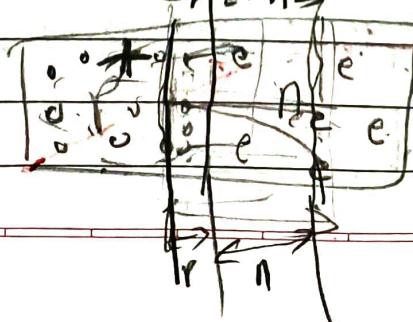
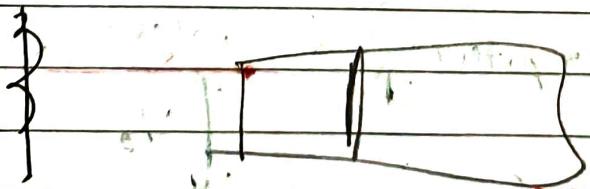
permittivity in free space

* The width of depletion layer in p-region is given as

$$W_p = \frac{W N_D}{N_A + N_D}$$

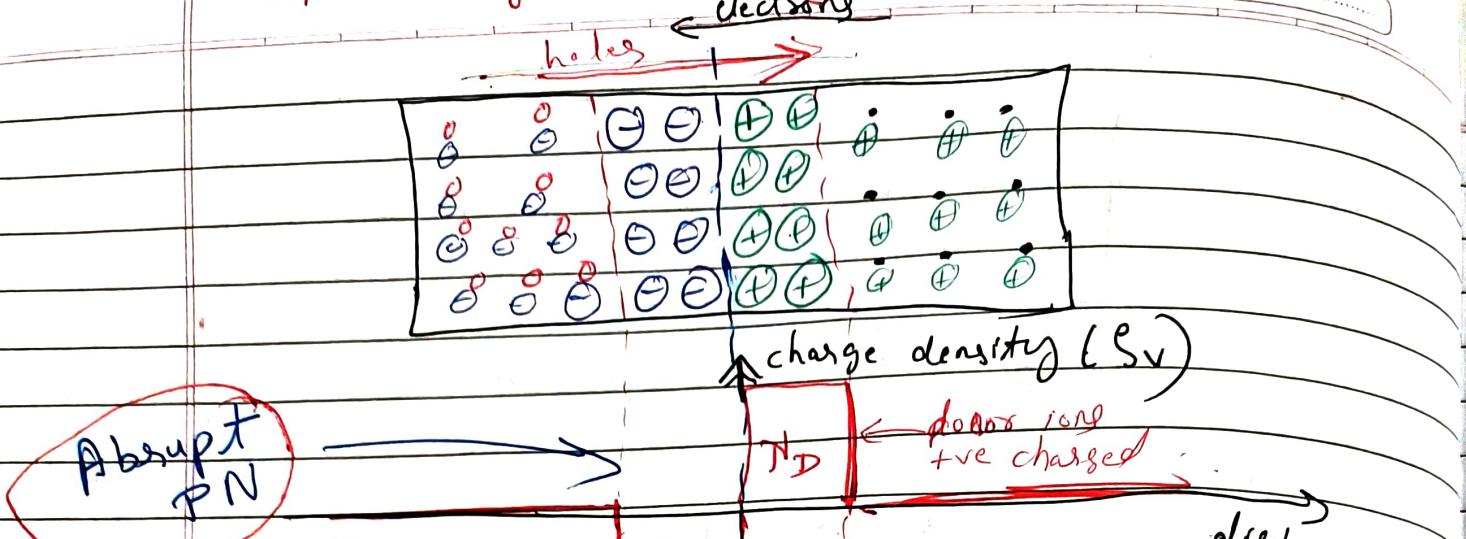
* Width of depletion layer in n-region is given as

$$W_n = \frac{W N_A}{N_A + N_D}$$



Electric field is always maximum at the junction irrespective of the doping concentration

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Integration we get

~~Max value of E at junction
Max value at $n=0$~~

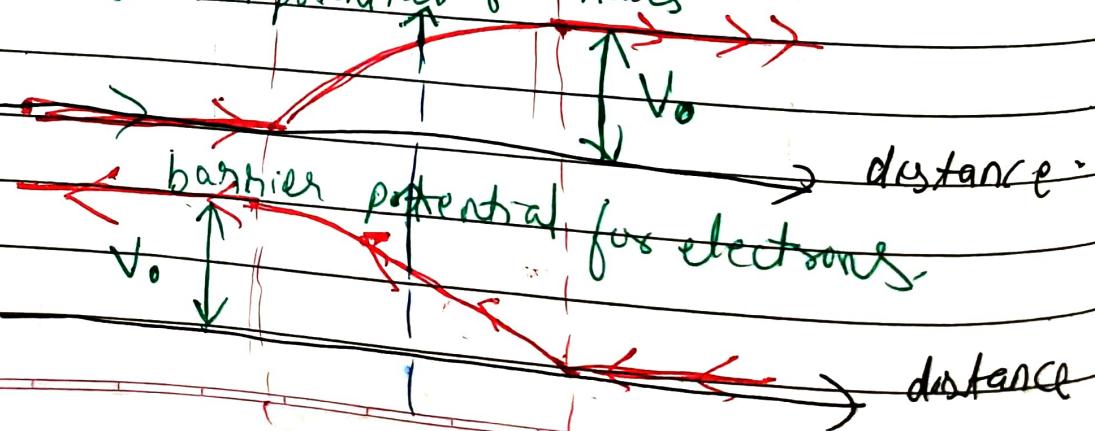
$$E_{max} = \frac{e N_A w_p}{\epsilon}$$

$$E_{max} = \frac{e N_D w_n}{\epsilon}$$

Linear graded PN junction

$$N_A w_p = N_D w_n$$

barrier potential for holes



* Brasing

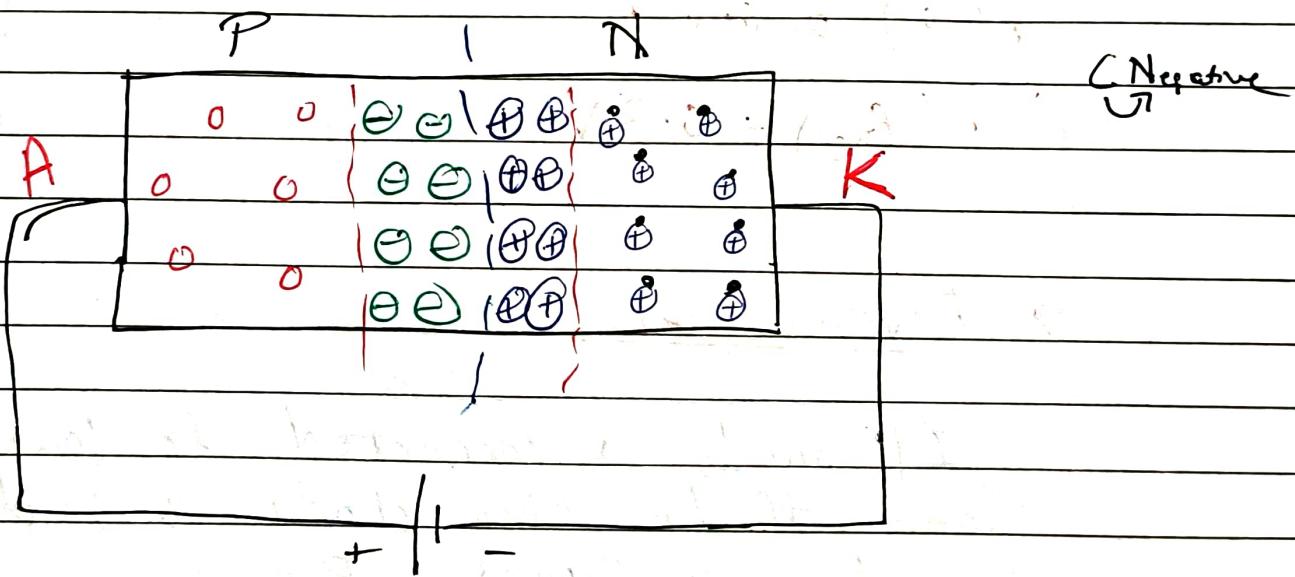
It is a process of application of external DC voltages.

There are two types of brasing:

- ① Forward Bias
- ② Reverse Bias

* Forward Bias

If anode is connected at higher potential than cathode, then the diode is said to be connected in forward bias.



- As the forward voltage increases, the majority charge carriers acquire energy.

- When voltage supply given is small, the energy acquired is not sufficient to cross the junction. Thereby current ~~is~~ is nearly equal to zero.

- After certain voltage known as cut-in voltage,

Metals do not have holes. only free electrons.

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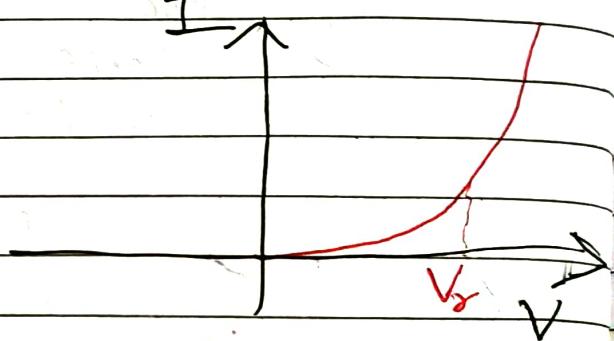
the energy acquired by the majority charge carrier is sufficient to cross the junction & thereby the current flows.

- This cut-in voltage is also called as offset voltage or threshold $[V_T(Si)] = 0.6 V$ $V_T(Ge) = 0.3 V$
- Under forward biased condition, the width of the depletion layer reduces.
Under forward biased condition, current is due to majority charge carrier & it is in the order of mA.

$V_T \rightarrow$ cut-in voltage

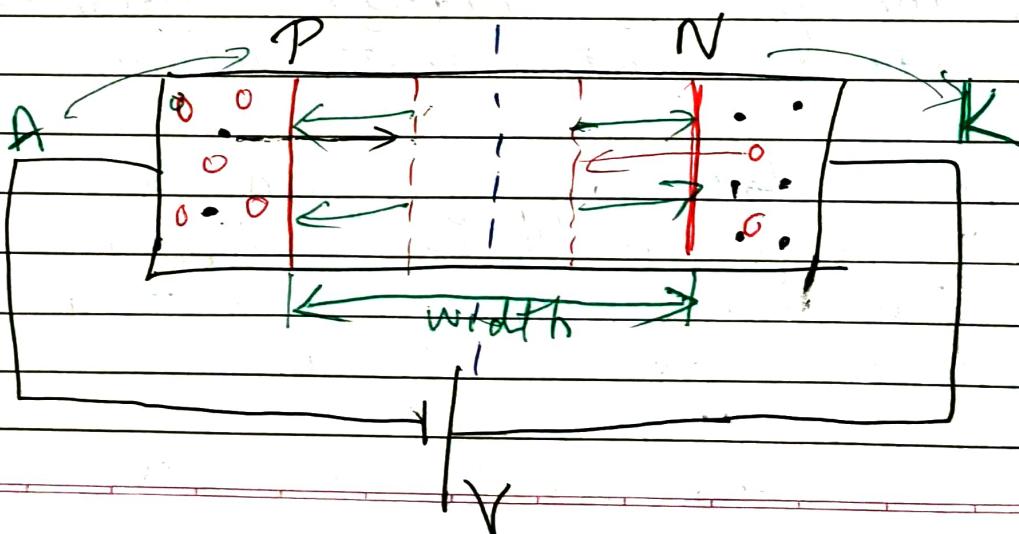
$$V_T(Si) = 0.6 V$$

$$V_T(Ge) = 0.3 V$$



* Reverse Bias

If anode is connected to lower potential than cathode then diode is said to be connected in Reverse Bias.



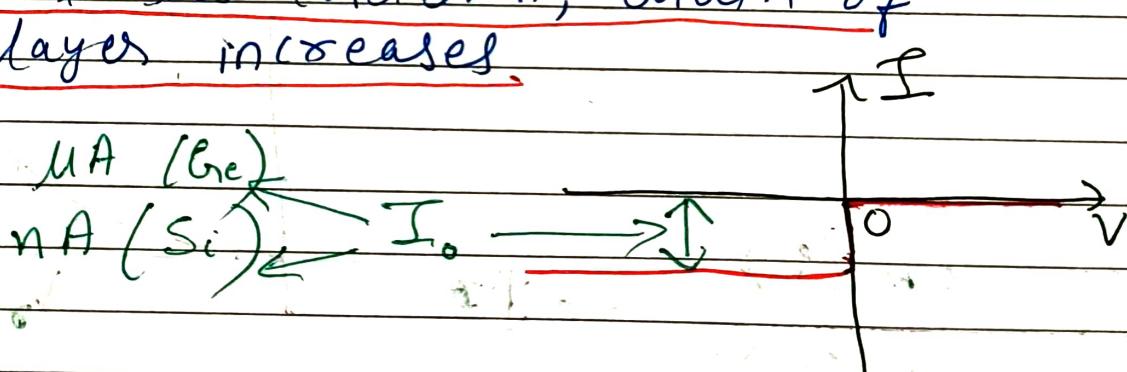
- Becoz of the applied reverse voltage, the majority charge carriers move away from the junction. Thereby the width of depletion layer increases & the internally induced electric field also increases.

- Becoz of this, majority charge carriers will not cross the junction but it will allow the minority charge carriers to cross the junction resulting in a small current known as reverse saturation current denoted as I_D .

- I_D is in order of μA for Ge & nA for Si.

- Under Reverse bias condition, current is due to minority charge carrier

- Under Reverse bias condition, width of depletion layer increases.



Diode current Equation

$$I = I_D \left(e^{\frac{V}{nV_T}} - 1 \right)$$

Where I_D - Reverse saturation current &

$$I_D = \frac{A_e D_p P_n N_o}{L_p} + \frac{A_e D_n n P_o}{L_n}$$

V - Diode voltage

V_T - Volt equivalent temperature

$$\eta = \begin{cases} 1 & \text{for } \text{Ge} \\ 1 & \text{for large current of Si} \\ 2 & \text{for small current of Si} \end{cases}$$

$$\text{From } I = I_0 e^{\frac{V}{\eta V_T}} - 1$$

$$\text{we get } V = \eta V_T \ln \left(1 + \frac{I}{I_0} \right)$$

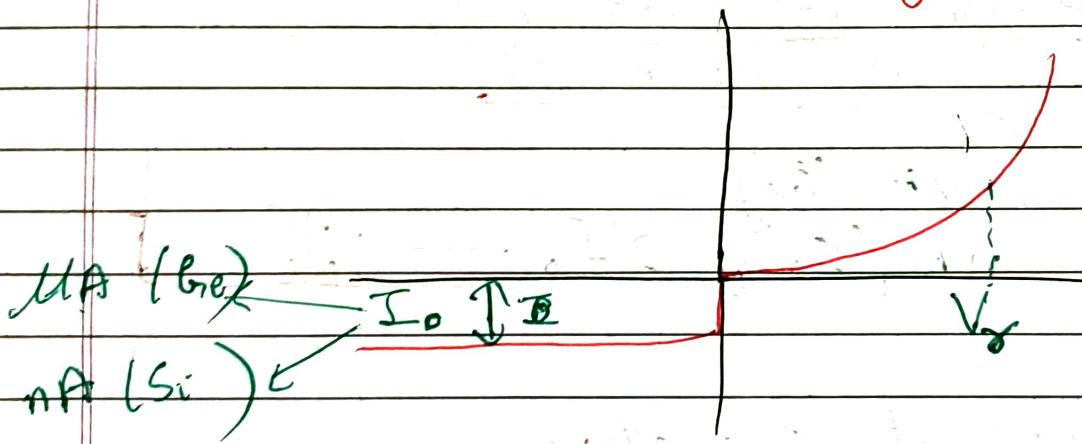
$$\text{For Reverse bias} \Rightarrow I = I_0 e^{\left(\frac{-10}{1 \times 25 \text{mV}} \right)} - 1$$

$$I = I_0 (e^{-400} - 1)$$

$$I = -I_0$$

$$\text{For forward bias} \Rightarrow I \propto (e^V - 1) \quad \begin{matrix} \text{exponentially} \\ \text{o/p at high } V \end{matrix}$$

* Temperature dependence of VI characteristics

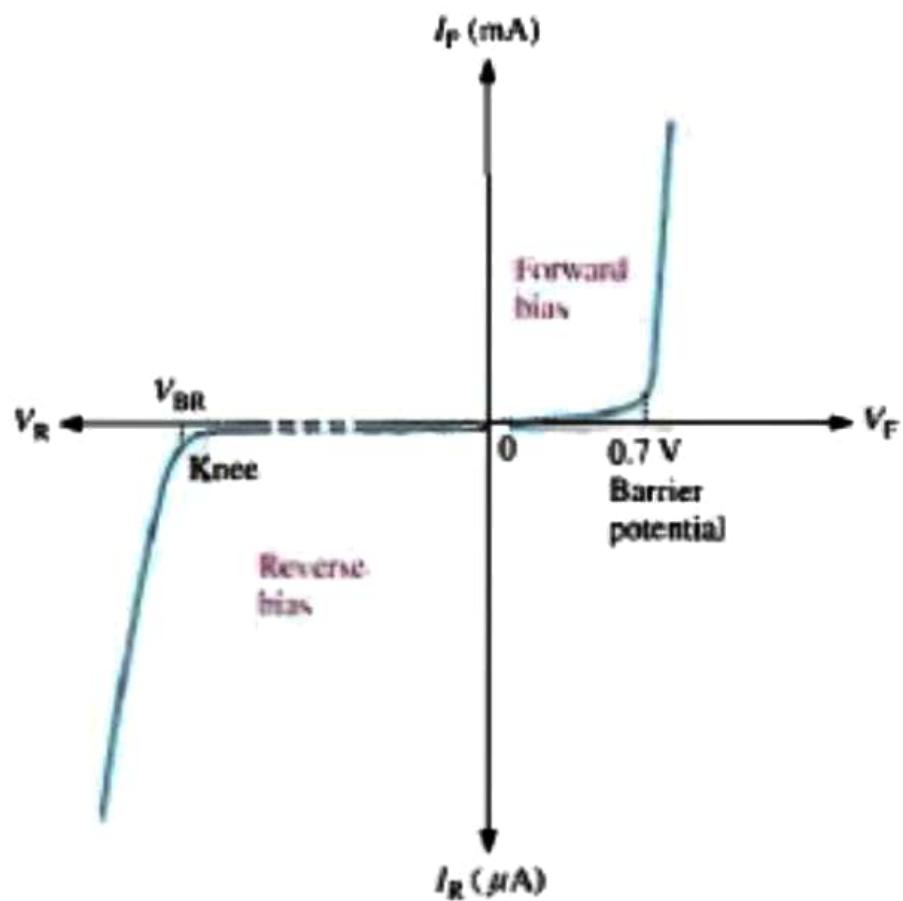


- Reverse saturation current doubles for every 10°C rise in temp.

- For 1°C it increases by 7%.

The Complete V-I Characteristic Curve

Combine the curves for both forward bias and reverse bias, and you have the complete V-I characteristic curve for a diode, as shown in Figure 1-29. Notice that the I_F scale is in mA compared to the I_R scale in μA .



◀ FIGURE 1-29

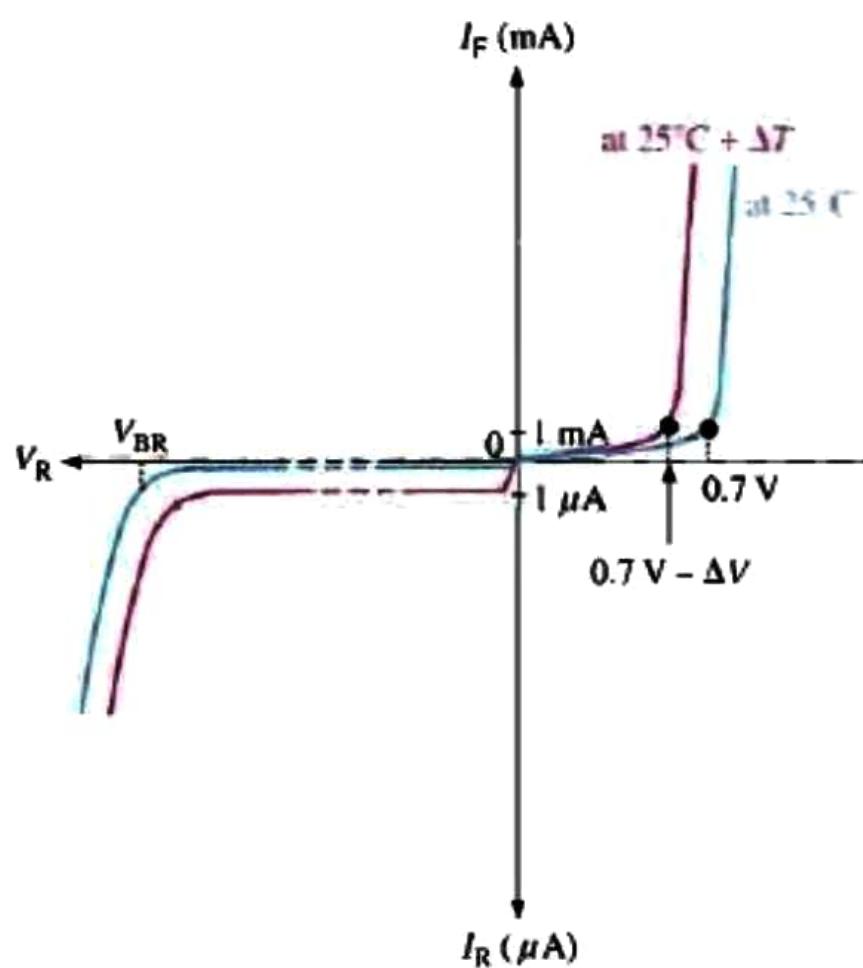
The complete V-I characteristic curve for a diode.

Temperature Effects For a forward-biased diode, as temperature is increased, the forward current increases for a given value of forward voltage. Also, for a given value of forward current, the forward voltage decreases. This is shown with the V-I characteristic curves in Figure 1-30. The blue curve is at room temperature (25°C) and the red curve is at an elevated temperature ($25^\circ\text{C} + \Delta T$). Notice that the barrier potential decreases as temperature increases.

For a reverse-biased diode, as temperature is increased, the reverse current increases. The difference in the two curves is exaggerated on the graph in Figure 1-30 for illustration. Keep in mind that the reverse current below breakdown remains extremely small and can usually be neglected.

► FIGURE 1-30

Temperature effect on the diode V - I characteristic. The 1 mA and 1 μ A marks on the vertical axis are given as a basis for a relative comparison of the current scales.



- Reverse saturation current at a temp T_2

$$I_{o2} = I_{o1} 2^{\frac{T_2 - T_1}{10}}$$

- The cut-in voltage decreased by $2.5 \text{ mV/}^\circ\text{C}$ is

$$\frac{dV}{dt} = -2.5 \text{ mV/}^\circ\text{C}$$

* Diode Resistance

Diode exhibits two types of resistance

- ① DC resistance R
- ② AC resistance.

* DC resistance (R)

At any point, the DC resistance is defined as ratio of voltage to current i.e. $R = \frac{V}{I}$

- It is also known as static resistance.

- Becoz of large variations in resistance values from point to point it is not used practically

* AC resistance (γ)

It is defined as the ratio of change in voltage to change in current.

$$\text{It is denoted by } \gamma = \frac{\partial V}{\partial I} = \frac{\Delta V}{\Delta I}$$

- Since its value nearly remains constant over a wide range of points, it is used practically.
- It is also called as dynamic resistance or incremental resistance -

~~Expression for Dynamic resistance (γ)~~

$$\text{We know that, } I = I_0 (e^{\frac{V}{nV_T}} - 1)$$

Differentiate w.r.t V

$$\frac{\partial I}{\partial V} = I_0 e^{\frac{V}{nV_T}} \left(\frac{1}{nV_T} \right) = 0$$

$$= I_0 e^{\frac{V}{nV_T}}$$

$$= \frac{I + I_0}{nV_T} \quad \boxed{I = I_0 e^{\frac{V}{nV_T}} - I_0}$$

$$\therefore \frac{dI}{dV} \approx \frac{I}{nV_T} \quad \text{as } I_0 \ll I$$

$$\therefore \boxed{\gamma = \frac{dV}{dI} = \frac{nV_T}{I}}$$

- Note:
- (1) Diode is a non-linear device but it can be assumed to be piece-wise linear.
 - (2) Diode behaves as a resistor at very high temperatures.

Silicon is more preferred, reverse saturation current is very small due to high forbidden gap between CB & VB

③ Diode offers less resistance in forward bias & high resistance in reverse bias. Hence it is used as a switch.

④ In R.B condition, the current flowing is also called as leakage current or unwanted current.

Ideally in R.B $I \xrightarrow{\text{should}} 0$

BeCoz of small reverse saturation current of silicon (nA), it is more preferred.

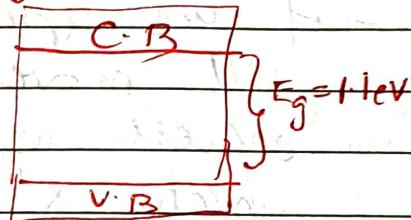
$$T_1 \quad T_2 = 10T_1$$

$$E_g(\text{Si}) = 1.1\text{eV}$$

$$\frac{E_g}{E_g} = \frac{1.1}{0.72} \text{ eV}$$

$$\text{Ge} \quad 10\mu\text{A} \xrightarrow{\text{double}} 20\mu\text{A}$$

$$\text{Si} \quad 10n\text{A} \xrightarrow{\text{double}} 20n\text{A}$$



BeCoz of small reverse saturation current of silicon, it is capable of withstanding higher temperature.

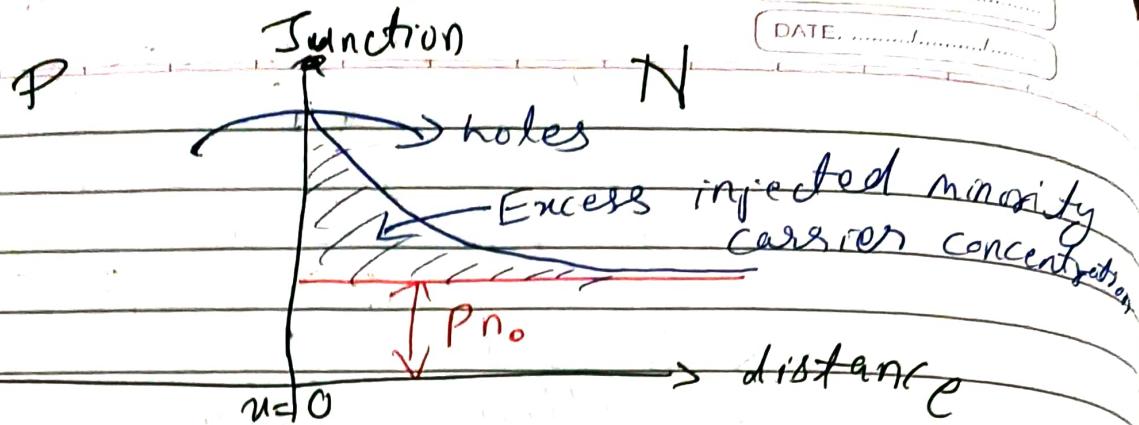
* Diode capacitance

Diode exhibits two types of capacitance.

- ① Diffusion capacitance
- ② Transition capacitance

* Diffusion capacitance

It is also called as storage capacitance



- Consider an n-type semi-conductor in a PN junction as shown in the fig above.
- The minority charge carriers (holes) under equilibrium are evenly distributed as shown in the fig with P_{n0} .

If we apply forward bias, then holes will move from P \rightarrow N, which is called excess injected minority carrier concentration which is more at the junction & decreases exponentially as we move away from the junction.

doubt - Similarly in p-type semiconductor, more no. of electrons are available at junction & its concentration decreases exponentially as we move away from junction.

- At either side of junction, the charge carriers are stored producing a capacitance effect known as diffusion or storage capacitance & is given as.

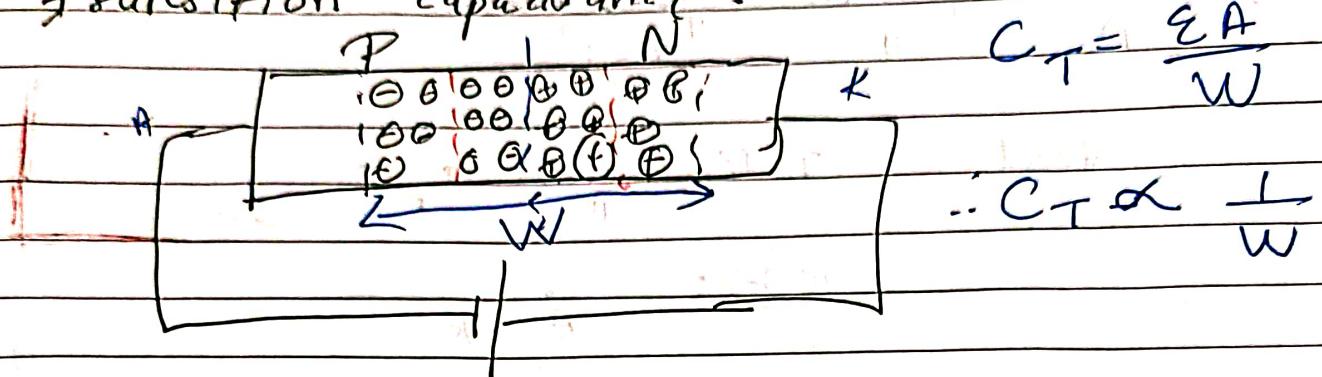
$$C_{\text{diffusion}} = I \cdot g$$

$$C_D = \frac{I}{g} \leftarrow A \cdot C \text{ resistance}$$

$$C_D = \frac{I I}{n V_T}$$

② Transition capacitance

Under Reverse bias condition, as reverse voltage increases, the width of the depletion layer increases, thereby uncovering more no. of immobile ions. This depletion effect producing capacitance effect is known as transition capacitance.



Thus transition capacitance is also called as depletion capacitance.

- Under RB condition, diode behaves as parallel plate capacitor

$$C_T \propto \frac{1}{\sqrt{V_B}} \quad \text{For abrupt PN junction}$$

↔ barriers ↔ voltage

$$C_T \propto \frac{1}{\sqrt{V_B}} \quad \text{For linearly graded junction.}$$

where $V_B = V_o + V_R$

V_o : open ckt potential \rightarrow Reverse voltage.

Under FB condition, C_D = diffusion capacitance is dominant while C_T is negligible.

Under RB condition

$C_D \rightarrow \text{negligible}$, $C_T \rightarrow \text{dominant}$

* * Diode equivalent ckt

A] DC equivalent ckt



Ideal :- F_B : A K

R_B : A K

V_R

I_R

(2)

F_B : A K V_r cut-in voltage

I_F

V_F

(3)

F_B : A K V_r R_F

I_F

V_F

(4)

B] AC equivalent ckt