RISC-V Simulator

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IDEAS

1) Introduction

This RISC V Simulator is written in **C++**.
It simulates the code written in RISC V, with some of the modifications and assumptions (given below under *Assumptions and Limitations*). The simulator will take a <filename>.asm file with the RISC V code written in it.

Sample codes and their outputs are present in *sample_codes* file in the github repo. The *main.cpp* file is the one that needs to be executed for simulating the assembly code.

GitFront link for the repository.

Functions

1) form_tokens(): takes any.*asm* file as input and converts it to a 2D vector of string tokens.

2) jump(): this function forms a map ‘jt’ that stores the indexes of the next instruction for all the locations mentioned in the code.

3) assign(): assigns all the registers their default values.

4) recog_instr(): recognizes the below mentioned instructions and executes them.

- li/sw/lw
- add
- sub
- mul
- div
- addi
- bne
- beq
- jal
- end

5) display_reg(): displays registers along with their corresponding values.

Assumptions and Limitations

1. The Simulator has no ecall functions.

2. We have provided an end keyword to end the program successfully.

3. The x2 register which is the Stack pointer register will be assigned value 0. But, this value can be changed later on.

4. As per reference from the Problem Statement pdf, no jalr function has been implemented.

5. All registers have been assigned with 0, as the default value.

6. The output of the program would be a list of all registers with the latest updated values.