Department of Electrical Engineering, IIT Palakkad

Hands-On Workshop On VLSI Design

RTL Simulation:
Synopsys VCS

INDIAN INSTITUTE
OF TECHNOLOGY
PALAKKAD

November 16, 2025

RTL Simulation with Synopsys VCS

- **Purpose:** Verify RTL functionality (logic correctness), exercise testbench scenarios, capture switching activity and early functional bugs before synthesis.
- **Flow:** Compile (elaboration) $\rightarrow$ Simulate $\rightarrow$ Inspect waveforms / logs.
- **Typical tools:** VCS (compile + sim), DVE/VERDI (waveform GUI launched by VCS -gui), simulators scripts / testbench for stimulus.

Compile & Run (examples)

Single command (compile + run + GUI):

```
vcs -R -gui -kdb -full64  rca_tb.v ../rtl/RCA.v
../rtl/FA.v ../rtl/register.v
```

- `-R` : compile and immediately run the simulation.
- `-gui` : open DVE/VERDI waveform GUI after simulation starts.
- `-kdb` : enable kernel debugger (interactive debug hooks).
- `-full64` : 64-bit build (recommended on modern hosts).

Waveform Capture (VCD / VPD / SAIF)

- **Common practice:** Add dump calls in the testbench for deterministic waveform output:

```
initial begin
  $dumpfile("dump.vcd");
  $dumpvars(0, tb_top);
  #1000 $finish;
end
```

- **VCS/DVE native:** VCS can produce `.vpd` files (fast and compact). DVE opens `.vpd` automatically when `-gui` is used.

Thank You!