MUE

LTSPICE ASSIGNMENT

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2019A3PS0178P · T2

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2019A3PS0297P T3

MUE LTSPICE ASSIGNMENT - 2

Question - 1.

Considerations taken while solving the question.

→ I_C of the BJT has been reduced since at lower I_C, g_m is also lesser leading to overall higher R_{out} and hence overall higher gain ($= g_m R_{out}$)

→ BJT has been biased such that $I_{req}/2 = 25\mu A$ is flowing through all BJT's in the cascode according to above mentioned point.

→ PNP transistor has been used for pull-up (load) side and NPN transistor have been used for driver side (pull-down) since ~~r_{out}~~ r_o of PNP is higher wrt NPN when working upwards

and NPN output resistance is higher when looking downwards as well. This same logic is used in designing CMOS inverters with PMOS load & NMOS driver.

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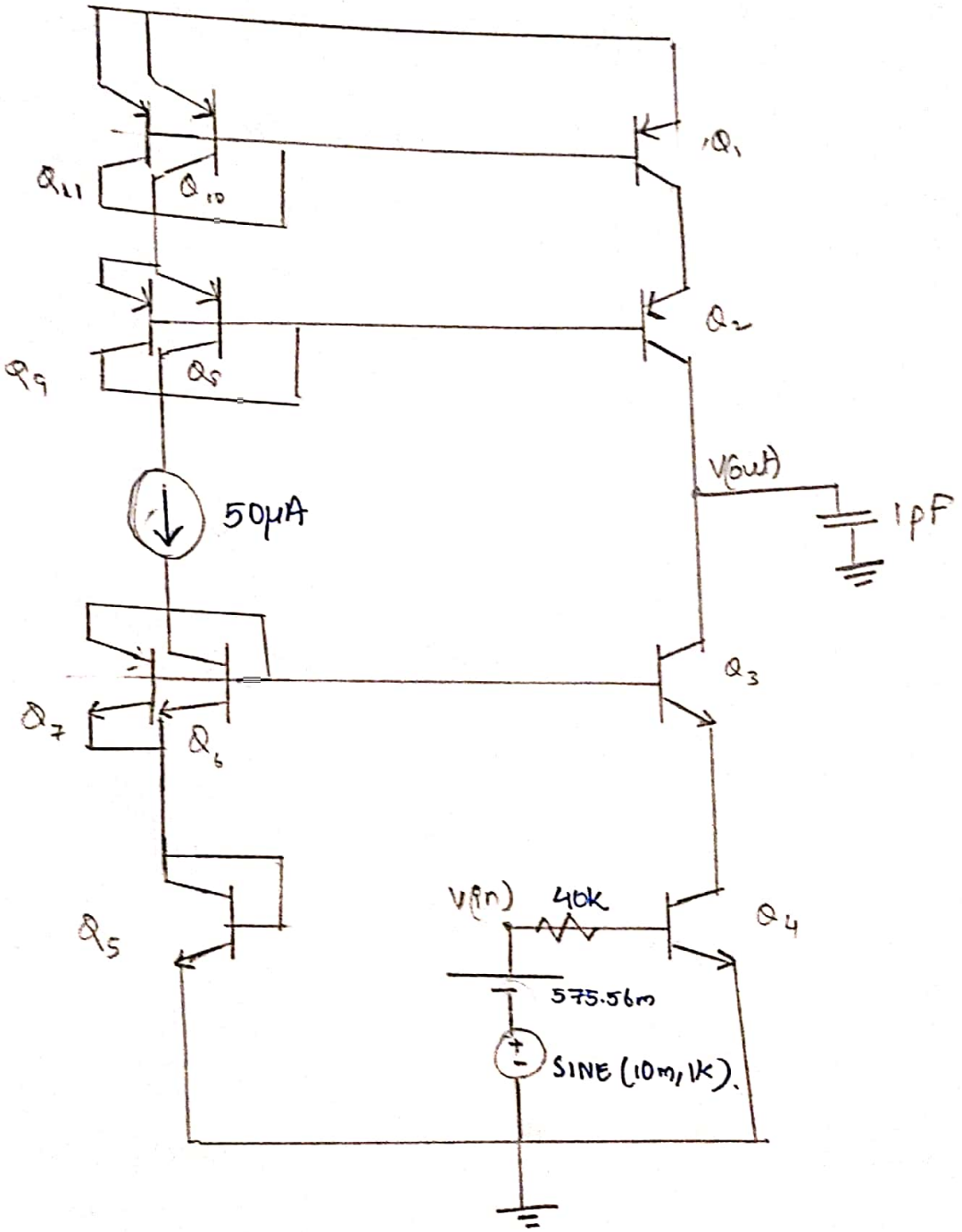
Design Topology



Hand calculations

1) g_m for pnp, npn

$$g_m = \frac{I_C}{V_T} = \frac{25\mu A}{26\times10^{-3}\ V} = 9.6\times10^{-4}\ A/V$$

$$= 0.96\ mA/V$$

Here $I_C = 25\mu A$ due to the reason that we have biased All BJT's at 25 μA.

2) r_o, r_π for PNP.

$$r_o = \frac{V_A}{I_C}\ ,\ r_\pi = \beta/g_m$$

for pnp model BC178B, V_A = early voltage is the parameter V_{af} in SPICE Library.

$V_{af} = 30.75\ V = V_A$.

β parameter is given library files as Bf or forward Beta.

$$\beta = Bf = 271.7.$$

$$(r_o)_{PNP} = \frac{30.75\ V}{25\mu A} = 1.23M\Omega$$

$$(r_\pi)_{pnp} = \frac{\beta}{g_m} = \frac{271.9}{9.6 \times 10^{-4}} = 283.229\ k\Omega$$

3) r_o, r_π for NPN

For NPN model BC108B (recommended)

$V_A = V_{af} = 59.59\ V$

$\beta_f = \beta = 381.7$

$$(r_o)_{npn} = \frac{59.59\ V}{25\ \mu A} = 2.3836\ M\Omega$$

$$(r_\pi)_{npn} = \frac{381.7}{9.6 \times 10^{-4}} = 397.604\ k\Omega$$

4) DC Analysis to get V_{BE} :

We know that $I_C = I_S e^{\frac{V_{BE}}{V_T}}$ for BJT

for our case, we are using NPN driver

hence for NPN model BC108B, I_S or the scaling current parameter is specified as

Is in library file.

$(I_S)_{npn} = 7.049\ fA = I_S$.

$(V_{BE})_{npn} = V_T \ln\left(\frac{I_C}{I_S}\right)$

$= 26\times10^{-3}\,V \times \ln\left(\frac{25\,mA}{7.049\,fA}\right)$

$= 26\times10^{-3}\,V \times \ln(3.54\times10^{9})$

$= 26\times10^{-3} \times 21.98$

$= 0.5717\ V$

$(I_S)_{pnp} = 336.7\,fA$

$(V_B)_{pnp} = V_T \ln\left(\frac{I_C}{I_S}\right) = 26\times10^{-3}\,V \times 18.12$

$= 0.471\,V$

for pnp BJT $V_{EB} = 0.471\,V$

In the circuit, we can see for Q_1 $V_E = 3.3\,V\ (= V_{CC})$ and then $V_B = 2.83\,V$ which is equivalent to the above req'd drop.

$V_C(Q_1)$ is same as V_B, since $\alpha \approx 1$ and hence no drop occurs through collector and base of pnp.

Since in cascode, $V_E(Q_2) = V_C(Q_1) = 2.831V$.

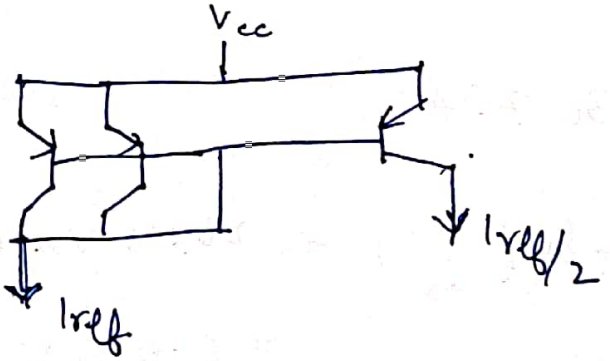
$V_B(Q_2) = 2.362V$, respectively above $V_{BE}(pnp) = 0.471V$ rule.

Now

5) Current Mirror Biasing.

Since we should not use resistors in the design active load current mirrors are used.

2 BJT's have been used in left arm to make $I_{rq} = 50\mu A$ (fixed) into $I_{ref} = 25\mu A$



DC Analysis for Rout

PTO

For BJT cascode circuit drawn the R_{out} is given as

$$R_{out} = R_{on} \parallel R_{op}$$

R_{op} = output resistance of PNP load.

R_{on} = output resistance of NPN driver.

R_{op} from small signal analysis of PNP

BJT $\Rightarrow R_{op} = g_{m_2} r_{o_2} (r_{o_1} \parallel r_{\pi_2})$

Here we are assuming $r_{o_2} = r_{o_1}$ since all PNP's are biased at $I_C = 25\mu A$ (hence $r_{\pi_2} = r_{\pi pnp}$)

$$R_{op} = g_{m_2} r_{o_2} r_{\pi_2} \quad (\text{since } r_{o_1} >> r_{\pi_2})$$

$$= \beta_{pnp} \times r_{o_2} \approx 334.43 M\Omega$$

Similarly $R_{on} = g_{m_3} r_{o_3} (r_{o_4} \parallel r_{\pi_3})$

$$= g_{m_3} r_{o_3} r_{\pi_3}$$

$$= (\beta)_{npn} r_{o_3}$$

$$= 909.51 M\Omega$$

Since in cascode, $V_G(Q_2) = V_G(Q_1) = 2.831V$

$V_S(Q_2)$ = [illegible]

Theoretical max gain

$$A_v = -g_m (R_{on} \| R_{op})$$

$$= -0.96 \times 10^{-3} (R_{on} \| R_{op})$$

$$= -0.96 \times 244.525\,M\Omega \times 10^{-3}$$

$$= -234744.4\ V/V$$

$$|A_v| = 87.41\ dB$$

Simulation Results

Amplifier specs:

1. Voltage gain = $80 \pm 5\%$ dB
2. current gain = $70 \pm 5\%$ dB
3. 3dB frequency = $40K \pm 5\%$ (rad/s) = $6.3kHz \pm 5\%$
4. $P_D = 2mW \pm 5\%$.

After many simulations, we arrived at

a Voltage gain = 62.03 dB.

current gain = 44.94 dB

3dB frequency = 6.12 KHz.

$P_D = 246\,\mu W + 60\,\mu W = 306\,\mu W \approx 0.3\,mW$

After probing to 3 significant digits for V_{in} to the driver BJT we arrived at

$$V_{in}\ (dc\ bias) = 0.57556\ V$$

$$= 575.56\ mV$$

At this voltage all the BJT's are having Ic very close to required 25μA.

Higher gain was definitely possible but we respected the 3dB frequency specification to get current value.

At a higher gain value the transistor would turn out to be slow and have poor bandwidth.

62dB was the maximum at which specified bandwidth was achieved; for the specified cascode topology.

Current gain was a byproduct and hence only 45dB was achievable with set voltage gain.

Phase margin = $\phi - (-180)$

where ϕ = Phase when gain = 0dB

$\phi = 11.194^\circ$.

Phase margin = $11.194 + 180$

$= 191.194^\circ > 45^\circ$ (required)

Gain Margin = 0 − (Gain when Phase = -180°)

For our design, Phase $= -180$ was never reached for even $\omega = 1$GHz, hence we have taken $G(\phi = -160^\circ) = -100$dB. for calculating gain margin.

∴ Gain margin ≈ 100 dB

$\omega_{\text{phase cross}} = 973$ KHz

$\omega_{\text{gain cross}} >> 1$GHz.

∴ System is stable.

Input swing

calculated using @.tf and. step param

is coming out to be 540m to 590m.