2 Input NOR Gate using CMOS

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Abstract

The design and implementation of a 2 Input CMOS NOR gate using the 28nm technology is to be explored in this paper. This NOR gate will be designed using the popular CMOS (Complementary metal-oxide semiconductor) technology as it reduces power dissipation, improves noise immunity, resulting in better performance. NOR gate is a Universal logic gate, made by logically inverting an OR gate. Giving a high output only when its inputs are low. All this implementation of the design is to be carried out using the Synopsys custom design tools.

Reference Circuit Details

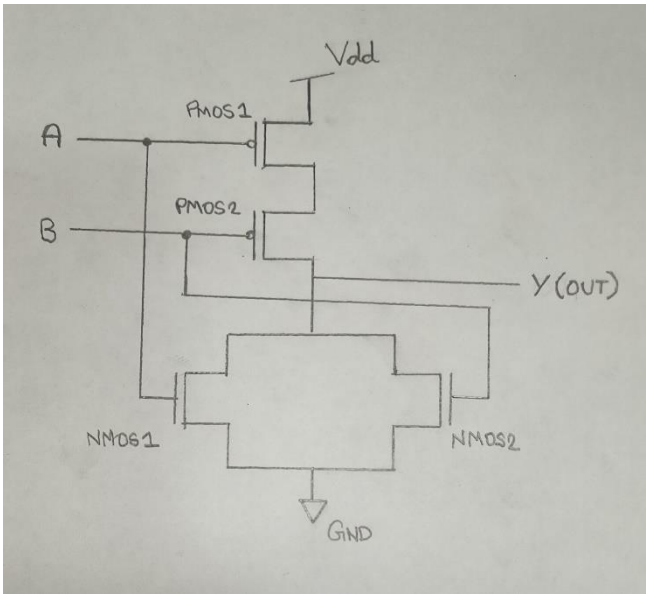
NOR gate is a universal gate. It is a logically inverted version of the basic OR gate. Two Inputs A and B along with an output Y are to be designed in the gate. The output to this gate will be high, only when all its inputs are low. To implement the CMOS technology for better performance, 2 PMOS transistors will be connected in series with one another, which then will be connected in series to 2 parallelly connected NMOS transistors.

Transistors PMOS1 and NMOS1 work as a complementary pair, as do transistors PMOS2 and NMOS2. Each pair is controlled by a single input signal (A and B respectively). The output of the CMOS NOR gate goes HIGH only when both inputs (A & B) are low, both the lower transistors get in Cutoff mode and both the upper transistors get Saturated. Otherwise, if either input A or input B is high, at least one of the lower transistors (NMOS1 or NMOS2) gets saturated making the output low.[1]

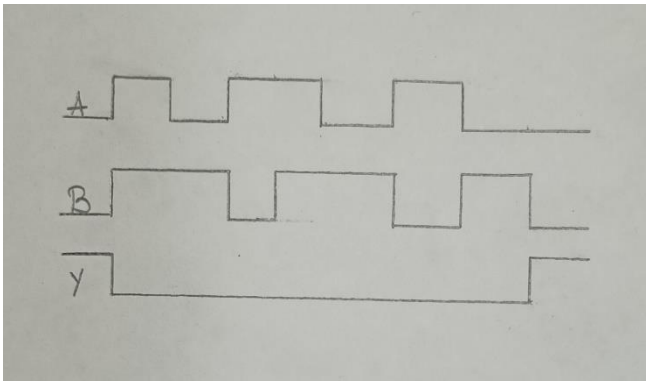
Truth Table

A	B	Y
Low	Low	High
Low	High	Low
High	Low	Low
High	High	Low

Reference Circuit



Reference Circuit Waveform



Reference

[1]https://www.researchgate.net/publication/316548029_Analysis_of_CMOS_based_NAeND_and_NOR_Gates_at_45_nm_Technology

[2]https://www.allaboutcircuits.com/textbook/digital/chpt-3/cmos-gate-circuitry/