Automated UVM Testbench Generator Using Python

Team:

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Problem Statement:

A verification engineer spends a lot of time coding repetitive UVM architectured testbenches for his designs. We can automate this testbench generation by using Python and keep the need and flexibility to code only the necessary testing logics.

Aim:

This project aims to read an input file specifying all requirements for the project, and generate skeleton files for the UVM Testbench architecture in Systemverilog.

Tools & Technologies:

Language	Python, SystemVerilog
Simulator	QuestaSim

Milestones:

Week 1	Finalize input file and requirements
Week 2	Implement parser and template infrastructure
Week 3	Generate agent/driver/monitor and necessary templates
Week 4	Generate sequence and environment files
Week 5	Compile & validate generated testbenches
Week 6	Complete documentation and deliverables