IQ wireless GmbH
Entwicklungsgesellschaft für Systeme und
Technologien der Telekommunikation

Highly Integrated S Band Transmitter for Pico and Nano Satellites

Mechanical, Electrical and Data Interfaces Specification

The HiSPiCO transmitter is a highly integrated S band transmitter with special focus in design and testing for Pico and Nano satellite applications.

Content of this document

Hardware Interface

The System Connector X2 provides the basic connections for power, data and control. It is a 12-pole SMC Connector with locking system. The male connecter is placed inside the transmitter.

Layout for System Connector X2:

A1	UBAT	PWR	Power supply + 3.3 V	RED
B1	UBAT	PWR	Power supply + 3.3 V	RED
A2	GND	PWR	Power supply GND	BLACK
B2	GND	PWR	Power supply GND	BLACK
A3	EXT_ON	IN	Switching signal to activate the transmitter (3.3 V high active)	WHITE
B3	V24_DX	OUT	TM (Temperature, CRC) V.24 data (38.400 Baud, 8N1) 3.3 V	YELLOW
A4	ADR_0	IN	Firmware selection by activation of transmitter (3.3 V high active)	BLUE
B4	\READY	OUT	NOT Ready signal of the transmitter (3.3V high in initialization or error state)	VIOLET
A5	ADR_1	IN	Firmware selection by activation of transmitter (3.3 V high active)	PINK
B5	DATA	IN	Transmit data (3-wire or UART input data)	BROWN
A6	\EN/FS	IN	Enable + Frame-Sync (not used with UART data interface)	GREAY
B6	CLK	IN/OUT	Clock for 3-wire data (usable as TC input with UART data interface)	YELLOW

Power Supply / Electrical Specification:

Input voltage	3.3 V nominal (3.0 V ...5.0 V)
Current draw	1.5 A (at P_{RF} = 27 dBm, depends on input voltage)
Enable voltage at EXT_ON Pin (X2:A4)	High Active: ≥ 2 V, max.: 5 V (a low active configuration is also available from manufacturer), pulled down to ground via 1MOhm resistor

All given voltages are specified with respect to the common ground level at the GND Pins (X2:A2,B2). Any other input pins then the EXT_ON Pin can tolerate a maximum voltage of 3.5 V.

The Firmware selection Pins (ADR_0, ADR_1 on X2:A4,A5) are pulled to ground via 10KOhm resistors. The V24_DX pin (X2:B3) is pulled up to internal 3.3V via a 10KOhm resistor. Any other signals are directly connected to the internal processor.

Transmitter Initialization:

The HiSPiCO Transmitter needs a setup time of maximal 1s for loading the selected firmware from the non-volatile memory, initialize the internal hardware and run a first self check. End of setup time and readiness for downloading data is given with the first telemetry output and the external \READY signal is turned to low again (see Diagram 1). Furthermore, the telemetry output should be checked for the correct parameters before sending data to the downlink data interface.

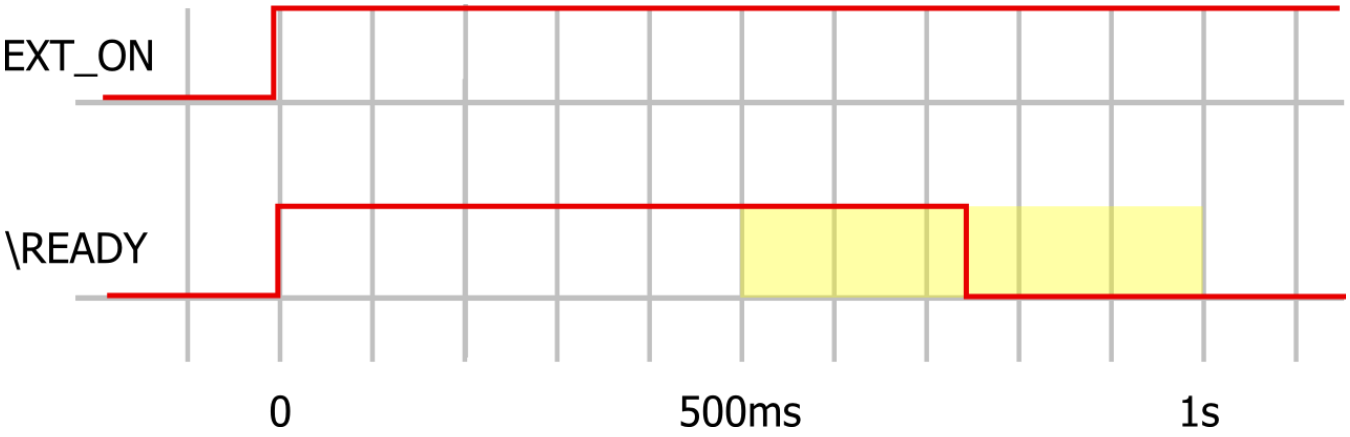

Diagram 1 EXT_ON and \READY-Signal during the startup.

For storing redundant or different transmitter firmware files, the internal non-volatile memory is divided into four sections. The satellite board computer selects the relevant firmware file by setting the signals on the ADR_0 and ADR_1 pins before the transmitter is enabled via the EXT_ON pin. ADR_0 and ADR_1 signals must be stable during the complete setup phase.

The integrity of the firmware data is checked via a CRC16 checksum, re-calculated and transferred to any telemetry output (see section below). After completing the setup phase, the satellite board computer can check the firmware checksum of the other firmware sections by selecting them on the ADR_0 and ADR1 pins without affecting the running program.

It is not possible for the internal processor to check the states of the ADR_0 and ADR1 pins.

Inrush Current:

The typical inrush current distribution is shown in Diagram 2, triggered with Ext_On-Signal. Please ensure that your power supply do not limit the current.

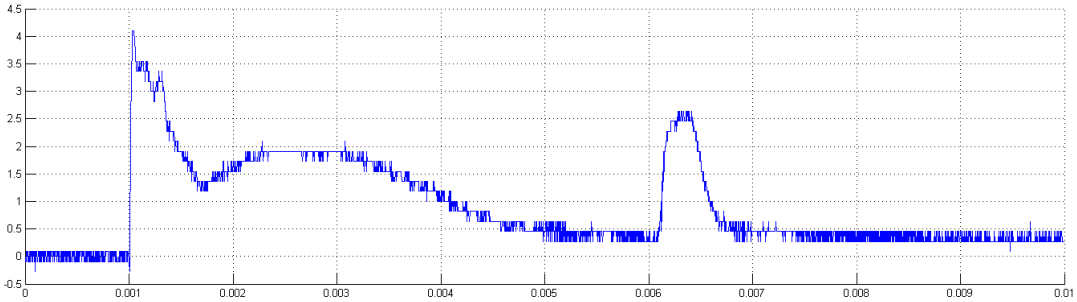

Diagram 2: Typical inrush current at startup (0.001 s) in A over time in s

3-wire Downlink Data Interface:

In standard 3-wire interface configuration, the Hispico Transmitter reads 8-bit words from the satellite board computer on a serial synchronous interface. Each 8-bit word is synchronized by a high active frame synchronization signal (\EN/FS) from the sender, which is detected on the first falling edge of the clock signal (CLK), which is also provided by the data sender.

Starting with the last falling CLK edge on an active frame synchronization impulse, the HiSPiCO transmitter reads the states of the DATA signal at eight consecutive falling edges of the CLK signal.

The Diagram 3 below shows the reception of downlink data bytes at the maximum data rate with frame synchronization impulses of one clock cycle duration following directly on the last data bit of the previous byte.

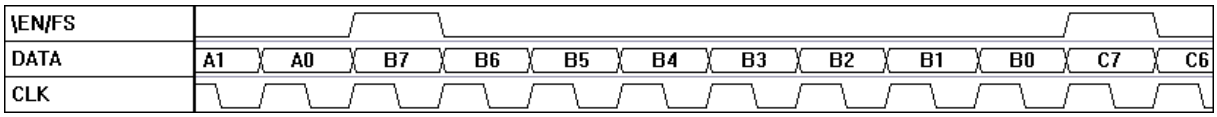

Diagram 3: Timing at max data rate (1.06MHz clock frequency)

A maximal clock frequency of 1.06MHz shall not be exceeded, because this is the maximum data rate for transmitting the data and there is no data buffer inside the transmitter.

In standard 3-wire operation, with the satellite board computer delivering the CLK and \EN/FS signals, it is possible to send less data by slowing the data and clock rate on the 3-wire interface or wait with the next frame synchronization impulse as a start signal for the next byte to transfer after the last byte has been transferred to the HiSPiCO Tx.
It is important that the 3-wire clock is running at least one clock cycle after the last data bit has been transferred, even if there is no directly follow-up of new data!

Any complete received data word will be transmitted by the HiSPiCO Transmitter in the same word order as it has been inputted into the downlink data interface.

Basically, the 3-wire interface is flexible for using different sampling clock edges and times or different frame synchronization level (low-active). It is also possible for the transmitter to act as the clock master or sample longer data words after one frame synchronization impulse. However, some of these parameters need changes in configuration to set the data interface compatible to a SPI interface whereas the frame synchronization signal is a low-active enable signal and the SPI-clock is stopped after a data word is transferred. Nevertheless, a frame synchronization signal or enable interrupt is needed after a particular data word length.
All these changes could only be performed by the HiSPiCO manufacturer within the firmware configuration procedure. The customer should contact the manufacturer (IQ wireless GmbH) in due time to check any specific interface requirements.

UART Downlink Data Interface:

Instead of the 3-wire interface, an UART compatible data interface can be provided on the HiSPiCO transmitter.

This would need only one signal line (pin DATA on X2:B5) for transferring the downlink data into the HiSPiCO Transmitter, but provides a lower data rate due to the asynchronous timing requirements.

In standard UART operation, the data interface uses a 8N1 UART configuration (8 data bits, no parity bit, one stop bit) for receiving the downlink data without any flow control.

The following baud rates are available at this time:
38400, 57600, 115200, 153600 Baud.

The used baud rate has to be set in the firmware configuration procedure with the manufacturer.

Other baud rates or UART configurations can be made available in customer specific firmware configurations. The customer should contact the manufacturer (IQ wireless GmbH) in due time to check any specific interface requirements.

The selection of the data interface type (3-wire or UART) is done in hardware as well as software during the manufacturing process and cannot be changed by the customer/user. Some parameters can be different in different firmwares in the four firmware sections, and can be changed by the customer/user on that firmware selection process.

Telemetry Interface:

Information about the state and the configuration of the HiSPiCO transmitter is given via an UART telemetry interface. The data is send out of the HiSPiCO transmitter on pin V24_DX (X2:B3) in 8N1 UART configuration (8 data bits, no parity bit, one stop bit) with a baud rate of 38400.
The telemetry data is outputted within a data block which contains mostly ASCII characters to make it readable for a connected satellite board computer and terminal console.

An example data block of the standard telemetry output is shown and explained in the tables below.

	example/pattern	Size in number of bytes
Start sequence (VT100-ClearScreen)	0x1B 0x5B 0x32 0x4A	4
Telemetry ASCII block (explained below)	Hispico: 01.03.00 May 30 2011 17:44:59 run: 0000002597 FLASH: F2A3/1A1A Temp: +039 Commands: 0000000023/0000000005/x Freq: 2200000 TxPo: 208 ON Normal 1.02 Data: 0010000000 UART 115200 Check:	195
End sequence (ASCII CRC16 checksum)	$xxxx_h$	4

Explanation of the example telemetry ASCII data block: (with end sequence)

Pos.	Fixed pattern	Example value	
0x04	"Hispico: "	"01.03.00"	Firmware and system version
0x15		" May 30 2011 17:44:59"	Data and time of firmware compilation
0x2A	" run: "	"0000002597"	Running time in seconds
0x3A	"\r\nFLASH: "	"F2A3/1A1A"	CRC16 checksum of firmware and configuration data in non-volatile memory
0x4C	" Temp: "	"+039"	Internal transmitter temperature
0x57	" Commands: "	"0000000023/0000000005/x"	Numbers and repetition of received/unknown/last Telecommand bytes
0x97	"\r\nFreq: "	"2200000"	Fixed configured transmit frequency
0x88	" TxPo: "	"208"	Configuration value for configured transmit power
0x92		" ON Normal 1.02"	States and operating modes of transmitter
0xA2	"\r\nData: "	"0010000000"	Number of transmitted downlink data since last power up
0xB4		" UART 115200"	Operating mode of data interface
0cC0	" Check: "	"3EF0"	CRC16 checksum of telemetry data block (example not correct)

The CRC16 calculation of the telemetry data is done over all 203 bytes, whereas the checksum value is set to zero. The checksums of the selected (by ADR_0 and ADR_1 pins) firmware and configuration data are calculated before every output of the telemetry data

block. Reference checksums for firmware and configuration data are provided by the manufacturer or can be read out at ground test operations.

Some telemetry data (e.g. version, frequency, state and operating modes) are for system state and system configuration information only and cannot be adjusted or configured at customer's side.

In standard configuration of the HiSPiCO Transmitter, this telemetry dataset is outputted in a time interval of five seconds.

It is possible to customize the content or behavior of the telemetry output at manufacturer's firmware creation and configuration process.

Telecommand Interface (optional)

In standard configuration, it is not possible to configure the HiSPiCO transmitter at customer's side or on board of a satellite.

If the customer requirements need additional configuration capabilities (e.g. changing the transmit power), an internal test and debug interface for commanding the HiSPiCO transmitter could be realized and be made available.

This is an UART compatible interface (8N1, 38400 Baud, 3.3V TTL) on the test and debug interface connector pin X1:A4 (same connector type then X2). It can receive and interpret single command bytes.

Details of the tele-command interface are created customer specifically by the HiSPiCO manufacturer. The customer should contact the manufacturer (IQ wireless GmbH) in due time to check any specific interface requirements.

Note that the X1 connector has no EMI filters.

If the HiSPiCO transmitter is configured for the UART downlink data interface, it is possible to use CLK line on pin X2:B6 for that tele-command interface.

Mechanical Interface (optional)

The form factor is designed to fit into a standard pico satellite "cubesat". Please use the inner M3 holes with internal thread for mounting the transmitter into your satellite structure. The holes are located on the top and on the bottom side. Do not screw those deeper than described in drawing. Otherwise you may destroy the inner PCB.

The heat from the transmitter is dissipated to the housing on the straight front side, where the cables are connected. There are four screws, which are connecting the metal housing with the internal heat sink (thermal hot spot) of the Tx device.

The attached drawing shows the mounting points and the optional thermal interface area, marked as "Heatsink" in more details. Please mount it with M2 screws, the inner thread provides 4 mm.

For any further questions or problems, please contact the IQ wireless office per email and/or telephone via the above given contact data.