AN1618

HOW TO USE SAMRH71 TCM WITH ERROR CORRECTION CODE?

Introduction

This application note provides information about configuring and using Tightly Coupled Memory with Hardened Error Correction Code (TCMHECC) with the Microchip SAMRH71 microcontroller using the MPLAB development environment.

The application note includes:

- An overview of the MICROCHIP SAMRH71
- Guidelines for configuring the TCM in Software

Table of Contents

1. Features

The Microchip SAMRH71 has the following features:

- Core:
  - ARM® Cortex®-M7 processor running at up to 100 MHz
  - 16-Kbytes Instruction-Cache and 16-Kbytes Data-Cache with Error Correction Code (ECC)
  - Memory Protection Unit (MPU) with 16 zones
  - Single- and double-precision hardware floating point unit
  - DSP instructions, Thumb-2 instruction set
  - Embedded Trace Module (ETM) with instruction trace stream, including Trace Port Interface Unit (TPIU)
- Memory:
  - 128-Kbytes embedded Flash with build in ECC
  - 384-Kbytes embedded SRAM for Tightly Coupled Memory (TCM)
  - 768 Kbytes of multiport SRAM
  - Hardened External Memory Controller (HEMC)

2. SAMRH71 Microcontroller

The aerospace qualified SAMRH71 microcontroller offers a high-performance core, an ARM Cortex-M7, with an advanced memory architecture with up to 768 Kbytes of multi-port internal SRAM and 384 KBytes of TCM memories.

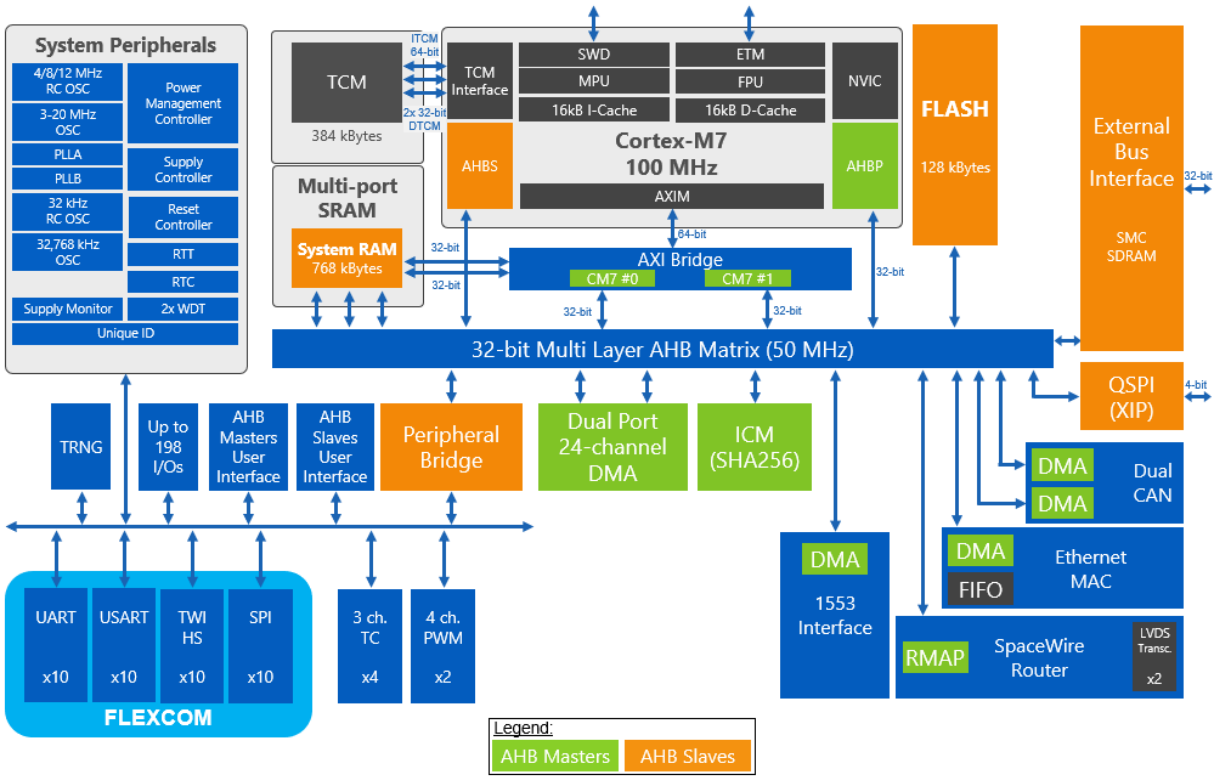
The SAMRH71 has a full set of peripherals, for more information, refer to the datasheet of the device.

To ensure a high-speed, low latency, and deterministic access for time critical code and data, the ARM® Cortex-M7 core is connected to a TCM memory. This TCM memory embeds a TCMHECC module to protect the data from radiation events.

A multilayer Bus MATRIX interconnects the peripherals with the multi-port SRAM (FlexRAM).

An architecture of the SAMRH71 microcontroller is presented in the following image.

Figure 2-1. System Architecture



3. TCM Memory VS Cache Memory VS FlexRAM Memory

This section highlights the key differences between TCM memory, Cache memory, and FlexRAM memory.

Table 3-1. TCM Memory VS Cache Memory VS FlexRAM Memory

Tightly Coupled Memory	Cache Memory	FlexRAM Memory
The processor core has a direct access to this memory. The TCM is running at the same speed as the processor. For the SAMRH71, there are two dedicated interfaces to TCM: • The Instruction TCM (128 Kbytes) • The Data TCM (256 Kbytes)	This is RAM integrated inside the Cortex-M7 core itself. For the SAMRH71, 16 Kbyte of Instruction Cache and 16 Kbyte of Data Cache are available.	This is a 768-Kbyte memory accessed by: • The peripherals by the AHB matrix • The processor by its direct connexions
It is part of the system memory map.	it is not part of the system memory map. It does not have a physical memory address.	It is part of the system memory map.
The user can decide the content to be stored in TCM at compilation time.	The user can decide whether to use the cache capabilities on a specific region or not. It shall be enabled and configured before usage.	The user can decide the content to be stored in FlexRAM at compilation time.
It is directly accessible to software.	During the program execution, the cache is loaded with instructions or data fetched from the memory to the CPU.	The memory is directly accessible to software.
It can be accessed both by the CPU and by the DMA.	It cannot be accessed by DMA.	It can be accessed by the CPU and by the DMA through the AHB_S port.
It has deterministic access time. It always takes a single cycle to access the TCM content.	It serves as an intermediate buffer between the processor and the memory to reduce the memory access time. The number of cycles needed to access a memory location differs for a *cache-hit* or a *cache-miss*.	It has no deterministic access time.

Note:
TCM content is not cachable. The TCM is directly connected to the Cortex-M7 core by I/DTCM interfaces. It can be accessed at the same speed as the cache without the penalty of a cache-miss or any cache coherence issues.

4. SAMRH71 TCM Memory

The SAMRH71 microcontroller architecture supports two TCM memory instances: Instruction TCM (ITCM) and Data TCM (DTCM).

The base address of each TCM is defined in the product address mapping:

- ITCM at 0x00000000 to 0x0001FFFF
- DTCM at 0x20000000 to 0x2003FFFF

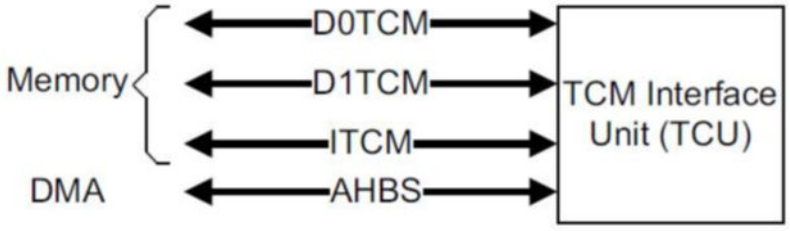
The ITCM overlaps with the HEMC PROM/Flash when it is enabled (the ITCM is not enabled by default). On the contrary, the DTCM is enabled by default.

4.1 TCM Interface Unit (TCU)

The TCM unit interfaces to the following:

- **ITCM**: A single 64-bit interface, to communicate efficiently with the processor.
- **DTCM**: Two 32-bit interfaces. Two 32-bit data can be fetched concurrently in a single cycle from the DTCM.
- **AHBS**: TCM memory can be accessed by DMA through the AHB Slave bus interface enabling peripherals to directly access the TCM memory without any CPU intervention.
  The following image shows the interfaces with a TCM unit.

Figure 4-1. TCM Interface



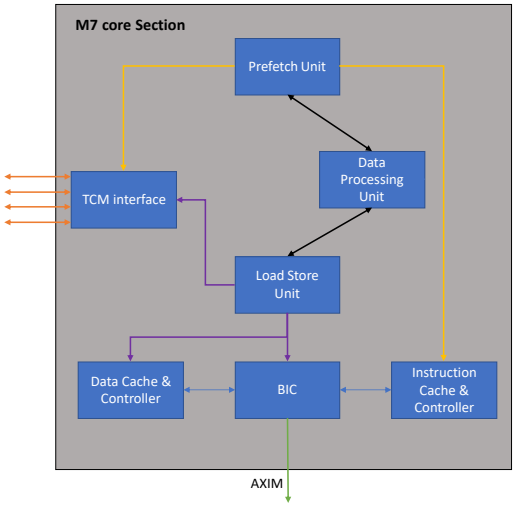
4.2 TCM Access

Read or write requests for each TCM interface are triggered by the following core interfaces.

- Load Store Unit (LSU)
- Pre-Fetch Unit (PFU)
- System AHBS Interface (AHBS)
- Debug Unit (DGU)

The TCM Interface Unit (TCU) contains arbitration logic to manage access requested by various interfaces. The PFU can only read from the TCM, whereas other interfaces can both read and write the TCM.

Figure 4-2. Cortex-M7 Architecture for TCM Interface



4.3 TCM Configuration

The TCM has a fixed configuration:

- 128 Kbytes for the ITCM
- 256 Kbytes for the DTCM

The TCM is accessed at the full processor clock speed (HCK). For the SAMRH71, the HCK can be up to 100 MHz without any wait states.

4.4 TCM Hardened Error Correction Code (TCMHECC)

The TCMHECC is a module embedded in the TCM interface to protect data against radiation effects.

The TCMHECC comprises of:

- Four Hamming encoders/decoders:
  - One Hamming for ITCM MSB – 32 bits
  - One Hamming for ITCM LSB – 32 bits
  - One Hamming for DTCM0 – 32 bits
  - One Hamming for DTCM1 – 32 bits
- An APB end-user interface:
  - To enable/disable the TCMHECC protection
  - To activate/deactivate the TCMHECC test mode for all Hamming blocks (independently in read or write mode)
  - To reset the TCMHECC fixable and unfixable counters
- An APB end-user interface for error status and reporting (either by interruption or by polling):
  - Indicates whether fixable errors have been detected, corrected on-the-fly, and count them
  - Indicates whether unfixable errors have been detected and count them
  - Indicates the address and the origin of the last TCMHECC error detected

5. TCM and ECC Software Implications

The following sections discuss the software implication of the TCM and its associated ECC.

5.1 SAMRH71 Boot Mode

The SAMRH71 can boot from several memories:

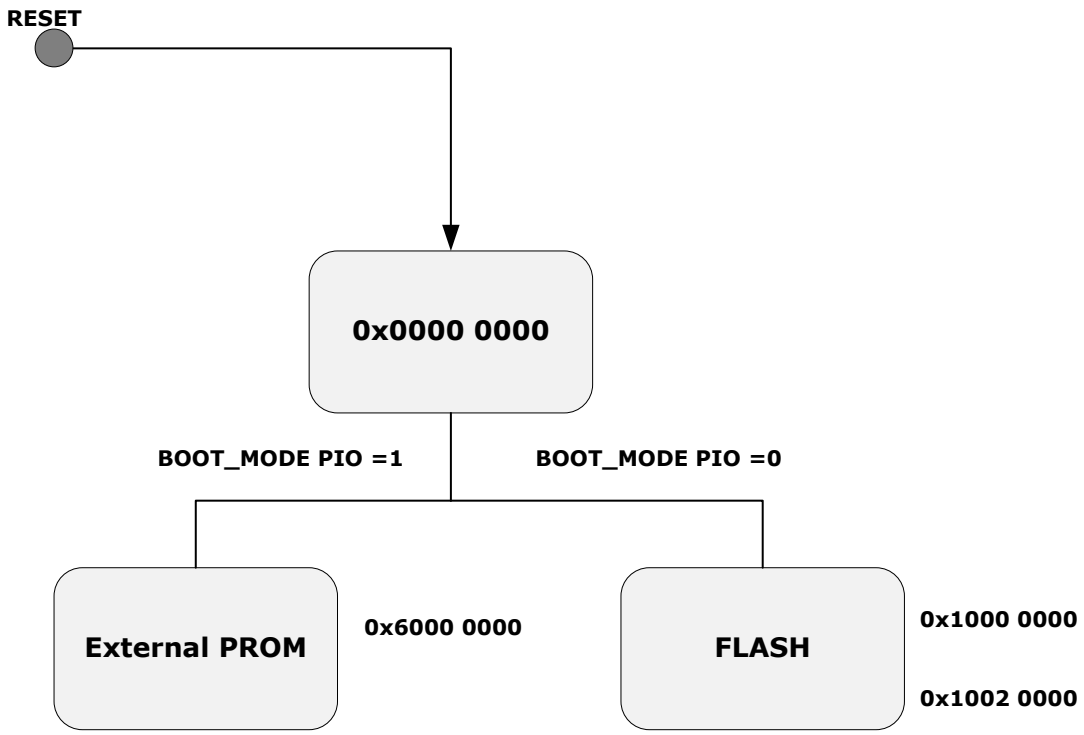
- Internal Flash memory through HEFC
- External PROM memory through HEMC

The selection is performed by reading `BOOT_MODE PIO (PF24)` at boot time:

- 0b0: internal Flash memory (HEFC)
- 0b1: external PROM memory (HEMC)

The selection made by the `BOOT_MODE PIO (PF24)` mirrors the address of the selected memory to `0x00000000`, allowing the processor to boot on this memory (PROM and FLASH).

Figure 5-1. Address "0" Mapping on ITCM Configuration



5.2 ITCM at Address 0x0

In the SAMRH71, when enabled, the ITCM region is mapped to 0x0000 0000 in place of the internal flash or the external PROM.

The bit [0] of the ITCMCR register is used to enable/disable the ITCM.

- When this bit is set, the Cortex-M7 fetches all the mapped instructions in the ITCM range (0x0 – last ITCM address) through the ITCM interface.

- The flash and PROM memories are still available at their physical memory address starting at 0x1000 0000 or 0x6000 0000 respectively.
- On reset, the ITCM is disabled and bit[0] of the ITCMCR register is cleared.

The Vector table and the start-up code can be located in the external PROM or the Flash.

The Cortex-M7 performs all the instruction accesses after a reset through the AXI bus and does not access the TCM interface. Therefore, the address 0x0000 0000 points to either the internal flash or the external PROM after a reset. However, as soon as the ITCMCR is configured to enable the ITCM, any access at address 0x0000 0000 would be to the ITCM through the TCM interface.

5.3 Mapping ITCM and Vector Table Relocation (VTOR) Register

The default vector table address is 0x0000 0000, if the ITCM is not used, it then points to the internal flash (0x1000 0000) or the external PROM (0x6000 0000) where the vector table is typically located. When an interrupt is triggered, its handler is fetched based on the VTOR offset.

If the ITCM is enabled, the VTOR does not point anymore to the beginning of the vector table located in Flash/PROM but, to the beginning of ITCM. It is necessary to update the VTOR to point to the start address of the Vector table.

There are two possible options to re-map the vector table:

- Write the VTOR register with the address of the interrupt vector table in Flash/PROM
- Copy the vector table to the ITCM and update the VTOR content to point to it

The user can also copy any critical interrupt handlers to ITCM to improve access speed and reduce latency while servicing interrupts. For fast and consistent interrupt responses to time-critical events, both vector table and event handlers should be located in the ITCM.

5.4 DTCM

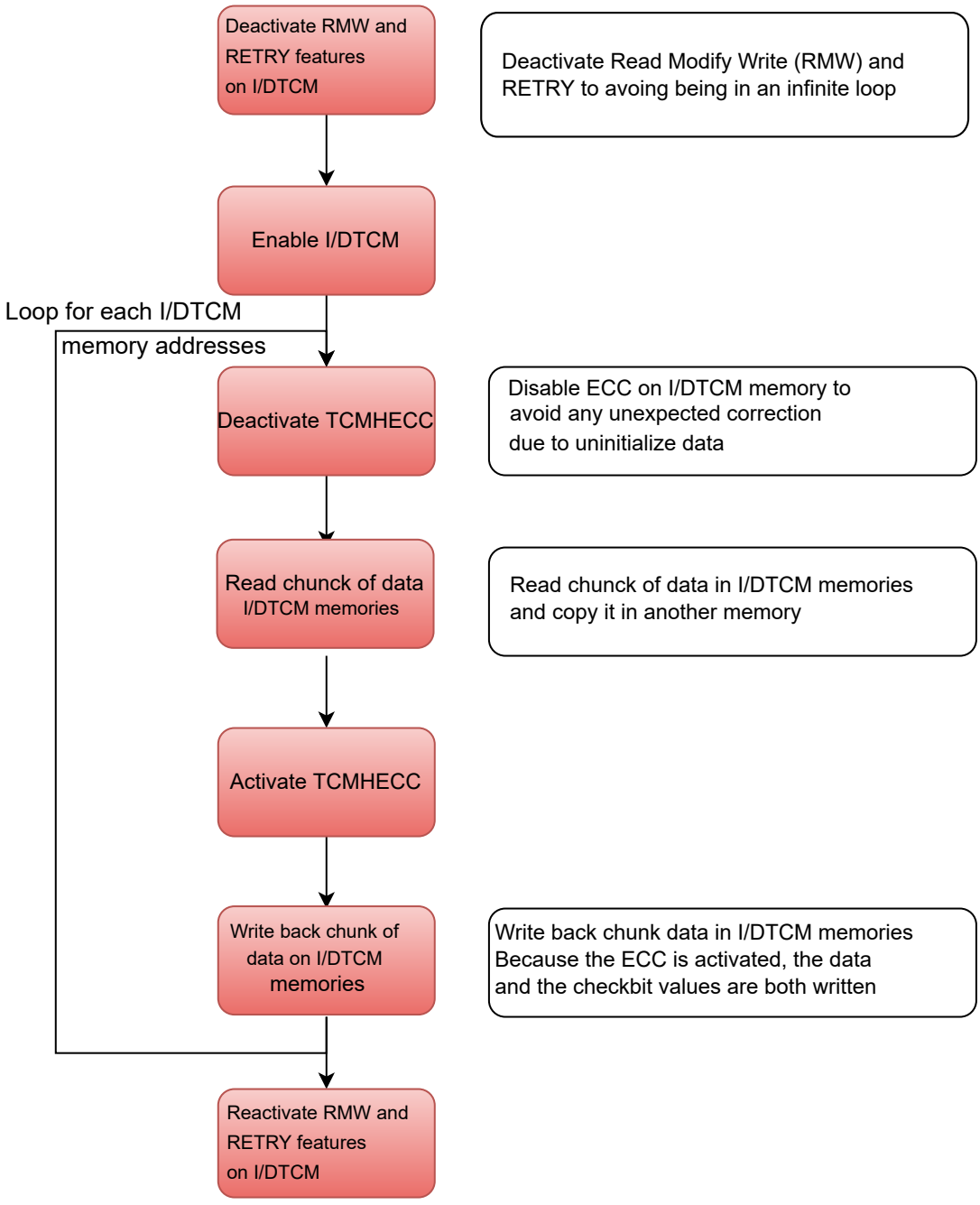
The DTCM size is fixed to 256 Kbytes.

Bit [0] in DTCMCR can be used to disable/enable the DTCM.

6. Programming Sequence for TCM ECC Application

The following flow chart demonstrates the programming sequence for the TCM ECC application.

Figure 6-1. Programming Sequence



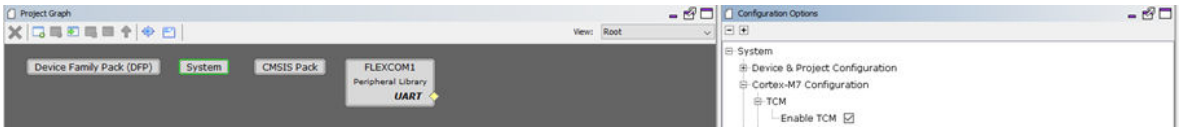
7. Example Software

The MPLAB project provided with this application note contains the linker file - *ATSAMRH71F20B.ld*– located in the *ARSAMRH71F20B* folder. It is available in the path - *C:\Program Files x86)\Microchip\MPLABX \"mplab_version"\packs\Microchip\SAMRH71_DFP\"dfp_version"\xc32\ATSAMRH71F20B*.

To set up the linker file to use the TCM, perform the following step.

1. In the MPLAB Harmony configurator, select **System** and then under **Cortex-M7 Configuration**, select the **Enable TCM** option. The ECC for the TCM is enabled by default.

Figure 7-1. Harmony System Overview



7.1 Software Flow in MPLAB

The code flow at startup in MPLAB is from `Reset_Handler()` and can be found in the *startup_xc32.c* file.

`Reset_Handler()` :

1. `TCM_EccInitialize()` : Initializes TCM with ECC.
2. `__pic32c_data_initialization()`: Initializes data after TCM is enabled.
3. `SCB->VTOR = ((uint32_t) pSrc & SCB_VTOR_TBLOFF_Msk)`: Sets the Vector table address in FLASH.
4. `__libc_init_array()`: Initializes the C library.
5. `Main()`: launch application's main function.

`TCM_EccInitialize()`:

1. `TCMECC_REGS→TCMECC_CR = 0x0` → deactivates TCMHECC.
2. `SCB→ITCMCR = (SCB_ITCMCR_EN_Msk)` → activates ITCM and deactivates RMW and RETRY.
3. `SCB→DTCMCR = (SCB_DTCMCR_EN_Msk)` → activates DTCM and deactivates RMW and RETRY.
4. ITCM and DTCM read and write back chunck of data loops.
5. `SCB→ITCMCR = (SCB_ITCMCR_EN_Msk | SCB_ITCMCR_RMW_Msk | SCB_ITCMCR_RETEN_Msk)` → activates RMW, RETRY, and ITCM.
6. `SCB→DTCMCR = (SCB_DTCMCR_EN_Msk | SCB_DTCMCR_RMW_Msk | SCB_DTCMCR_RETEN_Msk)` → activates RMW, RETRY, and DTCM.
7. `TCMECC_REGS→TCMECC_CR = 0x1` → activates TCMHECC.

7.2 Example

An example can be found in the MPLAB example directories, where, only the DTCM is used.

In the example code, in *main_rh71.c*, three buffers: `writeBuffer`, `readBuffer`, and `echoBuffer` are defined and placed in DTCM by using `__attribute__ ((tcm))`.

```
static char __attribute__ ((tcm)) writeBuffer[] = "**** Data TCM Demo \
****\r\n**** Demo uses TCM memory to handle cache coherency \
****\r\n**** Type a buffer of 10 characters and observe it echo back \
****\r\n**** LED toggles on each time buffer is echoed ****\r\n";
static char __attribute__ ((tcm)) readBuffer[READ_SIZE] = {};
static char __attribute__ ((tcm)) echoBuffer[READ_SIZE + 3] = {};
```

- `SYS_Initialize` function initialises clocks PIOs, XDMAC, and UART on Flexcom1 and NVIC.
- `XDMAC` function transfers data from UART to DTCM and vice versa.

- `memcpy(echoBuffer, readBuffer, READ_SIZE)` function copies data from `readBuffer` to `echoBuffer`.

As shown in the following image, after exectuting the code, you can see in the DTCM (Address 0x2000 0000) the writeBuffer variable.

Note: If you want to use the ITCM, use the same `__attribute__ ((tcm))` for your functions

Figure 7-2. Execution Memory

Address	00	02	04	06	08	0A	0C	0E	ASCII
									DTCM Memory
2000_0000	2A2A	2A2A	4420	7461	2061	4354	204D	6544	**** Dat a TCM De
2000_0010	6F6D	2A20	2A2A	0D2A	2A0A	2A2A	202A	6544	mo ****. .**** De
2000_0020	6F6D	7520	6573	2073	4354	204D	656D	6F6D	mo uses TCM memo
2000_0030	7972	7420	206F	6168	646E	656C	6320	6361	ry to ha ndle cac
2000_0040	6568	6320	686F	7265	6E65	7963	2A20	2A2A	he coher ency ***
2000_0050	0D2A	2A0A	2A2A	202A	7954	6570	6120	6220	*..**** Type a b
2000_0060	6675	6566	2072	666F	3120	2030	6863	7261	uffer of 10 char
2000_0070	6361	6574	7372	6120	646E	6F20	7362	7265	acters a nd obser
2000_0080	6576	6920	2074	6365	6F68	6220	6361	206B	ve it ec ho back
2000_0090	2A2A	2A2A	0A0D	2A2A	2A2A	4C20	4445	7420	****..** ** LED t
2000_00A0	676F	6C67	7365	6F20	206E	6165	6863	7420	oggles o n each t
2000_00B0	6D69	2065	7562	6666	7265	6920	2073	6365	ime buff er is ec
2000_00C0	6F68	6465	2A20	2A2A	0D2A	000A	0000	0000	hoed *** *.......

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8.1 Revision A - 04/2020

Initial revision.

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