

BOARD CHARACTERISTICS

Copper Layer Count: 8
 Board overall dimensions: 3.550" x 3.982"
 Min track/spacing: 0.006" / 0.006"
 Copper Finish: ENIG
 Castellated pads: No
 Edge card connectors: Yes, Bevelled, 30 degrees.
 Board Thickness: 0.062"
 Min hole diameter: 10.00 mils
 Impedance Control: Yes
 Plated Board Edge: No

FAB NOTES:

1. IPC-6012E Class 2
2. Matte Green soldermask, White silkscreen.
3. Fabricate on Nelco N7000-2HT
4. 1oz outer, 1oz inner copper.
5. Bevel edge connector 30 degrees minimum.
6. Fill all vias with non-conductive material.
7. Board target thickness shall be 0.062"
8. Immersion gold plating on finger thickness shall be 2U"
9. 13mil traces on layer 1&8 shall be impedance controlled to 50R single ended
10. 7 mil traces on layer 3&6 shall be impedance controlled to 90R differential

VENDOR ASSEMBLY NOTES:

1. J-STD-001G Class 2
2. BOM provided with submitted files shall be the controlling document for component information.
3. Do not apply solder to pads of DNP components
4. Assemble with leaded solder.

ASSEMBLY NOTES:

1. Stake components specified in BOM with 3M 2216
2. Conformal Coat with Arathane 5750:
 Ensure coating does not prevent electrical contact with connectors and mounting holes.

FAB COMMENTS:

1. Class 3 for PCBway, class 2 for US vendor.
2. Nelco N7000-2HT preferred for flight, but PCBway SH260 is acceptable.

ASSEMBLY COMMENTS:

1. Class 3 preferred



TECHNOLOGY DEVELOPMENT & ENGINEERING CENTER EAST
 11401 HOOVER ROAD, MILAN, OHIO 44846

TITLE

mainboard

SIZE

DWG NO.

B

REV

C

DRAWN BY

CH

ENGINEER

CH

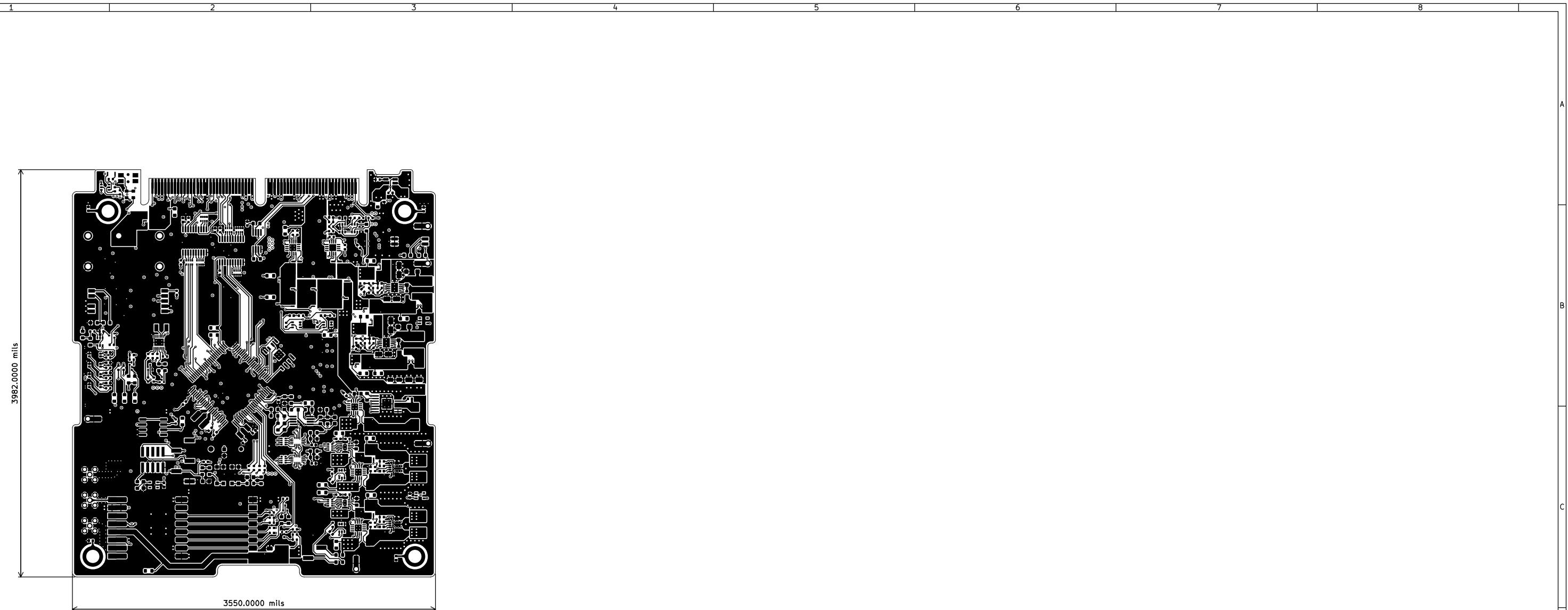
2023-06-21

FILE NAME

mainboard.kicad_pcb

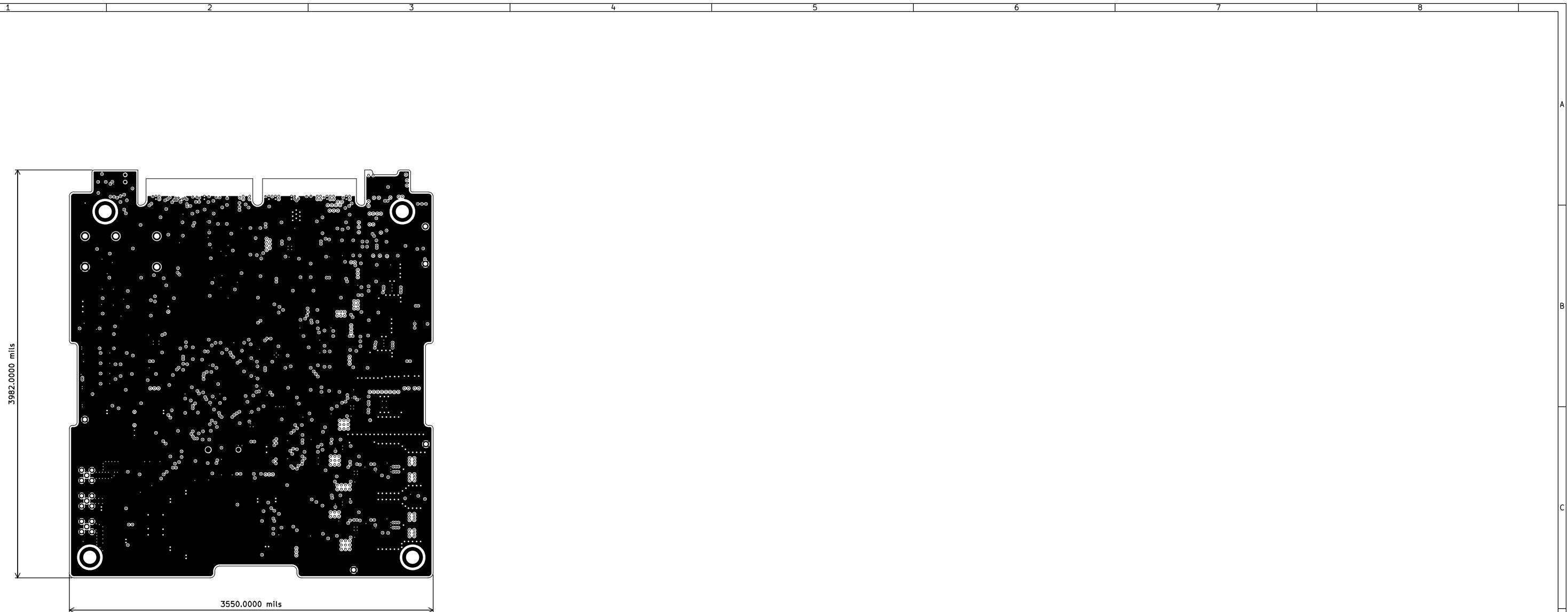
KiCad E.D.A. kicad 7.0.1

SHEET 1 OF 1



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TITLE				
SIZE	DWG NO.	REV		
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DRAWN BY	CH	ENGINEER	CH	2023-06-21
FILE NAME	mainboard.kicad_pcb	KiCad E.D.A. kicad 7.0.1		SHEET 1 OF 1



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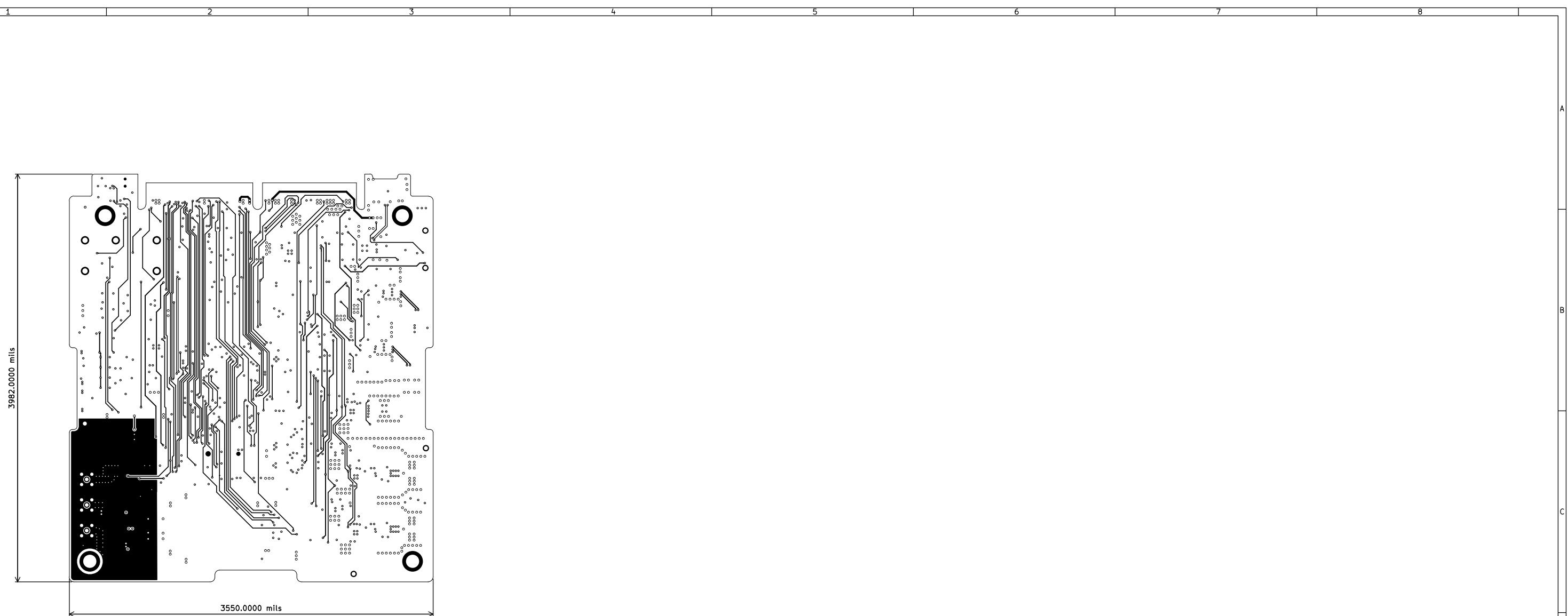
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mainboard

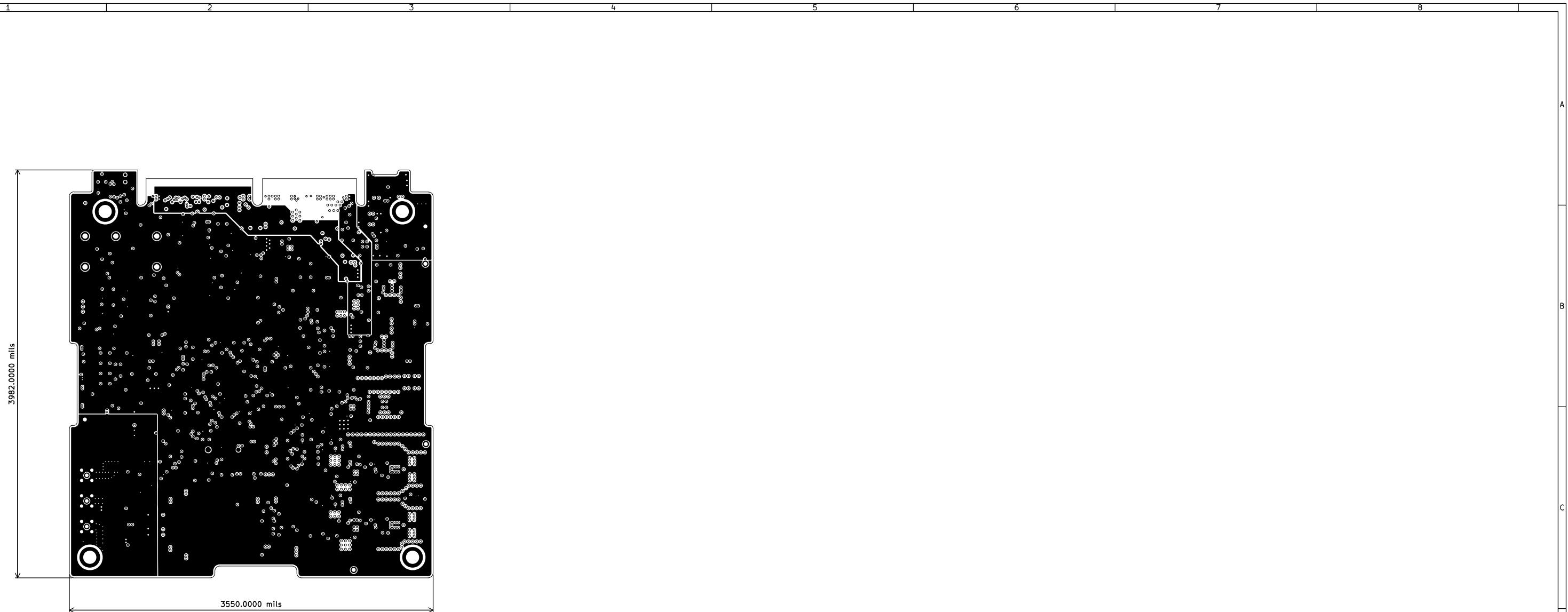
SIZE
B

DWG NO.
FILE NAME

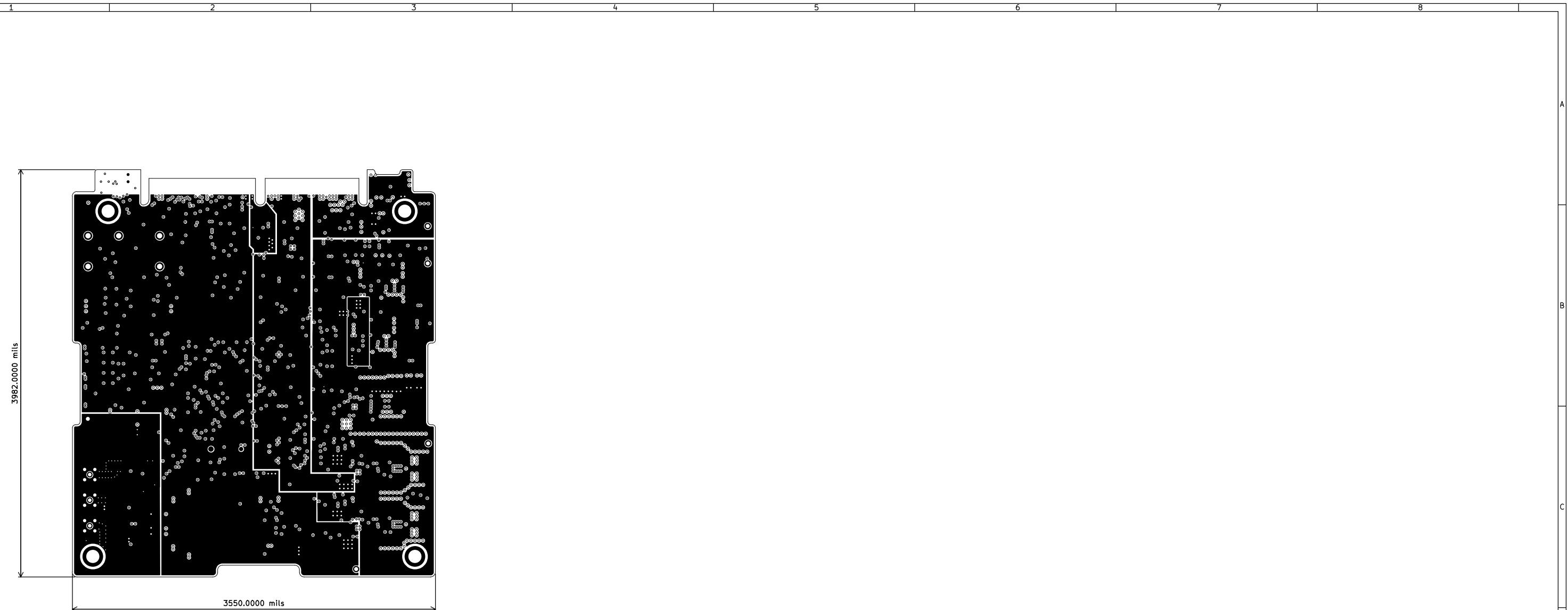
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2023-06-21
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SHEET 1 OF 1

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A						A	



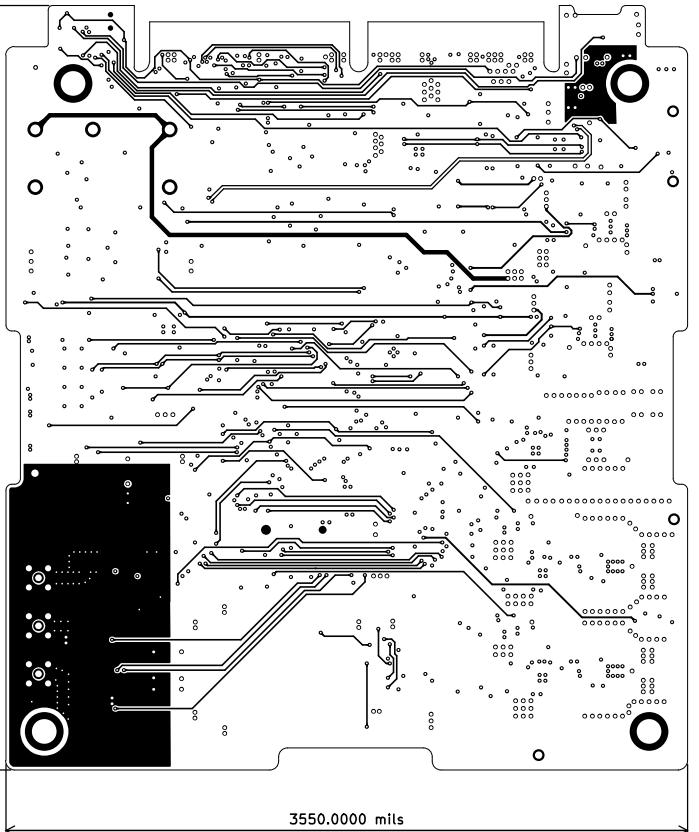
 SIERRA LOBO	TECHNOLOGY DEVELOPMENT & ENGINEERING CENTER EAST 11401 HOOVER ROAD, MILAN, OHIO 44846			
TITLE	mainboard			
SIZE	DWG NO.		REV	
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1982.0000 mils



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TITLE

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REV C

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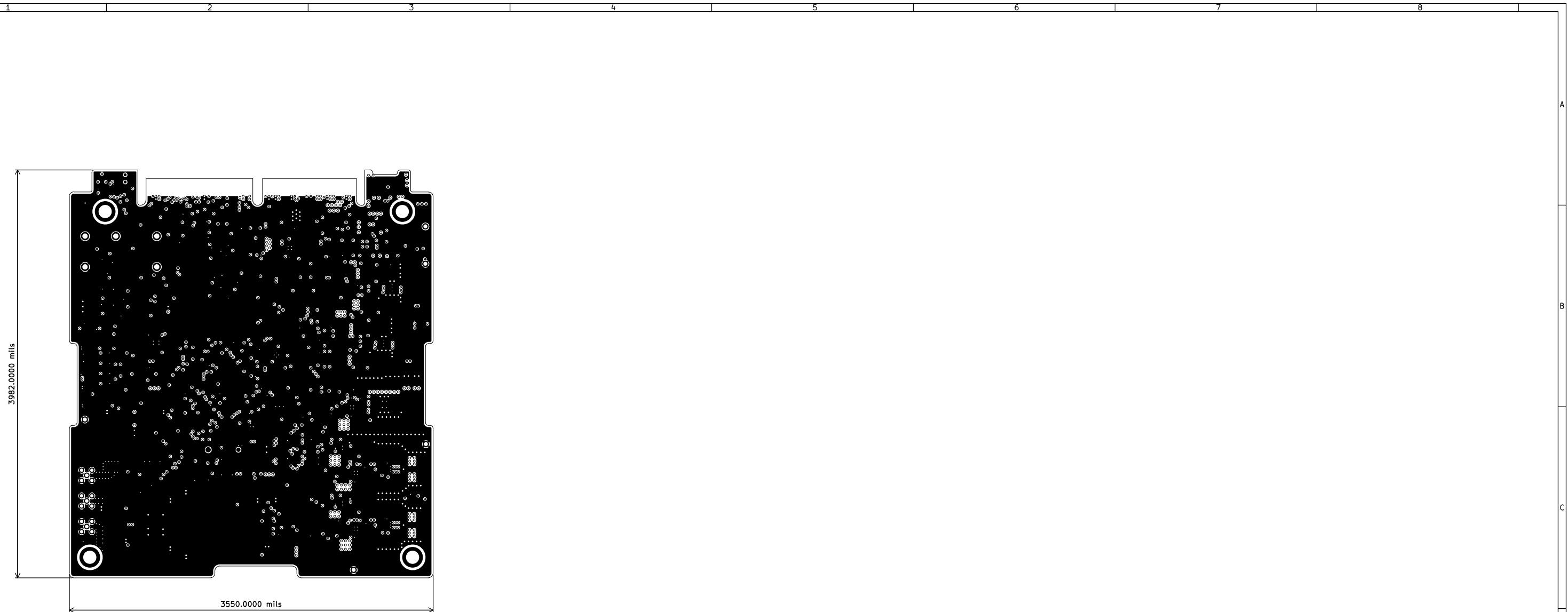
2023-06-21

FILE NAME

mainboard.kicad_pcb

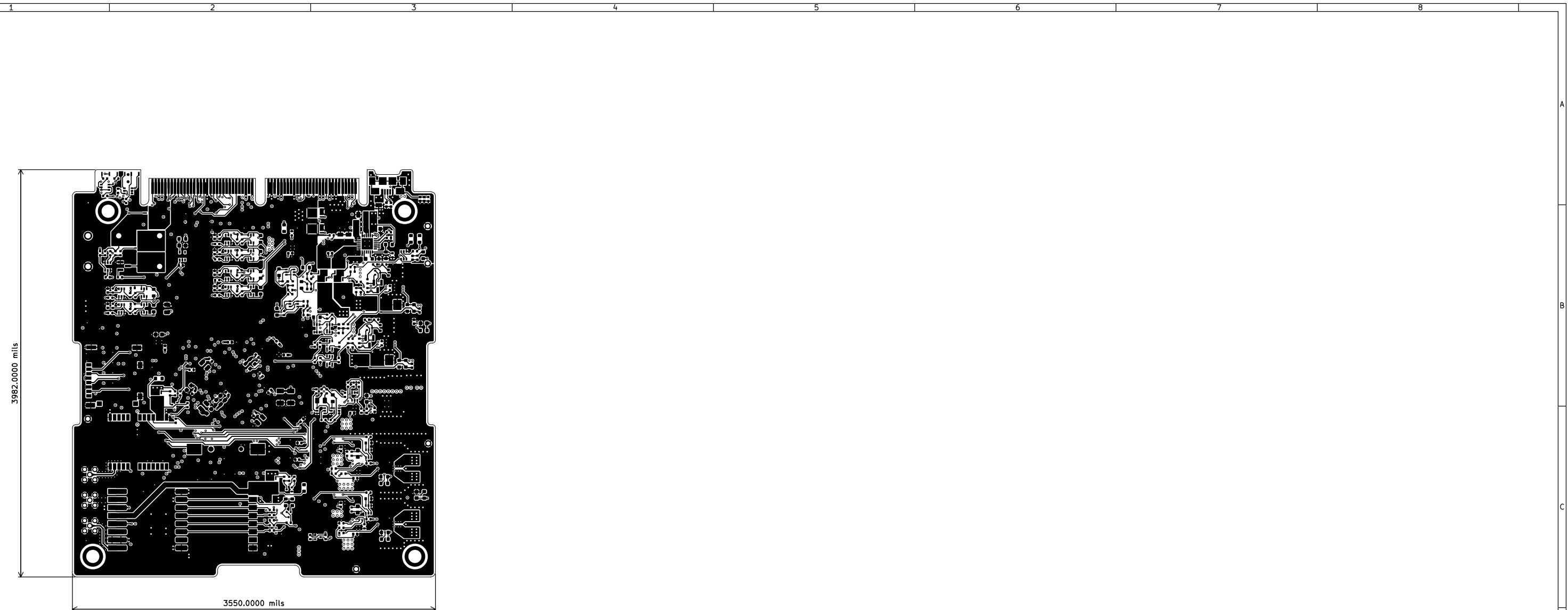
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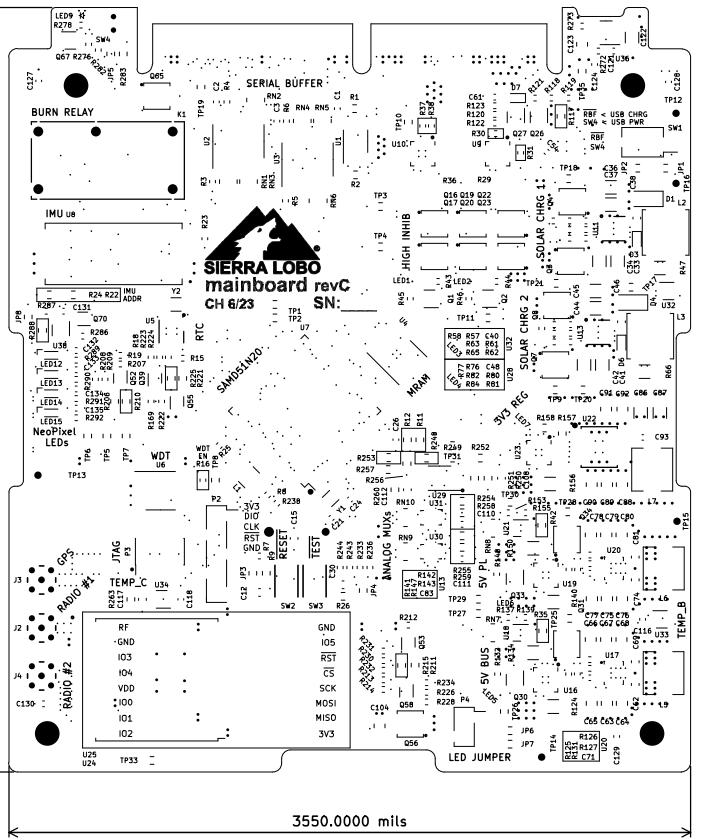
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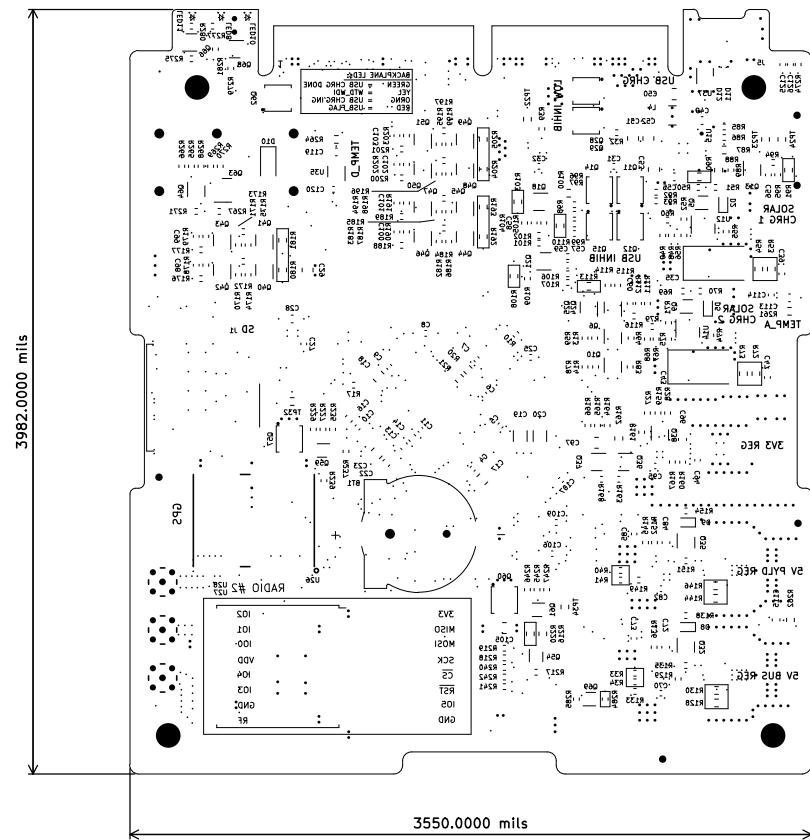
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A							A
B							B
C							C
D							D
E							E
1	2	3	4	5	6	7	8

1982.0000 mils

3550.0000 mils



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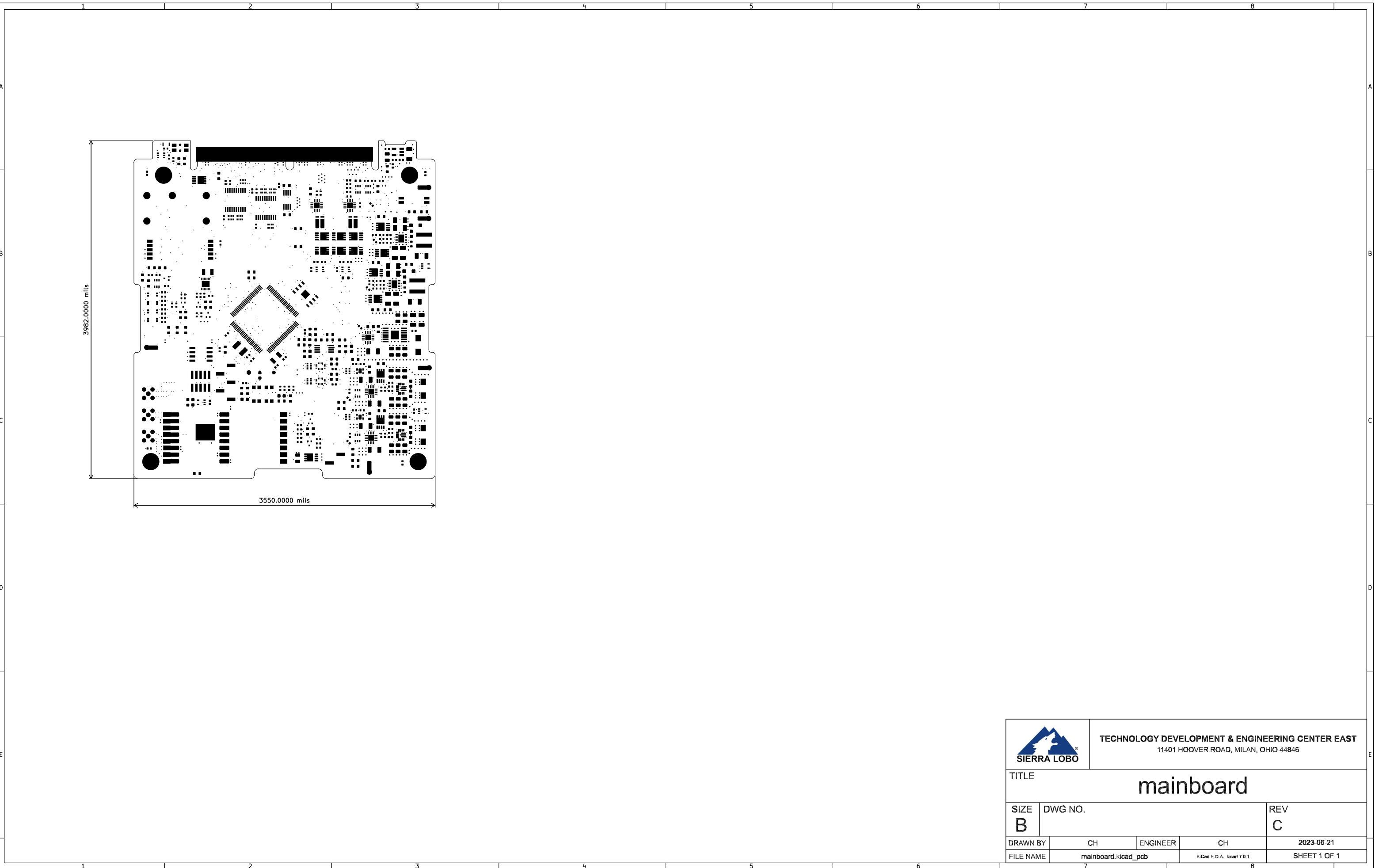
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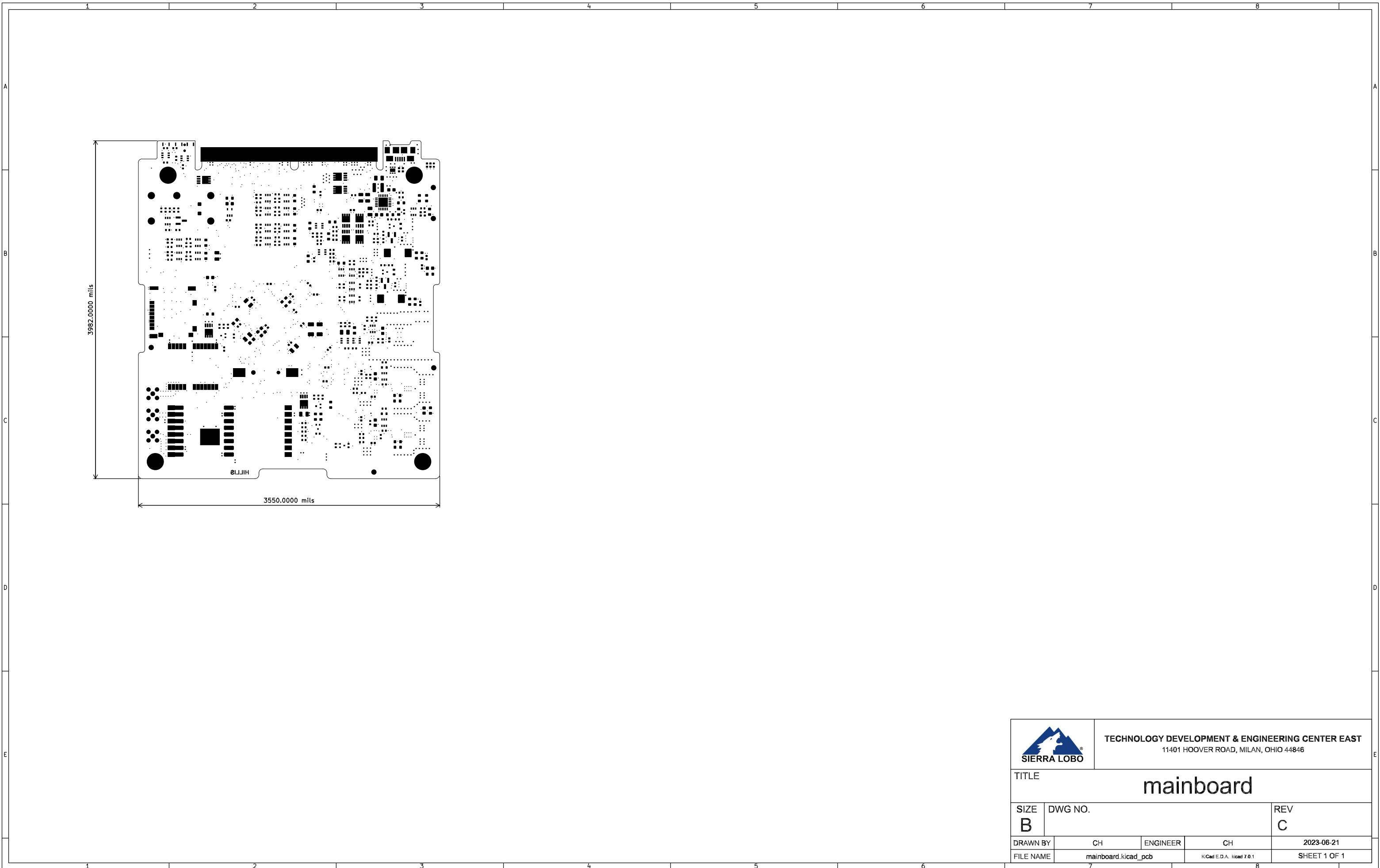
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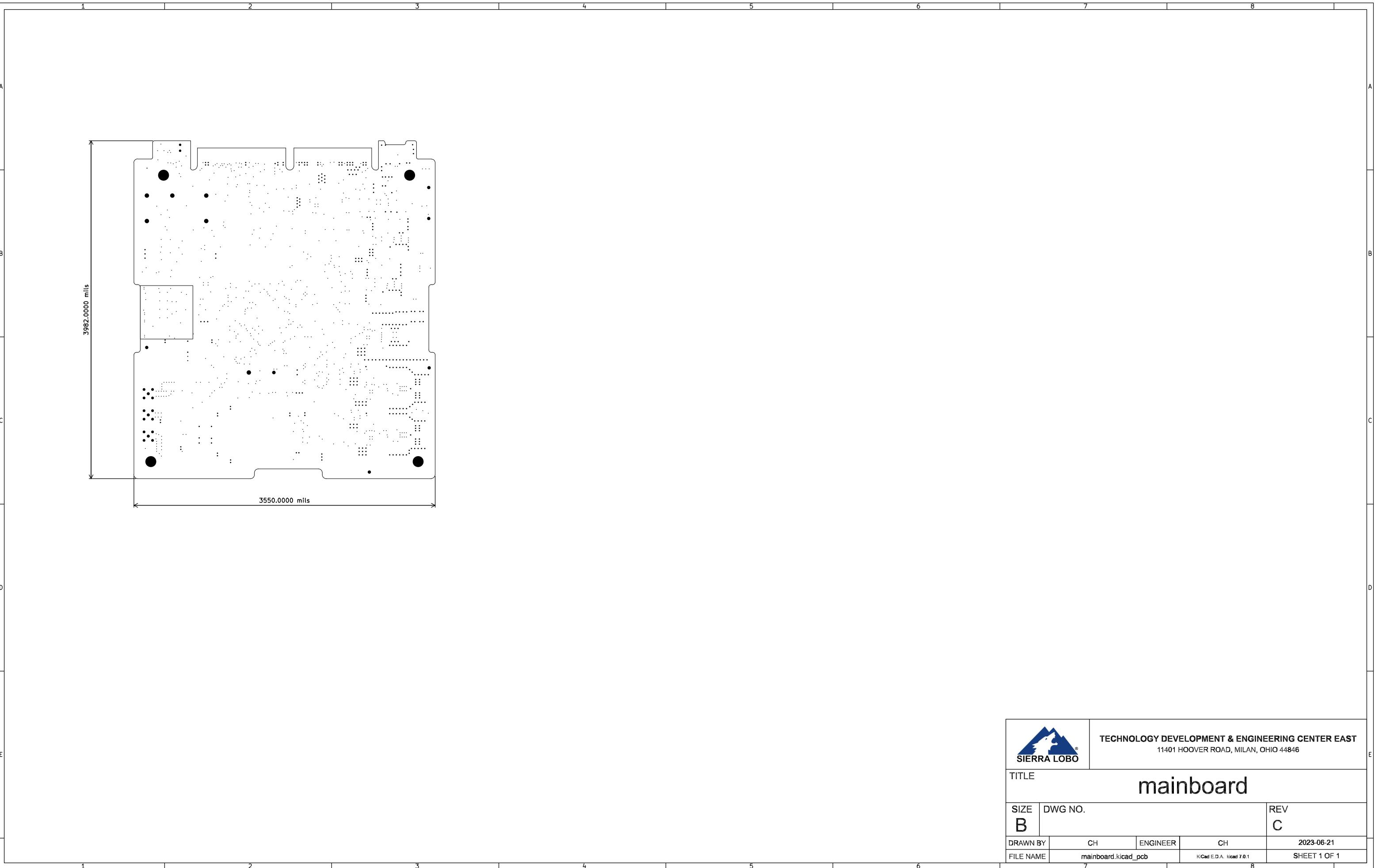
2023-06-21

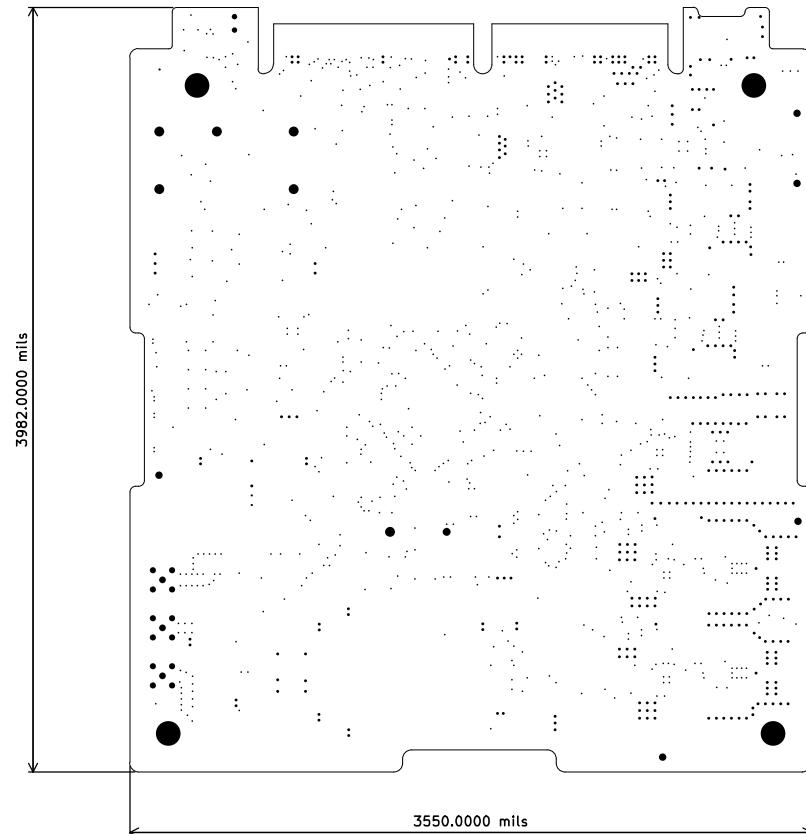
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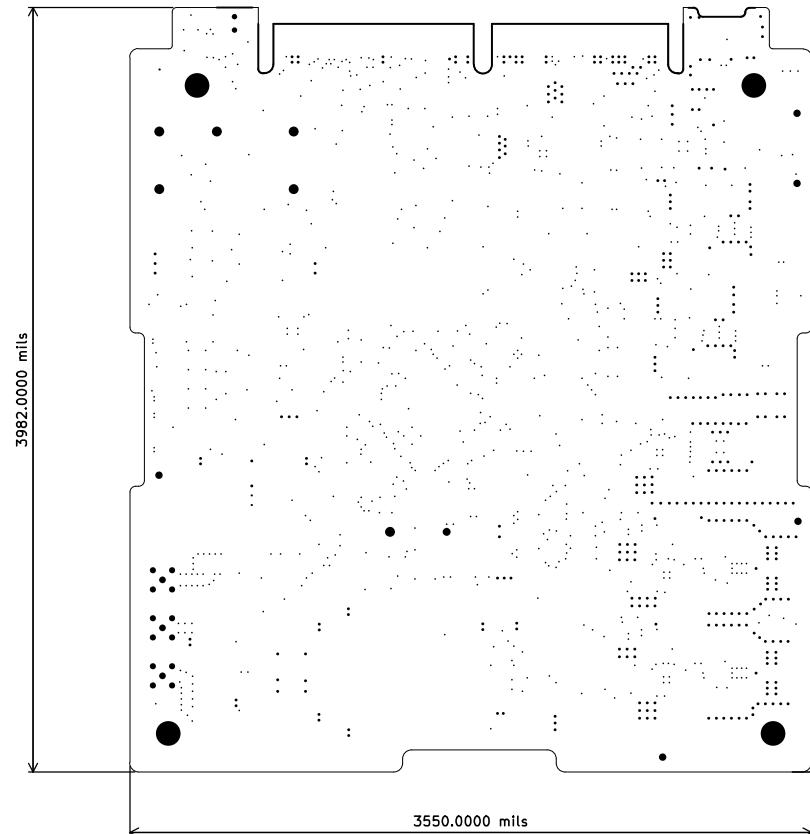
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A							A
B							B
C							C
D							D
E							E
1	2	3	4	5	6	7	8

1982.0000 mils

3550.0000 mils



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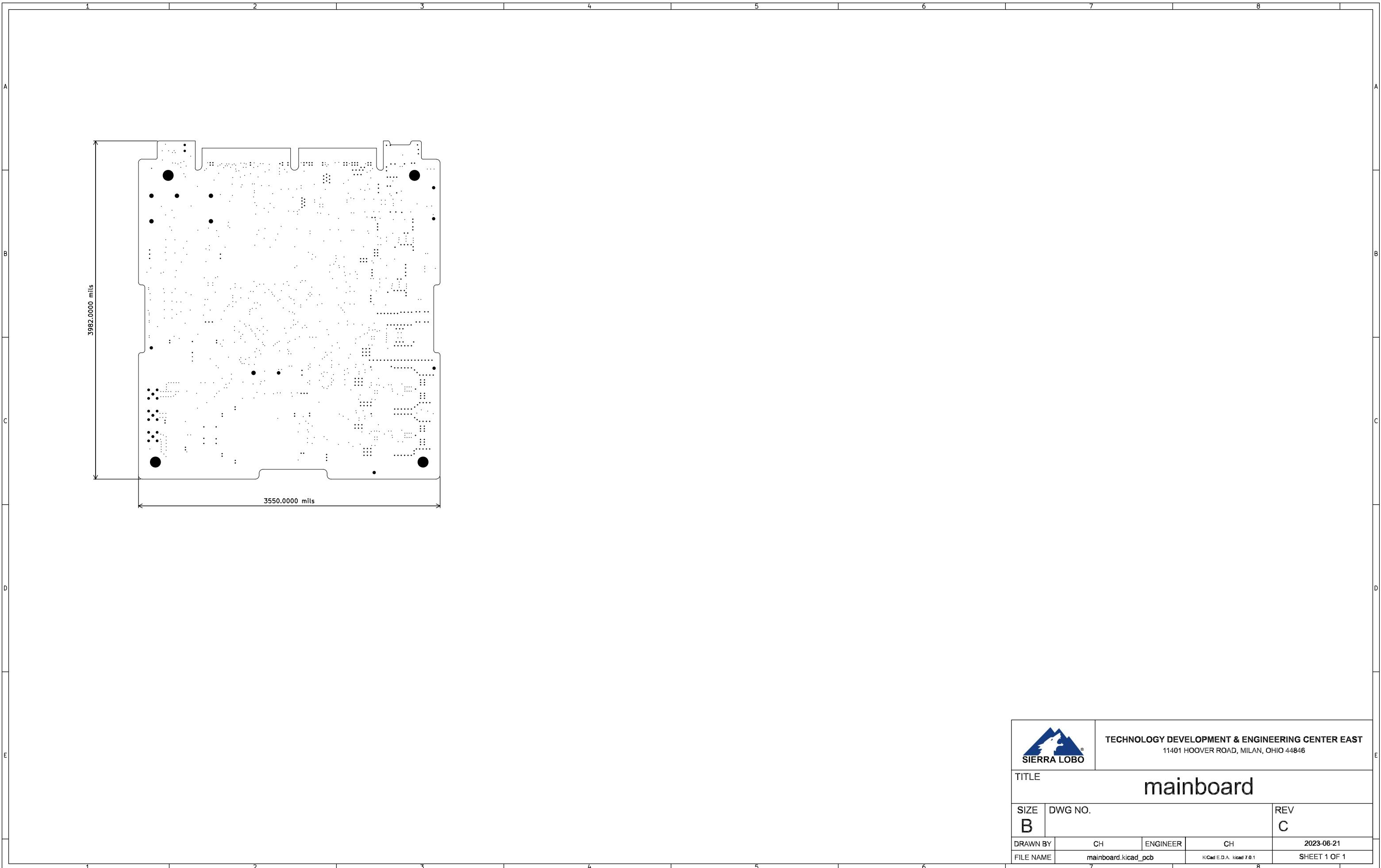
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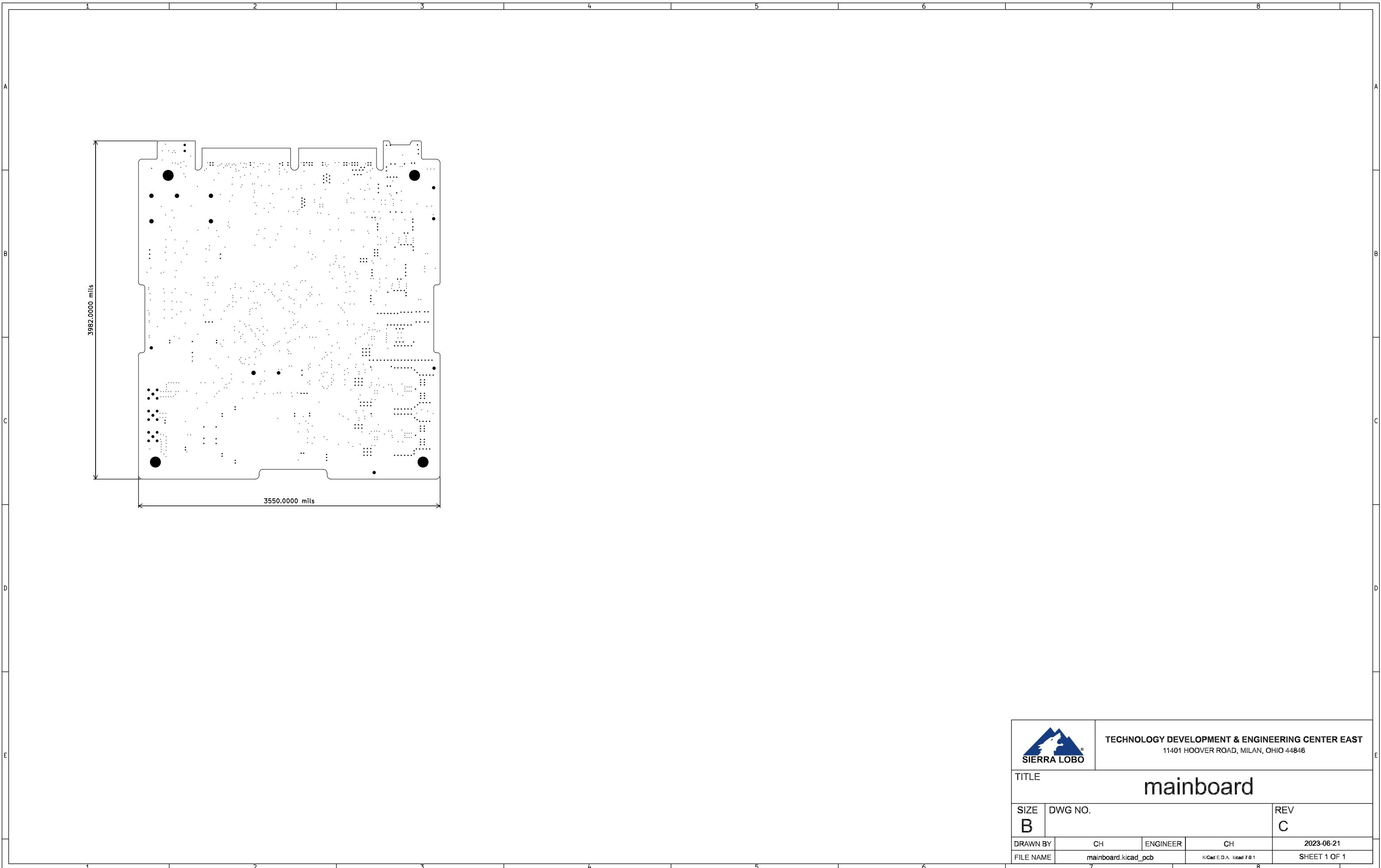
TITLE

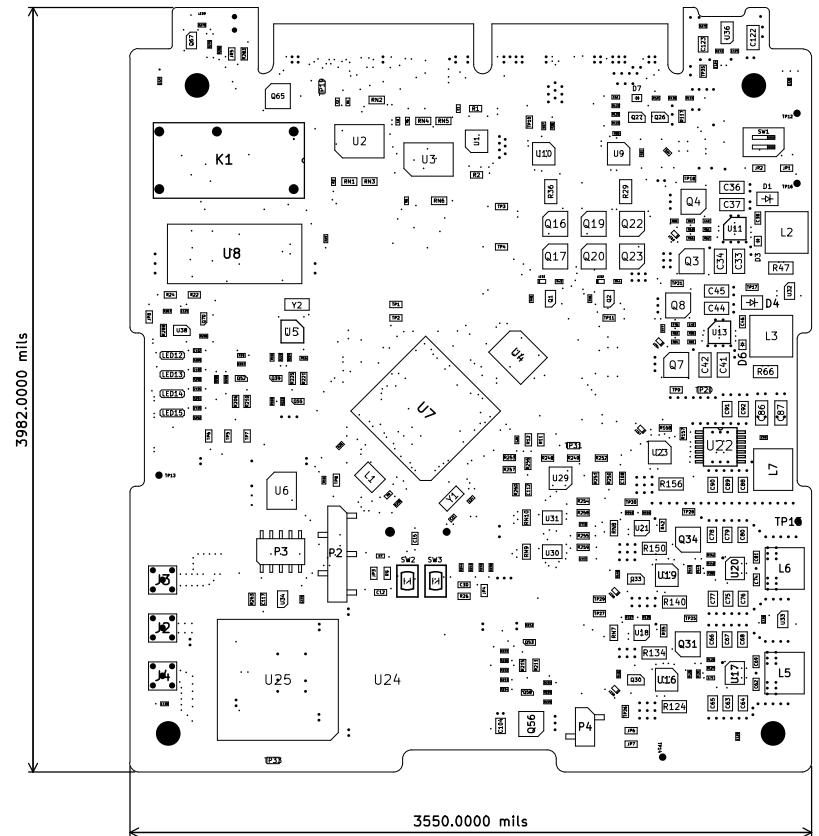
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VENDOR ASSEMBLY NOTES:

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C							C
D							D
E							E
1	2	3	4	5	6	7	8

