

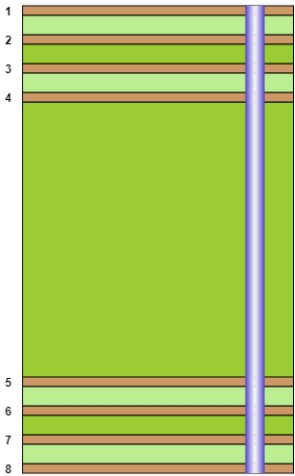
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Stack Report (STKNONBGA843)

Customer Input

Project Name / Rev	mianboard/C
PCB Size	3.55 inches X 3.98 inches
Board Type	Rigid
Material	N7000-2HT
Finished Thickness	0.062 inches
Layer Count	8
STD / HDI	STD
1 Oz Stackup	<input type="checkbox"/>
Layer Combination	4Signal 4Plane
Layer Sequence	SPSP-PSPS

8L_0-8-0_4S



Layer#	Material	Layer Type	Copper %		Finished Thickness (Mils)	Dielectric or Copper Base Thickness (Mils)	Copper Plating Thickness (Mils)	Dielectric Description (Mils)	Er (Dk @10 GHz)	Material Construction Details
	Solder Mask				0.5	0.5 mils		Soldermask 0.5 mils	4.2	
1	Foil	Signal	24%		1.45	0.35 (0.25 oz)	1.1			
	Prepreg				3.648	3.9		N7000-2HT Prepreg 3.9 mils	3.41	1x1080-68%
2	Copper	Plane	64%		0.7	0.7 (0.50 oz)				
	Core				4	4		N7000-2HT Core 4 mils 0.50 oz / 0.50 oz	3.7	(1x106+1x1080)-56%
3	Copper	Signal	24%		0.7	0.7 (0.50 oz)				
	Prepreg				7.016	7.8		N7000-2HT Prepreg 7.8 mils	3.41	2x1080-68%
4	Copper	Plane	64%		0.7	0.7 (0.50 oz)				
	Core				28	28		N7000-2HT Core 28 mils 0.50 oz / 0.50 oz	4.17	(2x2116+3x7628) -42%
5	Copper	Plane	64%		0.7	0.7 (0.50 oz)				
	Prepreg				7.016	7.8		N7000-2HT Prepreg 7.8 mils	3.41	2x1080-68%
6	Copper	Signal	24%		0.7	0.7 (0.50 oz)				
	Core				4	4		N7000-2HT Core 4 mils 0.50 oz / 0.50 oz	3.7	(1x106+1x1080)-56%
7	Copper	Plane	64%		0.7	0.7 (0.50 oz)				
	Prepreg				3.648	3.9		N7000-2HT Prepreg 3.9 mils	3.41	1x1080-68%
8	Foil	Signal	24%		1.45	0.35 (0.25 oz)	1.1			
	Solder Mask				0.5	0.5 mils		Soldermask 0.5 mils	4.2	
Total					65.428					



Impedance Calculator

Sr. No.	Signal Layer	Target Impedance (ohm) (tol-10%)	Tx Line model	Ref 1	Ref 2	Trace Width (mils)	Trace Spacing (mils)	TPS = W + S (mils)	Coplanar Spacing (mils)	Calculated Impedance (Ω)	Calculated Impedance before Mask (Ω)	Propagation Delay (ps/inch)
1	1	50	Coplanar Coated Microstrip Single Ended	2		6.25			10	49.956	54.653	144.799
2	6	90	Stripline Differential Pair	5	7	5.55	8	13.55		89.94	0	159.723
3	1	90	Coplanar coated Microstrip Differential Pair	2		6.4	8	14.4	8	90.158	99.848	141.711

Technology Parameters and Cost Index

PCB TECHNOLOGY LEVELS	Level 1	Level 2	Level 3
Mechanical Via Diameter (in mils)	8	7	6
Mechanical Via Pad Diameter (in mils)	14	13	12
Trace Width Top Layer (in mils)	5	4	4
Trace Width Inner Layers (in mils)	4	3.5	3
Trace Width Bottom Layer (in mils)	5	4	4
Cost Index	2.27	2.8	3.6

Via Set Information

This Stackup supports the following Via Set

L1-L8

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