

1 2 3 4 5 6

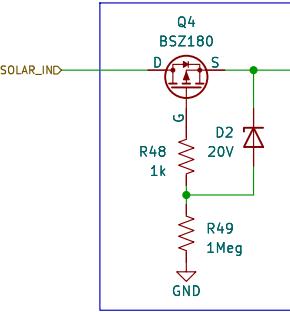
PARAMETERS

INPUT:
 Solar Panel: 9–24V 400mA (i.e. 7S Pumpkin Cell)
 Panel Temperature: Lm35 cathode ($10\text{mV}/\text{degK}$ absolute temperature sensor)

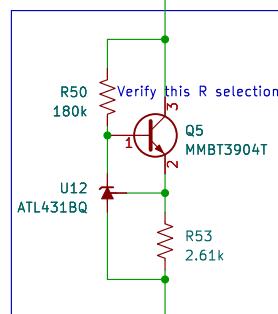
OUTPUT:
 8.4Vfloat, 0.8A (6.7W)

A

Input "Diode"
 Notice zener, V_{GS} may potentially exceed rating with margin applied.



LM35 Bias CC Source
 $\sim 450\mu\text{A}$ source provides constant Z_{IN} to temperature compensation
 10% margin on LM35 minimum current.

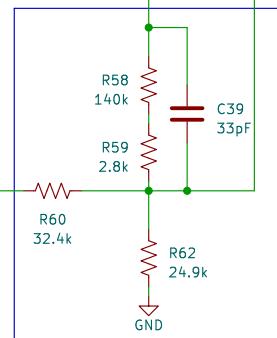


B

C

D

Input Voltage Regulation Programming



V_{IN_REG} : Input Voltage Regulation Reference.
 Maximum charge current is reduced when this pin is below 2.7V.

LT3652HV serves the maximum charge current required to maintain the programmed operational V_{IN} voltage, through maintaining the voltage on V_{IN_REG} at or above 2.7V.

$$\text{Goal: } V_{MP}(T) = V_{IN}(T)$$

$$V_{IN}(T) = [(2.7/R_{VIN_REG_2} - (V_{TLE}(T) - 2.7)R_{TLE})] * R_{VIN_REG_1}$$

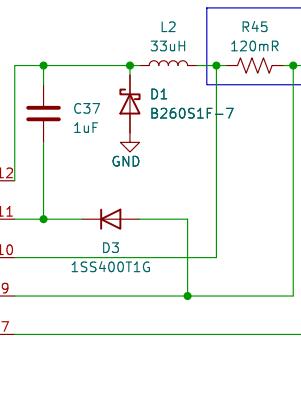
$$V_{MP} = m_{MP}(T) + b_{MP}$$

$$V_{TLE} = m_{TLE}(T) + b_{TLE}$$

$$\Rightarrow R_{VIN_REG_1} = (-m_{MP})/(m_{TLE})/(R_3)$$

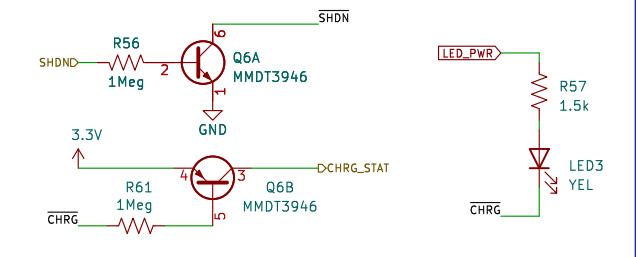
$$\Rightarrow R_{VIN_REG_2} = (R_1)(V_{REF})....$$

Charge Current Limit Programming
 Desired I_{CHRG} set to 800mA



Control Signals

SHDN turns off/on charger. Programmed V_{IN_MIN} takes precedence.
 $CHRG_STAT$ is high when charging.



Sheet: /Power/Solar Charger 1/
 File: solar_charger.kicad_sch

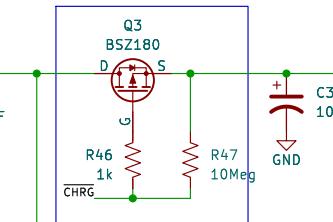
Title:

Size: A4 | Date:
 KiCad E.D.A. kicad 7.0.1

Rev:
 Id: 4/34

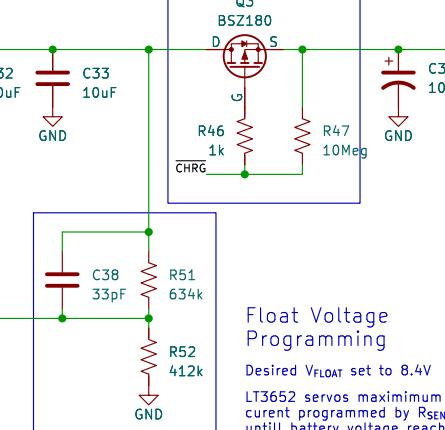
Output Switch

Prevents backflow when not charging ($CHRG$ low)
 Good idea when paralleling charging circuits...



Float Voltage Programming

Desired V_{FLOAT} set to 8.4V
 LT3652 serves maximum charge current programmed by R_{SEN} until battery voltage reaches V_{FLOAT}



3

4

5

6

1 2 3 4 5 6

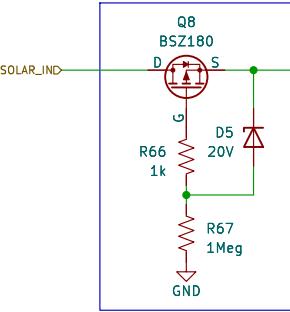
PARAMETERS

INPUT:
 Solar Panel: 9–24V 400mA (i.e. 7S Pumpkin Cell)
 Panel Temperature: Lm35 cathode ($10\text{mV}/\text{degK}$ absolute temperature sensor)

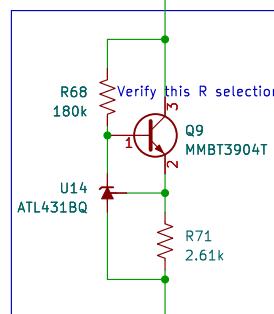
OUTPUT:
 8.4Vfloat, 0.8A (6.7W)

A

Input "Diode"
 Notice zener, V_{GS} may potentially exceed rating with margin applied.



LM35 Bias CC Source
 $\sim 450\mu\text{A}$ source provides constant Z_{IN} to temperature compensation
 10% margin on LM35 minimum current.



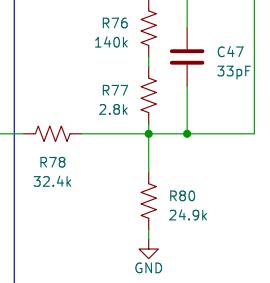
B

Input Voltage Regulation Programming

Temperature Sensor Input
 LM335 Temperature sensor on solar panels.
 $10\text{mV}/\text{degK}$ absolute sensitivity
 $400\mu\text{A}$ min current

ATL431 CC Source, set to $440\mu\text{A}$, 10% above LM335 functional minimum

SOLAR_TEMPD



V_{IN_REG} : Input Voltage Regulation Reference.
 Maximum charge current is reduced when this pin is below 2.7V.

LT3652HV serves the maximum charge current required to maintain the programmed operational V_{IN} voltage, through maintaining the voltage on V_{IN_REG} at or above 2.7V.

$$\text{Goal: } V_{MP}(T) = V_{IN}(T)$$

$$V_{IN}(T) = [(2.7/R_{VIN_REG_2} - (V_{TLE}(T) - 2.7)R_{TLE})] * R_{VIN_REG_1}$$

$$V_{MP} = m_{MP}(T) + b_{MP}$$

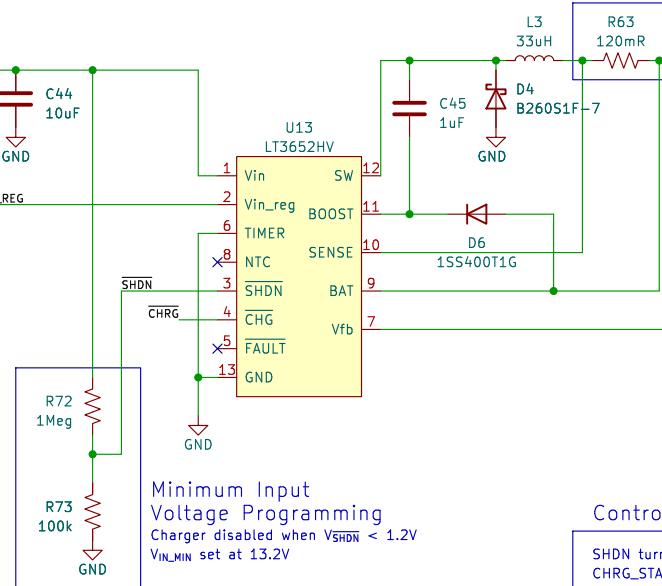
$$V_{TLE} = m_{TLE}(T) + b_{TLE}$$

$$\Rightarrow R_{VIN_REG_1} = (-m_{MP})/(m_{TLE})/(R_3)$$

$$\Rightarrow R_{VIN_REG_2} = (R_1)(V_{REF})....$$

C

Charge Current Limit Programming
 Desired I_{CHRG} set to 800mA

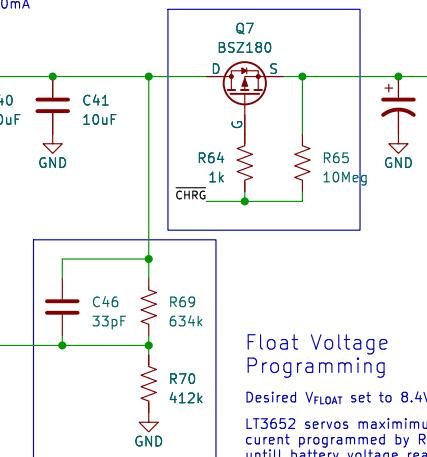


Minimum Input Voltage Programming
 Charger disabled when $V_{SHDN} < 1.2\text{V}$
 V_{IN_MIN} set at 13.2V

D

Output Switch

Prevents backflow when not charging ($CHRG$ low)
 Good idea when paralleling charging circuits...

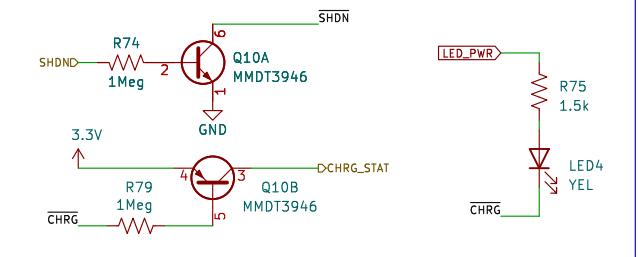


Float Voltage Programming

Desired V_{FLOAT} set to 8.4V
 LT3652 serves maximum charge current programmed by R_{SEN} until battery voltage reaches V_{FLOAT}

Control Signals

$SHDN$ turns off/on charger. Programmed V_{IN_MIN} takes precedence.
 $CHRG_STAT$ is high when charging.



Sheet: /Power/Solar Charger 2/
 File: solar_charger.kicad_sch

Title:

Size: A4 | Date:
 KiCad E.D.A. kicad 7.0.1

Rev:
 Id: 5/34

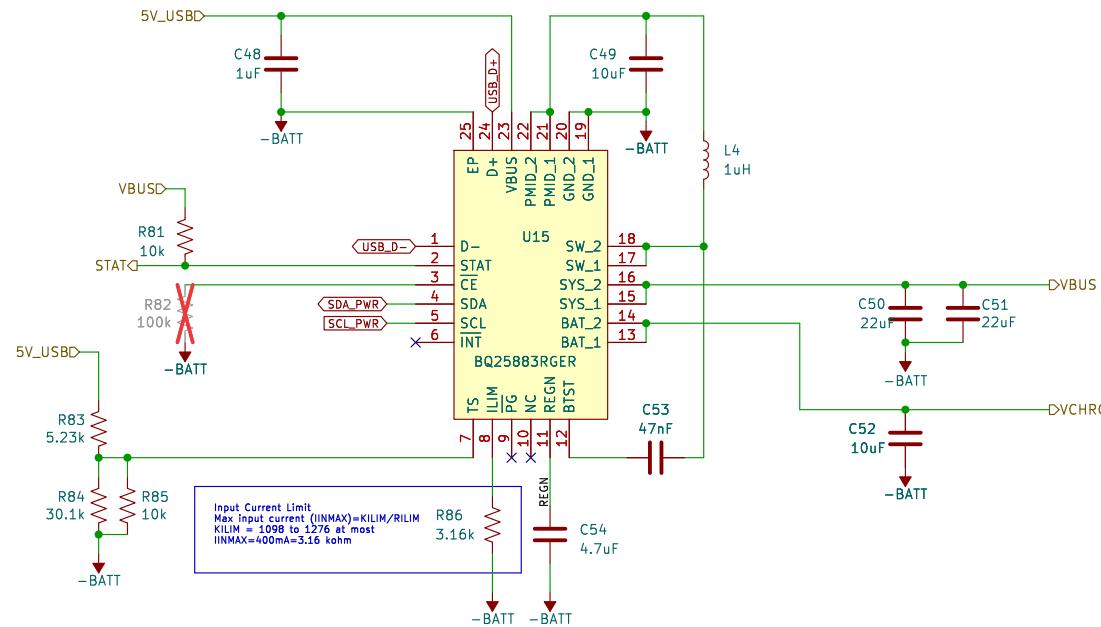
E

1 2 3 4 5 6

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USB (Boost) Charging for 2-cell Li-ion



Sheet: /Power/USB Charger/
File: usb_charger.kicad_sch

Title:

Size: A4 | Date:
KiCad E.D.A. kicad 7.0.1

Rev:
Id: 6/34

A

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B

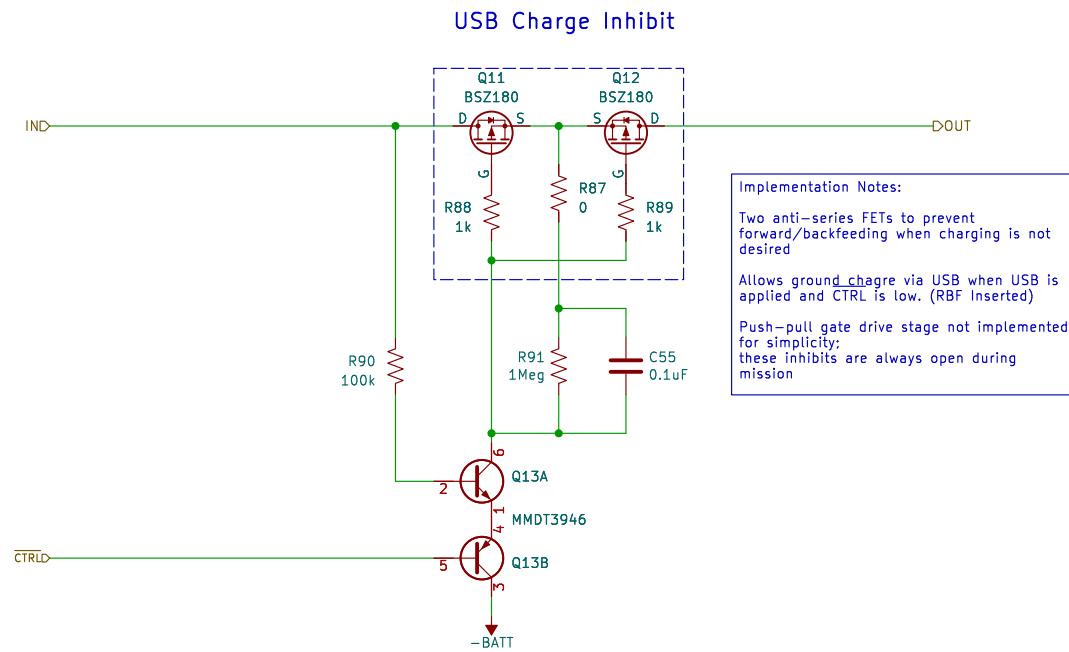
B

C

C

D

D



Sheet: /Power/USB Charge Inhibit/
File: usb_chrg_inhibit.kicad_sch

Title:

Size: A4 | Date:
KiCad E.D.A. kicad 7.0.1

Rev:
Id: 7/34

A

A

B

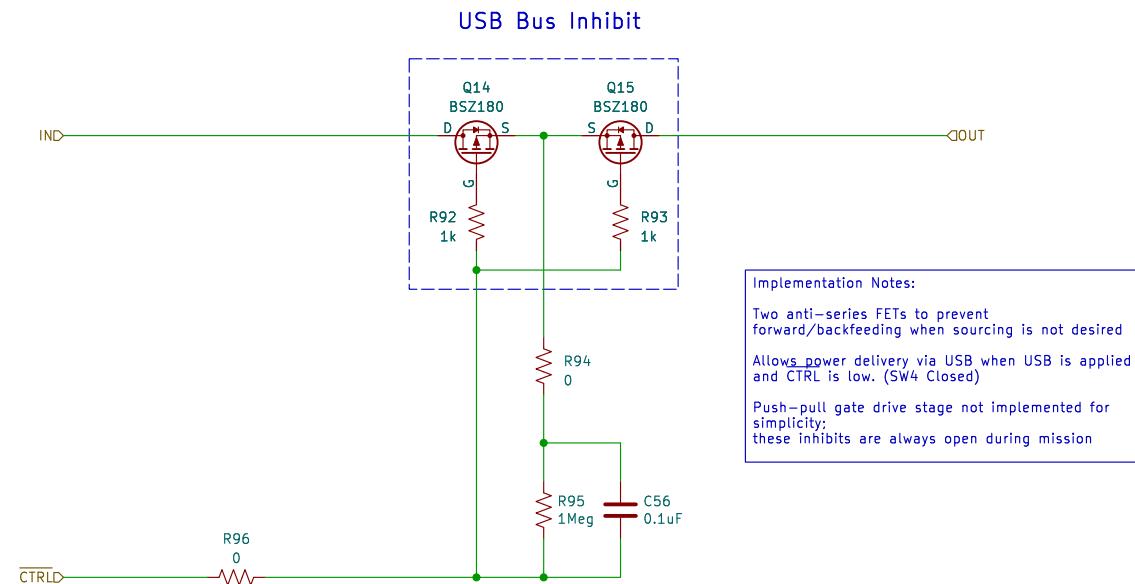
B

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D

D

**Implementation Notes:**

Two anti-series FETs to prevent forward/backfeeding when sourcing is not desired

Allows power delivery via USB when USB is applied and CTRL is low. (SW4 Closed)

Push-pull gate drive stage not implemented for simplicity; these inhibits are always open during mission

Sheet: /Power/USB Bus Inhibit/
File: usb_bus_inhibit.kicad_sch

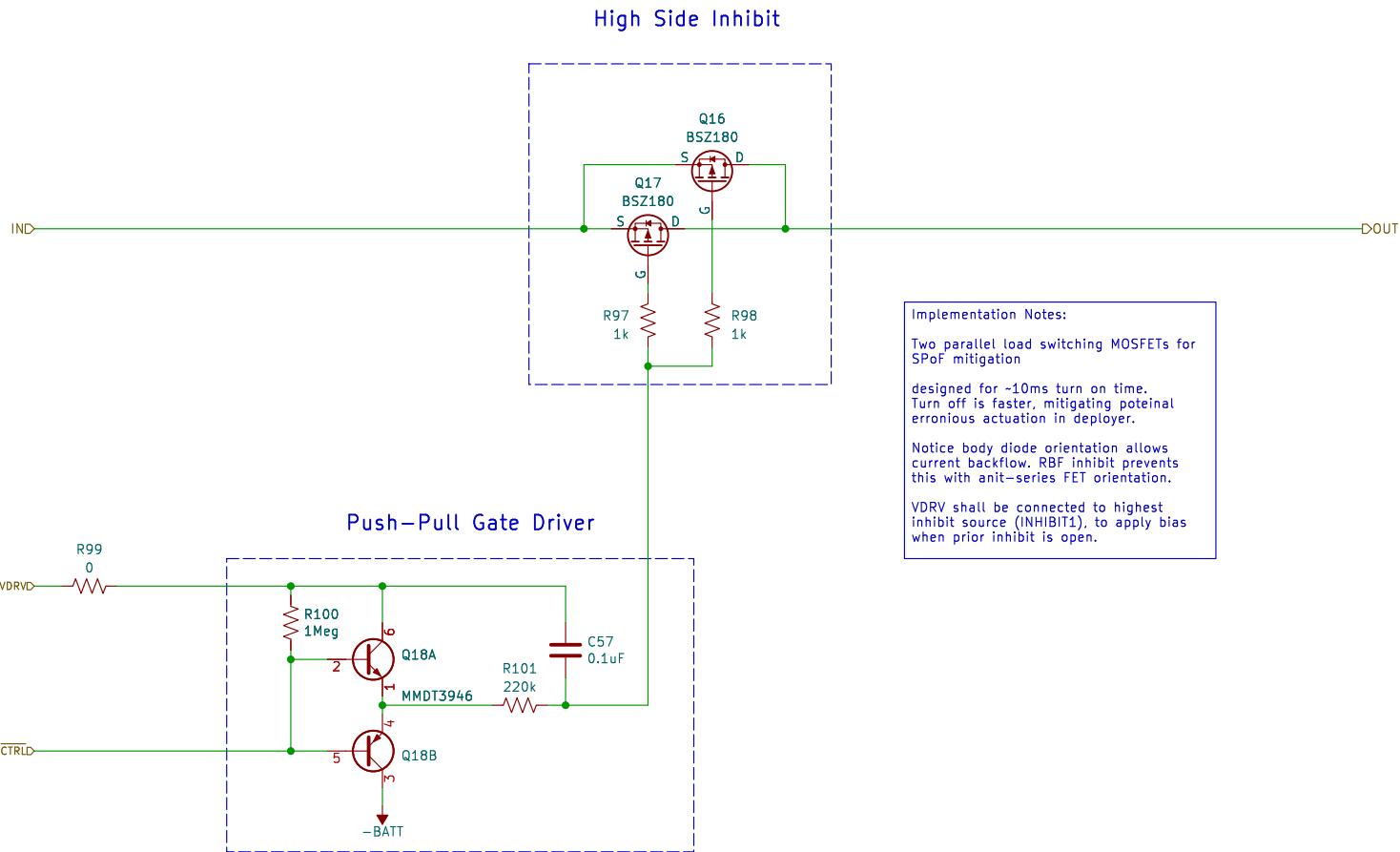
Title:

Size: A4 | Date:
KiCad E.D.A. kicad 7.0.1

Rev:
Id: 8/34

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A



Implementation Notes:
 Two parallel load switching MOSFETs for SPoF mitigation
 designed for ~10ms turn on time.
 Turn off is faster, mitigating potential erroneous actuation in deployer.
 Notice body diode orientation allows current backflow. RBF inhibit prevents this with anti-series FET orientation.
 VDRV shall be connected to highest inhibit source (INHIBIT1), to apply bias when prior inhibit is open.

Sheet: /Power/High Inhibit 1/
 File: high_inhib.kicad_sch

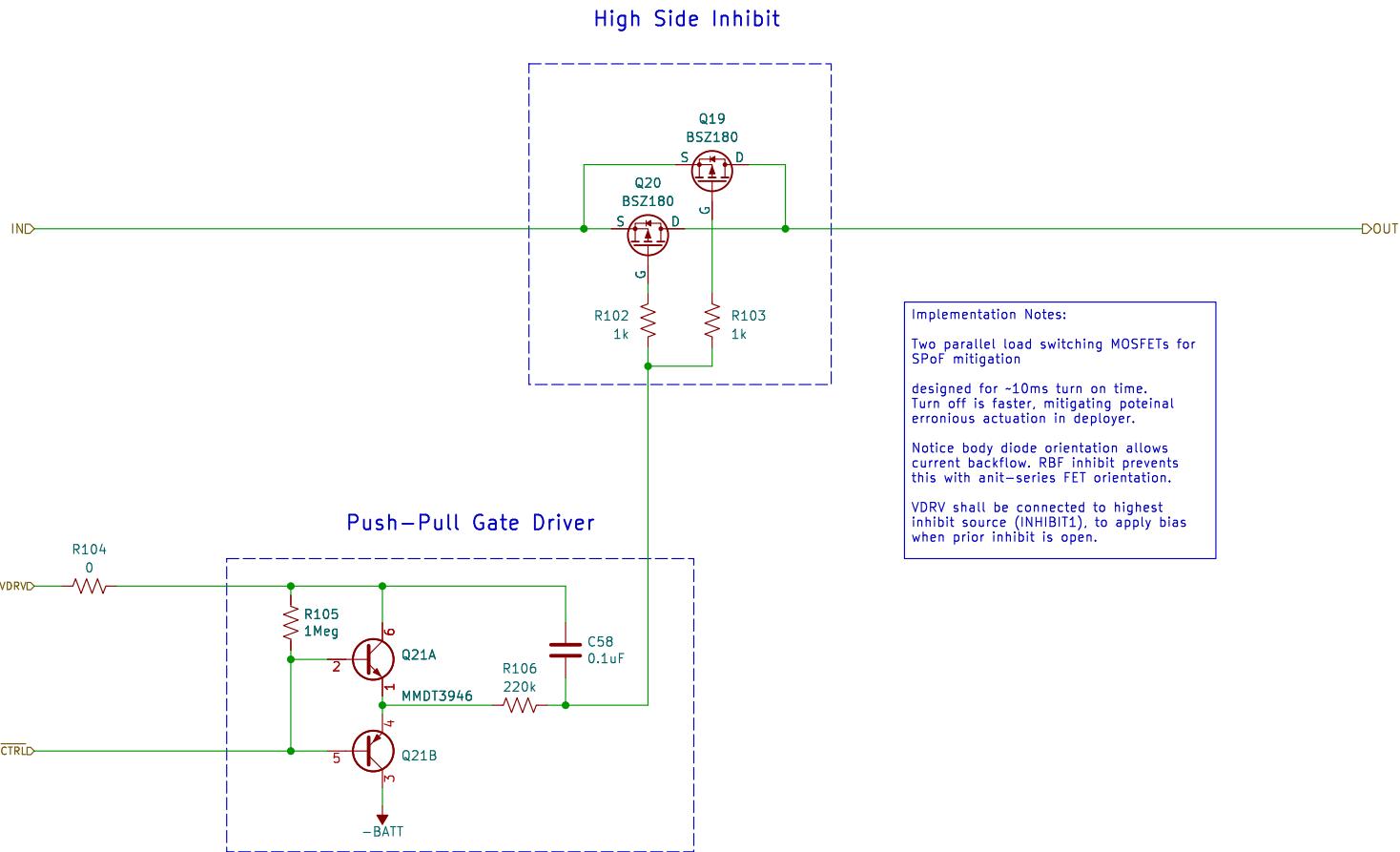
Title:

Size: A4 | Date:
 KiCad E.D.A. kicad 7.0.1

Rev:
 Id: 9/34

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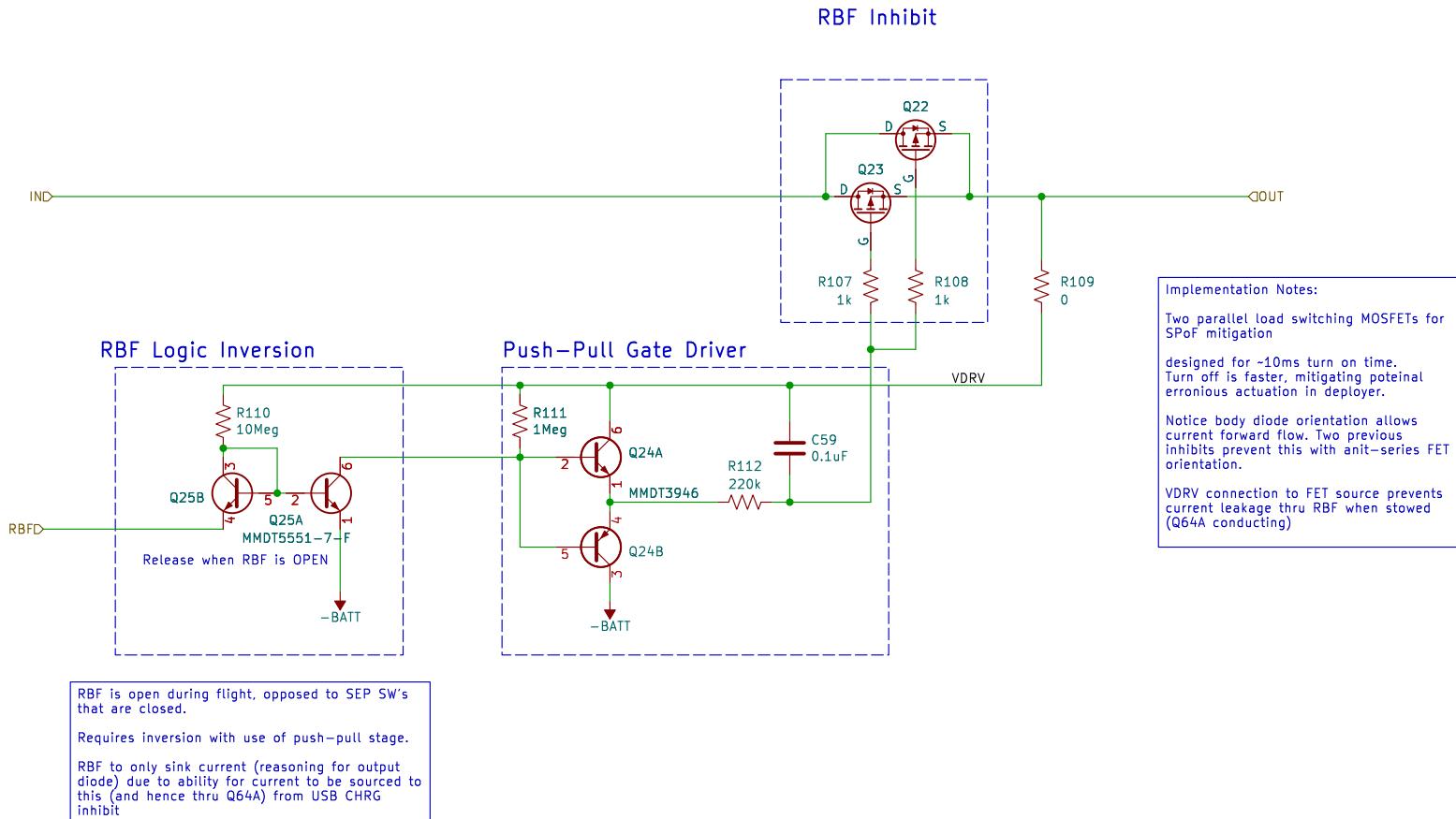
Implementation Notes:
 Two parallel load switching MOSFETs for SPoF mitigation
 designed for ~10ms turn on time.
 Turn off is faster, mitigating potential erroneous actuation in deployer.
 Notice body diode orientation allows current backflow. RBF inhibit prevents this with anit-series FET orientation.
 VDRV shall be connected to highest inhibit source (INHIBIT1), to apply bias when prior inhibit is open.

Sheet: /Power/High Inhibit 2/
 File: high_inhib.kicad_sch

Title:

Size: A4 | Date:
 KiCad E.D.A. kicad 7.0.1

Rev:
 Id: 10/34



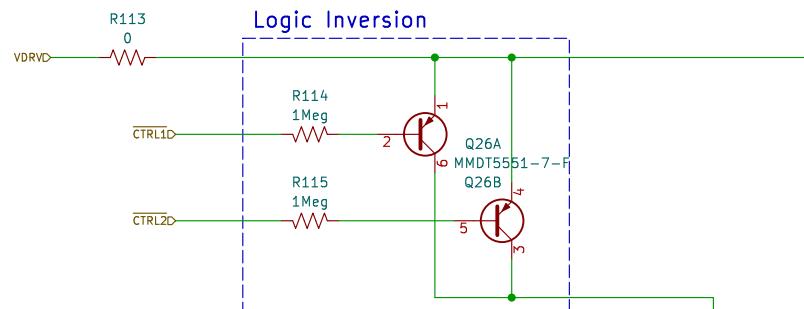
Sheet: /Power/RBF Inhibit/
File: rbf_inhib.kicad_sch

Title:

Size: A4 | Date:
KiCad E.D.A. kicad 7.0.1

Rev:
Id: 11/34

A

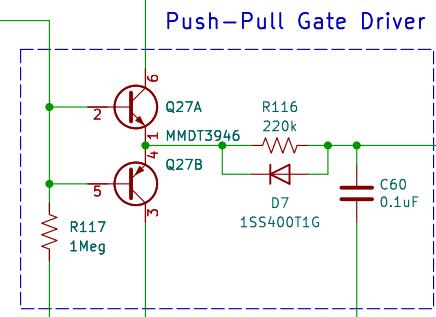
**Logic Inversion**

Implementation Notes:

Two parallel load switching MOSFETs for SPoF mitigation
designed for ~10ms turn on time.
Turn off is faster, mitigating potential erroneous actuation in deployer.
CTRL1 OR CTRL2 can turn this inhibit on,
CTRL2 shall be connected to SW4 "Debug SW" for easier debug, AI&T
VDRV shall be connected to VBUS (disables leakage when stowed).

B

SEP SW's are closed during flight, but low side inhibit is open when low.
Input to inverting push-pull stage requires inversion.

**Low Side Inhibit**

C

D

Sheet: /Power/Low_Inhibit/
File: low_inhibit.kicad_sch

Title:

Size: A4	Date:
KiCad E.D.A. kicad 7.0.1	Rev: Id: 12/34

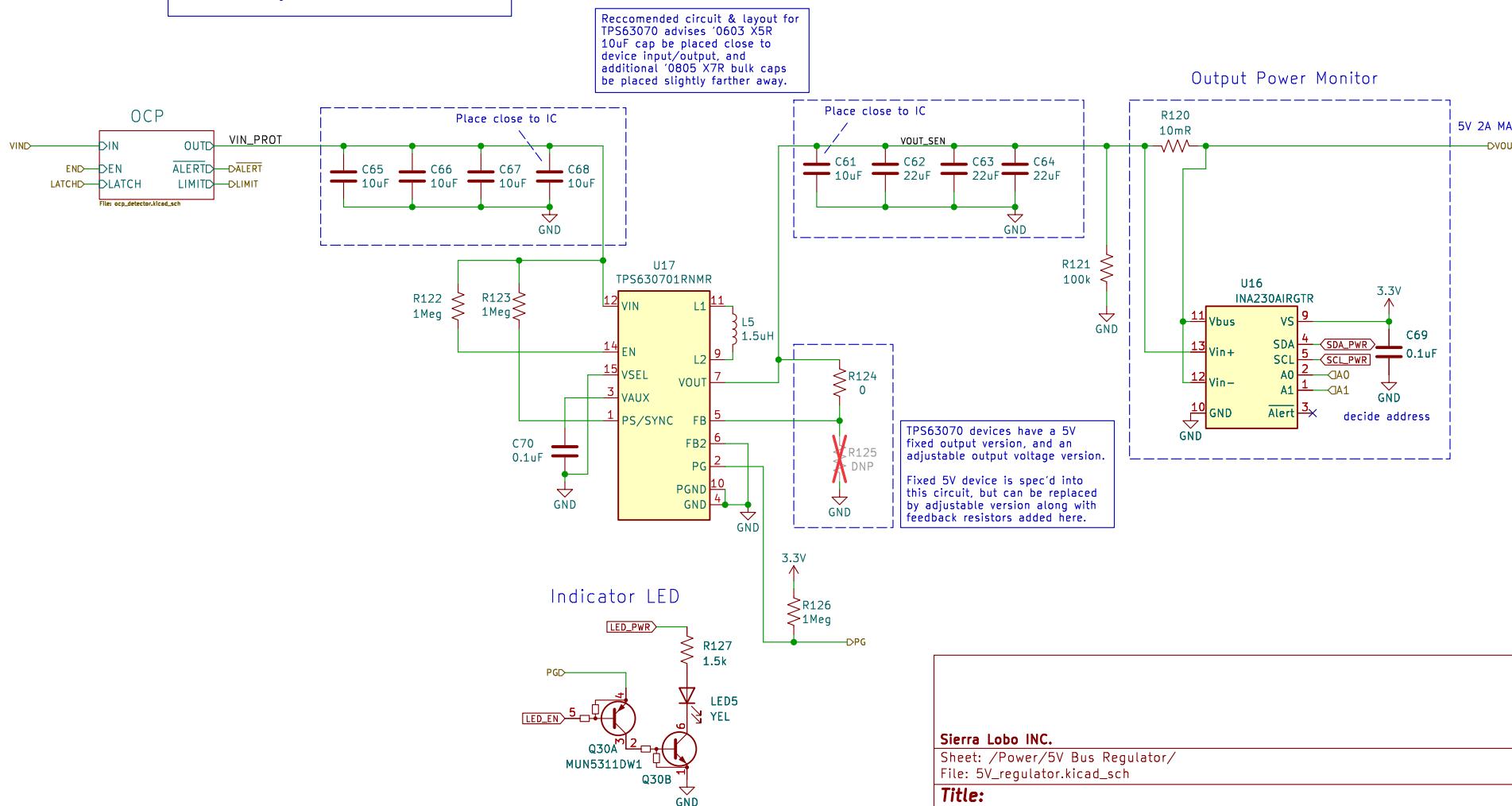
PARAMETERSINPUT:
VBUS 5–8.4VOUTPUT:
5V, 2A (max, 10W)**Implementation Notes:**

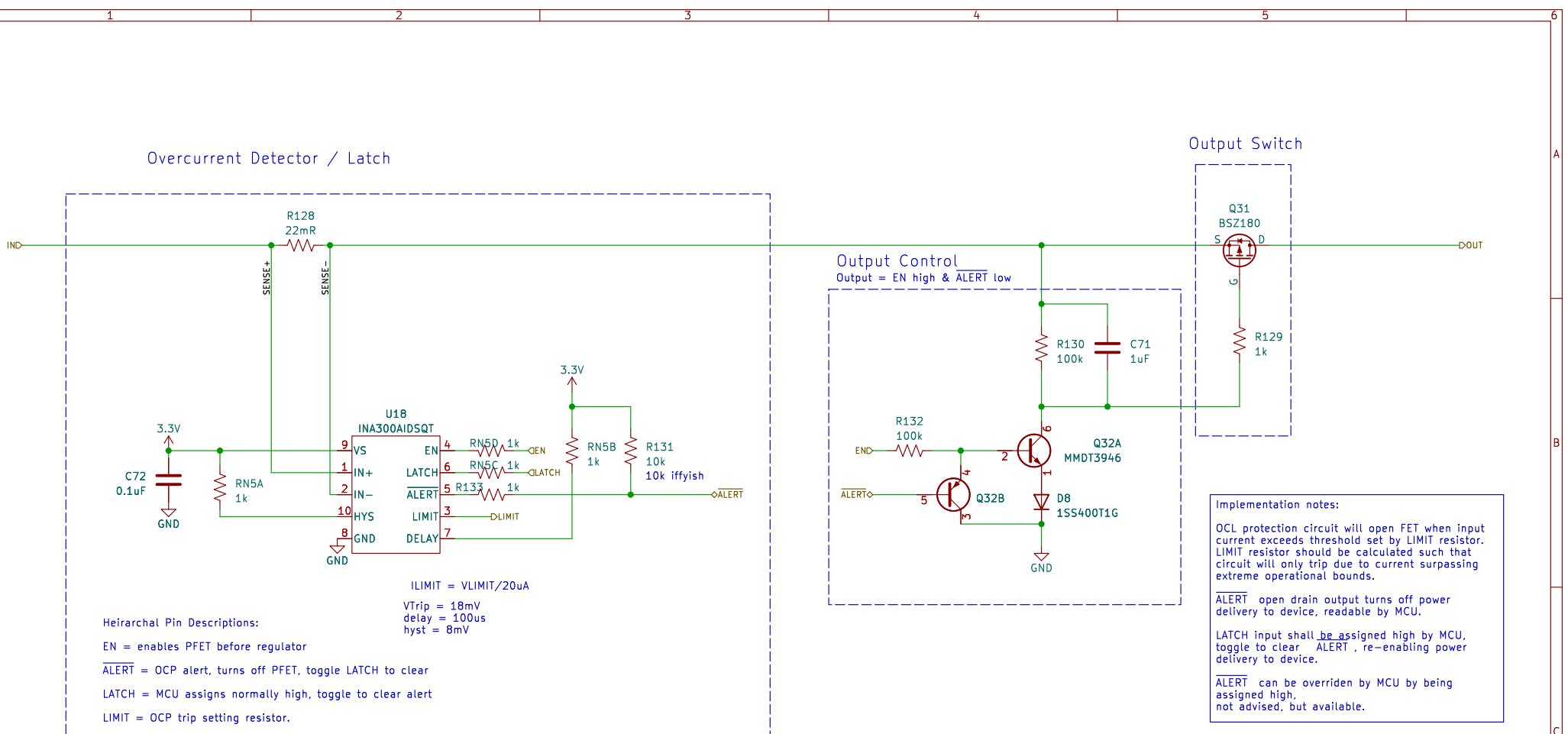
based from TI WebBench Design.

No heritage for TPS63070, failure of device has potential to cause catastrophic upstream fault.
 OCL protection circuit will disable power to device when input current exceeds threshold set by LIMIT resistor. LIMIT resistor shall be calculated such that OCL will only trip when current surpasses extreme operational bounds (i.e. 40% margin at 80% conversion efficiency).

Low input capacitance & device soft start will limit inrush when turned on, but current will still spike as device &/ downstream devices are used.

OCP circuit trips after 100μS of a sustained trip current additionally mitigating nuisance trips, but users should still be cognizant of such.

**Sierra Lobo INC.**Sheet: /Power/5V Bus Regulator/
File: 5V_regulator.kicad_sch**Title:**Size: A4 | Date:
KiCad E.D.A. kicad 7.0.1Rev:
Id: 13/34



Overcurrent Protection

Sheet: /Power/5V Bus Regulator/OCP/
File: ocp_detector.kicad_sch

Title:

Size: A4 | Date:
KiCad E.D.A. kicad 7.0.1

Rev:
Id: 14/34

PARAMETERS

INPUT:
VBUS 5–8.4VOUTPUT:
5V, 2A (max, 10W)

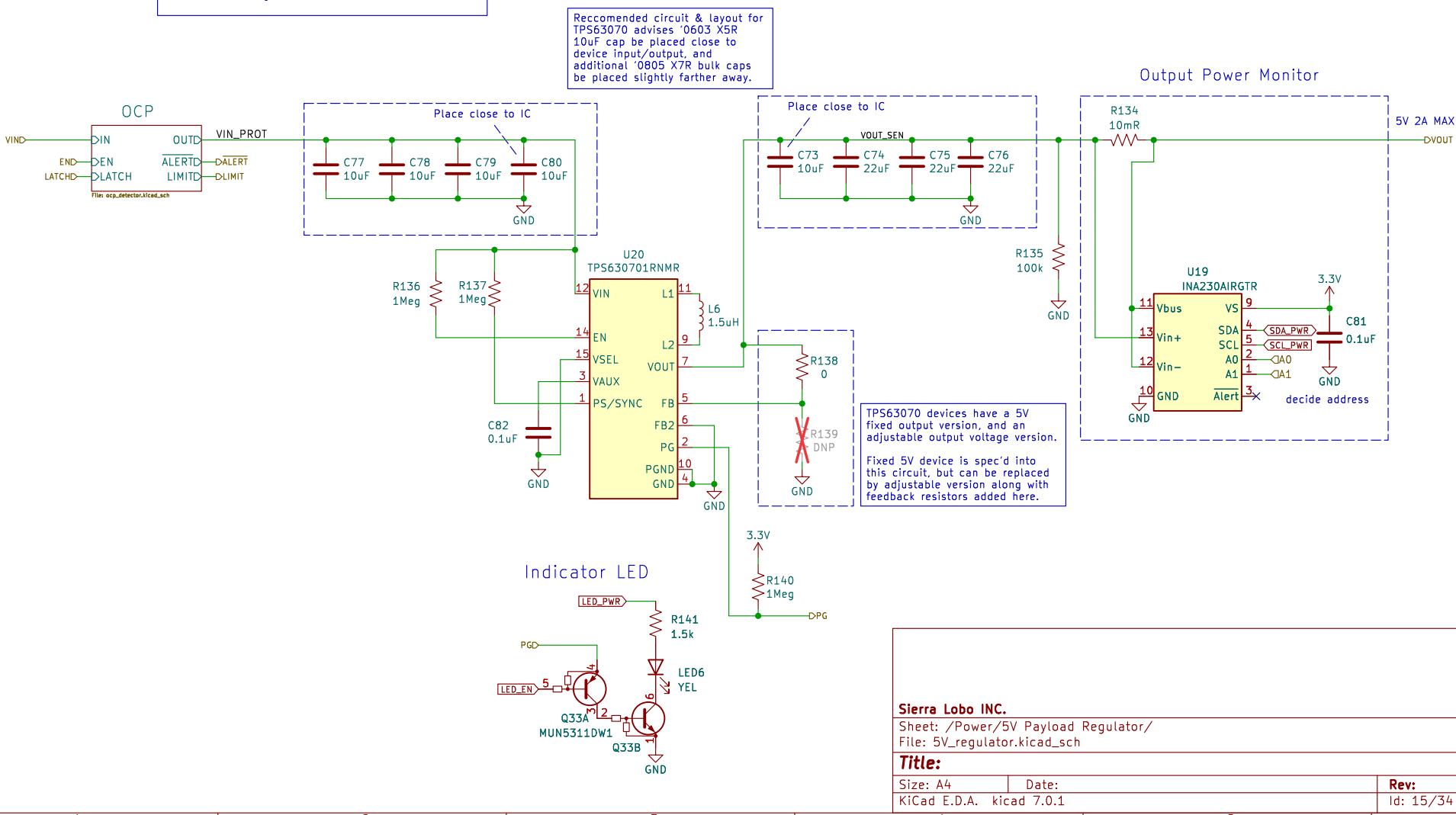
Implementation Notes:

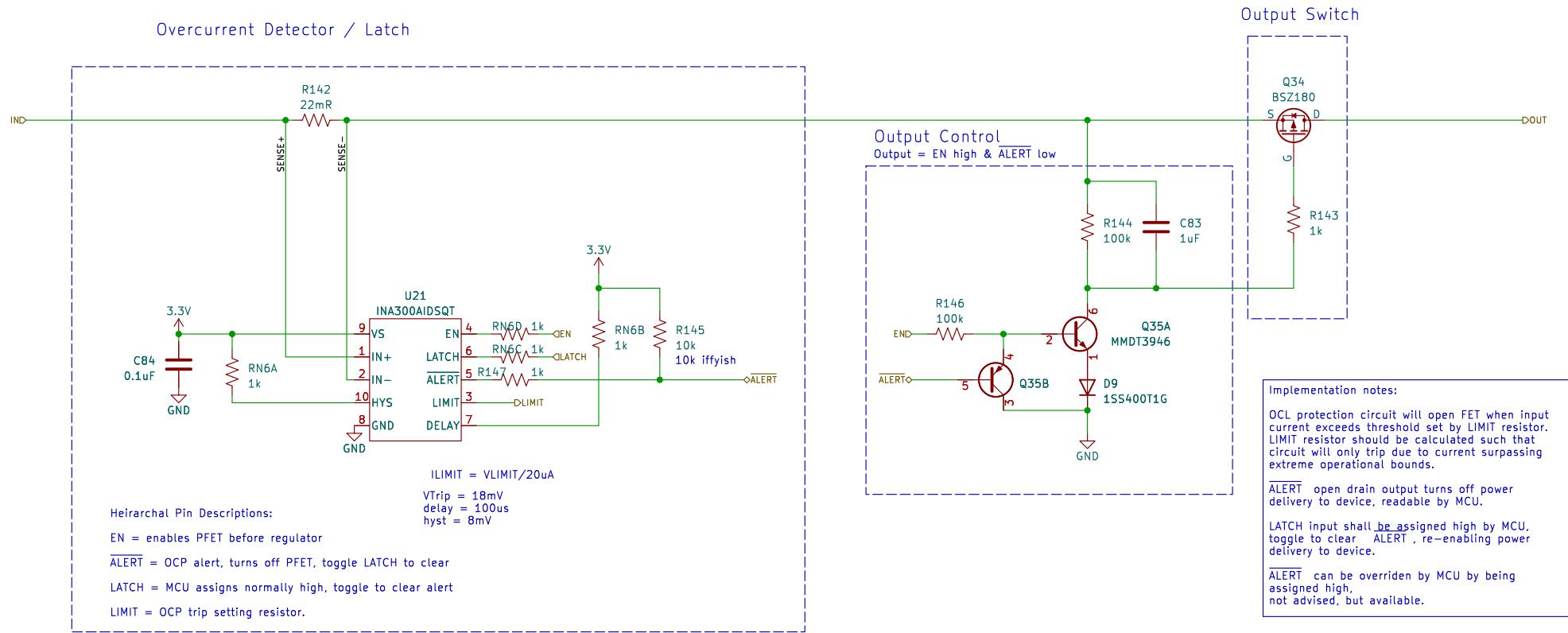
based from TI WebBench Design.

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 OCL protection circuit will disable power to device when input current exceeds threshold set by LIMIT resistor. LIMIT resistor shall be calculated such that OCL will only trip when current surpasses extreme operational bounds (i.e. 40% margin at 80% conversion efficiency).

Low input capacitance & device soft start will limit inrush when turned on, but current will still spike as device &/ downstream devices are used.

OCP circuit trips after 100μS of a sustained trip current additionally mitigating nuisance trips, but users should still be cognizant of such.





Overcurrent Protection

Sheet: /Power/5V Payload Regulator/OCP/
File: ocp_detector.kicad_sch

Title

Size: A4 Date:
KiCad E.D.A. kicad 7.0.1

Rev:
d: 16/34

1 2 3 4 5 6

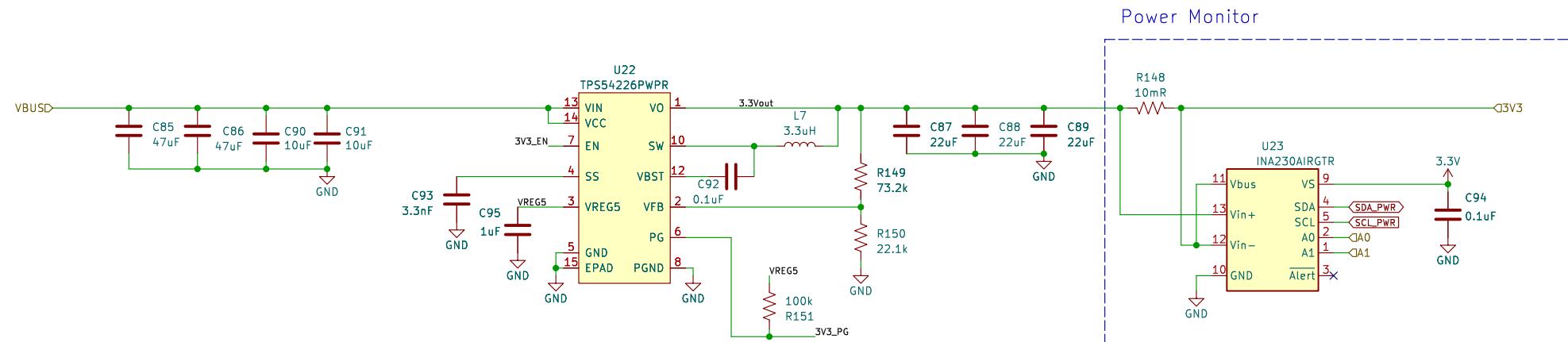
PARAMETERS

INPUT:
VBUS 4.5–18V

OUTPUT:
3.3V, ~1.5A (OCP)
~1.5A OCP (See datasheet p8 for more information.)

A

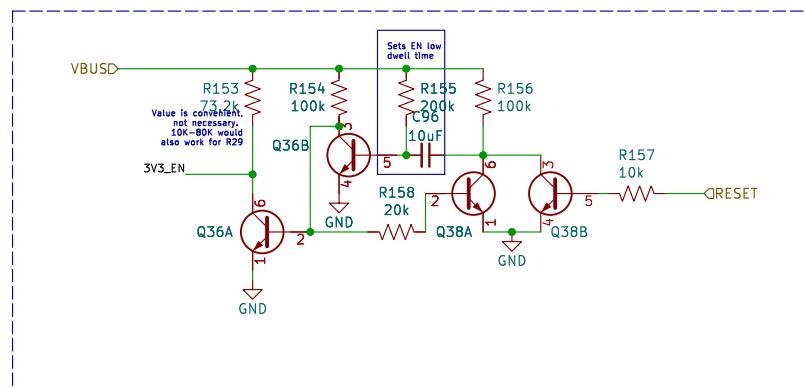
A



B

B

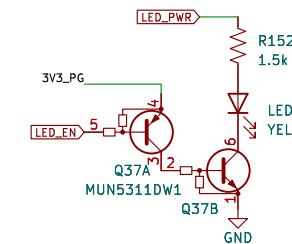
"One Shot" Regulator Reset



C

C

Indicator LED



Sheet: /Power/3.3V Regulator/
File: 3v3_reg.kicad_sch

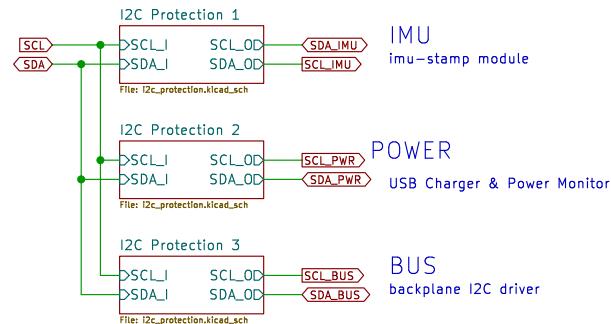
Title:

Size: A4 | Date:
KiCad E.D.A. kicad 7.0.1

Rev:
Id: 17/34

1 2 3 4 5 6

A

I2C Bus Protection

B

POWER

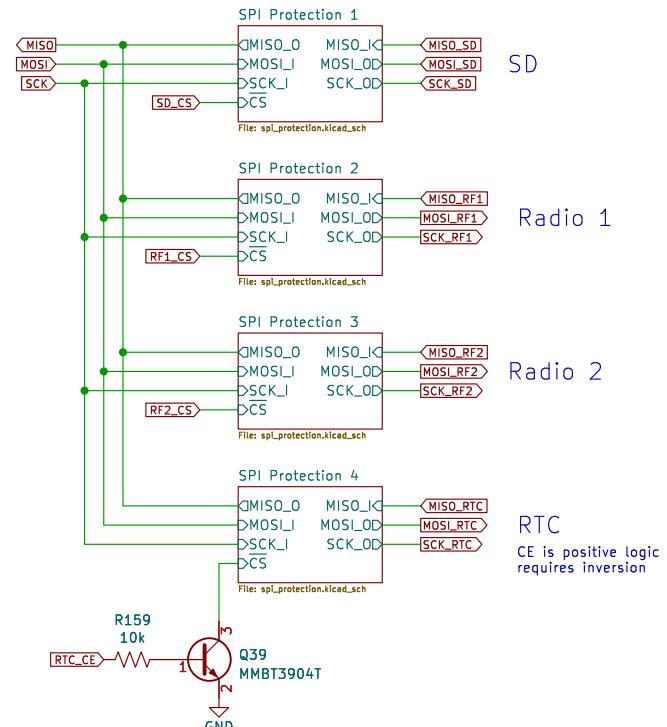
BUS
backplane I2C driver**NOTE**

These novel bus protection circuits prevent traditional I2C/SPI failure modes where a single slave failure can disable the entire bus.

Learn more:
<https://doi.org/10.36227/techrxiv.15166620>

By default, slave clock and/or data lines can be held low and the Master (SAMD51) will still be able to communicate with the remainder of the bus.

They can individually be bypassed by removing the transistor(s) and soldering the 0ohm jumpers below.



C

D

Bus Protection

Sierra Lobo INC.

Sheet: /Bus Protection/
File: Bus_Protection.kicad_sch

Title: PyCubed Mainboard

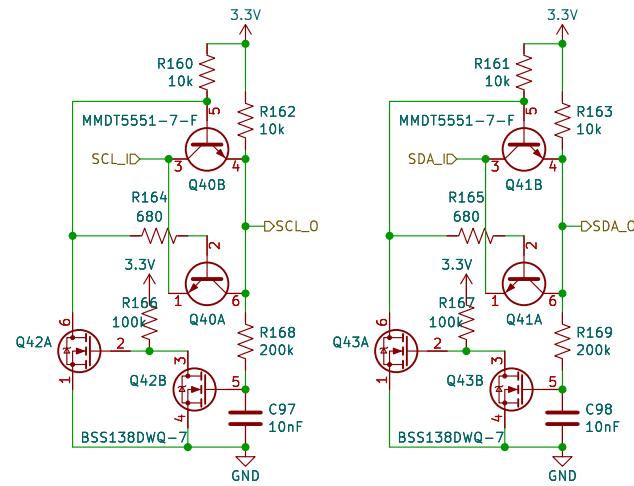
Size: A4 Date: 2021-06-09
KiCad E.D.A. kicad 7.0.1

Rev: v05c
Id: 18/34

A

A

Bus Protection



NOTE

These novel bus protection circuits prevent traditional I₂C/SPI failure modes where a single slave failure can disable the entire bus.

Learn more:
<https://doi.org/10.36227/techrxiv.15166620>

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They can individually be bypassed by removing the transistor(s) and soldering the 0Ω jumpers below.

I₂C Protection – Bypass Jumpers



Sheet: /Bus Protection/I₂C Protection 1/
File: i2c_protection.kicad_sch

Title:

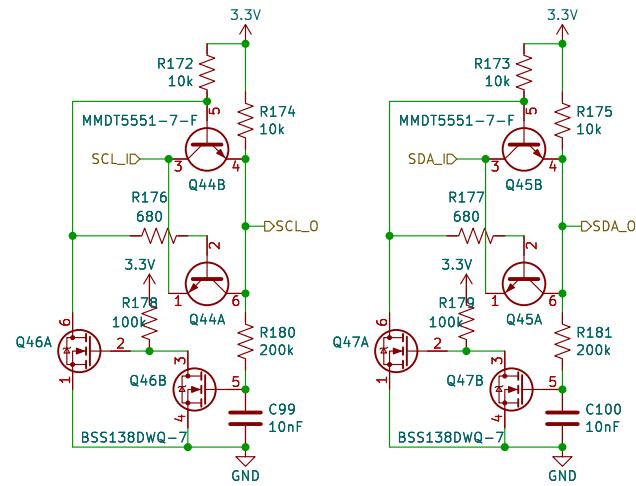
Size: A4 | Date:
KiCad E.D.A. kicad 7.0.1

Rev:
Id: 19/34

A

A

Bus Protection



NOTE

These novel bus protection circuits prevent traditional I₂C/SPI failure modes where a single slave failure can disable the entire bus.

Learn more:
<https://doi.org/10.36227/techrxiv.15166620>

By default, slave clock and/or data lines can be held low and the Master (SAMD51) will still be able to communicate with the remainder of the bus.

They can individually be bypassed by removing the transistor(s) and soldering the 0ohm jumpers below.

I₂C Protection – Bypass Jumpers



Sheet: /Bus Protection/I₂C Protection 2/
File: i2c_protection.kicad_sch

Title:

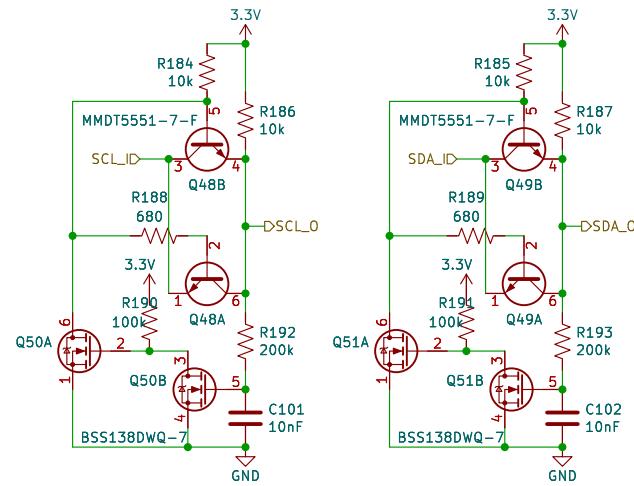
Size: A4 | Date:
KiCad E.D.A. kicad 7.0.1

Rev:
Id: 20/34

A

A

Bus Protection



NOTE

These novel bus protection circuits prevent traditional I₂C/SPI failure modes where a single slave failure can disable the entire bus.

Learn more:
<https://doi.org/10.36227/techrxiv.15166620>

By default, slave clock and/or data lines can be held low and the Master (SAMD51) will still be able to communicate with the remainder of the bus.

They can individually be bypassed by removing the transistor(s) and soldering the 0ohm jumpers below.

I₂C Protection – Bypass Jumpers



Sheet: /Bus Protection/I₂C Protection 3/
File: i2c_protection.kicad_sch

Title:

Size: A4 | Date:
KiCad E.D.A. kicad 7.0.1

Rev:
Id: 21/34

NOTE

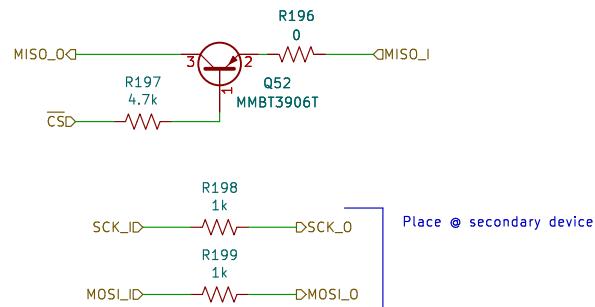
These novel bus protection circuits prevent traditional I²C/SPI failure modes where a single slave failure can disable the entire bus.

Learn more:

<https://doi.org/10.36227/techriv.15166620>

By default, slave clock and/or data lines can be held low and the Master (SAMD51) will still be able to communicate with the remainder of the bus.

They can individually be bypassed by removing the transistor(s) and soldering the 0ohm the jumpers below.

SPI Bus Protection

Place @ secondary device

Bypass Jumper

Jumper Bypass N/R for MOSI
Inline 1k resistors @ destination offer passive protection



Sheet: /Bus Protection/SPI Protection 1/
File: spi_protection.kicad_sch

Title:

Size: A4 | Date:
KiCad E.D.A. kicad 7.0.1

Rev:
Id: 22/34

NOTE

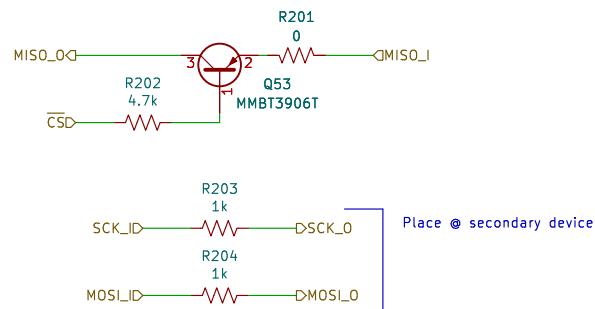
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Learn more:

<https://doi.org/10.36227/techriv.15166620>

By default, slave clock and/or data lines can be held low and the Master (SAMD51) will still be able to communicate with the remainder of the bus.

They can individually be bypassed by removing the transistor(s) and soldering the 0ohm the jumpers below.

SPI Bus Protection**Bypass Jumper**

Jumper Bypass N/R for MOSI
Inline 1k resistors @ destination offer passive protection



Sheet: /Bus Protection/SPI Protection 2/
File: spi_protection.kicad_sch

Title:

Size: A4 | Date:
KiCad E.D.A. kicad 7.0.1

Rev:
Id: 23/34

NOTE

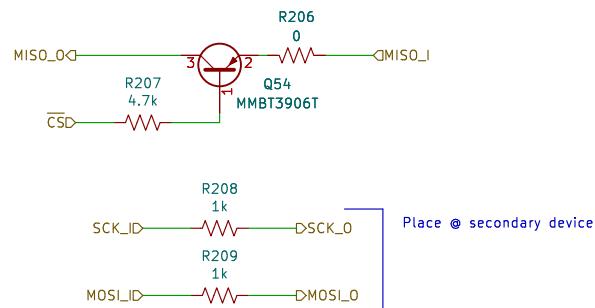
These novel bus protection circuits prevent traditional I₂C/SPI failure modes where a single slave failure can disable the entire bus.

Learn more:

<https://doi.org/10.36227/techriv.15166620>

By default, slave clock and/or data lines can be held low and the Master (SAMD51) will still be able to communicate with the remainder of the bus.

They can individually be bypassed by removing the transistor(s) and soldering the 0ohm the jumpers below.

SPI Bus Protection

Place @ secondary device

Bypass Jumper

Jumper Bypass N/R for MOSI
Inline 1k resistors @ destination offer passive protection



Sheet: /Bus Protection/SPI Protection 3/
File: spi_protection.kicad_sch

Title:

Size: A4 | Date:
KiCad E.D.A. kicad 7.0.1

Rev:
Id: 24/34

NOTE

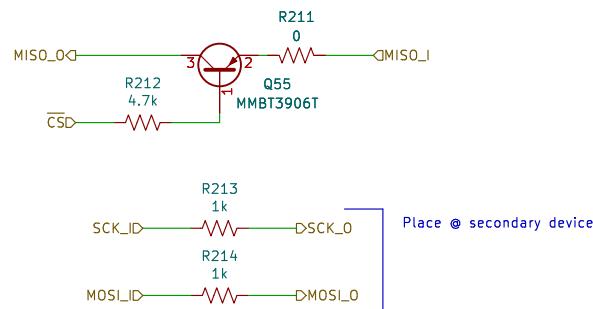
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Learn more:

<https://doi.org/10.36227/techriv.15166620>

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They can individually be bypassed by removing the transistor(s) and soldering the 0ohm the jumpers below.

SPI Bus Protection**Bypass Jumper**

Jumper Bypass N/R for MOSI
Inline 1k resistors @ destination offer passive protection



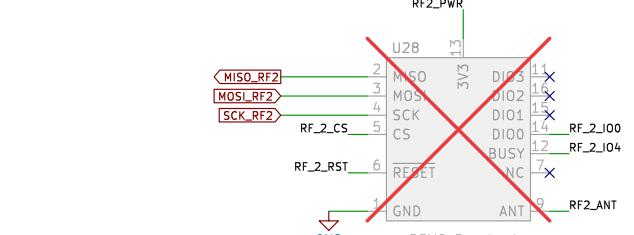
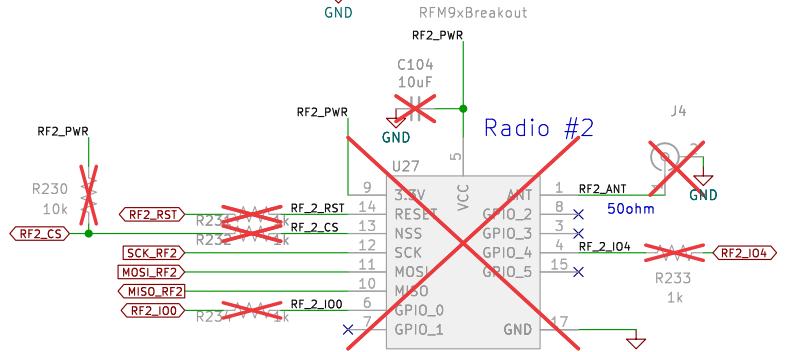
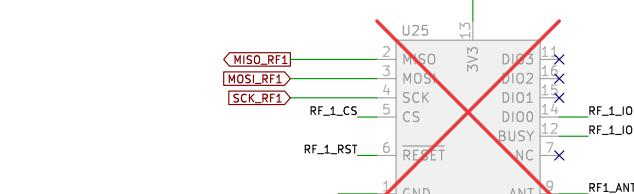
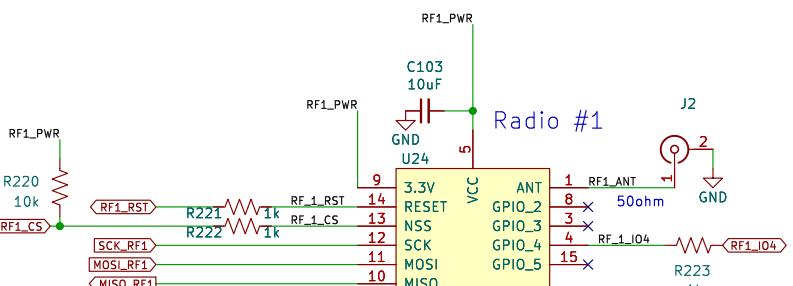
Sheet: /Bus Protection/SPI Protection 4/
File: spi_protection.kicad_sch

Title:

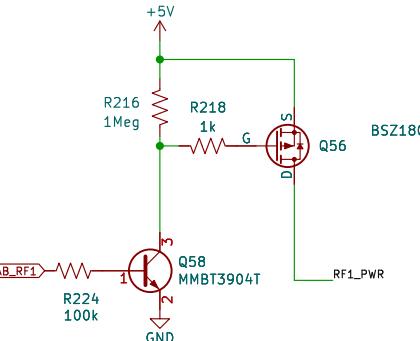
Size: A4 | Date:
KiCad E.D.A. kicad 7.0.1

Rev:
Id: 25/34

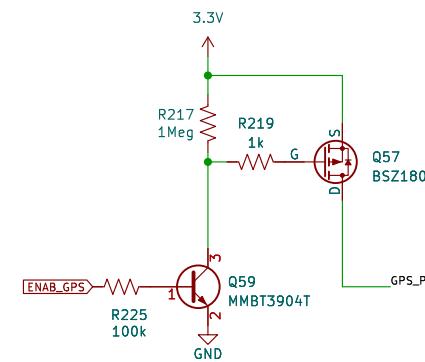
Modular Radios (HopeRF format)



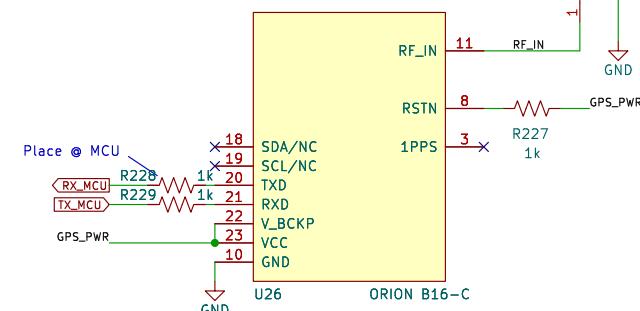
RF1 Power Switch



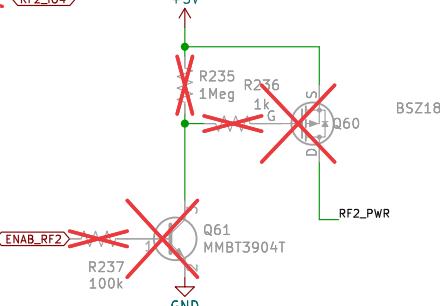
GPS Power Switch



GPS Module



RF2 Power Switch



NOTE: Components labeled "do not install" (DNI) are not populated by default

Radio, GPS, Payloads

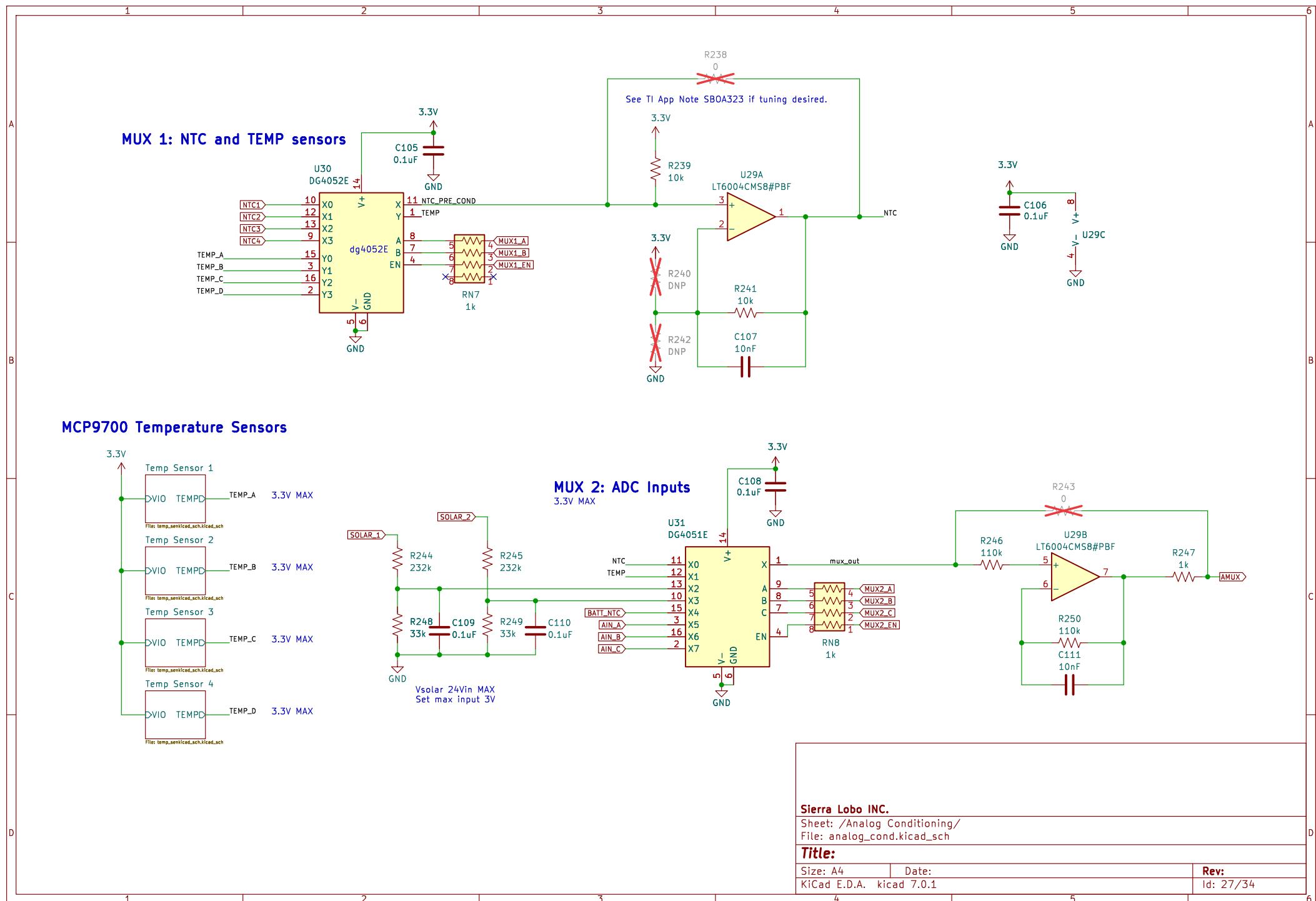
Sierra Lobo INC.

Sheet: /RF and GPS/
File: RF_and_GPS.kicad_sch

Title: PyCubed Mainboard

Size: A4 Date: 2021-06-09
KiCad E.D.A. kicad 7.0.1

Rev: v05c
Id: 26/34



A

A

B

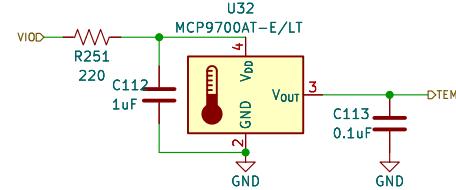
B

C

C

D

D



Sheet: /Analog Conditioning/Temp Sensor 1/
File: temp_senkicad_sch.kicad_sch

Title:

Size: A4 | Date:
KiCad E.D.A. kicad 7.0.1

Rev:
Id: 28/34

A

A

B

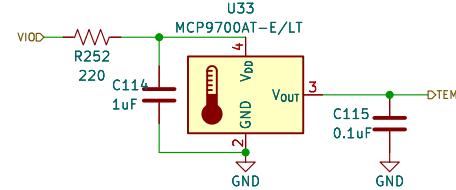
B

C

C

D

D



Sheet: /Analog Conditioning/Temp Sensor 2/
File: temp_senkicad_sch.kicad_sch

Title:

Size: A4 | Date:
KiCad E.D.A. kicad 7.0.1

Rev:
Id: 29/34

A

A

B

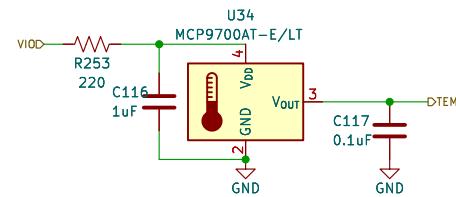
B

C

C

D

D



Sheet: /Analog Conditioning/Temp Sensor 3/
File: temp_senkicad_sch.kicad_sch

Title:

Size: A4 | Date:
KiCad E.D.A. kicad 7.0.1

Rev:
Id: 30/34

A

A

B

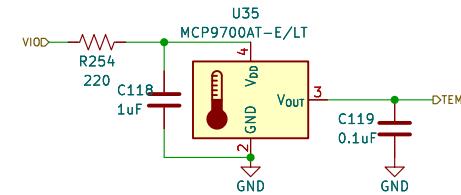
B

C

C

D

D



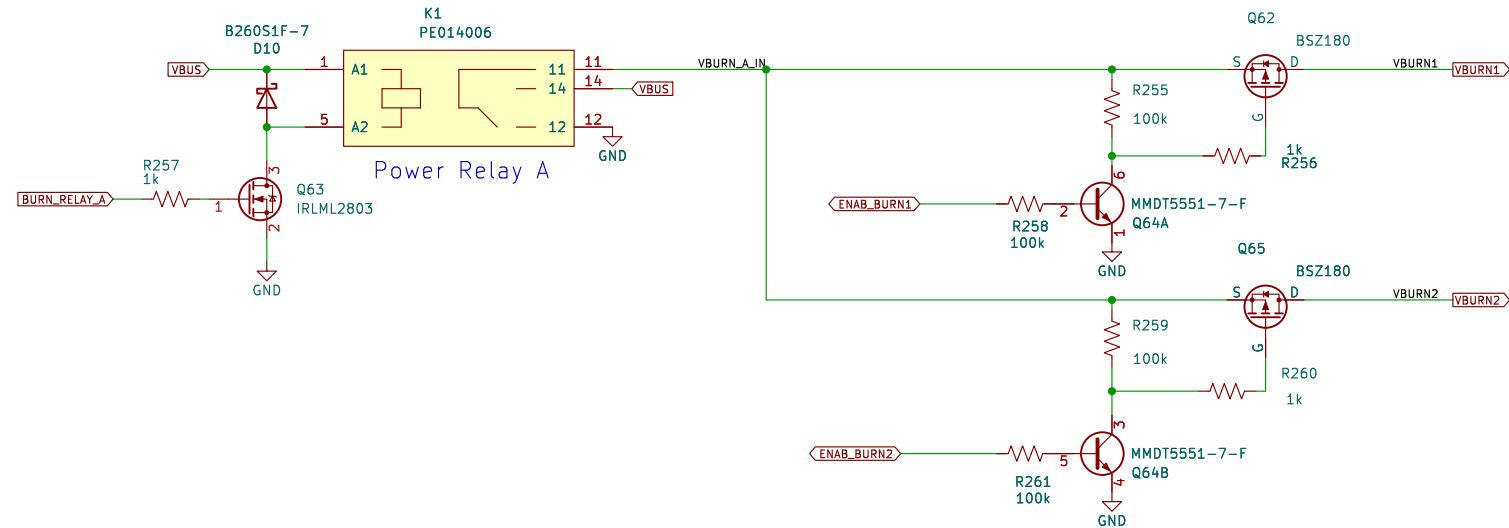
Sheet: /Analog Conditioning/Temp Sensor 4/
File: temp_senkicad_sch.kicad_sch

Title:

Size: A4 | Date:
KiCad E.D.A. kicad 7.0.1

Rev:
Id: 31/34

Burn Wire Control (Antenna Deployment)



NOTE: Components labeled "do not install" (DNI) are not populated by default

Burn Wires

Sierra Lobo INC.

Sheet: /Burn_Wires/
File: Burn_Wires.kicad_sch

Title: PyCubed Mainboard

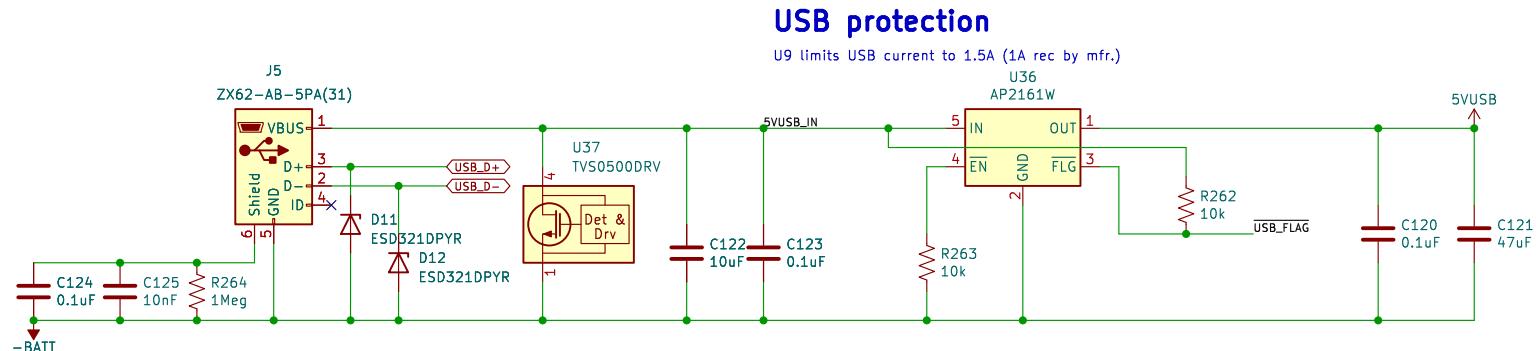
Size: A4 Date: 2021-06-09
KiCad E.D.A. kicad 7.0.1

Rev: v05c
Id: 32/34

1 2 3 4 5 6

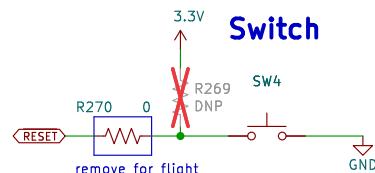
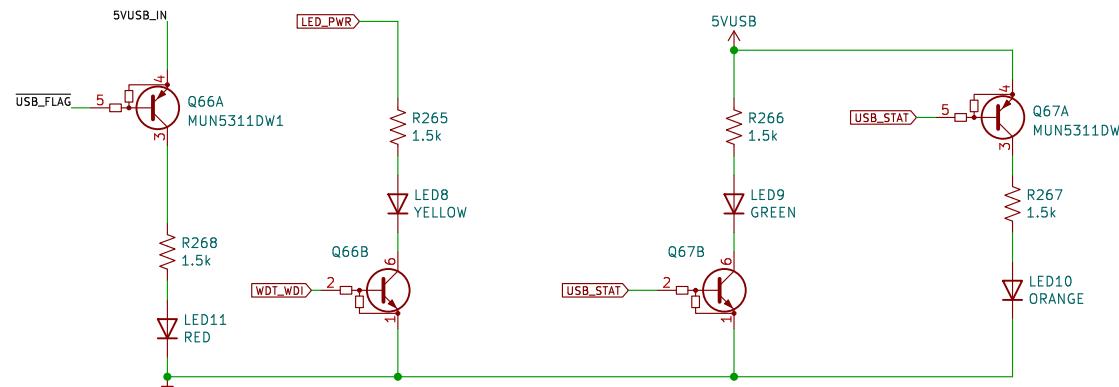
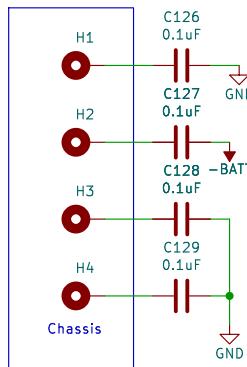
A

A



USB STATUS LEDs

Mounting Holes



Switch

Sierra Lobo INC.

Sheet: /Backplane Interface/
File: Blank-Card-Default.kicad_sch

Title:

Size: A4 | Date:
KiCad E.D.A. kicad 7.0.1

Rev:
Id: 33/34

1 2 3 4 5 6

See LEDs also on backplane card interface, they're not here since they explicitly shine thru the backplane.

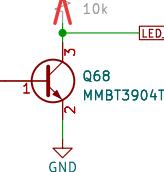
A

LED Jumper

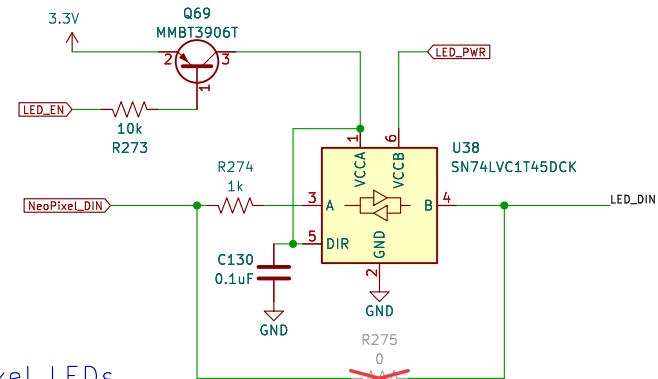


LED Open Collector Enable

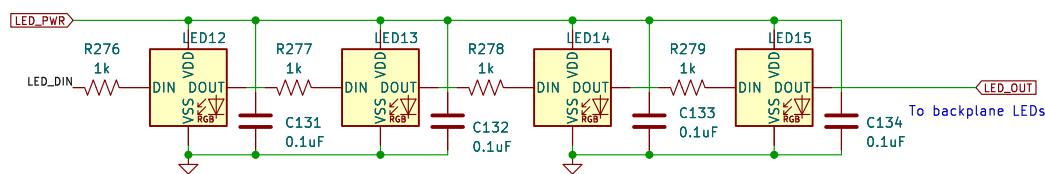
Problem: typical NPN low-side switch driven by power line signal still draws power when LED_PWR removed.
Solution: source open collector EN signal when no PG output



3.3V → 5V Logic Converter



NeoPixel LEDs



Sheet: /Debug LEDs/
File: leds.kicad_sch

Title:

Size: A4 | Date:
KiCad E.D.A. kicad 7.0.1

Rev:
Id: 34/34