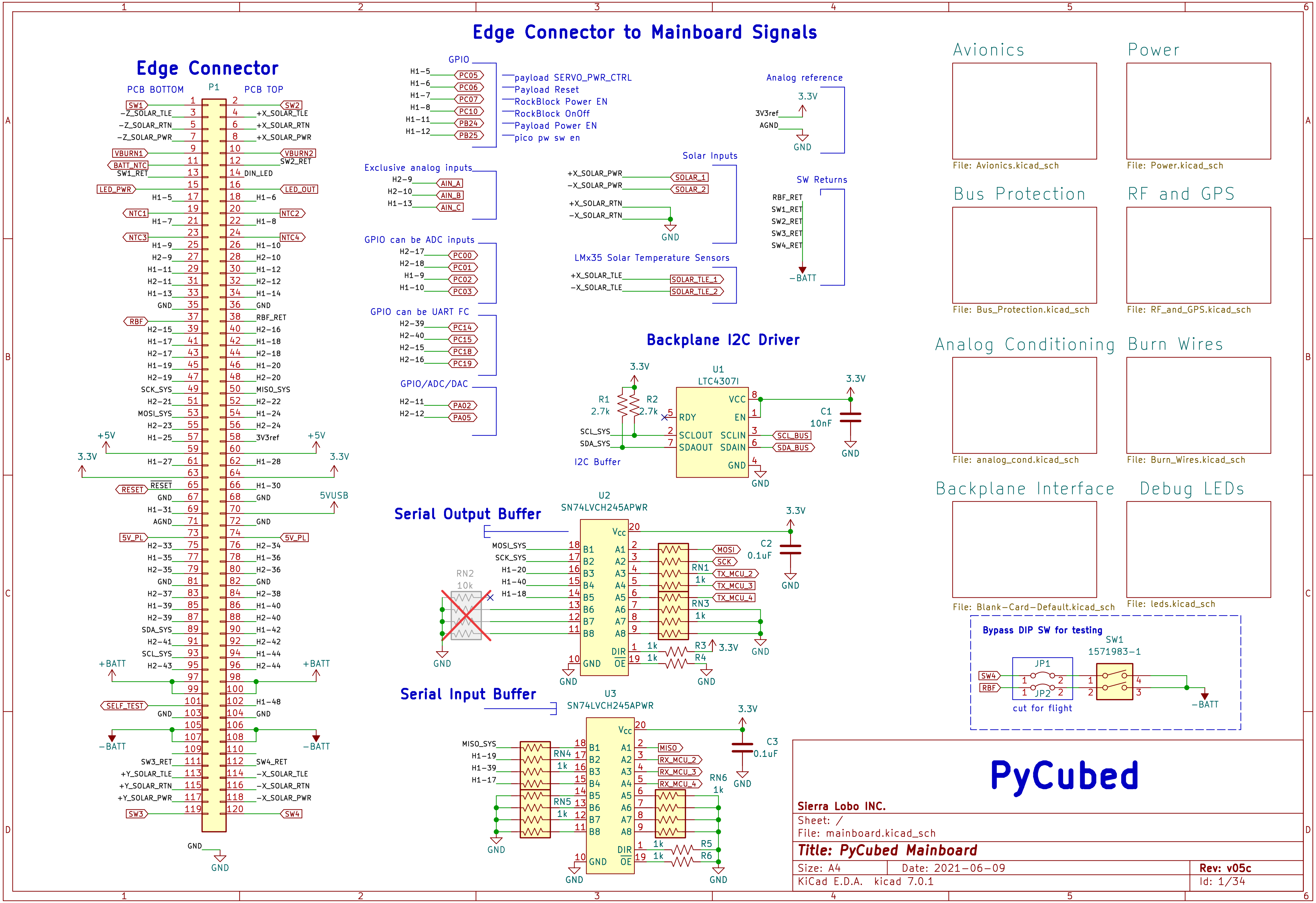
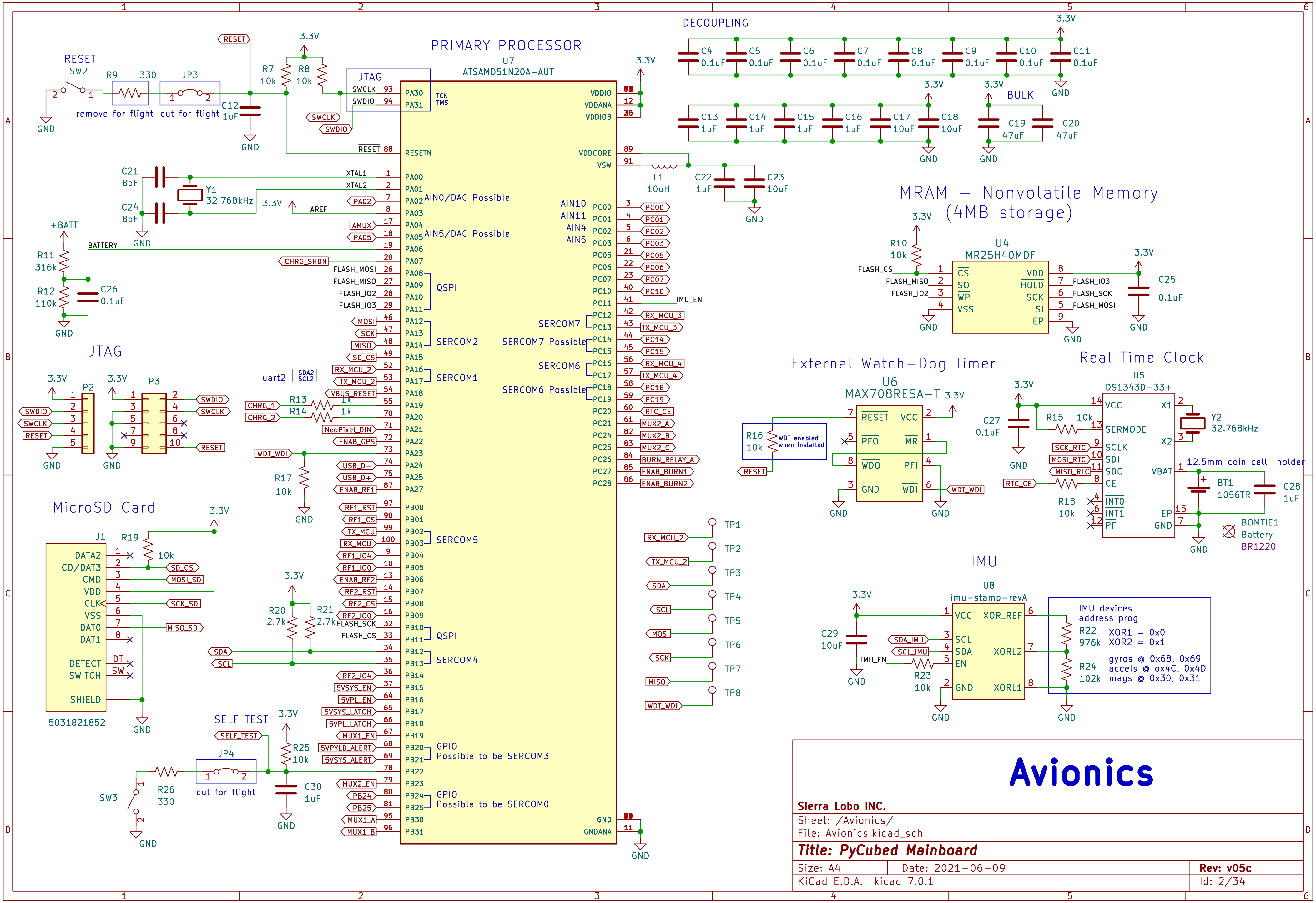
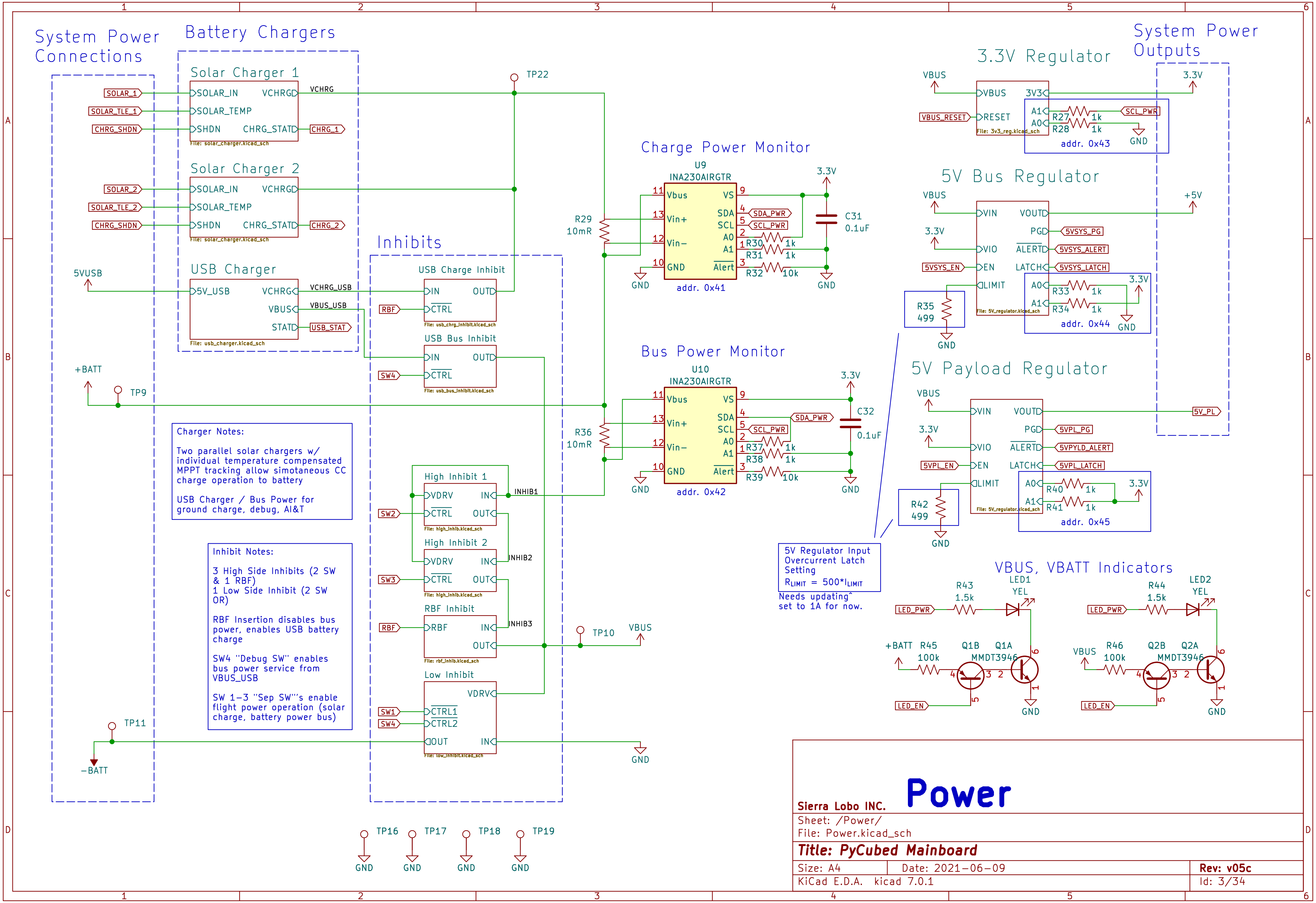
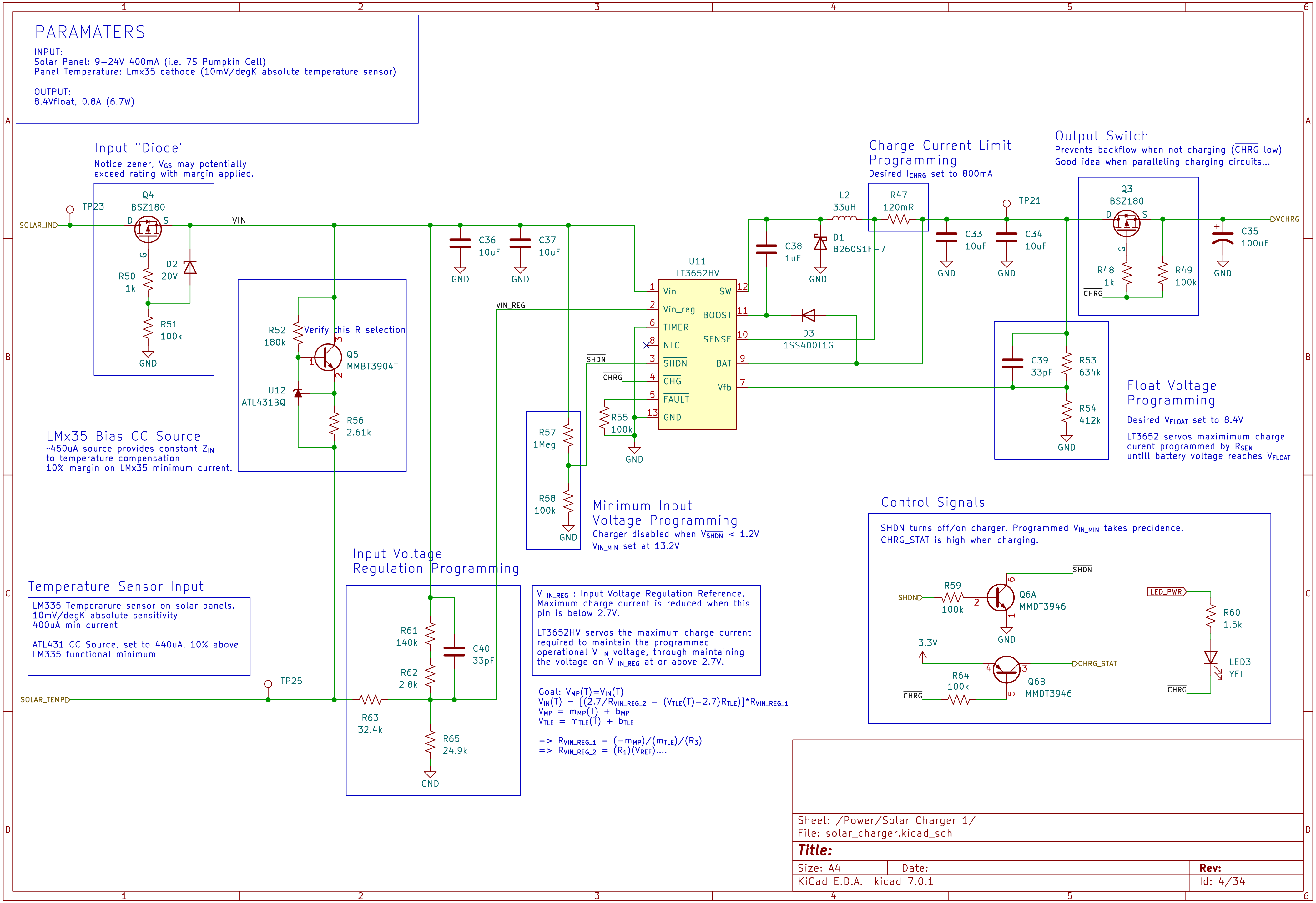
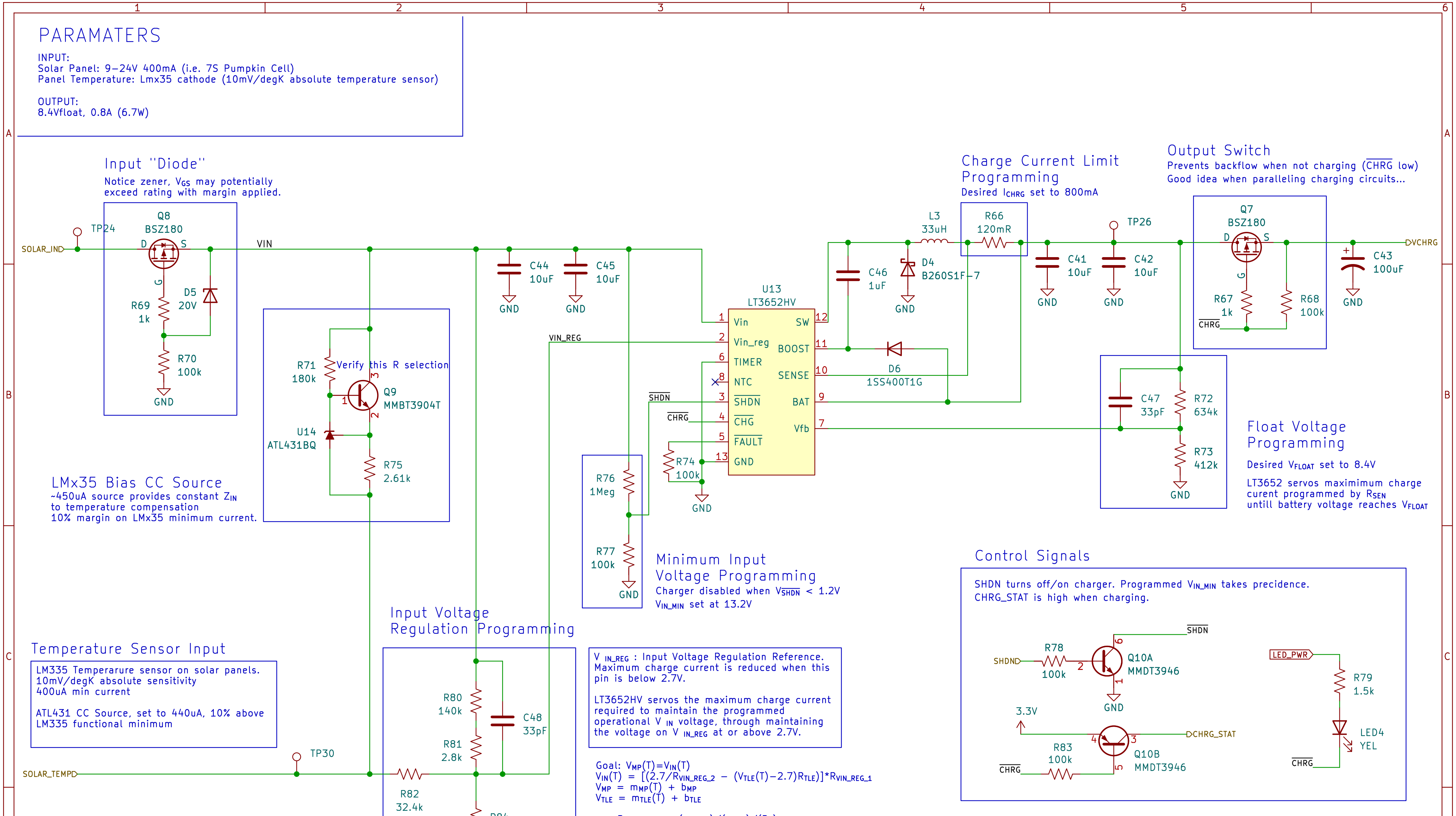

Edge Connector to Mainboard Signals
Edge Connector
PCB BOTTOM
P1
PCB TOP
SW1
SW2
-Z_SOLAR_TLE
+X_SOLAR_TLE
-Z_SOLAR_RTN
+X_SOLAR_RTN
-Z_SOLAR_PWR
+X_SOLAR_PWR
VBURN1
VBURN2
BATT_NTC
SW2_RET
SW1_RET
DIN_LED
LED_PWR
LED_OUT
NTC1
NTC2
NTC3
NTC4
RBF
RBF_RET
SCK_SYS
MISO_SYS
MOSI_SYS
3V3ref
+5V
3.3V
RESET
5VUSB
AGND
5V_PL
SDA_SYS
SCL_SYS
+BATT
SELF_TEST
-BATT
SW3_RET
SW4_RET
+Y_SOLAR_TLE
-X_SOLAR_TLE
+Y_SOLAR_RTN
-X_SOLAR_RTN
+Y_SOLAR_PWR
-X_SOLAR_PWR
SW3
SW4
GND
GPIO
payload SERVO_PWR_CTRL
Payload Reset
RockBlock Power EN
RockBlock OnOff
Payload Power EN
pico pw sw en
Exclusive analog inputs
AIN_A
AIN_B
AIN_C
GPIO can be ADC inputs
GPIO can be UART FC
GPIO/ADC/DAC
Analog reference
Solar Inputs
SOLAR_1
SOLAR_2
SW Returns
LMx35 Solar Temperature Sensors
SOLAR_TLE_1
SOLAR_TLE_2
Backplane I2C Driver
U1
LTC4307I
R1 2.7k
R2 2.7k
C1 10nF
I2C Buffer
SCL_BUS
SDA_BUS
Serial Output Buffer
U2
SN74LVCH245APWR
RN1 1k
RN2 10k
RN3 1k
R3 1k
R4 1k
C2 0.1uF
MOSI
SCK
TX_MCU_2
TX_MCU_3
TX_MCU_4
Serial Input Buffer
U3
SN74LVCH245APWR
RN4 1k
RN5 1k
RN6 1k
R5 1k
R6 1k
C3 0.1uF
MISO
RX_MCU_2
RX_MCU_3
RX_MCU_4
Avionics
File: Avionics.kicad_sch
Power
File: Power.kicad_sch
Bus Protection
File: Bus_Protection.kicad_sch
RF and GPS
File: RF_and_GPS.kicad_sch
Analog Conditioning
File: analog_cond.kicad_sch
Burn Wires
File: Burn_Wires.kicad_sch
Backplane Interface
File: Blank-Card-Default.kicad_sch
Debug LEDs
File: leds.kicad_sch
Bypass DIP SW for testing
SW1
1571983-1
JP1
JP2
cut for flight
PyCubed
Sierra Lobo INC.
Sheet: /
File: mainboard.kicad_sch
Title: PyCubed Mainboard
Size: A4
Date: 2021-06-09
KiCad E.D.A. kicad 7.0.1
Rev: v05c
Id: 1/34


PRIMARY PROCESSOR
U7
ATSAMD51N20A-AUT
RESET
SW2
R9 330
JP3
remove for flight
cut for flight
C12 1uF
R7 10k
R8 10k
JTAG
SWCLK
SWDIO
DECOUPLING
C4 0.1uF
C5 0.1uF
C6 0.1uF
C7 0.1uF
C8 0.1uF
C9 0.1uF
C10 0.1uF
C11 0.1uF
C13 1uF
C14 1uF
C15 1uF
C16 1uF
C17 10uF
C18 10uF
BULK
C19 47uF
C20 47uF
L1 10uH
C22 1uF
C23 10uF
C21 8pF
C24 8pF
Y1 32.768kHz
AIN0/DAC Possible
AIN5/DAC Possible
QSPI
SERCOM2
SERCOM1
SERCOM7
SERCOM7 Possible
SERCOM6
SERCOM6 Possible
SERCOM5
SERCOM4
GPIO
Possible to be SERCOM3
Possible to be SERCOM0
R11 316k
R12 110k
C26 0.1uF
BATTERY
R13 1k
R14 1k
R17 10k
R20 2.7k
R21 2.7k
MRAM – Nonvolatile Memory
(4MB storage)
U4
MR25H40MDF
R10 10k
C25 0.1uF
External Watch-Dog Timer
U6
MAX708RESA-T
R16 10k
WDT enabled when installed
Real Time Clock
U5
DS1343D-33+
C27 0.1uF
R15 10k
R18 10k
Y2 32.768kHz
12.5mm coin cell holder
BT1 1056TR
C28 1uF
BOMTIE1
Battery
BR1220
JTAG
P2
P3
MicroSD Card
J1
R19 10k
5031821852
SELF TEST
JP4
cut for flight
SW3
R26 330
R25 10k
C30 1uF
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
IMU
U8
imu-stamp-revA
C29 10uF
R23 10k
IMU devices
address prog
R22 976k XOR1 = 0x0
XOR2 = 0x1
R24 102k
gyros @ 0x68, 0x69
accels @ 0x4C, 0x4D
mags @ 0x30, 0x31
Avionics
Sierra Lobo INC.
Sheet: /Avionics/
File: Avionics.kicad_sch
Title: PyCubed Mainboard
Size: A4
Date: 2021-06-09
Rev: v05c
KiCad E.D.A. kicad 7.0.1
Id: 2/34


System Power Connections
Battery Chargers
Solar Charger 1
SOLAR_IN VCHRG SOLAR_TEMP SHDN CHRG_STAT
File: solar_charger.kicad_sch
Solar Charger 2
SOLAR_IN VCHRG SOLAR_TEMP SHDN CHRG_STAT
File: solar_charger.kicad_sch
USB Charger
5V_USB VCHRG VBUS STAT
File: usb_charger.kicad_sch
SOLAR_1 SOLAR_TLE_1 CHRG_SHDN SOLAR_2 SOLAR_TLE_2 CHRG_SHDN
CHRG_1 CHRG_2 USB_STAT
VCHRG VCHRG_USB VBUS_USB
5VUSB
+BATT
TP9 TP10 TP11 TP22
-BATT
Inhibits
USB Charge Inhibit
IN OUT CTRL
File: usb_chrg_inhibit.kicad_sch
USB Bus Inhibit
IN OUT CTRL
File: usb_bus_inhibit.kicad_sch
High Inhibit 1
VDRV IN CTRL OUT
File: high_inhib.kicad_sch
High Inhibit 2
VDRV IN CTRL OUT
File: high_inhib.kicad_sch
RBF Inhibit
RBF IN OUT
File: rbf_inhib.kicad_sch
Low Inhibit
VDRV CTRL1 CTRL2 OUT IN
File: low_inhibit.kicad_sch
RBF SW4 SW2 SW3 RBF SW1 SW4
INHIB1 INHIB2 INHIB3
Charger Notes:
Two parallel solar chargers w/ individual temperature compensated MPPT tracking allow simotaneous CC charge operation to battery
USB Charger / Bus Power for ground charge, debug, AI&T
Inhibit Notes:
3 High Side Inhibits (2 SW & 1 RBF)
1 Low Side Inhibit (2 SW OR)
RBF Insertion disables bus power, enables USB battery charge
SW4 "Debug SW" enables bus power service from VBUS_USB
SW 1-3 "Sep SW"'s enable flight power operation (solar charge, battery power bus)
Charge Power Monitor
U9
INA230AIRGTR
Vbus Vin+ Vin- GND VS SDA SCL A0 A1 Alert
R29 10mR
R30 1k R31 1k R32 10k
C31 0.1uF
SDA_PWR SCL_PWR
addr. 0x41
Bus Power Monitor
U10
INA230AIRGTR
Vbus Vin+ Vin- GND VS SDA SCL A0 A1 Alert
R36 10mR
R37 1k R38 1k R39 10k
C32 0.1uF
SDA_PWR SCL_PWR
addr. 0x42
3.3V Regulator
VBUS 3V3 RESET A1 A0
VBUS_RESET
R27 1k R28 1k
SCL_PWR
File: 3v3_reg.kicad_sch
addr. 0x43
5V Bus Regulator
VIN VOUT PG VIO ALERT EN LATCH LIMIT A0 A1
5VSYS_PG 5VSYS_ALERT 5VSYS_EN 5VSYS_LATCH
R33 1k R34 1k
R35 499
File: 5V_regulator.kicad_sch
addr. 0x44
5V Payload Regulator
VIN VOUT PG VIO ALERT EN LATCH LIMIT A0 A1
5V_PL 5VPL_PG 5VPYLD_ALERT 5VPL_EN 5VPL_LATCH
R40 1k R41 1k
R42 499
File: 5V_regulator.kicad_sch
addr. 0x45
System Power Outputs
3.3V +5V
5V Regulator Input Overcurrent Latch Setting
R_{LIMIT} = 500*I_{LIMIT}
Needs updating^ set to 1A for now.
VBUS, VBATT Indicators
LED_PWR R43 1.5k LED1 YEL
LED_PWR R44 1.5k LED2 YEL
+BATT R45 100k Q1B Q1A MMDT3946
VBUS R46 100k Q2B Q2A MMDT3946
LED_EN LED_EN
GND
TP16 TP17 TP18 TP19
Sierra Lobo INC.
Power
Sheet: /Power/
File: Power.kicad_sch
Title: PyCubed Mainboard
Size: A4 Date: 2021-06-09 Rev: v05c
KiCad E.D.A. kicad 7.0.1 Id: 3/34



PARAMATERS
INPUT:
Solar Panel: 9-24V 400mA (i.e. 7S Pumpkin Cell)
Panel Temperature: Lmx35 cathode (10mV/degK absolute temperature sensor)
OUTPUT:
8.4Vfloat, 0.8A (6.7W)
Input "Diode"
Notice zener, V_{GS} may potentially exceed rating with margin applied.
SOLAR_IN
TP23
Q4 BSZ180
D S G
VIN
R50 1k
D2 20V
R51 100k
GND
R52 180k
Verify this R selection
Q5 MMBT3904T
U12 ATL431BQ
R56 2.61k
LMx35 Bias CC Source
~450uA source provides constant Z_{IN} to temperature compensation
10% margin on LMx35 minimum current.
C36 10uF
C37 10uF
VIN_REG
U11 LT3652HV
Vin SW
Vin_reg BOOST
TIMER SENSE
NTC BAT
SHDN Vfb
CHG
FAULT
GND
R55 100k
R57 1Meg
R58 100k
Minimum Input Voltage Programming
Charger disabled when $V_{\overline{SHDN}}$ < 1.2V
V_{IN_MIN} set at 13.2V
L2 33uH
Charge Current Limit Programming
Desired I_{CHRG} set to 800mA
R47 120mR
C38 1uF
D1 B260S1F-7
D3 1SS400T1G
TP21
C33 10uF
C34 10uF
Output Switch
Prevents backflow when not charging ($\overline{CHRG}$ low)
Good idea when paralleling charging circuits...
Q3 BSZ180
R48 1k
R49 100k
C35 100uF
VCHRG
C39 33pF
R53 634k
R54 412k
Float Voltage Programming
Desired V_{FLOAT} set to 8.4V
LT3652 servos maximum charge current programmed by R_{SEN} untill battery voltage reaches V_{FLOAT}
Temperature Sensor Input
LM335 Temperarure sensor on solar panels.
10mV/degK absolute sensitivity
400uA min current
ATL431 CC Source, set to 440uA, 10% above LM335 functional minimum
SOLAR_TEMP
TP25
Input Voltage Regulation Programming
R61 140k
R62 2.8k
C40 33pF
R63 32.4k
R65 24.9k
V_{IN_REG} : Input Voltage Regulation Reference. Maximum charge current is reduced when this pin is below 2.7V.
LT3652HV servos the maximum charge current required to maintain the programmed operational V_{IN} voltage, through maintaining the voltage on V_{IN_REG} at or above 2.7V.
Goal: $V_{MP}(T)=V_{IN}(T)$
$V_{IN}(T) = [(2.7/R_{VIN\_REG\_2} - (V_{TLE}(T)-2.7)R_{TLE})]*R_{VIN\_REG\_1}$
$V_{MP} = m_{MP}(T) + b_{MP}$
$V_{TLE} = m_{TLE}(T) + b_{TLE}$
=> $R_{VIN\_REG\_1} = (-m_{MP})/(m_{TLE})/(R_3)$
=> $R_{VIN\_REG\_2} = (R_1)(V_{REF})$....
Control Signals
SHDN turns off/on charger. Programmed V_{IN_MIN} takes precidence.
CHRG_STAT is high when charging.
SHDN
R59 100k
Q6A MMDT3946
3.3V
R64 100k
Q6B MMDT3946
CHRG_STAT
LED_PWR
R60 1.5k
LED3 YEL
CHRG
Sheet: /Power/Solar Charger 1/
File: solar_charger.kicad_sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad 7.0.1
Id: 4/34



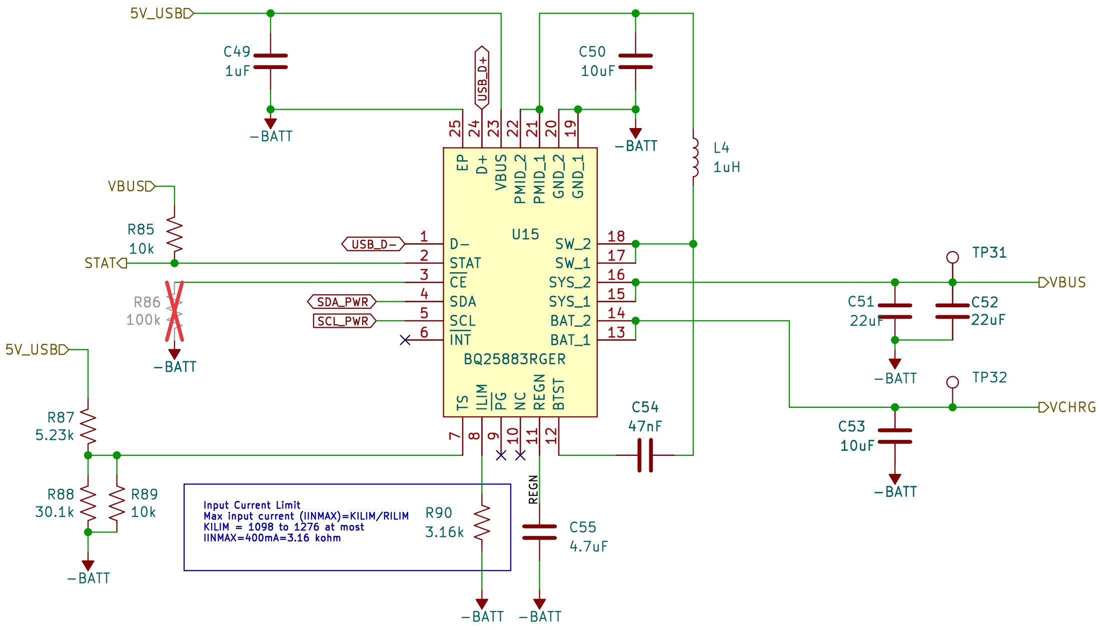
Sheet: /Power/Solar Charger 2/
File: solar_charger.kicad_sch

Title:

Size: A4 | Date: | Rev:

KiCad E.D.A. kicad 7.0.1 | Id: 5/34

USB (Boost) Charging for 2-cell Li-Ion

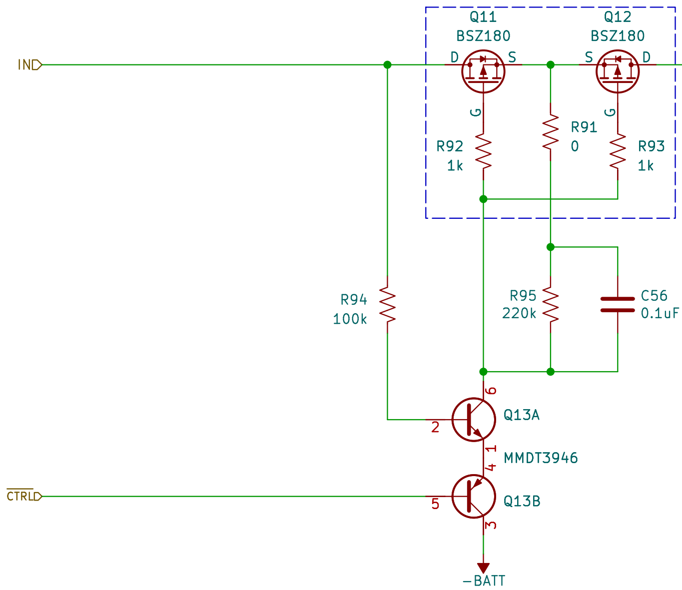


Sheet: /Power/USB Charger/
File: usb_charger.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 7.0.1		Id: 6/34

USB Charge Inhibit



Implementation Notes:

Two anti-series FETs to prevent forward/backfeeding when charging is not desired

Allows ground chagre via USB when USB is applied and CTRL is low. (RBF Inserted)

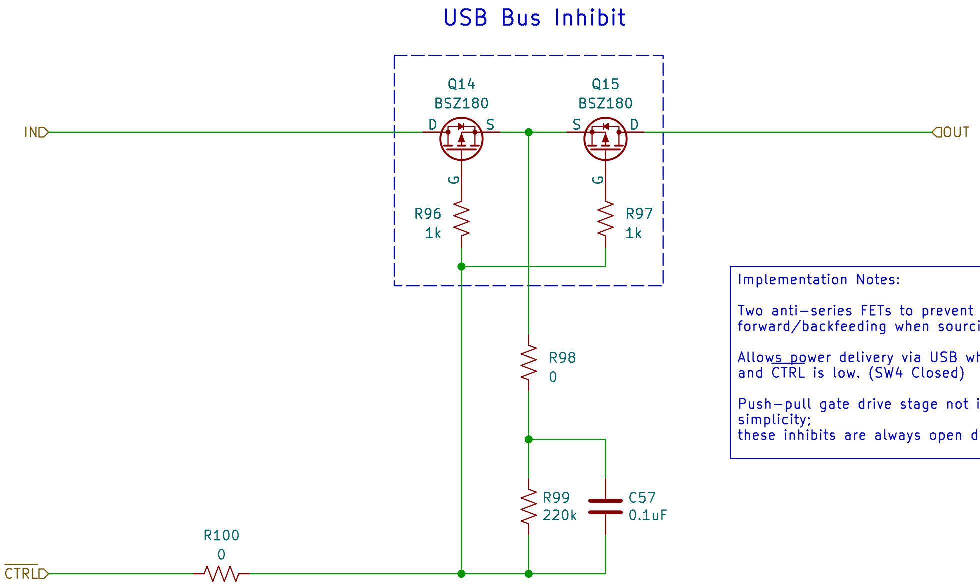
Push-pull gate drive stage not implemented for simplicity;
these inhibits are always open during mission

Sheet: /Power/USB Charge Inhibit/
File: usb_chrg_inhibit.kicad_sch

Title:

Size: A4 | Date: | **Rev:**

KiCad E.D.A. kicad 7.0.1 | Id: 7/34



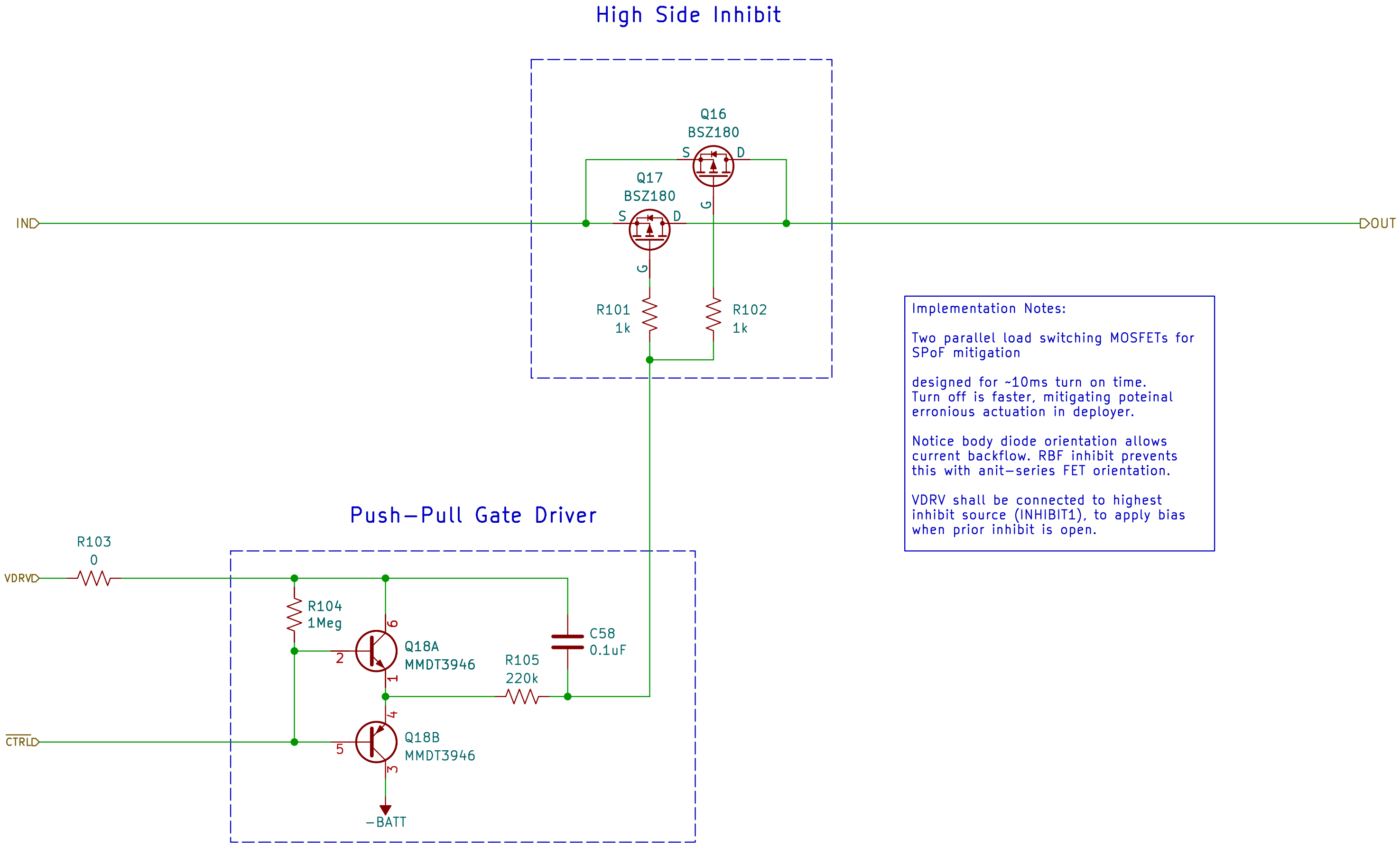
Implementation Notes:

Two anti-series FETs to prevent
forward/backfeeding when sourcing is not desired

Allows power delivery via USB when USB is applied
and CTRL is low. (SW4 Closed)

Push-pull gate drive stage not implemented for
simplicity;
these inhibits are always open during mission

Sheet: /Power/USB Bus Inhibit/		
File: usb_bus_inhibit.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 7.0.1		Id: 8/34



Implementation Notes:

Two parallel load switching MOSFETs for SPoF mitigation

designed for ~10ms turn on time.
Turn off is faster, mitigating poteinal erronious actuation in deployer.

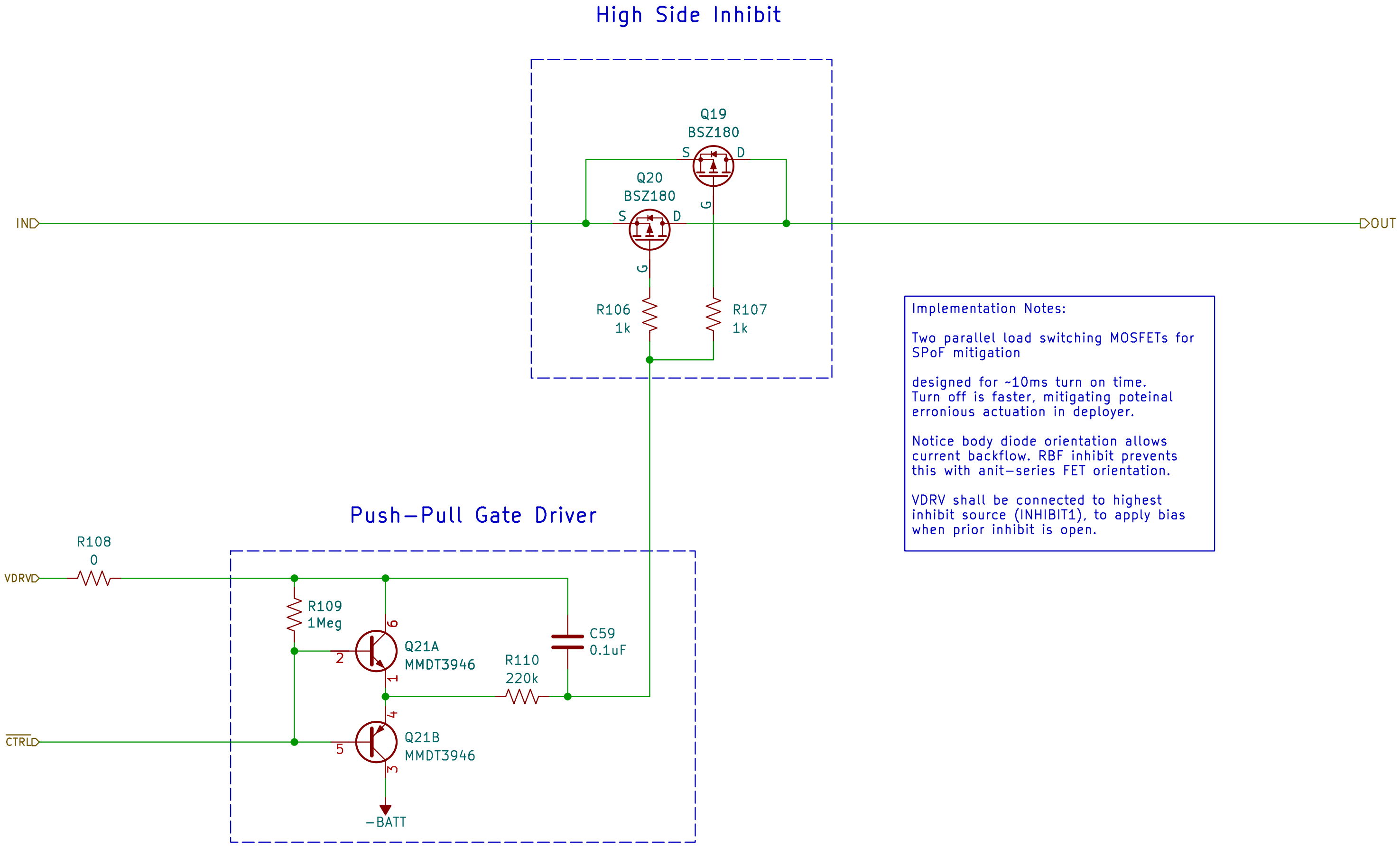
Notice body diode orientation allows current backflow. RBF inhibit prevents this with anit-series FET orientation.

VDRV shall be connected to highest inhibit source (INHIBIT1), to apply bias when prior inhibit is open.

Sheet: /Power/High Inhibit 1/
File: high_inhib.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 7.0.1		Id: 9/34



Implementation Notes:

Two parallel load switching MOSFETs for SPoF mitigation

designed for ~10ms turn on time.
Turn off is faster, mitigating poteinal erronious actuation in deployer.

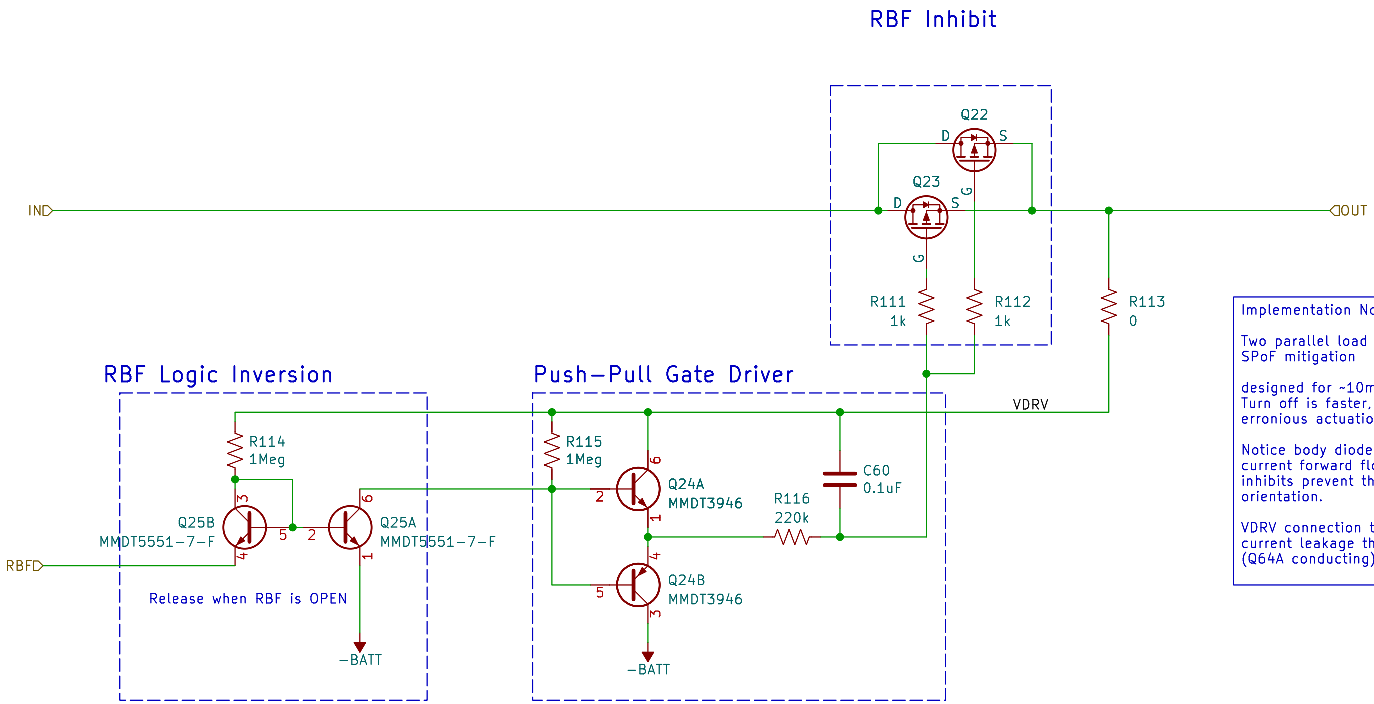
Notice body diode orientation allows current backflow. RBF inhibit prevents this with anit-series FET orientation.

VDRV shall be connected to highest inhibit source (INHIBIT1), to apply bias when prior inhibit is open.

Sheet: /Power/High Inhibit 2/
File: high_inhib.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 7.0.1		Id: 10/34



Implementation Notes:

Two parallel load switching MOSFETs for SPoF mitigation

designed for ~10ms turn on time.
Turn off is faster, mitigating poteinal erronious actuation in deployer.

Notice body diode orientation allows current forward flow. Two previous inhibits prevent this with anit-series FET orientation.

VDRV connection to FET source prevents current leakage thru RBF when stowed (Q64A conducting)

RBF is open during flight, opposed to SEP SW's that are closed.

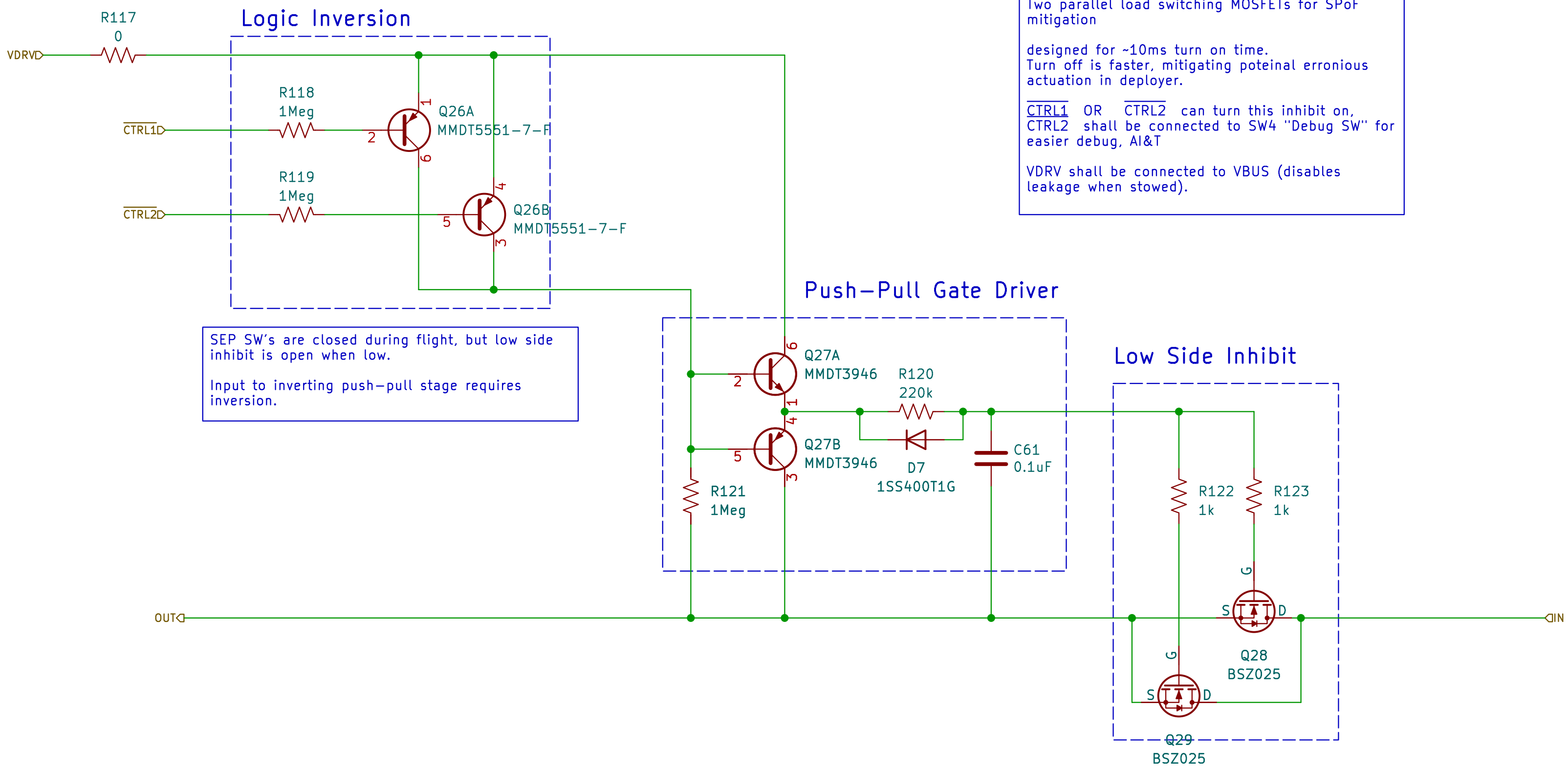
Requires inversion with use of push-pull stage.

RBF to only sink current (reasoning for output diode) due to ability for current to be sourced to this (and hence thru Q64A) from USB CHRG inhibit

Sheet: /Power/RBF Inhibit/
File: rbf_inhib.kicad_sch

Title:

Size: A4	Date:	Rev:
KiCad E.D.A. kicad 7.0.1		Id: 11/34



SEP SW's are closed during flight, but low side inhibit is open when low.

Input to inverting push-pull stage requires inversion.

Implementation Notes:

Two parallel load switching MOSFETs for SPoF mitigation

designed for ~10ms turn on time.
Turn off is faster, mitigating poteinal erronious actuation in deployer.

$\overline{\text{CTRL1}}$ OR $\overline{\text{CTRL2}}$ can turn this inhibit on, CTRL2 shall be connected to SW4 "Debug SW" for easier debug, AI&T

VDRV shall be connected to VBUS (disables leakage when stowed).

Sheet: /Power/Low Inhibit/
File: low_inhibit.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 7.0.1		Id: 12/34

PARAMATERS

INPUT:
VBUS 5–8.4V

OUTPUT:
5V, 2A (max, 10W)

Implementation Notes:

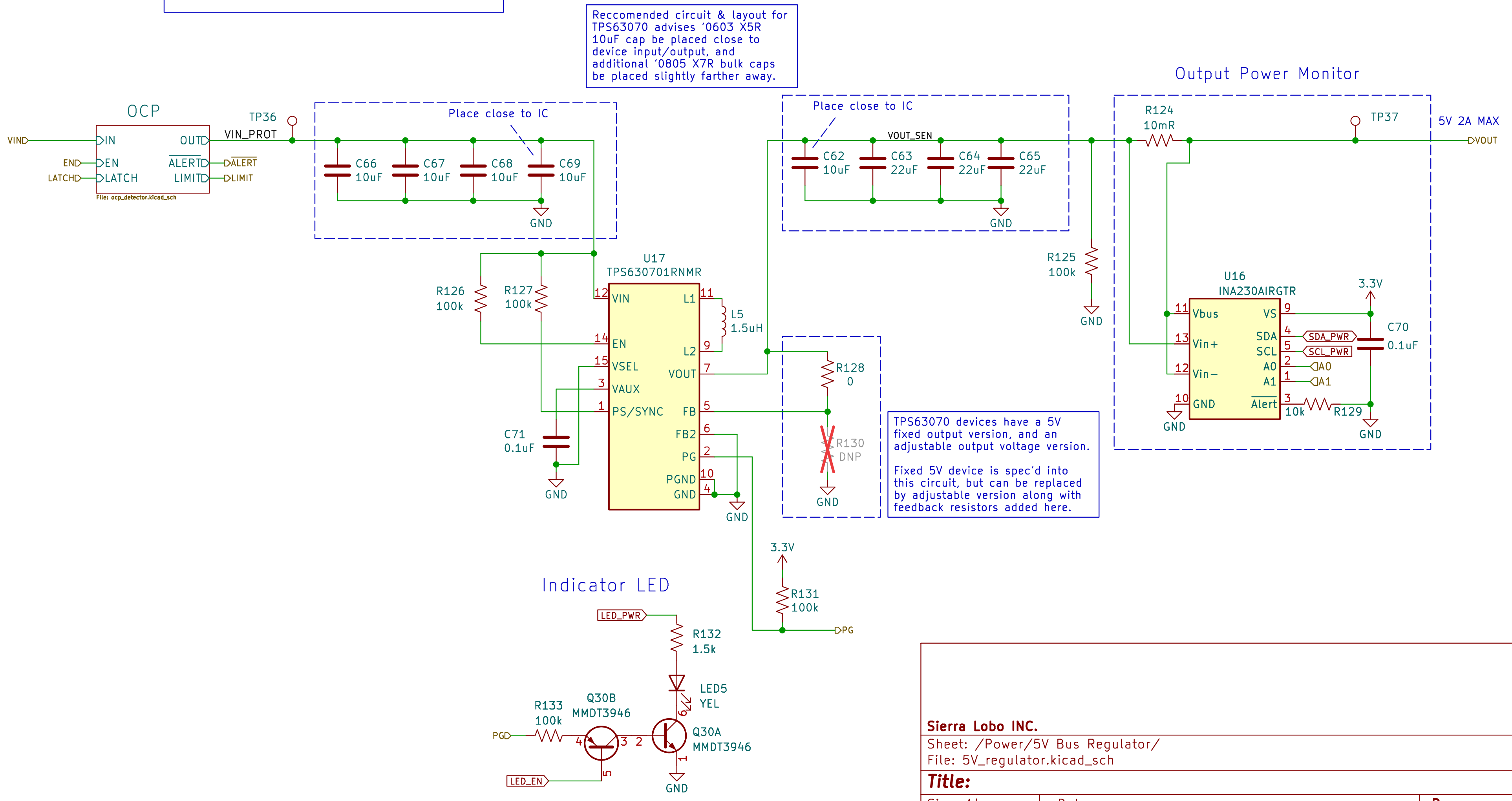
based from TI WebBench Design.

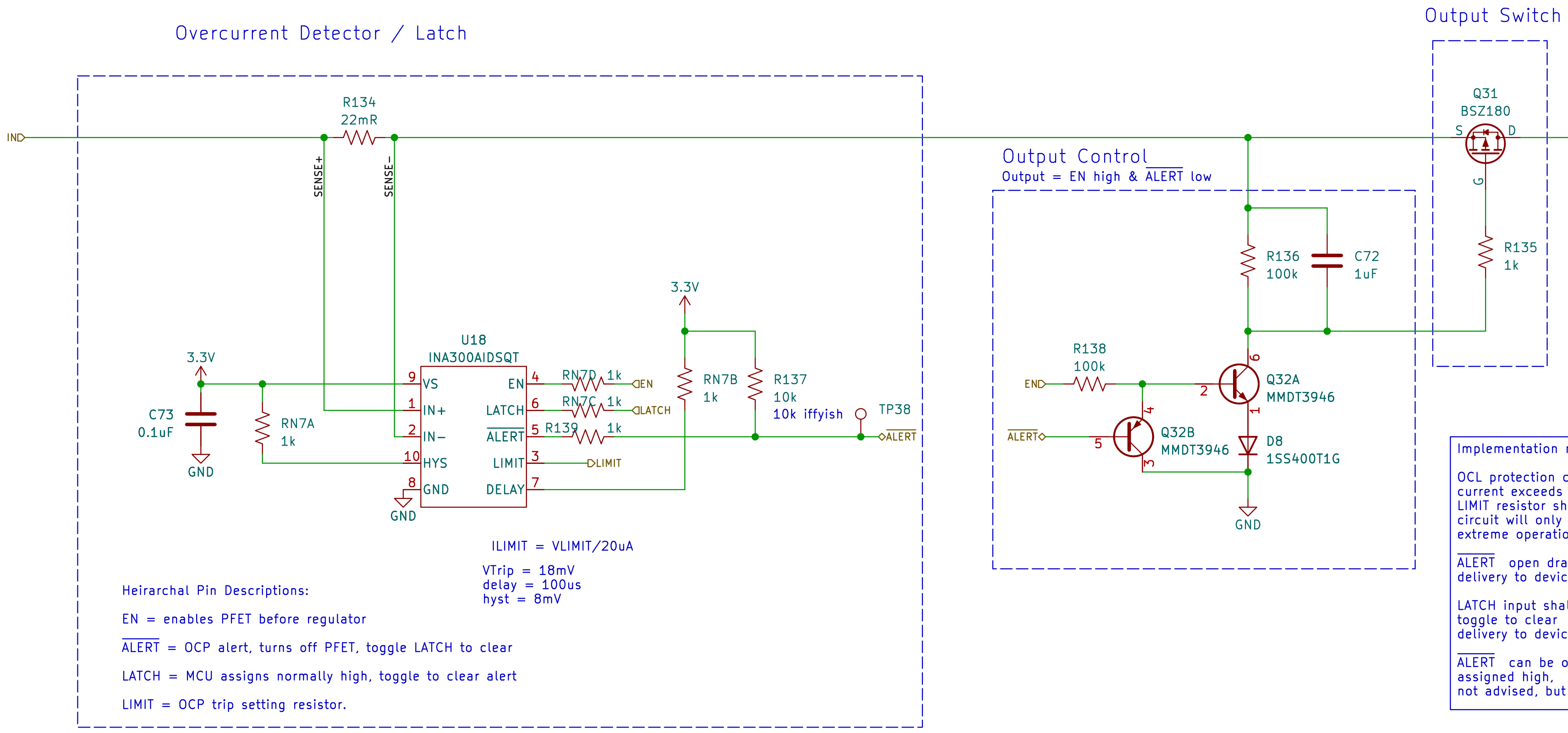
No heritage for TPS63070, failure of device has potenital to cause catastrophic upstream fault.

OCL protection circuit will disable power to device when input current exceeds threshold set by LIMIT resistor. LIMIT resistor shall be calculated such that OCL will only trip when current surpasses extreme operational bounds (i.e. 40% margin at 80% conversion efficiency).

Low input capacitance & device soft start will limit inrush when turned on, but current will still spike as device &/| downstream devices are used.

OCP circuit trips after 100uS of a sustained trip current additionally mitigating nusianse trips, but users should still be cogizant of such.





Implementation notes:

OCL protection circuit will open FET when input current exceeds threshold set by LIMIT resistor. LIMIT resistor should be calculated such that circuit will only trip due to current surpassing extreme operational bounds.

$\overline{\text{ALERT}}$ open drain output turns off power delivery to device, readable by MCU.

LATCH input shall be assigned high by MCU, toggle to clear ALERT, re-enabling power delivery to device.

$\overline{\text{ALERT}}$ can be overriden by MCU by being assigned high,
not advised, but available.

Overcurrent Protection

Sheet: /Power/5V Bus Regulator/OCP/
File: ocp_detector.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 7.0.1		Id: 14/34

PARAMATERS

INPUT:
VBUS 5–8.4V

OUTPUT:
5V, 2A (max, 10W)

Implementation Notes:

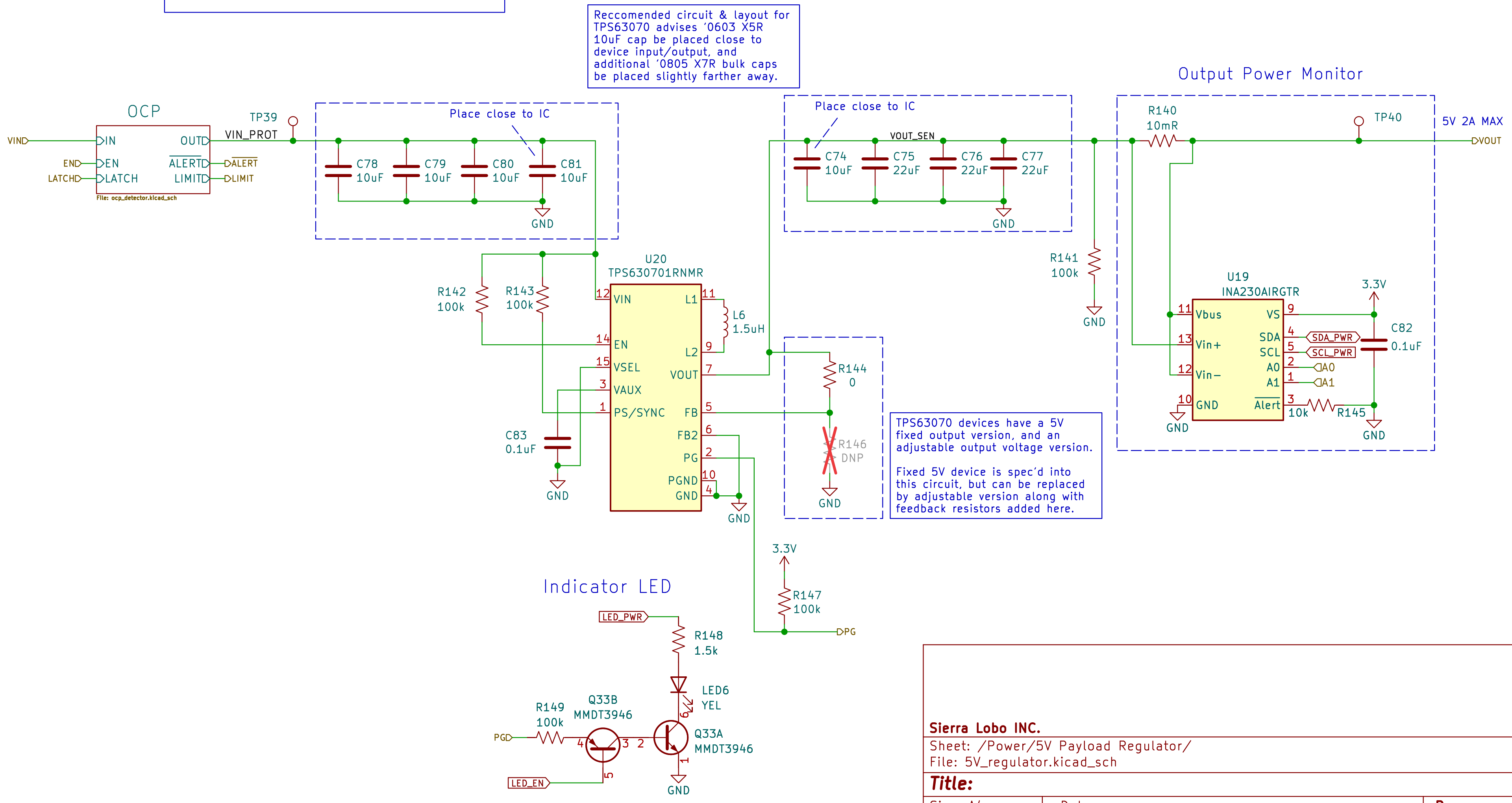
based from TI WebBench Design.

No heritage for TPS63070, failure of device has potential to cause catastrophic upstream fault.

OCL protection circuit will disable power to device when input current exceeds threshold set by LIMIT resistor. LIMIT resistor shall be calculated such that OCL will only trip when current surpasses extreme operational bounds (i.e. 40% margin at 80% conversion efficiency).

Low input capacitance & device soft start will limit inrush when turned on, but current will still spike as device &/| downstream devices are used.

OCP circuit trips after 100uS of a sustained trip current additionally mitigating nusianse trips, but users should still be cogizant of such.

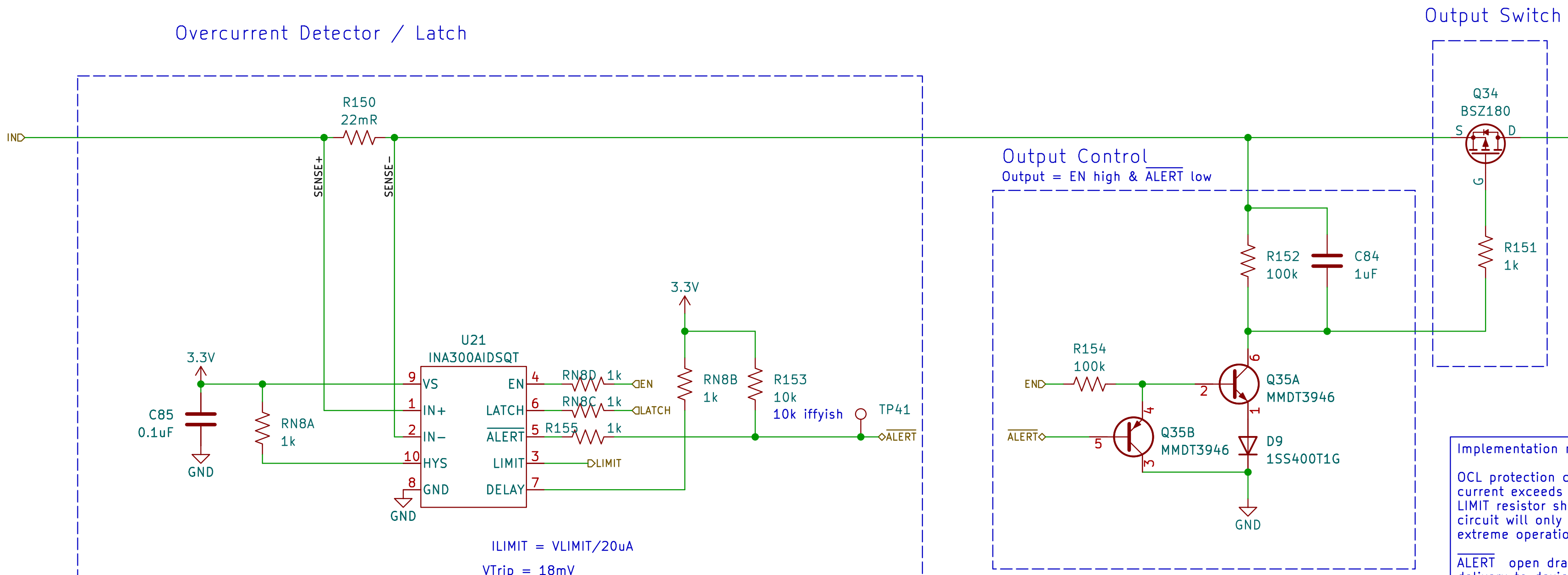


Sierra Lobo INC.

Sheet: /Power/5V Payload Regulator/
File: 5V_regulator.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 7.0.1		Id: 15/34



Heirarchal Pin Descriptions:

EN = enables PFET before regulator

ALERT = OCP alert, turns off PFET, toggle LATCH to clear

LATCH = MCU assigns normally high, toggle to clear alert

LIMIT = OCP trip setting resistor.

Implementation notes:

OCL protection circuit will open FET when input current exceeds threshold set by LIMIT resistor. LIMIT resistor should be calculated such that circuit will only trip due to current surpassing extreme operational bounds.

ALERT open drain output turns off power delivery to device, readable by MCU.

LATCH input shall be assigned high by MCU, toggle to clear ALERT , re−enabling power delivery to device.

ALERT can be overriden by MCU by being assigned high, not advised, but available.

Overcurrent Protection

Sheet: /Power/5V Payload Regulator/OCP/
File: ocp_detector.kicad_sch

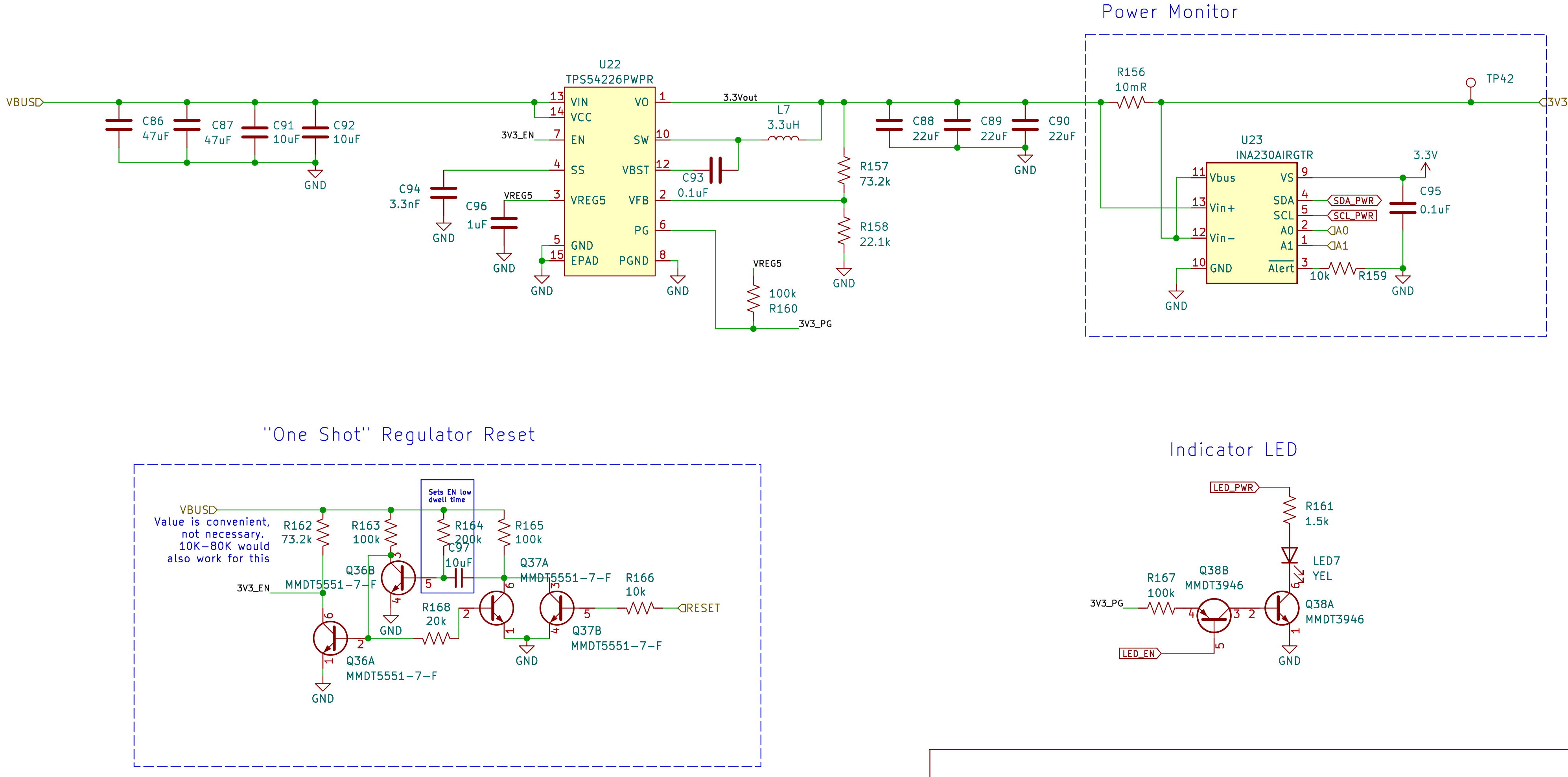
Title:

Size: A4	Date:	Rev:
KiCad E.D.A. kicad 7.0.1		Id: 16/34

PARAMATERS

INPUT:
VBUS 4.5–18V

OUTPUT:
3.3V, ~1.5A (OCP)
~1.5A OCP (See datasheet p8 for more information.)



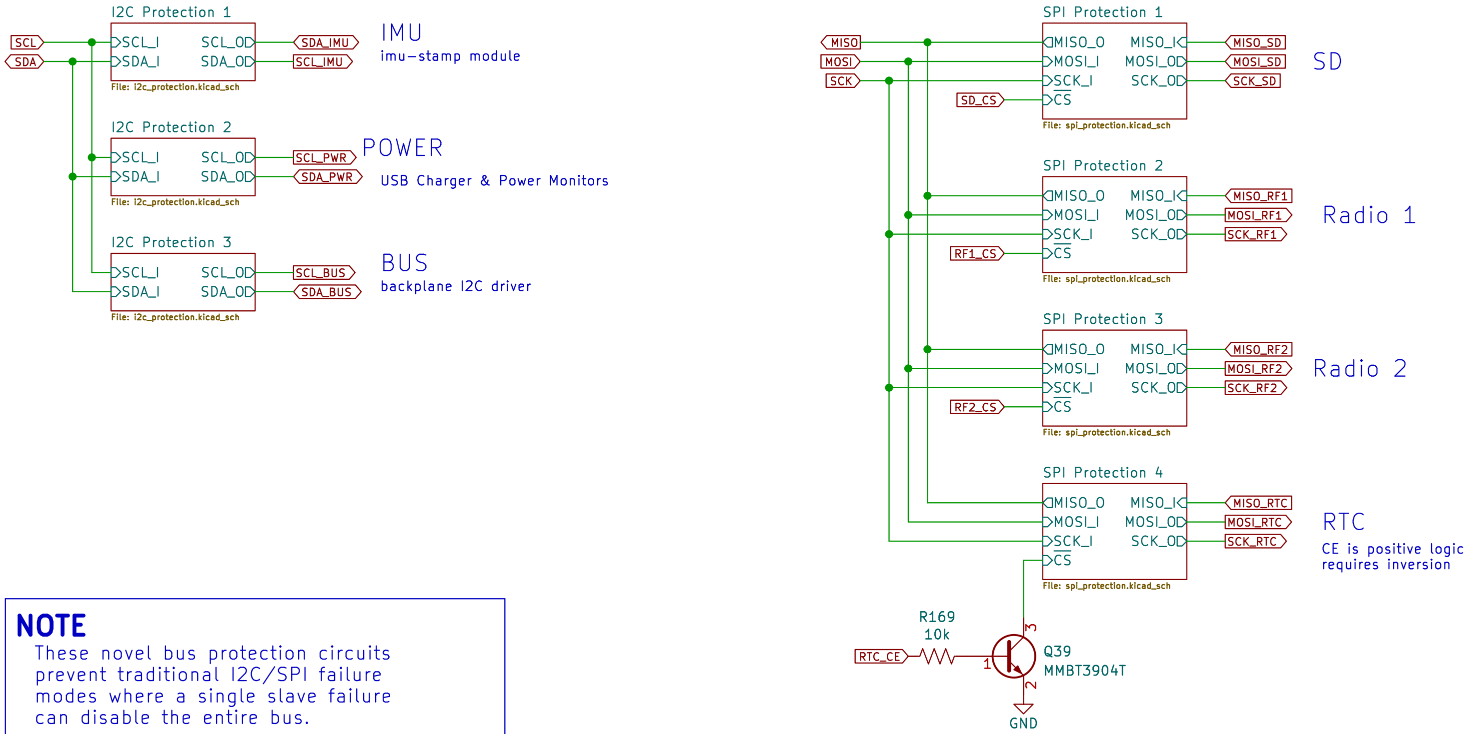
Sheet: /Power/3.3V Regulator/
File: 3v3_reg.kicad_sch

Title:

Size: A4 | Date: | **Rev:**

KiCad E.D.A. kicad 7.0.1 | Id: 17/34

I2C Bus Protection



NOTE

These novel bus protection circuits prevent traditional I2C/SPI failure modes where a single slave failure can disable the entire bus.

Learn more:
https://doi.org/10.36227/techrxiv.15166620

By default, slave clock and/or data lines can be held low and the Master (SAMD51) will still be able to communicate with the remainder of the bus.

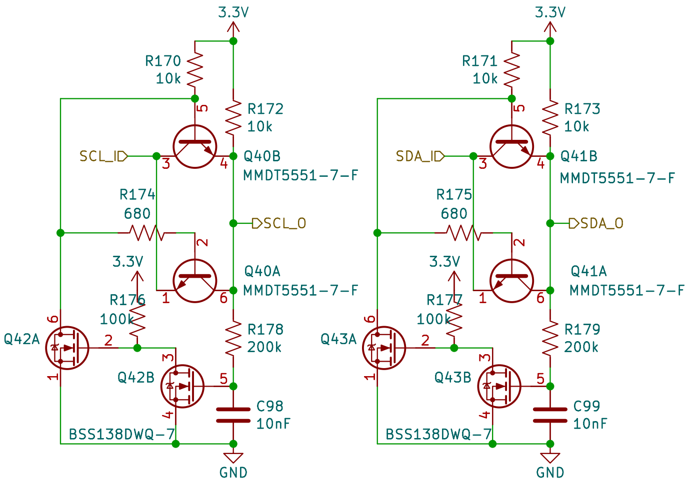
They can individually be bypassed by removing the transistor(s) and soldering the 0ohm the jumpers below.

Sierra Lobo INC.
Sheet: /Bus Protection/
File: Bus_Protection.kicad_sch

Title: PyCubed Mainboard

Size: A4	Date: 2021-06-09	Rev: v05c
KiCad E.D.A. kicad 7.0.1		Id: 18/34

Bus Protection



NOTE

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Learn more:
https://doi.org/10.36227/techrxiv.15166620

By default, slave clock and/or data lines can be held low and the Master (SAMD51) will still be able to communicate with the remainder of the bus.

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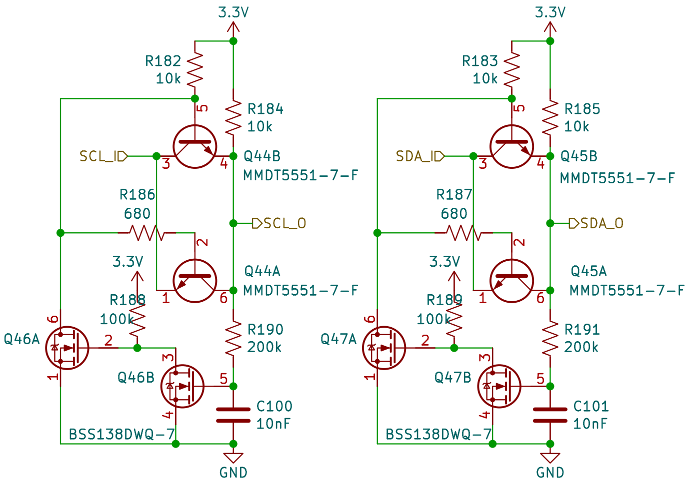
I2C Protection - Bypass Jumpers

Sheet: /Bus Protection/I2C Protection 1/
File: i2c_protection.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 7.0.1		Id: 19/34

Bus Protection



NOTE

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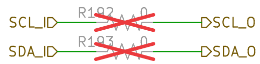
Learn more:
https://doi.org/10.36227/techrxiv.15166620

By default, slave clock and/or data lines can be held low and the Master (SAMD51) will still be able to communicate with the remainder of the bus.

They can individually be bypassed by removing the transistor(s) and soldering the 0ohm the jumpers below.

I2C Protection – Bypass Jumpers

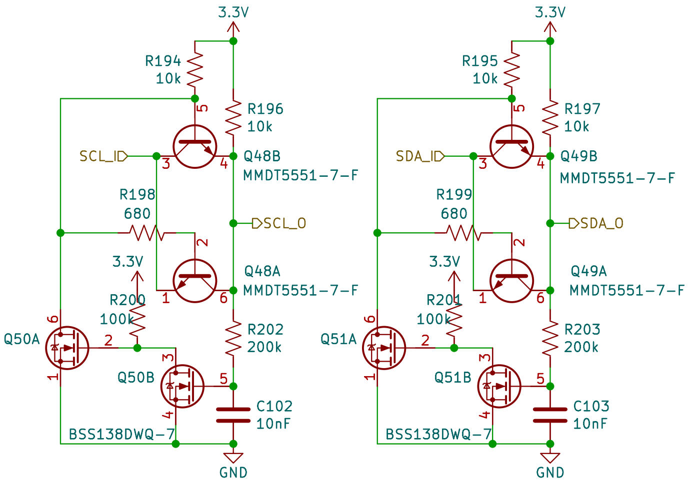


Sheet: /Bus Protection/I2C Protection 2/
File: i2c_protection.kicad_sch

Title:

Size: A4	Date:	Rev:
KiCad E.D.A. kicad 7.0.1		Id: 20/34

Bus Protection



NOTE

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Learn more:
https://doi.org/10.36227/techrxiv.15166620

By default, slave clock and/or data lines can be held low and the Master (SAMD51) will still be able to communicate with the remainder of the bus.

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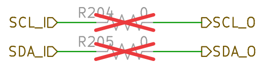
I2C Protection - Bypass Jumpers



Sheet: /Bus Protection/I2C Protection 3/
File: i2c_protection.kicad_sch

Title:

Size: A4	Date:	Rev:
KiCad E.D.A. kicad 7.0.1		Id: 21/34

NOTE

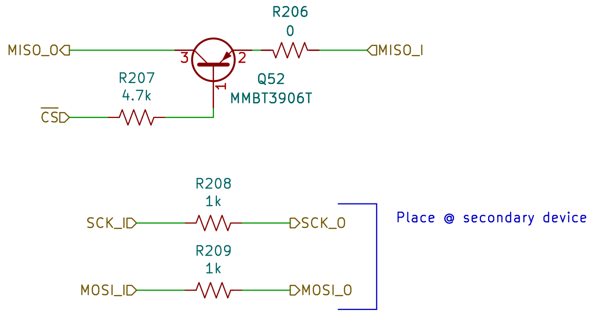
These novel bus protection circuits prevent traditional I2C/SPI failure modes where a single slave failure can disable the entire bus.

Learn more:
https://doi.org/10.36227/techrxiv.15166620

By default, slave clock and/or data lines can be held low and the Master (SAMD51) will still be able to communicate with the remainder of the bus.

They can individually be bypassed by removing the transistor(s) and soldering the 0ohm the jumpers below.

SPI Bus Protection



Bypass Jumper

Jumper Bypass N/R for MOSI
Inline 1k resistors @ destination offer passive protection

Sheet: /Bus Protection/SPI Protection 1/
File: spi_protection.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 7.0.1		Id: 22/34

NOTE

These novel bus protection circuits prevent traditional I2C/SPI failure modes where a single slave failure can disable the entire bus.

Learn more:
https://doi.org/10.36227/techrxiv.15166620

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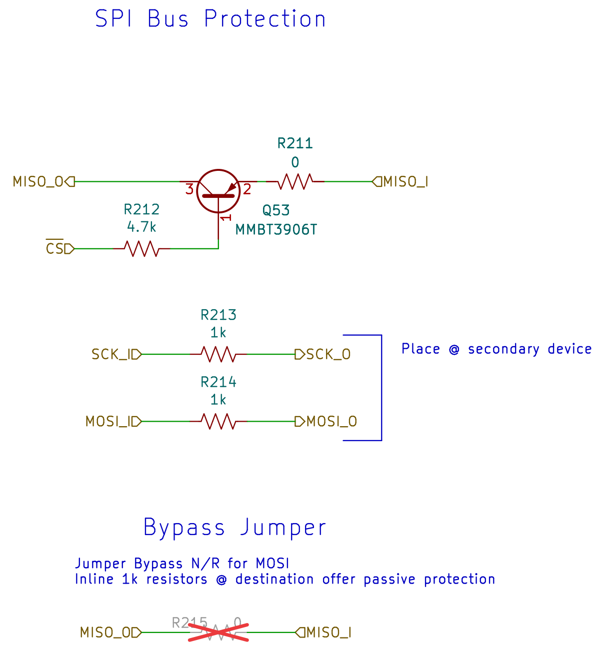
They can individually be bypassed by removing the transistor(s) and soldering the 0ohm the jumpers below.



Sheet: /Bus Protection/SPI Protection 2/
File: spi_protection.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 7.0.1		Id: 23/34

NOTE

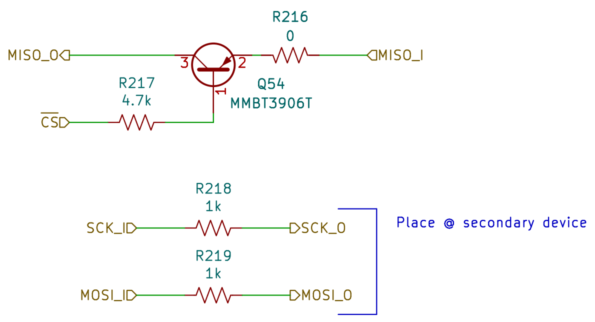
These novel bus protection circuits prevent traditional I2C/SPI failure modes where a single slave failure can disable the entire bus.

Learn more:
https://doi.org/10.36227/techrxiv.15166620

By default, slave clock and/or data lines can be held low and the Master (SAMD51) will still be able to communicate with the remainder of the bus.

They can individually be bypassed by removing the transistor(s) and soldering the 0ohm the jumpers below.

SPI Bus Protection



Bypass Jumper

Jumper Bypass N/R for MOSI
Inline 1k resistors @ destination offer passive protection

Sheet: /Bus Protection/SPI Protection 3/
File: spi_protection.kicad_sch

Title:

Size: A4 | Date: | **Rev:**

KiCad E.D.A. kicad 7.0.1 | Id: 24/34

NOTE

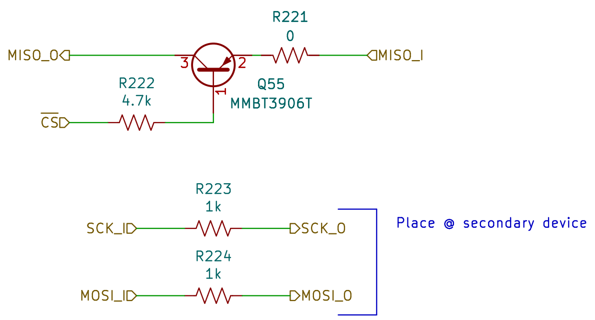
These novel bus protection circuits prevent traditional I2C/SPI failure modes where a single slave failure can disable the entire bus.

Learn more:
https://doi.org/10.36227/techrxiv.15166620

By default, slave clock and/or data lines can be held low and the Master (SAMD51) will still be able to communicate with the remainder of the bus.

They can individually be bypassed by removing the transistor(s) and soldering the 0ohm the jumpers below.

SPI Bus Protection



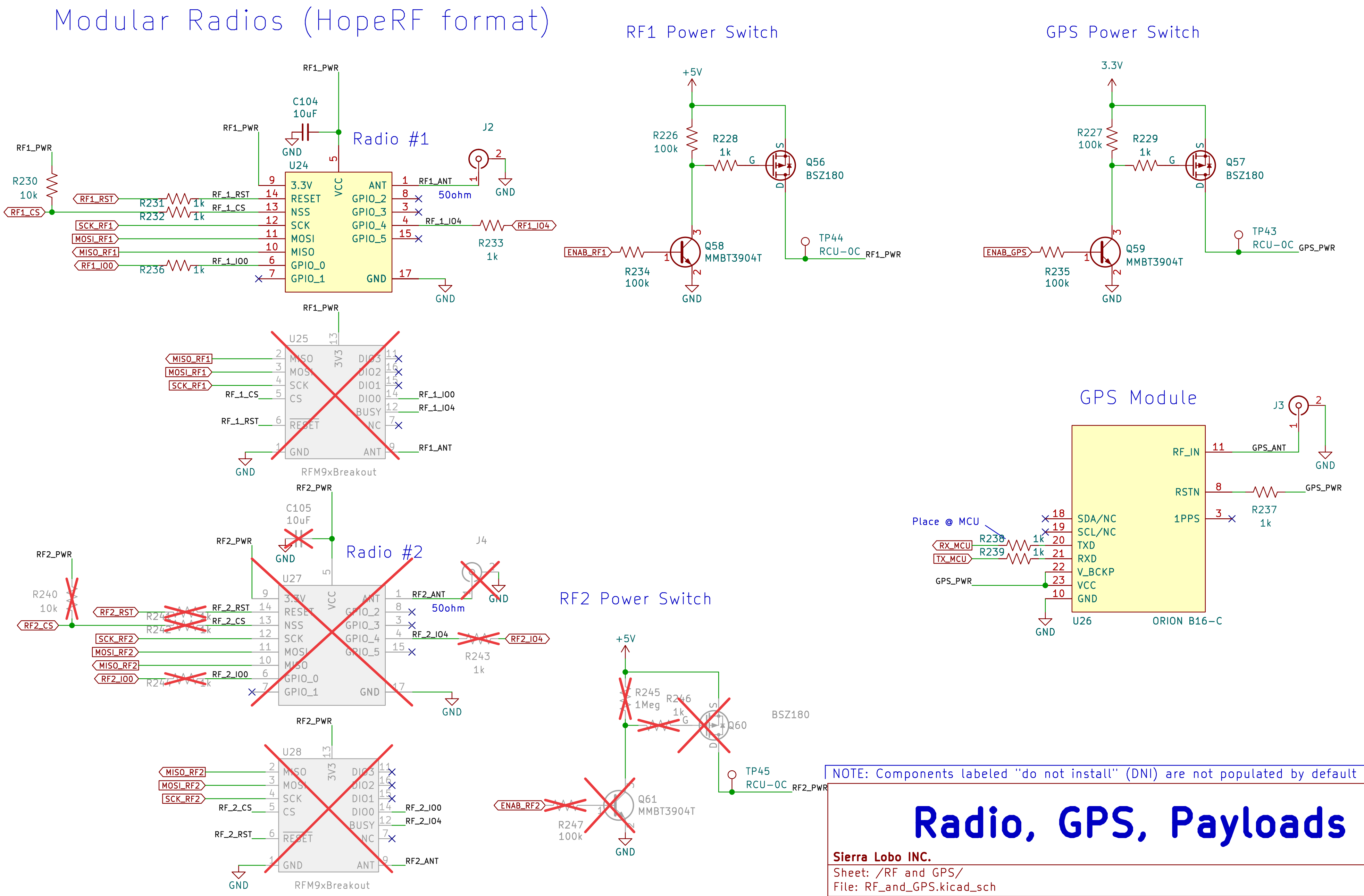
Bypass Jumper

Jumper Bypass N/R for MOSI
Inline 1k resistors @ destination offer passive protection

Sheet: /Bus Protection/SPI Protection 4/
File: spi_protection.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 7.0.1		Id: 25/34



NOTE: Components labeled "do not install" (DNI) are not populated by default

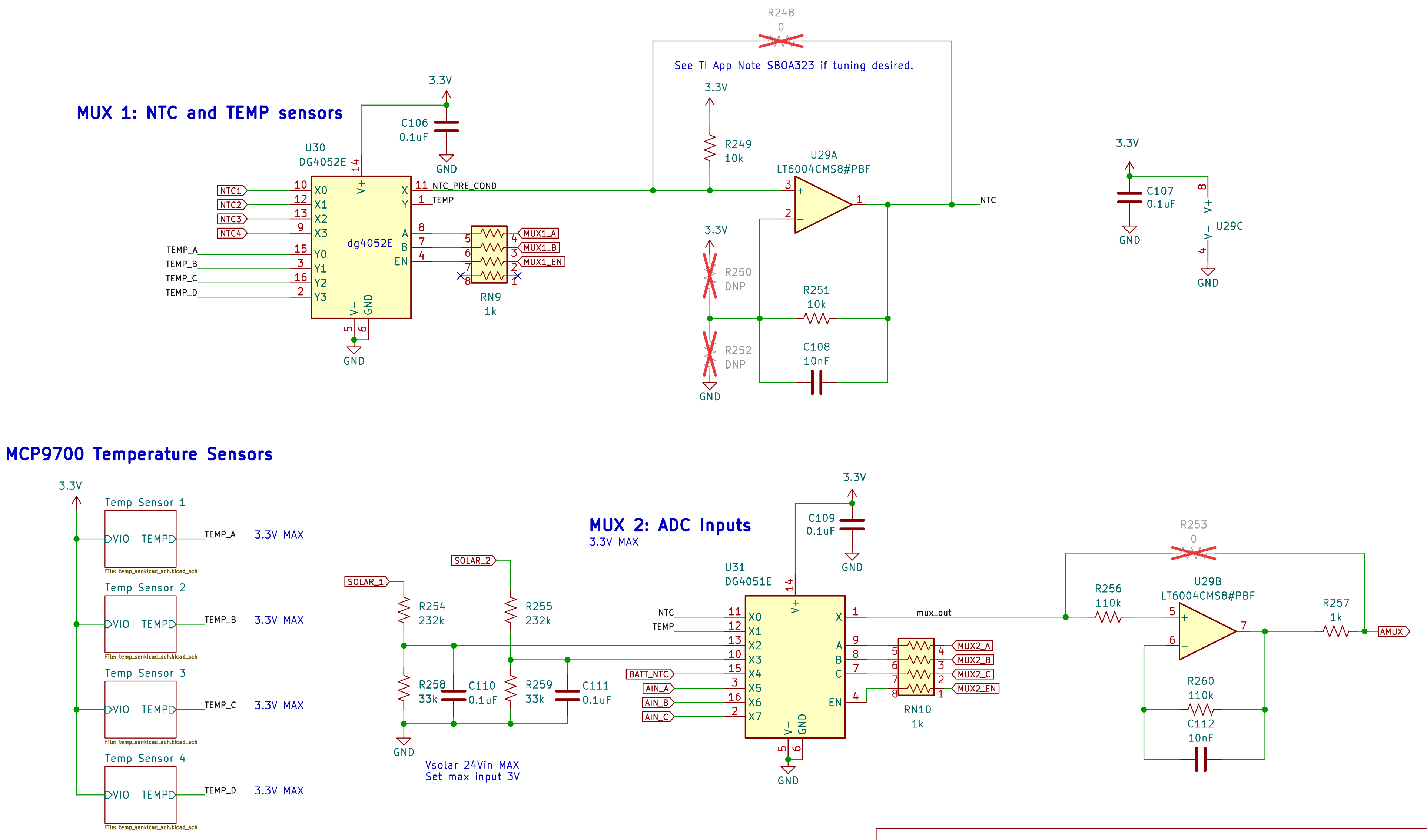
Radio, GPS, Payloads

Sierra Lobo INC.

Sheet: /RF and GPS/
File: RF_and_GPS.kicad_sch

Title: PyCubed Mainboard

Size: A4	Date: 2021-06-09	Rev: v05c
KiCad E.D.A. kicad 7.0.1		Id: 26/34

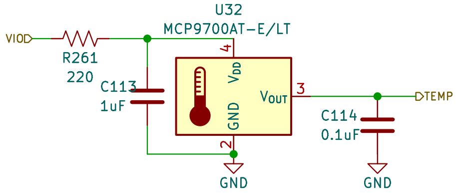


Sierra Lobo INC.

Sheet: /Analog Conditioning/
File: analog_cond.kicad_sch

Title:

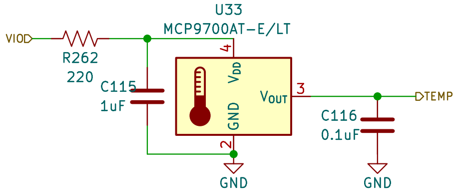
Size: A4	Date:	Rev:
KiCad E.D.A. kicad 7.0.1		Id: 27/34



Sheet: /Analog Conditioning/Temp Sensor 1/
File: temp_senkicad_sch.kicad_sch

Title:

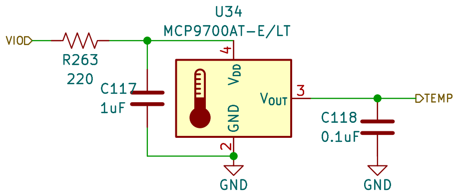
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 7.0.1		Id: 28/34



Sheet: /Analog Conditioning/Temp Sensor 2/
File: temp_senkicad_sch.kicad_sch

Title:

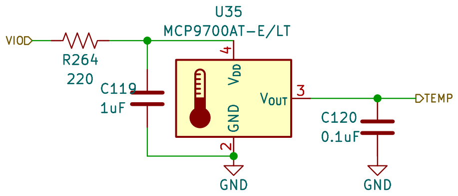
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 7.0.1		Id: 29/34



Sheet: /Analog Conditioning/Temp Sensor 3/
File: temp_senkicad_sch.kicad_sch

Title:

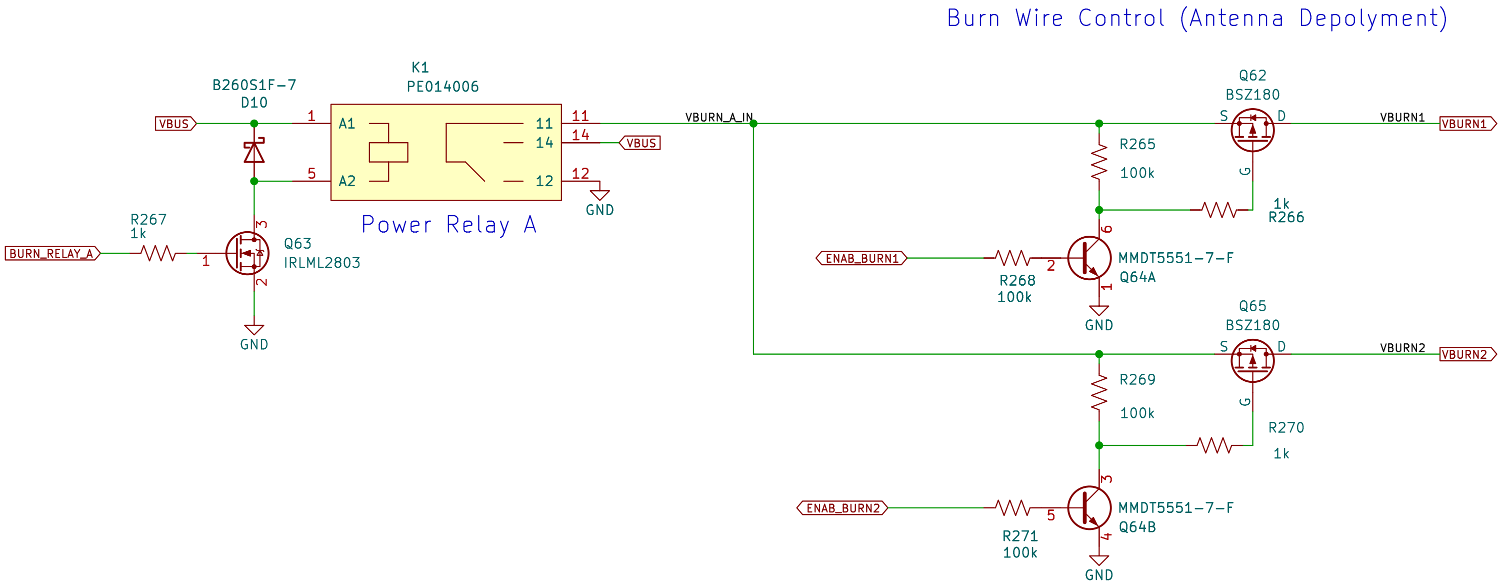
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 7.0.1		Id: 30/34



Sheet: /Analog Conditioning/Temp Sensor 4/
File: temp_senkicad_sch.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 7.0.1		Id: 31/34



NOTE: Components labeled "do not install" (DNI) are not populated by default

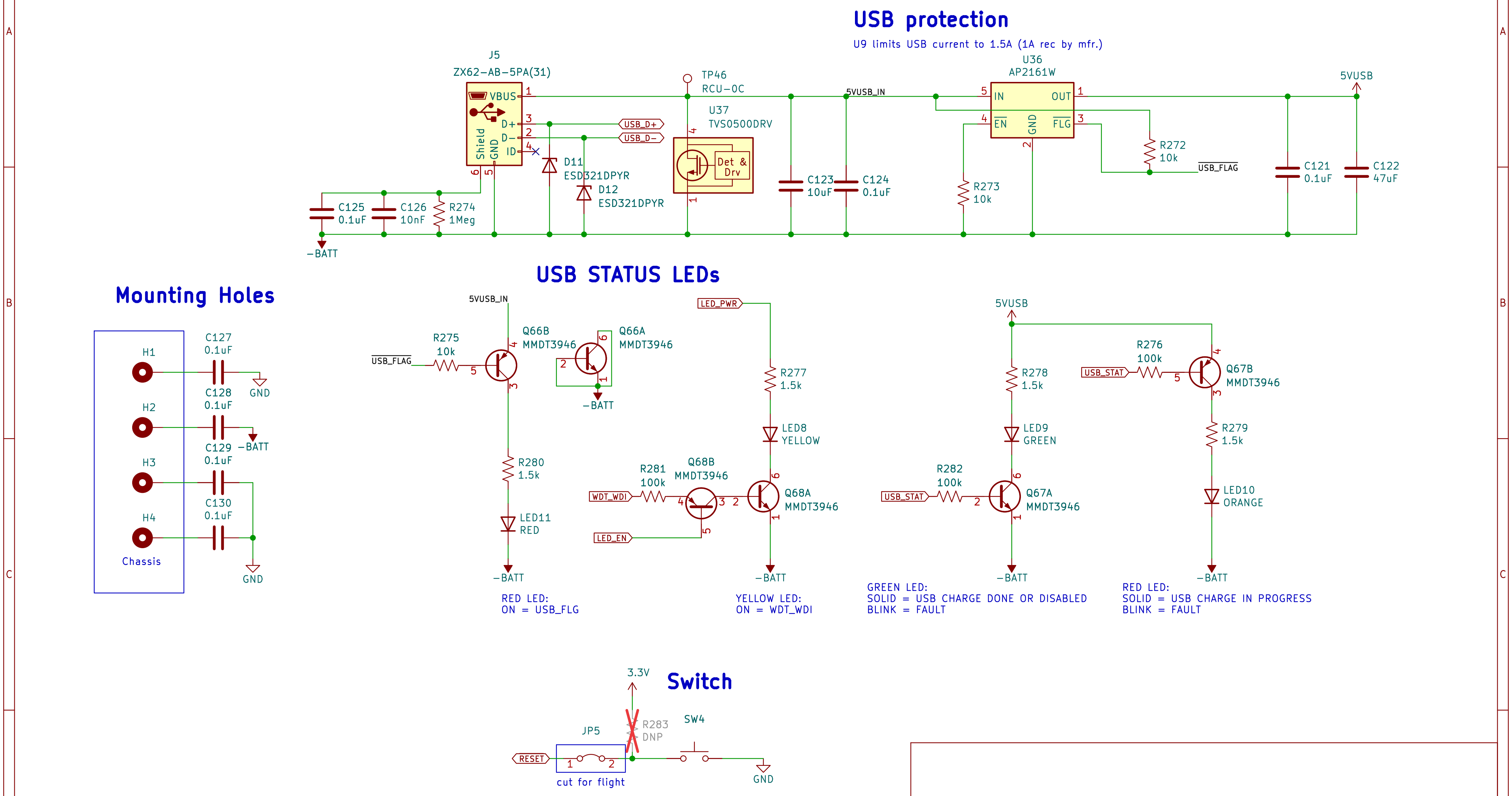
Burn Wires

Sierra Lobo INC.

Sheet: /Burn Wires/
File: Burn_Wires.kicad_sch

Title: PyCubed Mainboard

Size: A4	Date: 2021-06-09	**Rev: v05c**
KiCad E.D.A. kicad 7.0.1		Id: 32/34



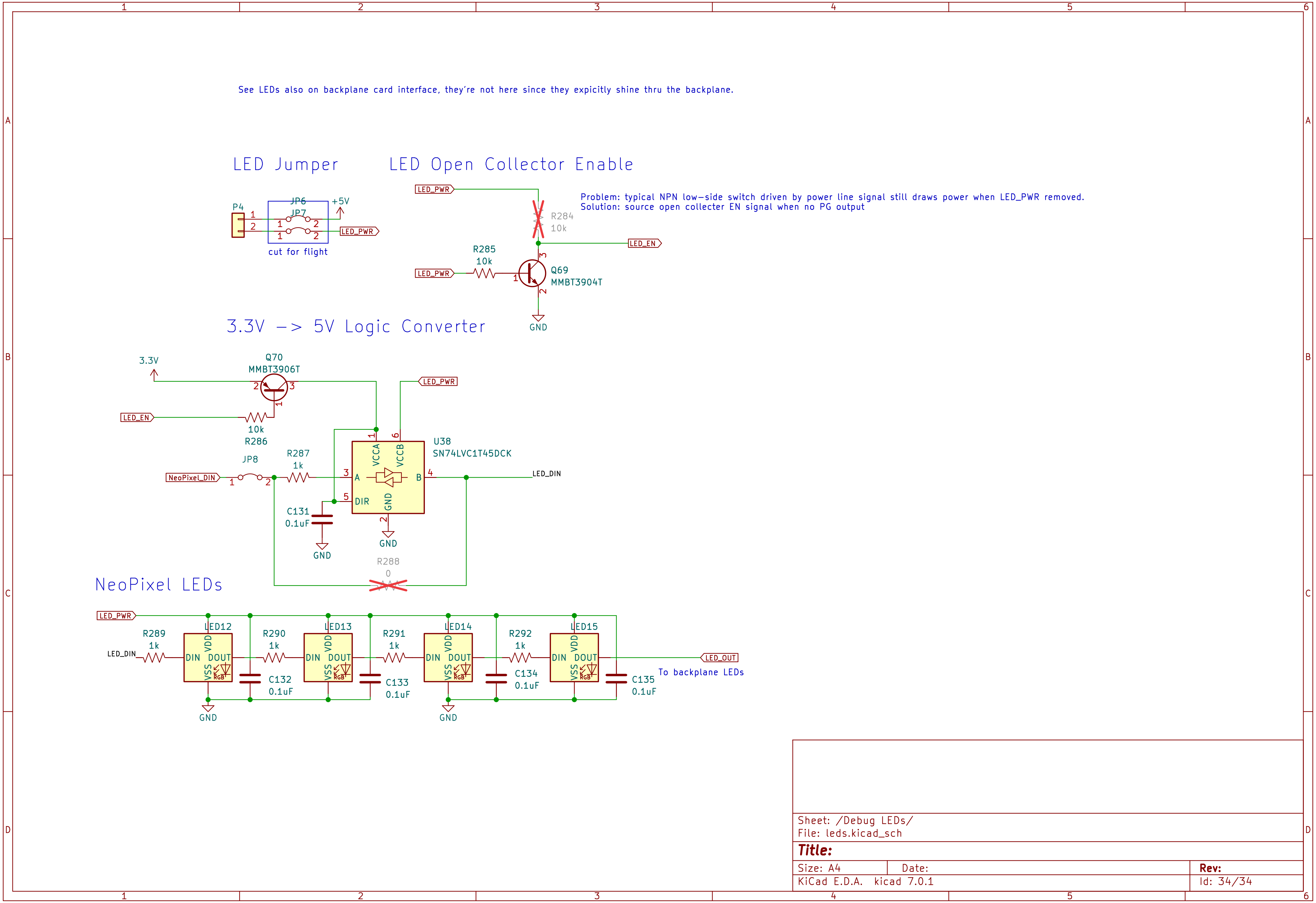
Sierra Lobo INC.

Sheet: /Backplane Interface/

File: Blank-Card-Default.kicad_sch

Title:

Size: A4	Date:	Rev:
KiCad E.D.A. kicad 7.0.1		Id: 33/34



See LEDs also on backplane card interface, they're not here since they expicitly shine thru the backplane.
LED Jumper
LED Open Collector Enable
P4
JP6
JP7
+5V
LED_PWR
cut for flight
Problem: typical NPN low-side switch driven by power line signal still draws power when LED_PWR removed.
Solution: source open collecter EN signal when no PG output
R284
10k
LED_EN
R285
10k
Q69
MMBT3904T
GND
3.3V -> 5V Logic Converter
3.3V
Q70
MMBT3906T
R286
10k
JP8
NeoPixel_DIN
R287
1k
U38
SN74LVC1T45DCK
VCCA
VCCB
DIR
GND
LED_DIN
C131
0.1uF
R288
0
NeoPixel LEDs
LED12
LED13
LED14
LED15
R289
R290
R291
R292
1k
DIN
DOUT
VDD
VSS
RGB
C132
C133
C134
C135
0.1uF
LED_OUT
To backplane LEDs
Sheet: /Debug LEDs/
File: leds.kicad_sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad 7.0.1
Id: 34/34