

**VENDOR ASSEMBLY NOTES:**

1. J-STD-001G Class 2
2. BOM provided with submitted files shall be the controlling document for component information.
3. Do not apply solder to pads of DNP components
4. Assemble with leaded solder.



**TECHNOLOGY DEVELOPMENT & ENGINEERING CENTER EAST**  
11401 HOOVER ROAD, MILAN, OHIO 44846

	TITLE
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mainboard

SIZE	B
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DWG NO.	
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REV
C

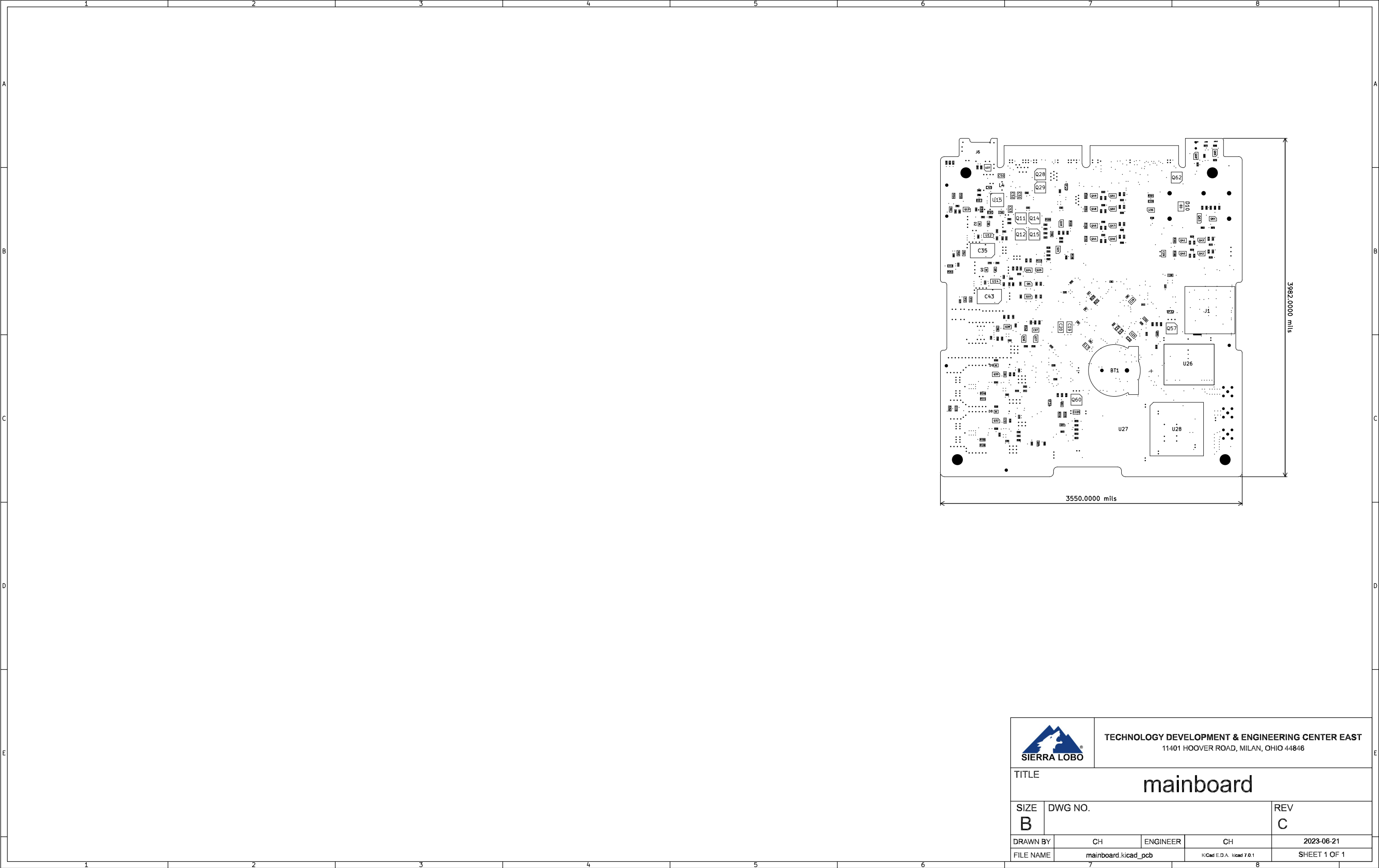
DRAWN BY


CH

ENGINEER
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KiCad E.D.A. kicad 7.0.1

SHEET 1 OF 1



 SIERRA LOBO®		TECHNOLOGY DEVELOPMENT & ENGINEERING CENTER EAST 11401 HOOVER ROAD, MILAN, OHIO 44846			
TITLE					
mainboard					
SIZE	DWG NO.			REV	
B				C	
DRAWN BY	CH	ENGINEER	CH	2023-06-21	
FILE NAME	mainboard.kicad_pcb		KiCad E.D.A. - kicad 7.0.1		SHEET 1 OF 1