United International University
Department of Computer Science and Engineering

CSE 1325: Digital Logic Design

Final Exam: Spring 2022 Time: 2 hours Marks: 40

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Answer Any Three Questions from Q1 to Q4

1. Design a synchronous counter to count the following arbitrary sequence using D flip flops and basic gates. [1.5+2.5+2+2]

   Sequence : $0 \to 2 \to 1 \to 4 \to 3 \to 7 \to 6 \to 0 \to 2 \to 1 \cdots$, The next number of the missing number 5 will be 0.

   (a) Draw the state Diagram

   (b) Find the state table with D flip flop inputs

   (c) Minimize the functions of flip flop inputs

   (d) Draw the circuit diagram using block Diagram of D flip flops and basic gates

2. Design a synchronous sequential circuit to recognize 1001 subsequences including overlaps in an input sequence $x = 001001001000100100$, which gives output $y = 000001001000000100$, Design the circuit using JK flip flop and basic gates. [2 + 2 + 2 + 2]

   (a) Draw the state Diagram by assigning state using gray code

   (b) Draw the state table with output and JK flip flop inputs

   (c) Minimize the functions of output and flip flop inputs

   (d) Draw the circuit diagram using block Diagram of JK flip flops and basic gates

3. A sequential circuit has two flip-flops (A and B), two inputs (x and y) and an output (z). The flip-flop input functions and the circuit output function are as follows:

   $J_A = xB + y'B'$, $K_A = xy'B'$, $J_B = xA'$, $K_B = xy' + A$ and $z = xyA + x'y'B$

   Obtain the logic diagram, state table and the state diagram. [8]

4. Design a 4 bit register with shift right and shift left operations using D flip flops and basic gates. There Is an asynchronous signal named RIGHT/LEFT, If this bit is 1, the operation will be RIGHT shift, otherwise it will be LEFT shift operation. There will be Serial Right Shift Input (SRI) and Serial Right Shift Output (SRO) for Right shift operation. At the same time there will be Serial Left Shift Input (SLI) and Serial Left Shift Output (SLO) for Left shift operation.The block diagram of the circuit is given in Figure 1(right). [8]

State		Inputs					
Present state	Next state	S	R	J	K	D	T
0	0	0	X	0	X	0	0
0	1	1	0	1	X	1	1
1	0	0	1	X	1	0	1
1	1	X	0	X	0	1	0

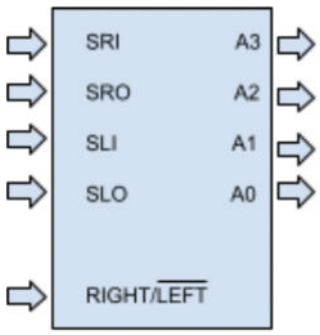

Figure 1: Excitation table for flip-flops (right) and block diagram for ripple register (right).

Answer Any Two Questions from Q5 to Q7

5. Consider a UIU alarm system with five inputs: fire (F-011), water-tank-full (W-001), burglary (B-100), smoke (S-111) and dust(D-010). For this alarm system an alarm signal (A) is on if any of these events occur a three bit code is shown to denote the incident. In case of multiple events, a priority is followed as: $F > B > S > D > W$. For this alarm system, find out the simplified expression of the alarm signal (A) and the encoding bits for the associated 5×3 priority encoder and draw the logic diagram. [8]

6. (a) Design a 16×1 multiplexer using 4×1 multiplexers only. Draw the logic diagram and show the working principle with an example. [4]

   (b) A combinational circuit is defined by the following Boolean function:

$$F = \overline{x + z} + xyz$$

   Design the circuit with a 2×1 MUX and a decoder (you can not use any other gates). [4]

7. (a) Implement a 3-to-8 decoder using two 2-to-4 decoders and a single NOT gate (you can not use any other gates). Label the decoder pin names and their inputs/outputs carefully. [4]

   (b) Consider a digital system with four binary bits as input and a single bit as output. The binary output is 1 if the number of 1s in the input is less than the number of 0s, otherwise the output is 0. Implement this system using a 8x1 MUX and a single NOT gate only (you can not use any other gates). [4]