United International University
Department of Computer Science and Engineering

CSE 1325: Digital Logic Design

Final Exam: Fall 2022 Time: 2 hours Marks: 40

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Answer Any Three Questions from Q1 to Q4

1. Design a synchronous sequential circuit to recognize **0100** subsequences including overlaps in an input sequence x = 0000010010011, which gives output y =0000000100100. Design the circuit using **D flip flop** and basic gates. [2+2+2+2]

   (a) Draw the state Diagram by assigning states.

   (b) Draw the state table with output and flip flop inputs.

   (c) Minimize the functions of output and flip flop inputs.

   (d) Draw the circuit diagram using block Diagram of D flip flops and basic gates.

2. A sequential circuit has two **JK flip-flops** (A and B), two inputs (X and Y) and an output (Z). The flip-flop input functions, and the circuit output function are as follows: [3+3+2]

$$J_A = X \oplus B, K_A = Y \oplus A$$

$$J_B = Y \oplus B, K_B = X \oplus A$$

$$Z = (X \oplus Y).(A \oplus B)$$

   (a) Draw the logic diagram of the circuit.

   (b) Derive the state table.

   (c) Derive the state diagram.

3. Design a 4-bit sequential circuit which can do the following operations based on the two control inputs A and B as given below. You can use any kind of flip-flops and other necessary gates as required. Draw a neat logic diagram of your solution. [8]

A	B	Operation
0	0	Parallel Load
0	1	Up Count
1	0	Down Count
1	1	No change

4. In mathematics, the Fibonacci numbers form a sequence, the Fibonacci sequence, in which each number is the sum of the two preceding ones. The sequence commonly starts from 0 and 1. The first few values of the sequence are 0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144. Now design a synchronous counter for counting the following Fibonacci sequence using the **T flip-flop** and basic gates. [2+2+2+2]

Sequence:$1 \Rightarrow 2 \Rightarrow 3 \Rightarrow 5 \Rightarrow 8 \Rightarrow 13 \Rightarrow 1 \Rightarrow 2 \Rightarrow \ldots\ldots\ldots\ldots$

Q-4 continued....

(a) Draw the State Diagram.

(b) Find the State Table with T flip-flop inputs.

(c) Minimize the functions of T flip-flop inputs.

(d) Draw the logic diagram using T flip-flops and basic gates.

Answer Any Two Questions from Q5 to Q7

5. Consider a system which indicates the damaged part of a laptop. There are six possible events here: fan damaged (F-101), keyboard damaged (K-111), speaker damaged (S-011), track-pad damaged (T-001), ethernet port damaged (E-010) and USB port damaged (U-100). Here, the first letter is the input and the three bits are the output. For example, in T-001, T is the input and 001 is the output. To maintain priority during the occurrence of multiple events at the same time, the priority sequence is: $F > K > D > E > U > T$. Design an encoder that can encode the events based on given priority. [3+3+2]

   You have to answer the followings:

   (a) Derive the truth table of the priority encoder including the valid bit.

   (b) Derive the Boolean expressions for all the outputs.

   (c) Draw the logic diagram using basic gates.

6. (a) Implement the following Boolean function using a 4:1 MUX (you can only a number of 4:1 Mux) and necessary basic gates. [4]

$$F(A, B, C, D) = \sum m(0, 1, 4, 6, 9, 12, 14)$$

   (b) Draw the diagram of a parallel adder to perform addition of the numbers $(11)_8$ and $(6)_8$. First, you need to determine the size of the required parallel adder (i.e. ripple carry adder). After that, you need to draw the diagram and show the process to add the two numbers that are given. [4]

7. (a) You have to build a circuit with 3-bits number (A, B, C) as input and 2-bits number (X, Y) as output. [4]

   - If the total number of ones in the input bit is even then X will be '0' else X will be '1'. For example, if input is "101" then the X will be '0'
   - If the decimal equivalent of the input is odd then Y will be '0' else Y will be '1'. For example, if the input "101" then Y will be '1'.

   Implement the circuit using decoder of your choice and OR gates only.

   (b) Design D flip flop using i) JK flip flop and ii) T flip flop. [4]