United International **University (UIU)**

Department of Computer Science and Engineering

CSE 1325: DIGITAL LOGIC DESIGN, Final Fall 2023

Total Marks: **40** Duration: 2 hours

Answer ALL Questions

1. You have designed a new flip-flop named **X** and the excitation table for **X** flip-flop is as follows:

Q(t)	Q(t+1)	X
0	0	1
0	1	0
1	0	0
1	1	1

You want to design a sequential circuit using the **X** flip-flop, which could recognize the sequence **0101**. While designing the circuit, consider the overlaps of the sequence. The sequential circuit will give output "**1**" when the given sequence is recognized, otherwise will provide output "**0**".

For such a circuit, complete the following steps:

A. Draw the state diagram while assigning the following coding to the states: [2]
   1^{st} state is coded as **00**, 2^{nd} state as **01**, 3^{rd} state as **11**, and 4^{th} state as **10**

B. Draw the state table with output and input function for **X** flip-flop. [2]

C. Minimize the functions of output and flip-flop inputs. [2]

D. Based on the designed sequential circuit, provide the outputs for the following input sequences: [2]

   i) 000100101011

   ii) 010110100101

2. Design a synchronous counter to count the following arbitrary sequence using JK flip flops and basic gates.

Sequence : $5 \rightarrow 3 \rightarrow 1 \rightarrow 2 \rightarrow 4 \rightarrow 6 \rightarrow 5 \rightarrow \cdots$. Here, the next sequence of the missing numbers 0 is 2, and for missing number 7 the next sequence is 5.

A. Draw the state Diagram [1.5]

B. Find the state table with JK flip flop inputs [2.5]

C. Minimize the functions of flip flop inputs [2]

D. Draw the circuit diagram using block Diagram of JK flip flops and basic gates [2]

3. Design a 3-bit universal shift register with the functions given in the function table below. Here two control bits P and Q determine the mode of operation. Use D Flip Flops for your design. [4]

P	Q	Operation
0	0	Parallel Load
0	1	Clear Register to 0
1	0	Toggle
1	1	Shift Left

4. It's the last week of classes before the finals at UIU and you have so many tasks at hand! Class tests, quizzes, lab tests, assignment submissions, and whatnot! When you have a lot of tasks, the best way to get to them (without getting overwhelmed!) is based on their order of priority.

You thought a specialized alarm system could be quite helpful. You'll put in the first letter of the tasks you may have (given below) as the input and a priority encoder will give a 3-bit output. Here is the list of tasks with their input-output labels and priority:

Priority	**Task**	**Input-Output**
1 (highest)	Project Submissions	P-010
2	Class Tests	C-011
3	Lab Tests	L-111
4	Quizzes	Q-001
5 (lowest)	Assignment Submissions	A-110

Now, design a priority encoder that would work as your personal task manager and alarm system for this hectic week. To do it, complete the following steps:

A. Derive the truth table of the priority encoder including the valid bit. [3]
B. Derive the Boolean expressions for all the outputs. [3]
C. Draw the logic diagram using basic gates. [2]

5 Suppose you are designing an access control system for a secure facility. The system uses keycards with embedded codes. There are 3 security guards in the facility and each have a keycard that is encoded with a 3 bit unique identifier. The keycards are shown below: [4]

The access control system is only enabled from 8:00 am to 3:00 pm. That means even if the guards try to enter the facility at night, the control system won't be able to give them access. Design a combinational circuit that has an active low enabler or inverted output that recognizes the unique identifier on the keycard and grants access only to authorized individuals using decoder and NAND gate. Show the truth table and logic circuit using decoder block diagram.

6 Design a Hexadecimal to Binary Encoder. [4]

A. Draw the function table
B. Write the equations for the output of your encoder.
C. Draw the logic diagram of the encoder

7 Implement the following Boolean function using a 4:1 MUX and necessary basic gates. [4]

$$F(A,B,C,D) = \Pi_M(1,2,3,4,5,11,12,15)$$

Excitation Tables for different Flip-Flops

Q(t)	Q(t+1)	D	Operation
0	0	0	Reset
0	1	1	Set
1	0	0	Reset
1	1	1	Set

Q(t)	Q(t+1)	J	K	Operation
0	0	0	x	No change/reset
0	1	1	x	Set/complement
1	0	x	1	Reset/complement
1	1	x	0	No change/set