United International University (UIU)
Dept. of Computer Science& Engineering (CSE)

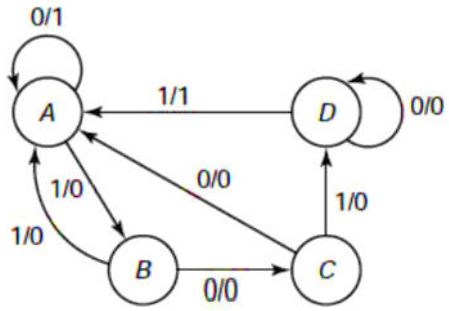
Final Exam. Trimester: Summer 2020

Course Code: CSE 1325, Course Title: DIGITAL LOGIC DESIGN

Total Marks: **25** Duration: 1 hour 15 minutes + 15 minutes (for uploading)

Answer any 3 Questions from Q1 to Q4 [3 × 5 = 15]

1. Design a sequential circuit for the given state diagram using **D flip-flops**. You must show [5]
   (a) flip-flops' input table
   (b) K-map minimizations of inputs and output
   (c) the logic diagram



Flip-Flop Excitation Tables

(a) JK Flip-Flop

Q(t)	Q(t + 1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

2. Using **J-K flip-flops**, design a synchronous counter that goes through the sequence, 3, 5, 6, 7, 1, 4 … and repeat. You have to show [5]
   (a) the flip-flops' input table
   (b) flip-flops' input equations
   (c) the logic diagram.

3. A sequential circuit with two D flip-flops A and B, one input X, and one output Z is specified by the following equations: [5]

$$D_A = \bar{B}X + AX, \quad D_B = \bar{A}X, \quad Z = AB$$

   (a) draw the logic diagram of this circuit
   (b) derive the state table and
   (c) draw the state diagram.

4. Design a 4-bit ripple counter with two control bits C and D. The circuit counts up when the control variable C is logic 'HIGH' and counts down when C is logic 'LOW'. The circuit will work only if $D = 1$ and remains unchanged if $D = 0$. [5]

Answer any 2 Questions from Q5 to Q7 [2 × 5 = 10]

5. Design a 4-input Priority Encoder with inputs D_0, D_1, D_2, D_3 and outputs Y_1, Y_0. Y_1 and Y_0 are the two bits representing the binary equivalent of the inputs Ds. For example, D_0 is encoded to 00, D_1 to 01 and so on. [5]

   (a) Derive the truth table of the priority encoder where priority is set according to the following sequence of priority from highest to lowest $D_1 > D_3 > D_0 > D_2$.
   (b) Derive the Boolean expressions for Y_1 and Y_0.
   (c) Draw the circuit diagram.

6. a) Is it possible to use a 16 × 1 MUX as a 4 × 1 MUX? Explain your answer with necessary diagram. [2]
   b) Implement a 3 × 8 line decoder using 1 × 2 line decoders only. [3]

7. (a) Implement the following Boolean function using a 8×1 line multiplexer and other basic gates. [2]

$$F(A, B, C, D) = \prod M\,(0, 2, 3, 7, 9, 13, 14, 15)$$

(b) Suppose you have to build a circuit with a 4-bit number as input and 2 output bits, O_1 and O_0. [3]

- If the input number is even, O_1 will be '1' otherwise it will be '0'.
- If the input number is divisible by 6, O_0 will be '1' otherwise it will be '0'.

Implement this circuit using a single decoder of your choice and OR gates only.