United International University
Department of Computer Science and Engineering
CSE 1325: Digital Logic Design, Final Assessment, Spring 2021
Total Marks: 40
Time: 1 hour 30 minutes + 15 minutes (for uploading)

"Any examinee found adopting unfair means will be expelled from the trimester / program as per UIU disciplinary rules."

Answer all of the questions from 1 to 5

1. Design a sequential circuit that can recognize the sequence 1010 using JK flip flop. You have to find the followings: [8]
   i) State diagram.
   ii) State table with Flip-flop inputs.
   iii) K-map minimization of input and outputs.

2. **a)** Consider a system which indicates which part of a laptop is damaged. There are six possible events here: fan damaged (F-001), keyboard damaged (K-111), speaker damaged (S-010), track-pad damaged (T-101), ethernet port damaged (E-011) and USB port damaged (U-100). Here, the first letter is the input and the three bits are the output. For example, in **F-001**, F is the input and **001** is the output. To maintain priority during the occurrence of multiple events at the same time, the priority sequence followed is $F > K > T > E > U > S$. Design an encoder that can encode the events based on given priority.You have to answer the followings: [5]

   i) Derive the truth table of the priority encoder including valid bit.
   ii) Derive the Boolean expressions for all the outputs.

   b) Design a 3 bit asynchronous down counter with positive edge triggered JK Flip flops. [3]

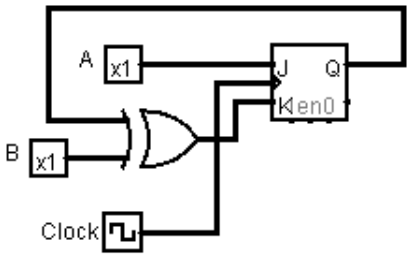
3. **a)** Describe the undefined or race condition of SR latch with an example circuit. [3]

   b) Implement $F(A, B, C) = \Pi_M(1, 3, 5, 6)$ using one 2-to-1 line mux and logic gates. Draw truth table and logic diagram. [5]

4. **a)** Design a logic function that will take a 4 bit binary number as input and output if the total number of 1 in input is greater than 2 or not. For example, if input is 0011, then output is 0, if input is 0111, output is 1. Now implement this fucntion with 4x1 MUX. You can use more than one 4x1 MUX but you can't use any basic gates(AND,OR,XOR,NOT etc).

   (i) Draw the truth table [4]
   (ii) Draw the logic diagram [4]

5. **a)**You are analyzing the output of the following circuit with one JK Filp flop and two inputs A and B. Assume the initial output Q = 1. [3]



What will be value of Q and name of the operation(Set/Reset/Complement/Unchanged) if you give the following three inputs to the circuit one after another and why?

(i) Clock = 1, A = 1 and B = 0

(ii) Clock = 0, A = 1 and B = 0

(iii) Clock = 1, A = 1 and B = 0

b) Implement $F(A, B, C) = \Pi_M(0, 1, 5, 6, 7)$ using 2-to-4 line active high decoders and basic gates. Draw the logic diagram with proper symbols. [5]