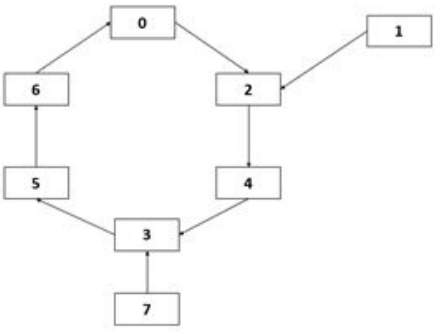
United International University
Department of Computer Science and Engineering
CSE 225 / CSE 1325: Digital Logic Design, Final Exam, Fall 2019
Total Marks: 40, Time: 2:00 Hours

Section A: Answer both of the questions, Question 1 and Question 2.

1. Design a sequential circuit that can recognize the pattern 1100. Use J-K flip flops for your design. You must show state diagram, state table, flip-flop input functions, k-map minimizations of output and circuit diagram. [2+2+2+2=8]

2. Design an arbitrary synchronous counter circuit that counts the sequence given in Figure 1(a). You must show state table, flip-flop input functions, k-map minimizations of output and circuit diagram. You can use any type of flip-flop. [2+2+2+2=8]



(a)

SR Flip-flop

Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

D Flip-flop

Q(t)	Q(t+1)	DR
0	0	0
0	1	1
1	0	0
1	1	1

JK flip-flop

Q(t)	Q(t+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

T flip-flop

Q(t)	Q(t+1)	DR
0	0	0
0	1	1
1	0	1
1	1	0

(b)

Figure 1: (a)Sequence diagram for Question 2 and (b) Excitation table for different FlipFlops.

Section B: Answer any one of the Question 3 and Question 4.

3. A sequential circuit with two D flip- flops (Q is the flipflop output and D is the flipflop input), one input Y, and one output Z is specified by the following input equations:

$$D_1 = Q_2Y + \overline{Q_1}Y, D_2 = \overline{Y}, Z = \overline{Q_1Q_2}$$

For this circuit, i) draw the logic diagram, ii) derive the state table and iv) draw the state diagram. [2+3+3=8]

4. Design a 4-bit register that can perform shift right or shift left based on a control bit C. If C=0, the register will shift right and if the control bit C=1, the register will shift left. [8]

Section C: Answer any two of the Question 5,6 and 7.

5. Design a 4-input Priority Encoder with inputs D0,D1,D2,D3 and outputs Y1,Y0. Y1 and Y0 are the two bits representing the binary equivalent of the inputs Ds. For example D0 is encoded to 00, D1 to 01 and so on. Derive the truth table of the priority encoder where priority is set according to the following sequence of priority from highest to lowest D0>D1>D3>D2. Derive the Boolean expressions for Y1 and Y2 and draw the circuit diagram. [8]

6. (a) Implement the following Boolean function using a 4-to-1 line multiplexer and other necessary gates. [5]

$$F(A, B, C, D) = \prod M(1, 2, 4, 7, 8, 9, 12, 13, 14, 15)$$

   (b) Implement a 2-to-4 line decoder using 1-to-2 line decoders only. [3]

7. (a) Design a 16:1 MUX using 4:1 MUX (as many as you require) only. [4]

   (b) A majority function has an output value of 1 if there are more 1s than 0s on its inputs. The output is 0 otherwise. On the other hand, a parity function gives output 0 if there are even number of 1s and output 1 if there are odd number of 1s. You have to implement both of the functions using a single decoder and OR gates only. Consider 3-bit input. [4]