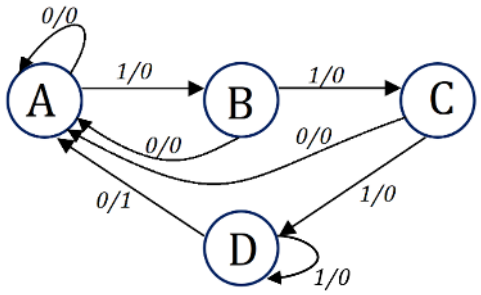
United International University
Department of Computer Science and Engineering
CSE 1325: Digital Logic Design, Final Assessment, Summer 2021
Total Marks: 25
Time: 1 hour 15 minutes + 15 minutes (for uploading)

"Any examinee found adopting unfair means will be expelled from the trimester / program as per UIU disciplinary rules."

Answer all of the questions from 1 to 5

1. The state diagram for recognizing a particular sequence of bits is given below:



   i) Identify and write the sequence that's being recognized. Suppose an input bit stream "01110111110" is given to this system. What will be the output stream? [1]
   iii) Complete the design of this sequence recognizer using D Flip flops by drawing the state table with Flip-flop's excitation inputs. [3]
   (b) Show the K-map minimization of input and output functions. [2]

2. Design a 3 bit synchronous up-down counter with two control bits C and D. The circuit counts up when the control variable $C = 1$ and counts down when $C = 0$. Also, the circuit will work if $D = 1$ and remains unchanged if $D = 0$. You can't use more than three negative edge triggered JK Flip flops. Only draw the logic diagram with appropriate labels [5]

3. Design a function that will take a 3 bit binary number as input and the output will be "HIGH" if total number of 1s in input is less than or equal to total number of 0s and "LOW" otherwise. Now implement this fucntion with 2x1 MUX. You can use more than one 2x1 MUX if necessary but you can't use any basic gates(AND,OR,XOR,NOT etc).
   (i) Draw the truth table [2]
   (ii) Draw the logic diagram [2]

4. **a)** Design a decimal to excess-3 encoder which can only take 3 bits of input. Derive the truth table and the boolean expression for all the outputs. No need to draw logic diagram. [3]

(b) In a clocked SR NOR latch, why do we use two AND gates in front of the two NOR gates? Give proper reason with a short example. [2]

5. **a)** Why JK Flip flop is designed in master-slave fashion? Explain your reason properly with an example diagram. [3]

   b) Implement the following two functions using 2-to-4 decoders.

$$F(A, B) = \Pi_M(0, 1)$$
$$F(X, Y) = \sum_m(0, 1)$$

   (i) Draw the logic diagram with proper symbols. [1]

   (ii) Can you complete the design with a single decoder? Why or why not? [1]