



United International University (UIU)

Department of Computer Science and Engineering CSE 225: DIGITAL LOGIC DESIGN, Final Summer 2019

Total Marks: **40**

Duration: 2 hour

Section A: Answer both of the Questions, 1 and 2.

1.	Using J-K flip-flops , design a synchronous counter that goes through the sequence 1, 4, 3, 6, 7, 0, 5 ... and repeat. You have to show (a) the flip-flops' input table, (b) equations and (c) the logic diagram.	<table><tr><th colspan="4">(a) JK Flip-Flop</th></tr><tr><th>Q (t)</th><th>Q (t + 1)</th><th>J</th><th>K</th></tr><tr><td>0</td><td>0</td><td>0</td><td>X</td></tr><tr><td>0</td><td>1</td><td>1</td><td>X</td></tr><tr><td>1</td><td>0</td><td>X</td><td>1</td></tr><tr><td>1</td><td>1</td><td>X</td><td>0</td></tr></table>	(a) JK Flip-Flop				Q (t)	Q (t + 1)	J	K	0	0	0	X	0	1	1	X	1	0	X	1	1	1	X	0	[3+ 3+ 2]
(a) JK Flip-Flop																											
Q (t)	Q (t + 1)	J	K																								
0	0	0	X																								
0	1	1	X																								
1	0	X	1																								
1	1	X	0																								
2.	Using D flip-flops , design a sequence recognizer that can recognize the sequence, "0110". You have to show (a) state diagram, (b) the flip-flops' input table, (c) equations and (d) the logic diagram.	[2x4]																									

Section B: Answer any two of the Questions from 3, 4 and 5.

3.	<p>(a) Implement a 3-to-8 decoder using two 2-to-4 decoders and a single NOT gate. Label the decoder pin names and their inputs/outputs carefully.</p> <p>(b) Consider a digital system with four binary bits as input and a single bit as output. The binary output is 1 if the number of 1s in the input is less than the number of 0s, otherwise the output is 0. Implement this system using a 8x1 MUX and a single NOT gate only.</p>	[4+4]
4.	<p>(a) Design a 16x1 multiplexer using 4x1 multiplexers only. Draw the logic diagram and show the working principle with an example.</p> <p>(b) A combinational circuit is defined by the following Boolean function:</p> $F = \overline{x} + \overline{z} + xyz$ <p>Design the circuit with a 2x1 MUX and a decoder (you can not use any other gates).</p>	[4+4]
5.	<p>Consider a UIU alarm system with five inputs: fire (F-011), water-tank-full (W-001), burglary (B-100), smoke (S-111) and dust(D-010). For this alarm system an alarm signal (A) is on if any of these events occur a three bit code is shown to denote the incident. In case of multiple events, a priority is followed as: F>B>S>D>W. For this alarm system, find out the simplified expression of the alarm signal (A) and the encoding bits for the associated 5x3 priority encoder and draw the logic diagram.</p>	[8]

Section C: Answer any one Question from 6 and 7.

6.	<p>A sequential circuit with two D flip-flops A and B, two inputs X and Y, and one output Z is specified by the following input equations:</p> $D_A = BY + \bar{A}Y, D_B = \bar{Y}, Z = \overline{AB}$ <p>(a) Draw the logic diagram of the circuit. (b) Derive the state table. (c) Derive the state diagram.</p>	[3+2+2]
7.	<p>(a) Design a 3-bit ripple up counter using negative edge triggered D-flipflops. You have to draw a neat logic diagram and label all the pins accordingly.</p> <p>(b) Design a 4-bit shift left register using any type of flip-flop. You have to draw a neat logic diagram and label all the pins accordingly.</p> <p>(c) There are four types of flip-flops: S-R, J-K, D and T. Which do you prefer to use in your designs and why?</p>	[3+3+2]