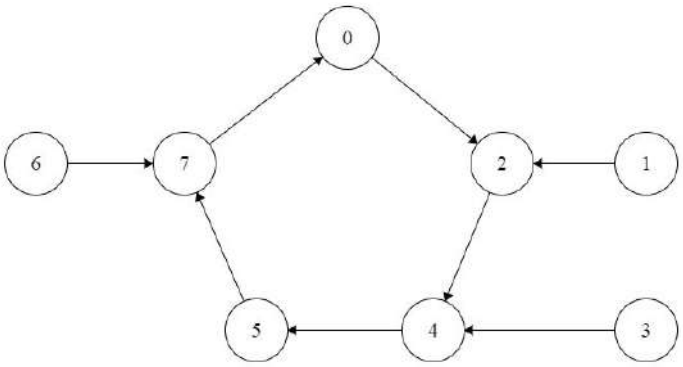
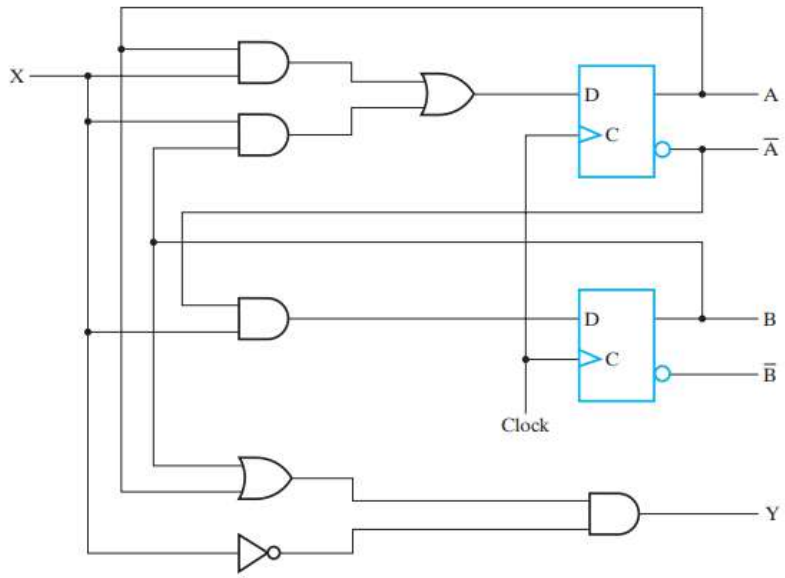
United International University (UIU)

Department of Computer Science and Engineering

CSE 1325: DIGITAL LOGIC DESIGN, Midterm Spring 2023

Total Marks: **40** Duration: 2 hours

Answer ALL Questions

1.	Design a clocked sequential circuit that recognizes the 4-bit input sequence 1111, including overlap. Design the circuit using D Flip-Flops. You have to show the following: A. The state diagram B. The flip-flop input table C. The simplified equation(s) for the flip-flop input(s) and the output(s) D. The final circuit diagram E. Suppose an input bit stream "011110100111111011" is given to this system. What will be the output stream?	[2] [1.5] [1.5] [1.5] [1.5]
2.	A. Find the state table with T/JK flip flop inputs. B. Minimize the functions of flip flop inputs. C. Draw the circuit diagram using T/JK flip flops and basic gates 	[3] [3] [2]
3.	 From the above circuit, you have to show the following: A. Boolean expressions for the inputs of each flip-flops and the output. B. The state table. C. The state diagram.	[3] [3] [2]

4.	Implement the following Boolean function using a 4-to-1 multiplexer. $$F(A,B,C,D) = \sum m\,(1,3,5,7,9,13,14,15)$$ Draw the logic diagram with proper labelling of input lines and selection pins.	[4]
5.	Design a 4-to-16 decoder with enable using 1-to-2 and 3-to-8 decoders only. You cannot use any gates.	[4]
6.	A calling bell system is required to be developed for an IT office consisting of a manager, a project lead, a senior engineer, a junior engineer, and an intern. The priority of the calling bell system should be determined in the following order: manager (highest priority), project lead, senior engineer, junior engineer, and intern (lowest priority). Your task is to design a priority encoder for the calling bell system, ensuring the correct prioritization of the five individuals mentioned, based on their respective input signals. The corresponding input pin labels and output signals for each individual are as follows: Manager (M-101), Project Lead (L-111), Senior engineer (S-000), Junior Engineer (J-100), and Intern (I-110). A. Construct the truth table for the given priority encoder including valid bit. B. Derive the Boolean expressions for each output signal along the valid bit. C. Draw the implementation diagram.	[3] [3] [2]

Q(t)	Q(t+1)	J	K	Operation
0	0	0	x	No change/reset
0	1	1	x	Set/complement
1	0	x	1	Reset/complement
1	1	x	0	No change/set

Q(t)	Q(t+1)	T	Operation
0	0	0	No change
0	1	1	Complement
1	0	1	Complement
1	1	0	No change