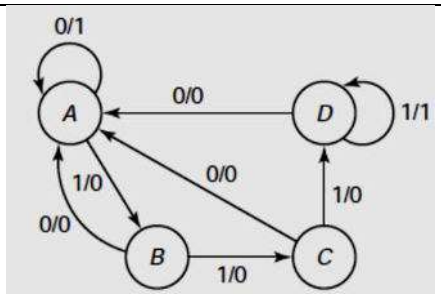
United International University (UIU)

Department of Computer Science and Engineering

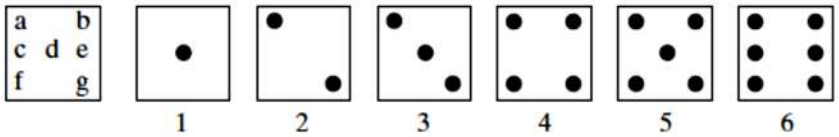
CSE 225: DIGITAL LOGIC DESIGN, Midterm Fall 2018

Total Marks: **40** Duration: 2 hour

Section A: Answer <u>both</u> of the Questions, 1 and 2.

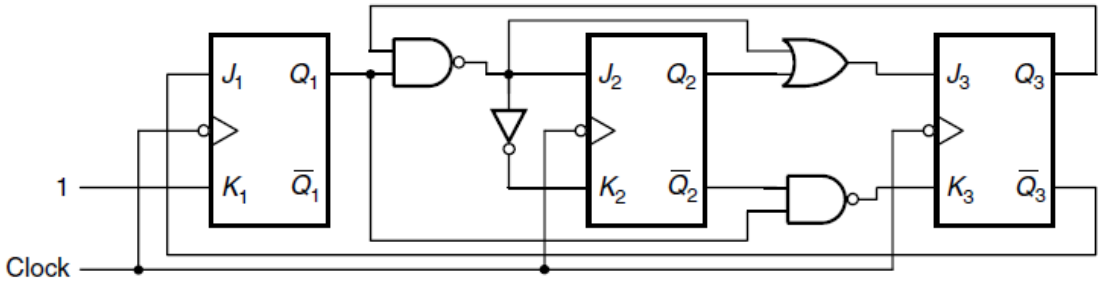
1.	For the given state diagram, find out (a) the flip-flops' input table, (b) equations and (c) the logic diagram when **J-K flip-flops** are being used **(a) JK Flip-Flop** $Q(t)$ | $Q(t+1)$ | J | K 0 | 0 | 0 | X 0 | 1 | 1 | X 1 | 0 | X | 1 1 | 1 | X | 0 	[3+ 3+ 2]
2.	Using **D flip-flops**, design a synchronous counter that goes through the sequence, 7, 4, 3, 6, 1, 2 … and repeat. You have to show (a) the flip-flops' input table, (b) equations and (c) the logic diagram.	[3+ 3+ 2]

Section B: Answer <u>any two</u> of the Questions from 4, 5 and 6.

3.	A) An electronic game uses an array of seven LEDs (light-emitting diodes) to display the results of a random roll of a die. Use a 3–to–8-line decoder and OR gates to map the 3-bit combinations on inputs X_2, X_1, and X_0 for values 1 through 6 to the outputs **a** through **g**. Input combinations 000 and 111 are don't-cares.  B) Construct a 1-bit full adder using two 1-bit half adders.	[6] [2]
4.	A) Implement the following Boolean function F with an 8-to-1 line multiplexer and necessary basic logic gates. $F(A, B, C, D)=\sum m(0, 2, 4, 5, 7, 9, 10, 11, 15)$ B) Design a 3-to-8 active low decoder using 2-to-4 active low decoder. Label the decoder pin names and their inputs/outputs carefully.	[5] [3]
5.	A) Design an 8-to-1 multiplexer using 4-to-1 multiplexer and 2-to-1 multiplexer. B) Design an Octal-to-Binary encoder. Show the function table and the equations only. C) Design a 6-bit full adder using multiple 2-bit full adders. Show the diagram only.	[3] [3] [2]

Section C: Answer <u>any one</u> Question from7 and 8.

6. A) What sequence should be repeated for the sequential circuit of the following Figure for the following initial state **$Q_3Q_2Q_1$: 001**? [6]



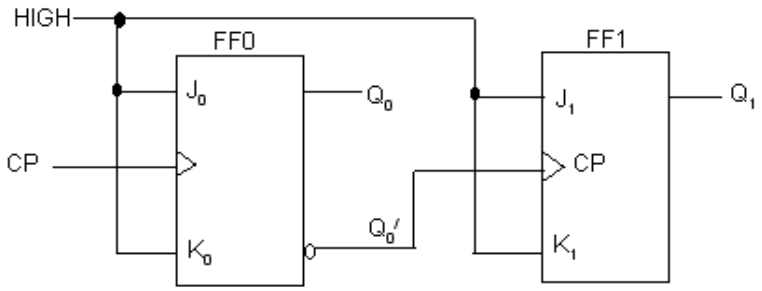
B) Draw the diagram of a master-slave flip-flop using D flip-flops. [2]

7. A) Design a 4 bit register which can do the following operations based on the two control INPUTS X and Y as given below: [5]

X	Y	Operation
0	0	Right Shift
0	1	Parallel Load
1	0	1's complement
1	1	Left Shift

You can use any kind of flip-flops and other necessary gates as required. Draw a neat logic diagram of your solution.

B) Following is a logic diagram for an asynchronous ripple counter. [3]



Now, if the FF1 is replaced with a flip-flop that has negative edge triggered clock, the circuit will behave in a different way. Find out the sequence it will show in Q_1Q_0 for that situation.