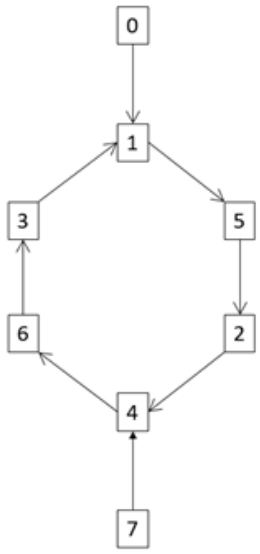
United International University
Department of Computer Science and Engineering
CSE 225 / CSE 1325: Digital Logic Design, Final Exam, Fall 2018
Total Marks: 40, Time: 2:00 Hours

Section A: Answer both of the questions, Question 1 and Question 2.

1. Design a sequential circuit that can recognize the pattern 0110. Use J-K flip flops for your design. You must show state diagram, state table, flip-flop input functions, k-map minimizations of output and circuit diagram. [2+2+2+2=8]

2. Design an arbitrary synchronous counter circuit that counts the sequence given in Figure 1(a). You must show state table, flip-flop input functions, k-map minimizations of output and circuit diagram. You can use any type of flip-flop. [2+2+2+2=8]



(a)

SR Flip-flop

Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

D Flip-flop

Q(t)	Q(t+1)	DR
0	0	0
0	1	1
1	0	0
1	1	1

JK flip-flop

Q(t)	Q(t+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

T flip-flop

Q(t)	Q(t+1)	DR
0	0	0
0	1	1
1	0	1
1	1	0

(b)

Figure 1: (a)Sequence diagram for Question 2 and (b) Excitation table for different FlipFlops.

Section B: Answer any one of the Question 3 and Question 4.

3. Consider a sequential circuit with states denoted by 2 bits and one input X. The equations of the two JK flips flops are given below: $J_A = Q_B$,$K_A = Q_B X'$, $J_B = X'$, $K_B = Q_A X' + Q'_A X$. For this circuit, i) draw the logic diagram, ii) derive the state table and iv) draw the state diagram. [2+3+3=8]

4. Design a 3-bit counter with two control bits C and D. The circuit counts up when control variable C is a 1 and counts down when C is a 0. Counting stays at the same state when the control variable D is a 0. [8]

Section C: Answer any two of the Question 5,6 and 7.

5. Design a 4-input Priority Encoder with inputs and outputs like the encoder in the table given below. Derive the truth table of the priority encoder where priority is set according to the following sequence of priority from highest to lowest $D1 > D2 > D0 > D3$. Derive the boolean expressions for Y_1 and Y_2 and draw the circuit diagram. [4+2+2=8]

D_3	D_2	D_1	D_0	Y_1	Y_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

6. (a) Implement the following Boolean function using a 8-to-1 line multiplexer and other necessary gates. [4]

   $F(A, B, C, D) = AC' + B'D + A'CD + ABCD$

   (b) Using any number of 2×4 active high decoders, implement a 4×16 active high decoder. You must draw the circuit diagram for your design and label the decoder pin names and their inputs/outputs carefully. [4]

7. (a) Implement a 1 bit full adder using a Decoder and necessary OR gates. [4]

   (b) Design a 16:1 MUX using 2:1 MUX (as many as you require) only and illustrate the working mechanism of your designed circuit using appropriate input-outputs for a 16:1 MUX. [4]