Mid Assignment – 2

Course: Digital Logic Design (CSE 1325)

Section: K

Submission Guideline

- Solve every question on your own. Copying will result in zero marks.
- **Deadline: 20th September 2024**
- You must submit soft copy of the assignment.
- Submit Mid Assignment-1, Mid Assignment-2 and Assignment-1 separately in their corresponding submission thread.

---

5. A) Optimize the following function using K-map. You have to show the minimized Product of Sum (POS) form. **[4]**

$$F(W, X, Y, Z) = WXZ + WXZ' + W'XY$$ **[2]**

B) Implement the following function using PLA

$$F(A, B, C, D) = A'B'C'D + A'B'CD + A'B'CD' + A'BC'D$$

6. Imagine a quality control system for a fruit basket packaging line. The system checks the presence of four types of fruits in each basket: apples (A), bananas (B), cherries (C), and dates (D). If the value of a variable is 1 that means the fruit is present in the basket and 0 means the fruit is absent from the basket. **[5]**

The basket is considered high quality (output 1) if there is an apple or a banana present and a cherry or a date present. It's acceptable if both apples and bananas are present, and both cherries and dates are present.

Design a boolean function F that can be used to make a circuit to check these conditions in the packaging.

You have to (i) Show the truth table (ii) Find the simplified expression for the output bit in Sum-of-Product form (iii) Implement the simplified expression using basic gates.

For example:
Input : 0011, Output: 0, There are no apples or bananas present in the basket.
Input : 1010, Output: 1, There are apples and cherries present in the basket.
Input : 1100, Output: 0, There are no cherries or dates present in the basket.
Input : 1111, Output: 1, All fruits are present in the basket.