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Sec: 01

CSE 350 (lab ~~rep~~ 4)

lab report

Datasheet for circuit 1: RF = 1K

S.N	D	C	B	A	Output
1	0	0	0	0	0.0027
2	0	0	0	5	-0.0497
3	0	0	5	0	-0.997
4	0	0	5	5	-1.497
5	0	5	0	0	-1.997
6	0	5	0	5	-2.497
7	0	5	5	0	-2.997
8	0	5	5	5	-3.497
9	5	0	0	0	-3.997
10	5	0	0	5	-4.497
11	5	0	5	0	-4.997
12	5	0	5	5	-5.497
13	5	5	0	0	-5.997
14	5	5	0	5	-6.497
15	5	5	5	0	-6.997
16	5	5	5	5	-7.497

Datasheet for circuit 2.

S.N	D	C	B	A	output
1	0	0	0	0	0.0049
2	0	0	0	5	-0.620
3	0	0	5	0	-1.245
4	0	0	5	5	-1.870
5	0	5	0	0	-2.495
6	0	5	0	5	-3.120
7	0	5	5	0	-3.755
8	0	5	5	5	-4.370
9	5	0	0	0	-4.995
10	5	0	0	5	-5.620
11	5	0	5	0	-6.245
12	5	0	5	5	-6.870
13	5	5	0	0	-7.495
14	5	5	0	5	-8.120
15	5	5	5	0	-8.745
16	5	5	5	5	-9.370

Report 91: NO. I can't get output higher than 15V as the supply to the omamp is up to 15V.

2) Resulation $= \frac{R_F}{R_1} V$

$= \frac{1}{10} \times 5$

$= 0.5$

for circuit 2 $\Rightarrow \frac{10}{20} \left(\frac{1}{\frac{1}{5} + \frac{1}{5} + \frac{1}{5} + \frac{1}{5}} \right)$

$\Rightarrow \frac{1}{2} \left(\frac{5}{4} \right)$

$\Rightarrow \frac{5}{8} = 0.625$

3) ~~a~~ when ~~we input some digital signal~~ we will get

4) ans: if the high voltage is the sum of my (as two digit ID then, high voltage $= 8+4 = 12$

Applying this 12V as high input on circuit 1.

S.N	D	C	B	A	Output
1	0	0	0	0	0.0027
2	0	0	0	12	−1.197
3	0	0	12	0	−2.397
4	0	0	12	12	−3.597
5	0	12	0	0	−4.797
6	0	12	0	12	−5.997
7	0	12	12	0	−7.197
8	0	12	12	12	−8.397
9	12	0	0	0	−9.596
10	12	0	0	12	−10.796
11	12	0	12	0	−11.996
12	12	0	12	12	−13.196
13	12	12	0	0	−13.496
14	12	12	0	12	−13.496
15	12	12	12	0	−13.495
16	12	12	12	12	−13.494

(5) ~~RF~~ Stepsiz ∝ RF. aslong as the ~~stepsize~~ ~~RF~~ ~~increase the resolu~~ stepsize (RF) increase the ~~resoluti~~ RF (stepsize) also increase proportionally.

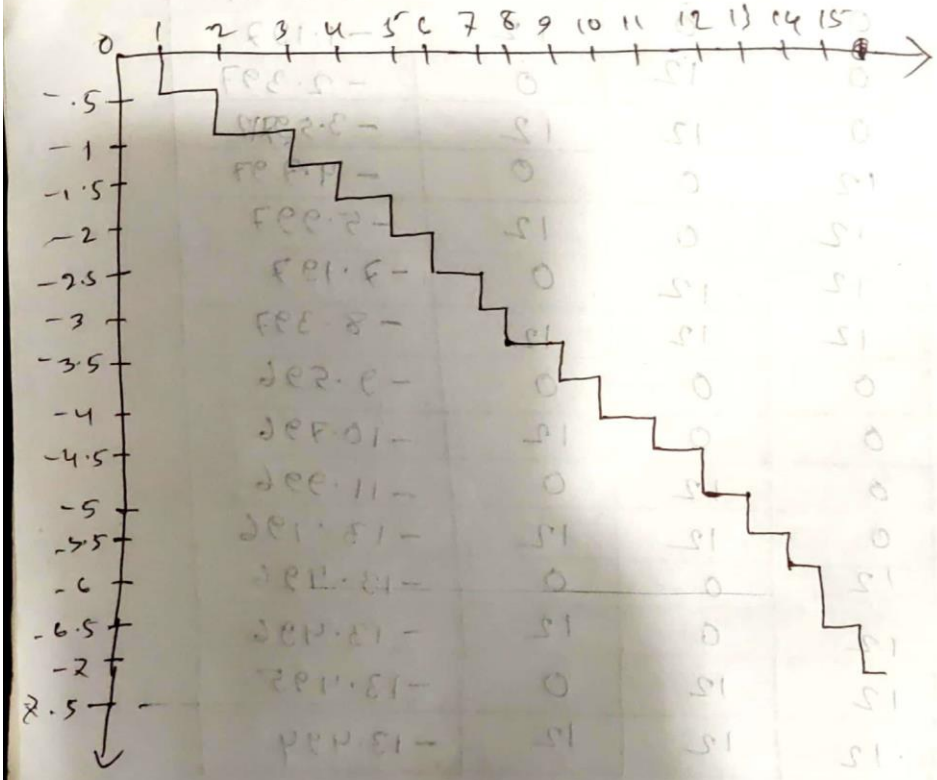
For, example if we set RF = 2.

~~steps~~ For, 0000 → 0.0043
0001 → 0.99
0010 → 1.99

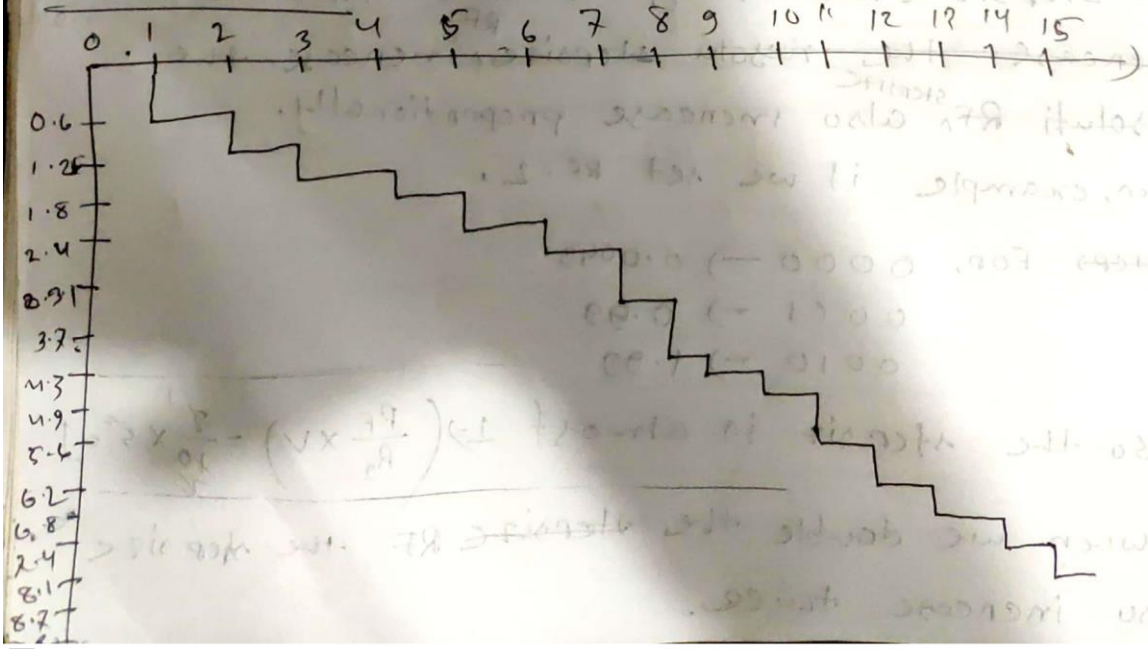
so the stepsiz is almost $1 \rightarrow \left(\frac{R_F}{R_2} \times V\right) = \frac{2}{10} \times 5 = 1$

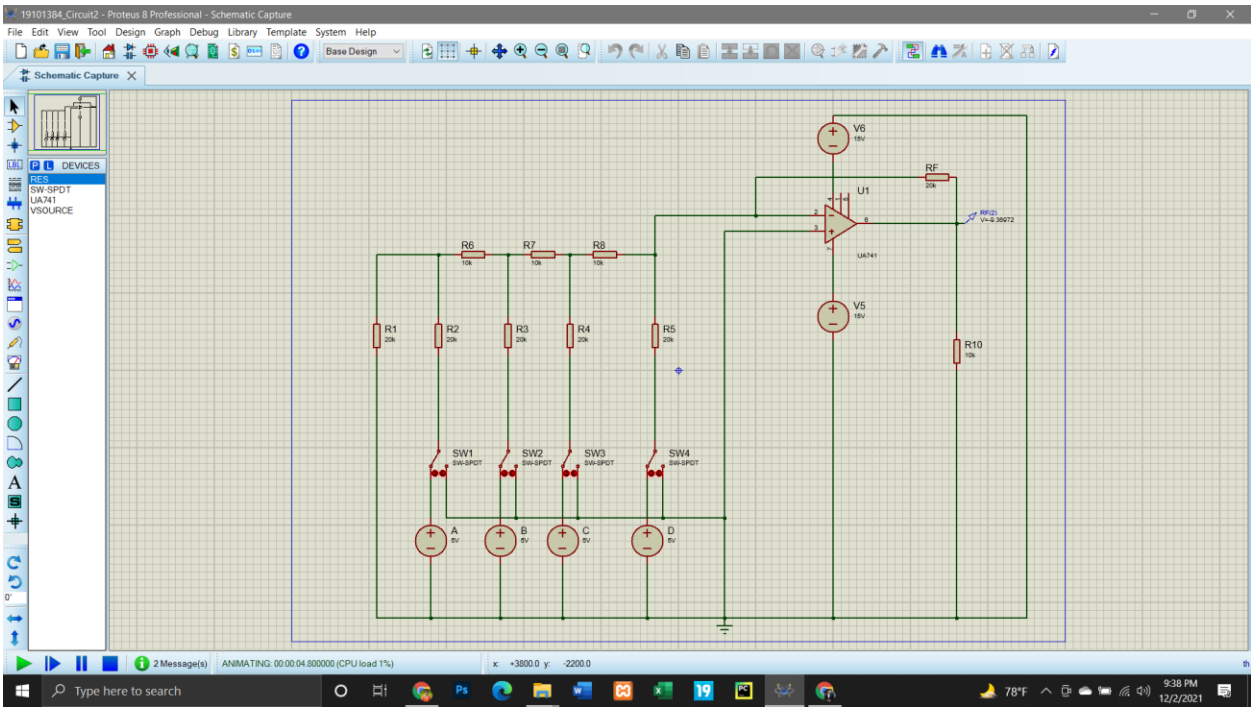
So, when we double the ~~stepsize~~ RF the stepsize also increase twice.

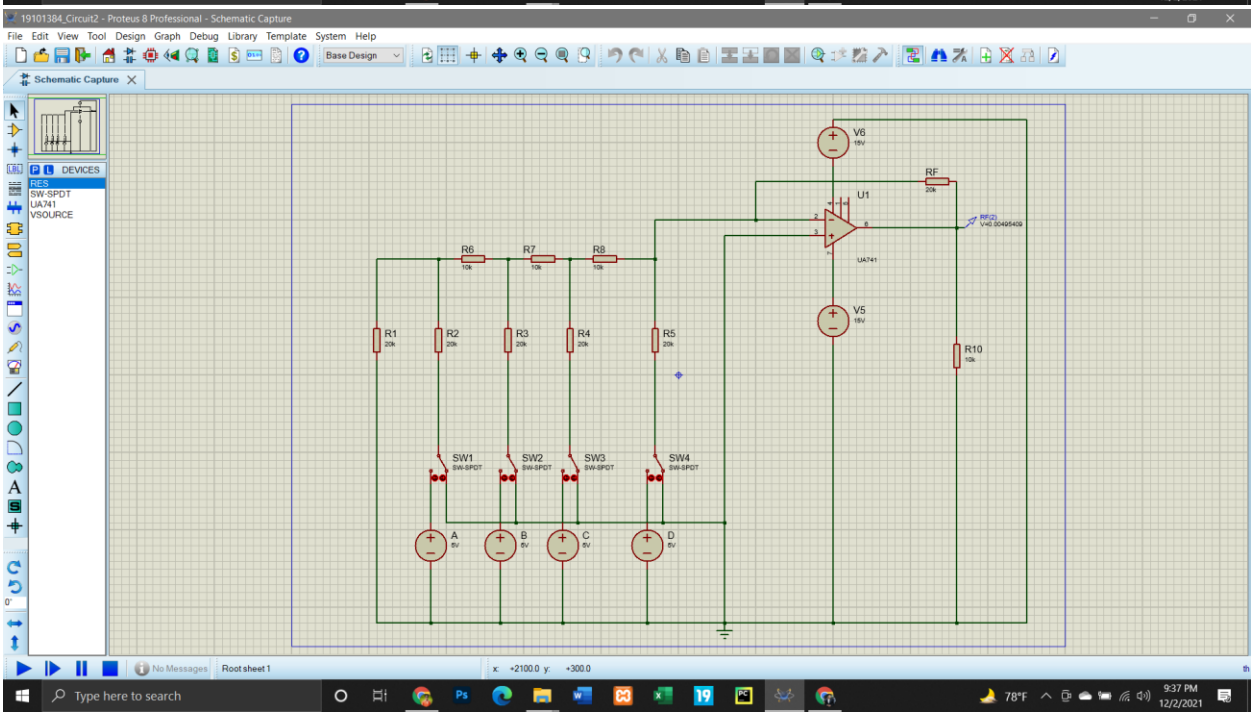
Graph → For circuit 1



For circuit 2 :-




19101384_Circuit2 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
RES
SW-SPDT
UA741
VSOURCE
V6
15V
RF
20k
U1
UA741
V5
15V
R10
10k
R6
10k
R7
10k
R8
10k
R1
20k
R2
20k
R3
20k
R4
20k
R5
20k
SW1
SW-SPDT
SW2
SW-SPDT
SW3
SW-SPDT
SW4
SW-SPDT
A
5V
B
5V
C
5V
D
5V
2 Message(s)
ANIMATING: 00:00:04.800000 (CPU load 1%)
x: +3800.0 y: -2200.0
Type here to search
78°F
9:38 PM
12/2/2021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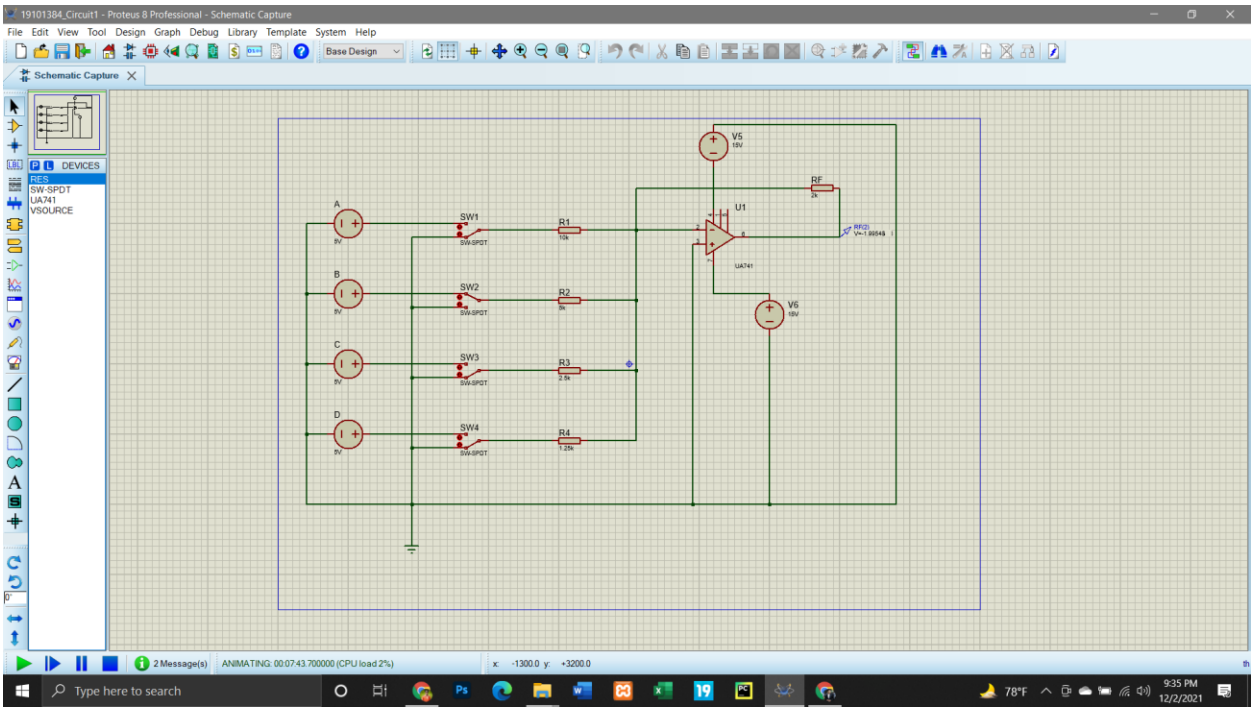
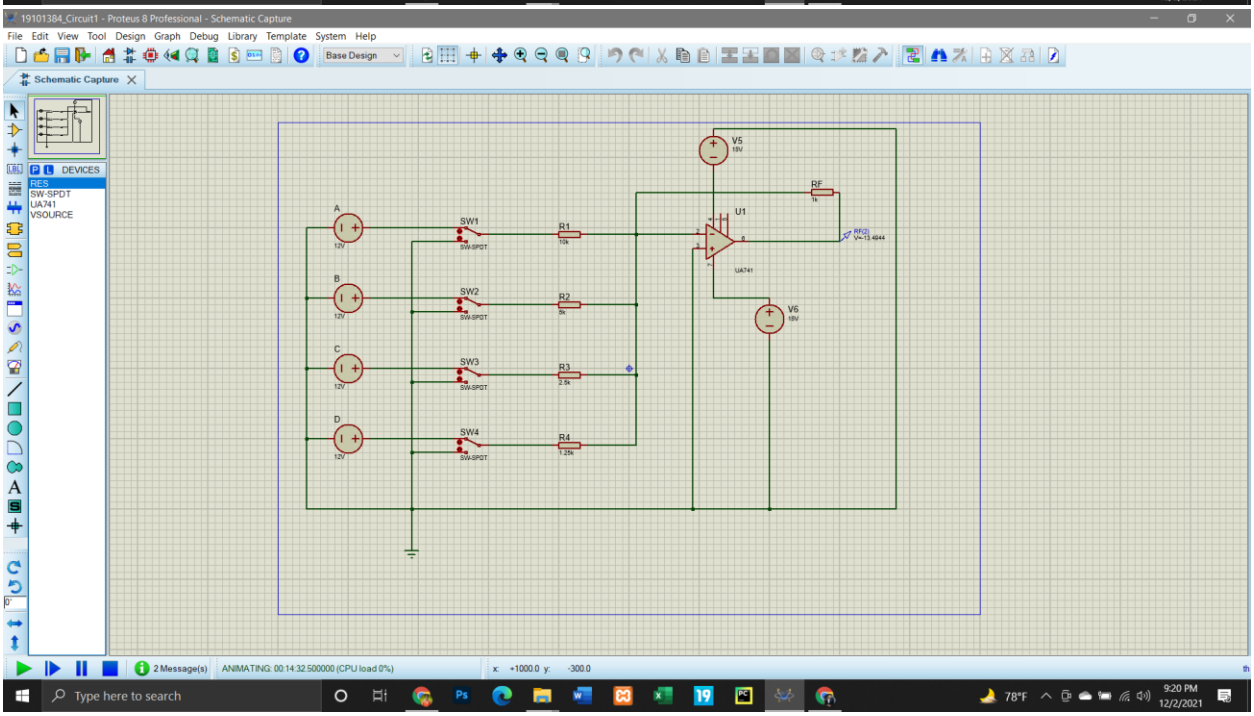
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
RES
SW-SPDT
UA741
VSOURCE
V6
15V
RF
20k
U1
UA741
V5
15V
R10
10k
R6
10k
R7
10k
R8
10k
R1
20k
R2
20k
R3
20k
R4
20k
R5
20k
SW1
SW-SPDT
SW2
SW-SPDT
SW3
SW-SPDT
SW4
SW-SPDT
A
5V
B
5V
C
5V
D
5V
No Messages
Root sheet 1
x: +2100.0 y: +300.0
Type here to search
78°F
9:37 PM
12/2/2021


19101384_Circuit1 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Schematic Capture
DEVICES
RES
SW-SPDT
UA741
VSOURCE
V5
18V
RF
2k
U1
UA741
V6
18V
A
B
C
D
SW1
SW2
SW3
SW4
R1
10k
R2
5k
R3
2.5k
R4
1.25k
2 Message(s)
ANIMATING: 00:07:43.700000 (CPU load 2%)
x: -1300.0 y: +3200.0
Type here to search
78°F
9:35 PM
12/2/2021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File Edit View Tool Design Graph Debug Library Template System Help
Schematic Capture
DEVICES
RES
SW-SPDT
UA741
VSOURCE
V5
18V
RF
1k
U1
UA741
V6
18V
A
B
C
D
SW1
SW2
SW3
SW4
R1
10k
R2
5k
R3
2.5k
R4
1.25k
2 Message(s)
ANIMATING: 00:14:32.500000 (CPU load 0%)
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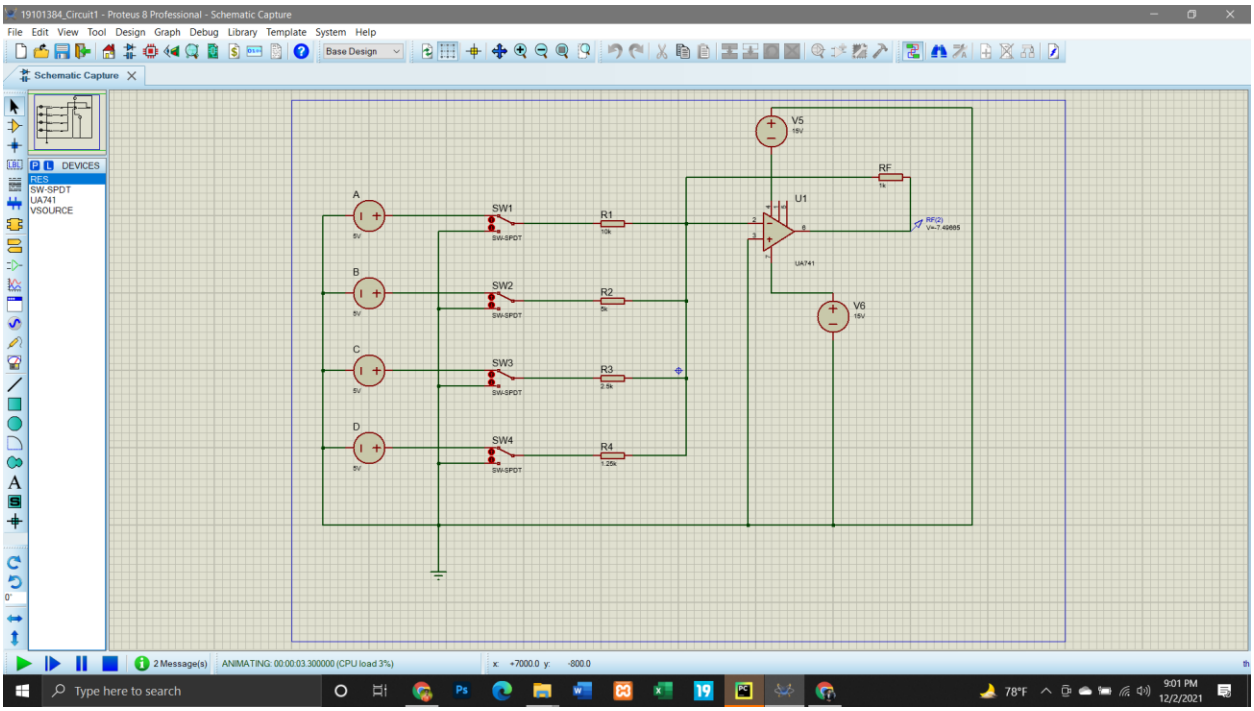
Type here to search
78°F
9:20 PM
12/2/2021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File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
RES
SW-SPDT
UA741
VSOURCE
A
B
C
D
SW1
SW2
SW3
SW4
R1
R2
R3
R4
RF
U1
UA741
V5
V6
2 Message(s)
ANIMATING: 00:00:03.300000 (CPU load 3%)
Type here to search
78°F
9:01 PM
12/2/2021