Name: Sifat Abdullah
ID: 19101384
Sec: 01

CSE350 (lab01)

Report

OR gate:

V_A	V_B	V_{R_1}	V_{R_2}	I_{R_1}	I_{R_2}	$V_R = y$
5	5	0	0	2.2×10^{-5}	2.2×10^{-5}	4.4349
5	0	0.01	0	4.4×10^{-5}	4.4×10^{-5}	4.4087	

(1) ans: in diode And circuit we can see when one input is high and other input is low then the output is low, but when both the input is low the output is also low but when both the circuit is high the output is also high which is what we expect from and gate.

2) If we change the value of $V_A = V_B = 6$ in the software the output is still same as 5 V. so the diode is working.

OR Gate:

OR Gate:

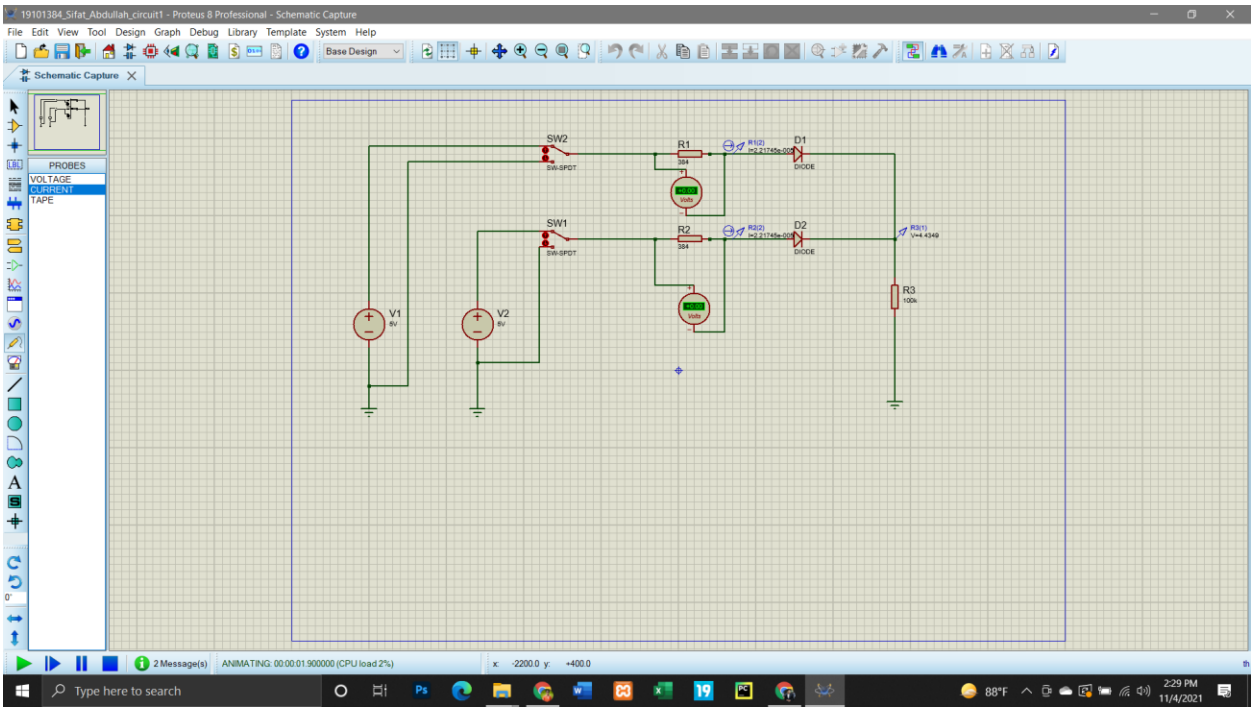
Va	Vb	Vr1	Vr2	Ir1	Ir2	Vr=Y
5	5	0	0	2.21e-005	2.21e-005	4.4349
5	0	0.1	0	4.4e-005	4.4e-012	4.4087
0	5	0	0.1	4.4e-012	4.4e-005	4.4087
0	0	0	0	1.19e-02	1.19e-02	1.38e-015

And Gate:

Va	Vb	Vr1	Vr2	Ir1	Ir2	Vr=Y
5	5	0	0	5e-012	5e-012	5
5	0	0	-0.01	9.41e-012	4.4e-005	0.591
0	5	-0.01	0	4.4e-005	9.41e-012	0.591
0	0	0	0	2.21e-005	2.21e-005	0.5651

Inverter:

vi	Vr1	Vr2	vrc	I1	I2	ib	ic	Y
5	4.3	5.7	-4.89	0.0002	5.7e-005	0.0002	0.002	0.108
0	0.65	4.35	0	4.35e-005	4.3e-005	3.196e-012	1.7e-011	5


19101384_Sifat_Abdullah_circuit1 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
PROBES
VOLTAGE
CURRENT
TAPE
SW2
SW1
SW-SPDT
R1
R2
384
D1
D2
DIODE
R3
100k
V1
V2
6V
2 Message(s)
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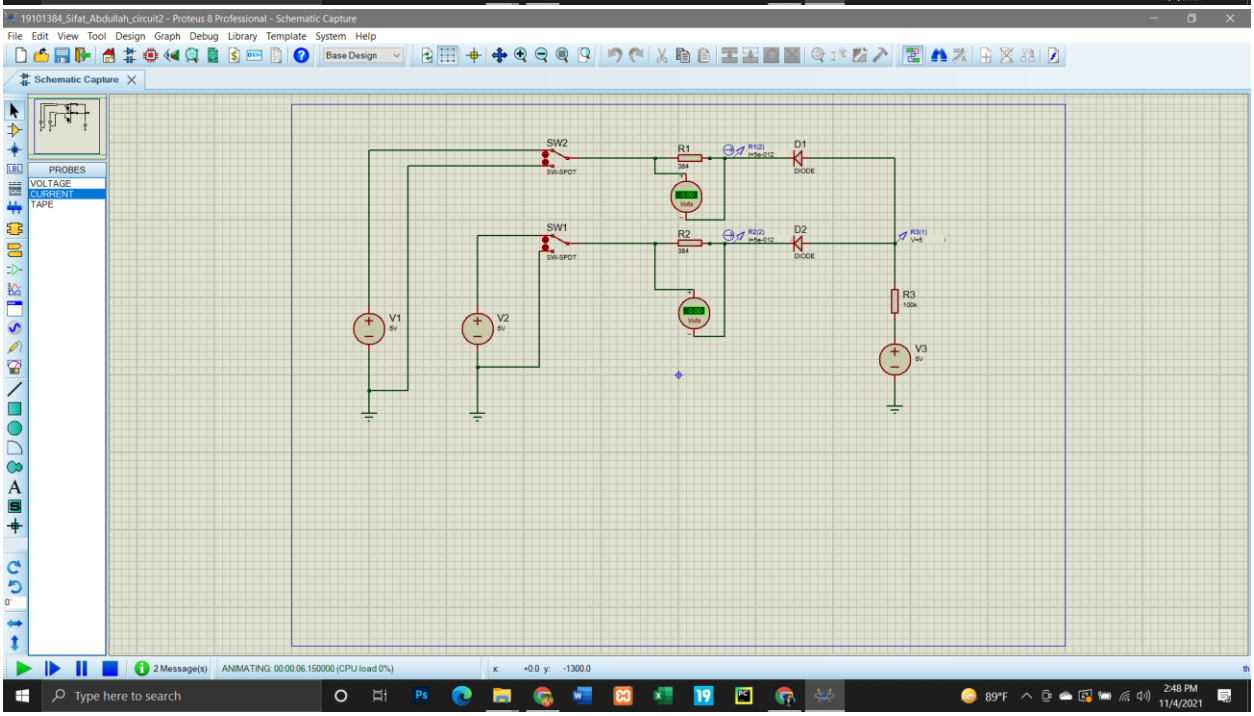
88°F
2:29 PM
11/4/2021


19101384_Sifat_Abdullah_circuit2 - Proteus 8 Professional - Schematic Capture
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Base Design
Schematic Capture
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VOLTAGE
CURRENT
TAPE
SW2
SW1
SW-SPDT
R1
R2
384
D1
D2
DIODE
R3
100k
V1
V2
V3
6V
2 Message(s)
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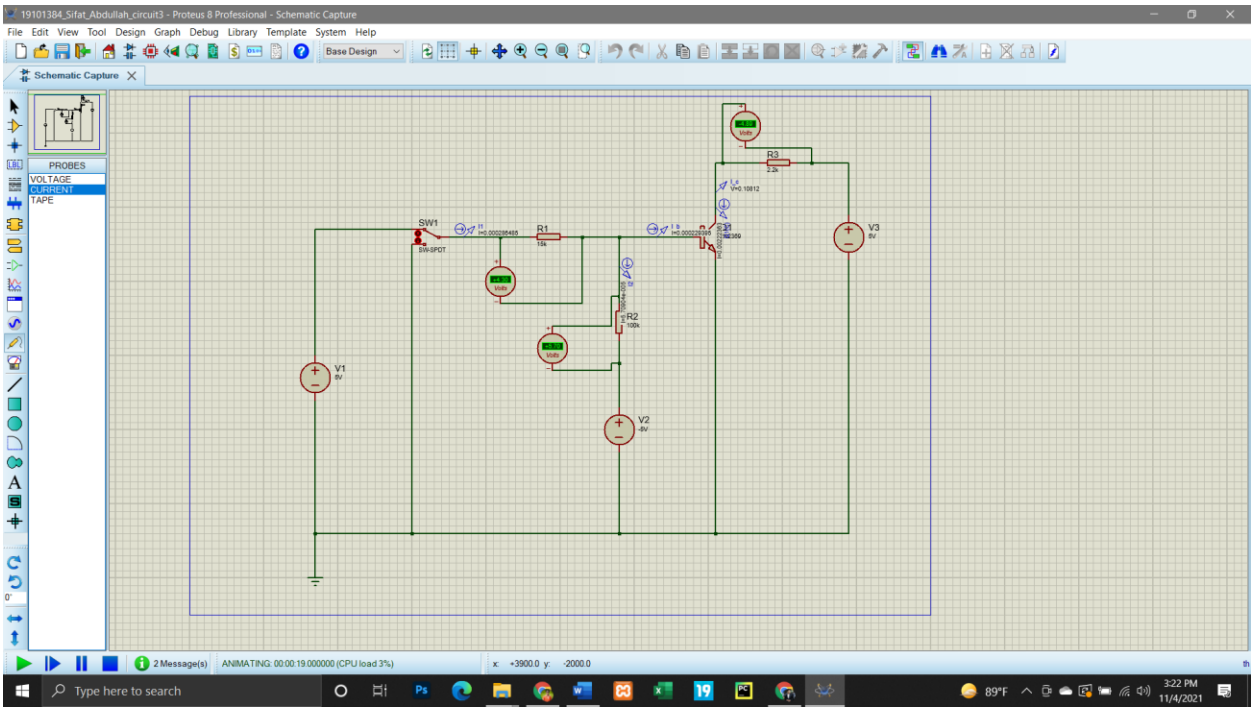
11/4/2021


19101384_Sifat_Abdullah_circuit3 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
PROBES
VOLTAGE
CURRENT
TAPE
SW1
SW-SPDT
R1
10k
R2
100k
R3
2.2k
V1
0V
V2
-5V
V3
5V
2 Message(s)
ANIMATING: 00:00:19.000000 (CPU load 3%)
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Type here to search
89°F
3:22 PM
11/4/2021