M

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Sec: 01

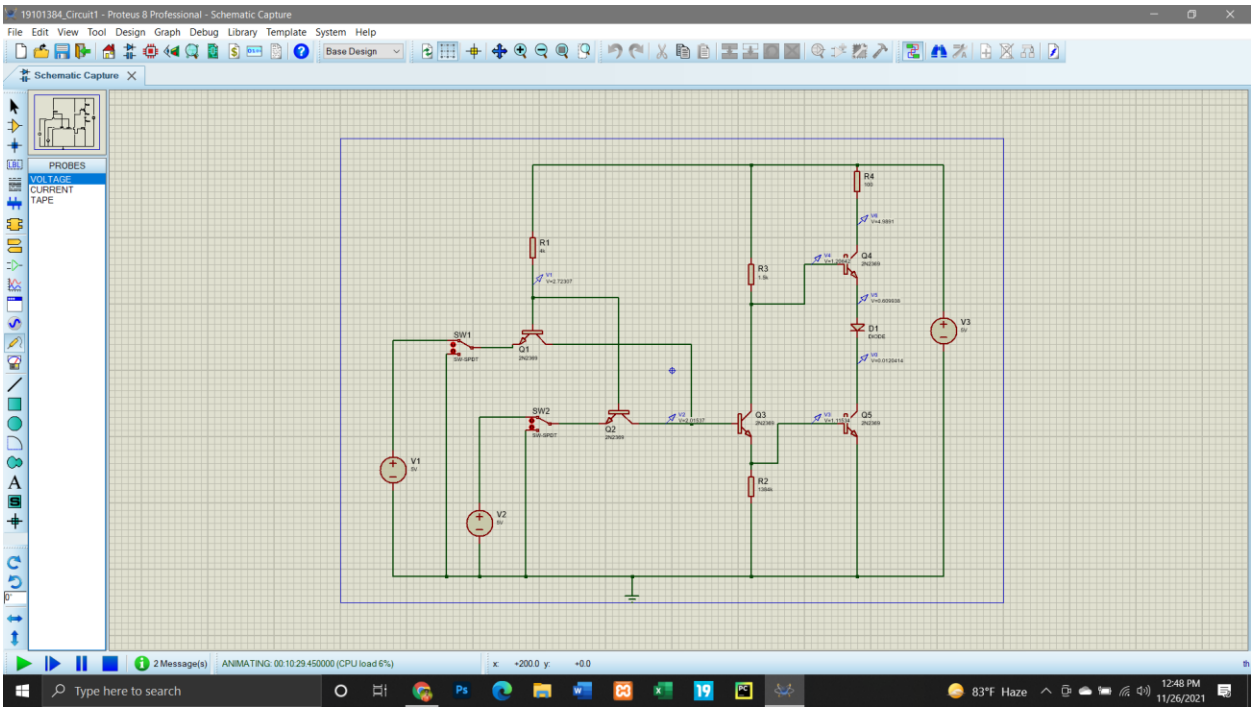
CSE 350 (lab 3)

lab report

$R_2 = 1384$

| A | B | $V_A$ | $V_B$ | $V_o$ | $V_1$ | $V_2$ | $V_3$ | $V_4$ | $V_5$ | $V_6$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 4.61 | 0.717 | 0.007 | $9.58 \times 10^{-08}$ | 5 | 4.803 | 5 |
| 0 | 1 | 0 | 5 | 4.61 | 0.755 | 0.049 | $9.6 \times 10^{-08}$ | 5 | 4.803 | 5 |
| 1 | 0 | 5 | 0 | 4.61 | 0.755 | 0.049 | $9.6 \times 10^{-08}$ | 5 | 4.803 | 5 |
| 1 | 1 | 5 | 5 | 0.012 | 2.723 | 2.015 | 1.115 | 1.206 | 0.609 | 4.98 |

① we know in nand gate when both the output is high only then the output will be low. in all other cases the output will be high. in our circuit we can see the same scenario. so, it works like an Nand gate. when one input is low the $Q_1$ is in saturation, $Q_2$ will be cutoff so, $Q_3$ will be in active mode. then the output becomes high. when both the input is high the $Q_1$ is in reverse activ, $Q_2$ is in saturation so, then $Q_3$ will be in cutoff so the output will below


19101384_Circuit1 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
PROBES
VOLTAGE
CURRENT
TAPE
R1
R2
R3
R4
Q1
Q2
Q3
Q4
Q5
D1
DIODE
SW1
SW2
V1
V2
V3
2 Message(s)
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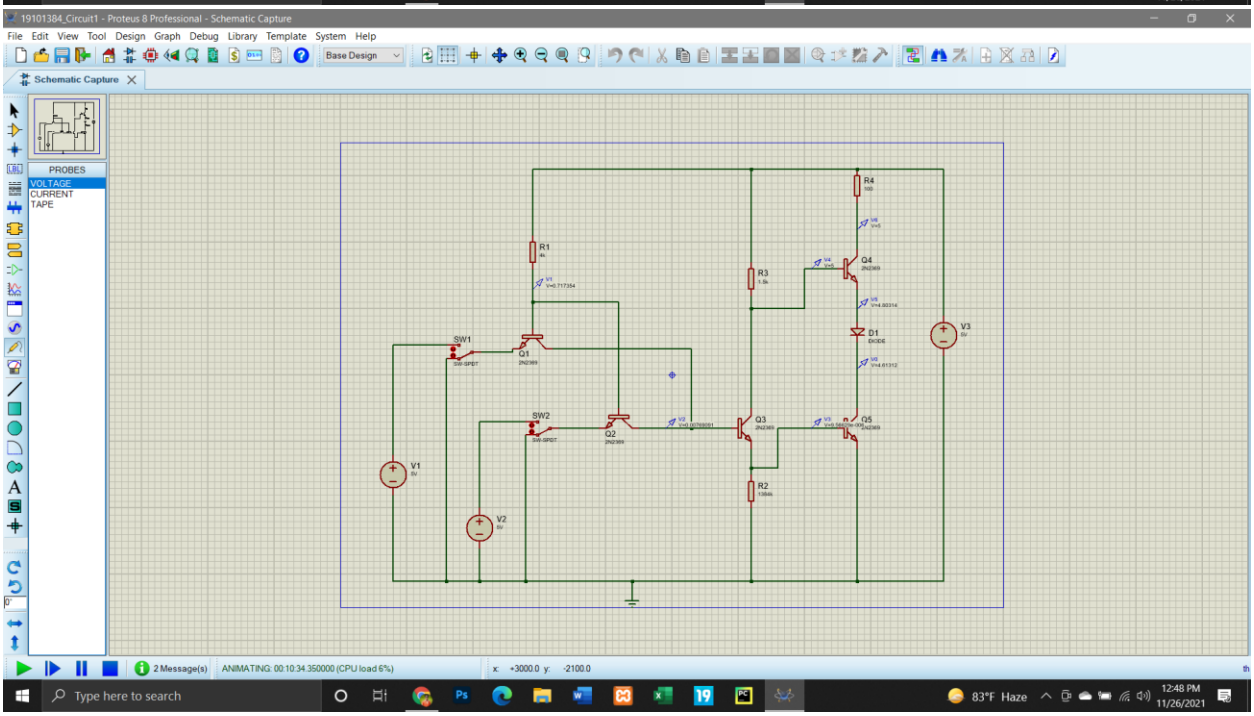
Type here to search
83°F Haze
12:48 PM
11/26/2021


19101384_Circuit1 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
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PROBES
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R1
R2
R3
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Q4
Q5
D1
DIODE
SW1
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V1
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2 Message(s)
ANIMATING: 00:10:34.350000 (CPU load 6%)
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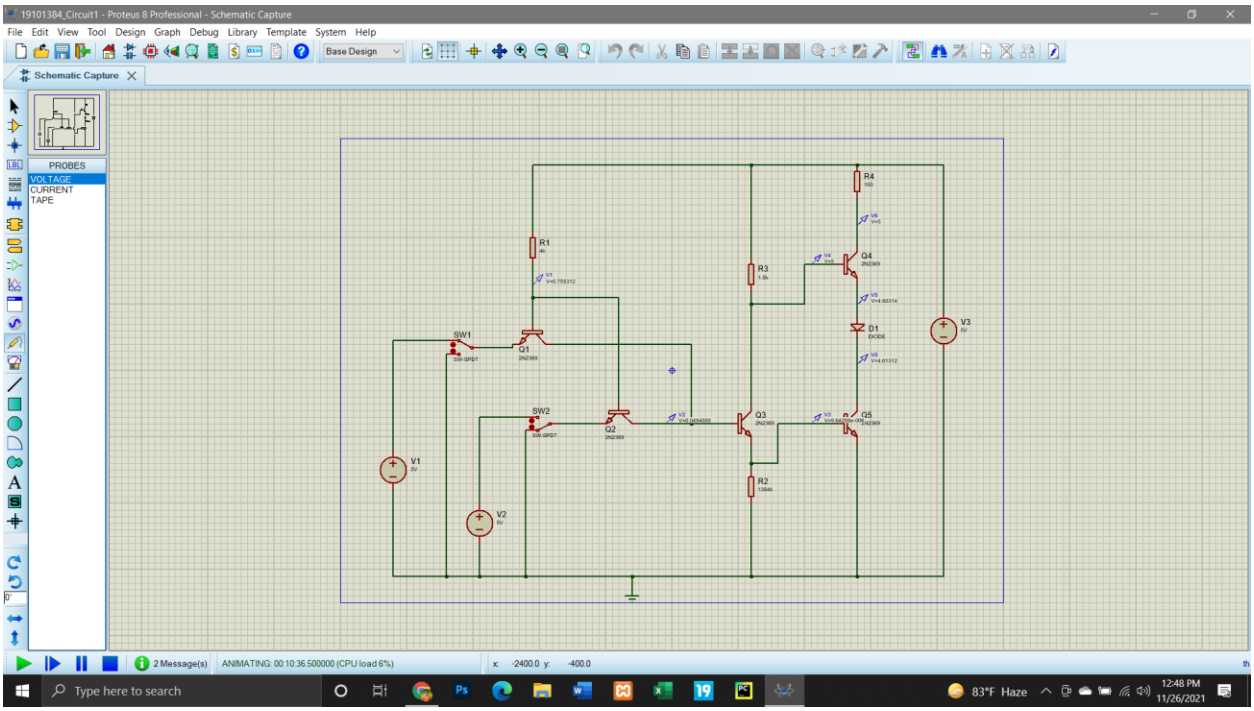
19101384_Circuit1 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
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PROBES
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R1
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2 Message(s)
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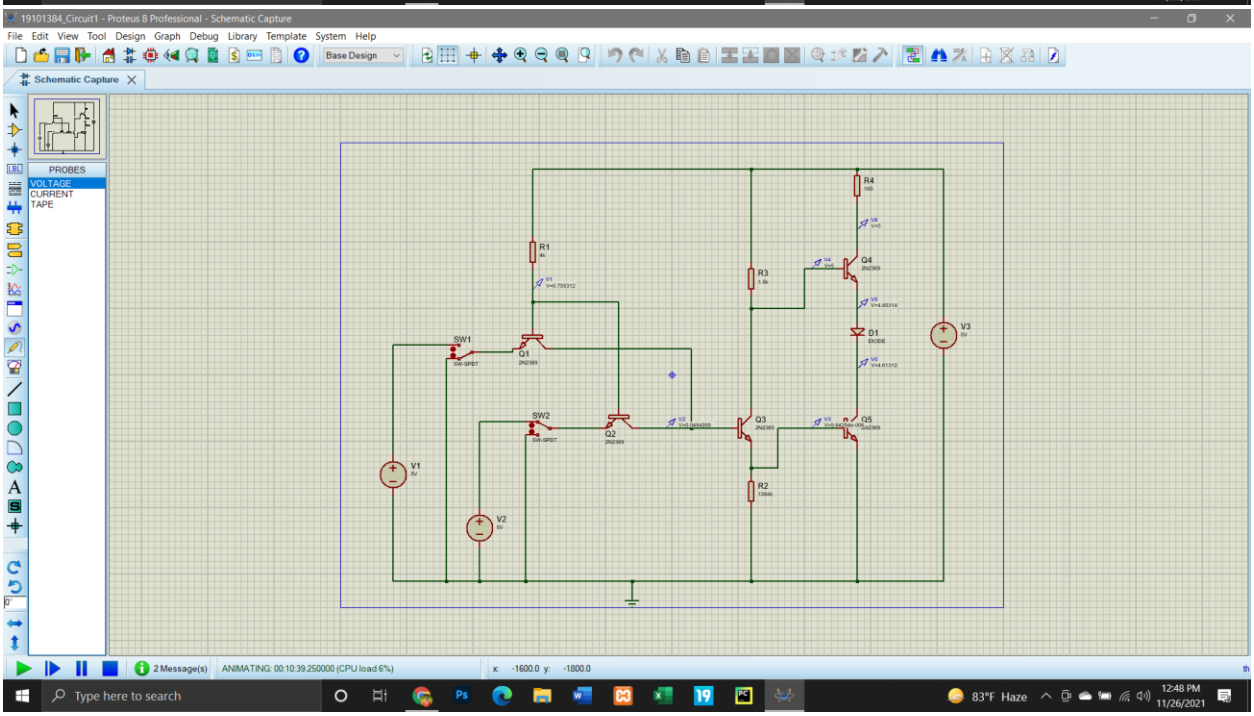
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File Edit View Tool Design Graph Debug Library Template System Help
Base Design
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PROBES
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2 Message(s)
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83°F Haze
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