EAST WEST UNIVERSITY
Department of Computer Science and Engineering
B.Sc. in Computer Science and Engineering Program
Mid Term I Examination, Spring 2022

Course: CSE360 – Computer Architecture, Section-3
Instructor: Md. Nawab Yousuf Ali, PhD, Professor, CSE Department
Full Mark: 25
Time: 1 Hour and 20 Minutes

Note: There are SIX questions, answer ALL of them. Course outcomes (CO), cognitive levels and marks of each question are mentioned at the right margin.

---

1. The hypothetical machine has two instructions: [CO1, C2, Mark: 6]
   - 0100 = Load AC from I/O
   - 0101 = Store AC to I/O
   - 0110 = Add AC to Memory

   In these cases, the 12-bit address identifies a particular I/O device. Show the program execution (using the format of Figure 1) for the following program:
   a) Load AC from device 21
   b) Add contents of memory location 940
   c) Store AC to device 26

   Assume that the next value retrieved from device 21 is 7 and that location 940 contains a value of 13

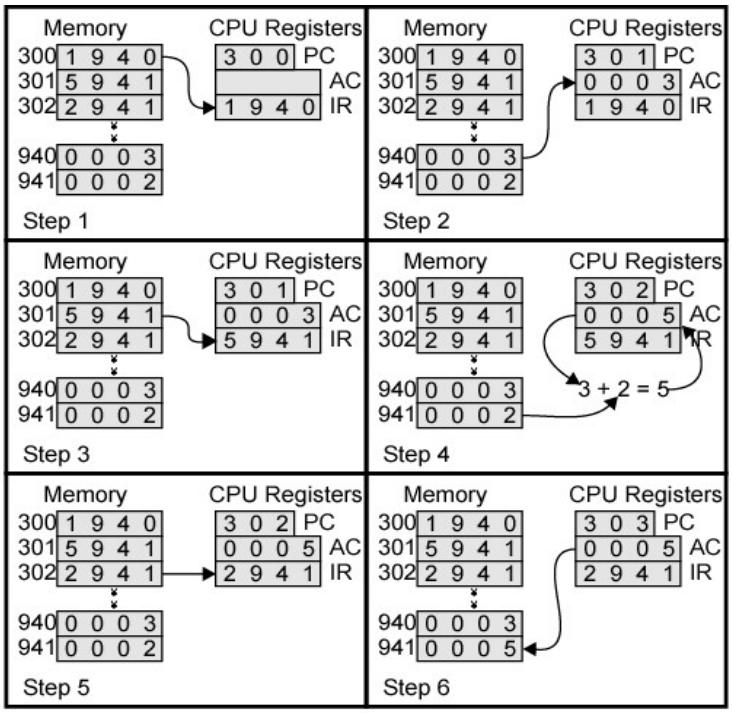

Figure 1. Example of Program Execution

2. A program is run first on a 300MHz and then on a 400 MHz processor. The executed program consists of 1.5 million instructions, with the following instruction mix and clock cycle count. [CO1, C2, Mark: 5]

Instruction Type	Instruction Count	Cycles per Instructions
Integer arithmetic	250000	2
Data transfer	200000	3
Floating point	150000	3
Control transfer	40000	2

Determine the effective CPI and MIPS rate for both the cases.

3. A microprocessor has a decrement memory direct instruction, which subtracts 2 from the value in a memory location. The instruction has five stages: fetch opcode (3 bus clock cycle), fetch operand address (5 bus clock cycle), fetch operand (7 bus clock cycle), subtract 2 from operand (6 clock cycle), and store operand (4 clock cycle). [CO1, C2, Mark: 3+2]
   a) By what amount in percent will the duration of the instruction increase if we insert two bus wait states in each memory read and four bus wait states in memory write operations?
   b) Repeat assuming that the decrement operation taken 12 clock cycles instead of 6 clock cycles.

4. Consider a 64-bit microprocessor whose bus cycle is the same duration as that of a 32-bit microprocessor. Assume that, on average, 20% of the operands and instructions are 64 bits long, 40% are 32 bits long, and 40% are only 16-bits long. Calculate the improvement achieved when fetching instructions and operands with the 64-bit microprocessor. [CO1, C3, Mark: 3]

5. A 32-bit microprocessor, with a 32-bit external data bus is driven by an 64-MHz input clock. What is the maximum data transfer rate when maximum duration of a bus cycle is equal four input clock cycle? [CO1, C3, Mark: 3]

6. Add the following two numbers and normalize the result in a single precision floating point standard. [CO1, C3, Mark: 3]
The numbers are: $10.1101.10101x2^7$ and $111.0010x2^6$