



EAST WEST UNIVERSITY

Department of Computer Science and Engineering B.Sc. in Computer Science and Engineering Program Mid Term I Examination, Summer 2022

Course: CSE360 – Computer Architecture, Section-3
Instructor: Md. Nawab Yousuf Ali, PhD, Professor, CSE Department
Full Mark: 25
Time: 1 Hour and 20 Minutes

Note: There are SIX questions, answer ALL of them. Course outcomes (CO), cognitive levels and marks of each question are mentioned at the right margin.

1. The hypothetical machine has two instructions: [CO1, C2, Mark: 6]

0001 = Load AC from I/O

0101 = Store AC to I/O

0010 = Add AC to Memory

In these cases, the 12-bit address identifies a particular I/O device. Show the program execution (using the format of Figure 1) for the following program:

- Load AC from device 17
- Add contents of memory location 940
- Store AC to device 20

Assume that the next value retrieved from device 17 is 8 and that location 940 contains a value of 6

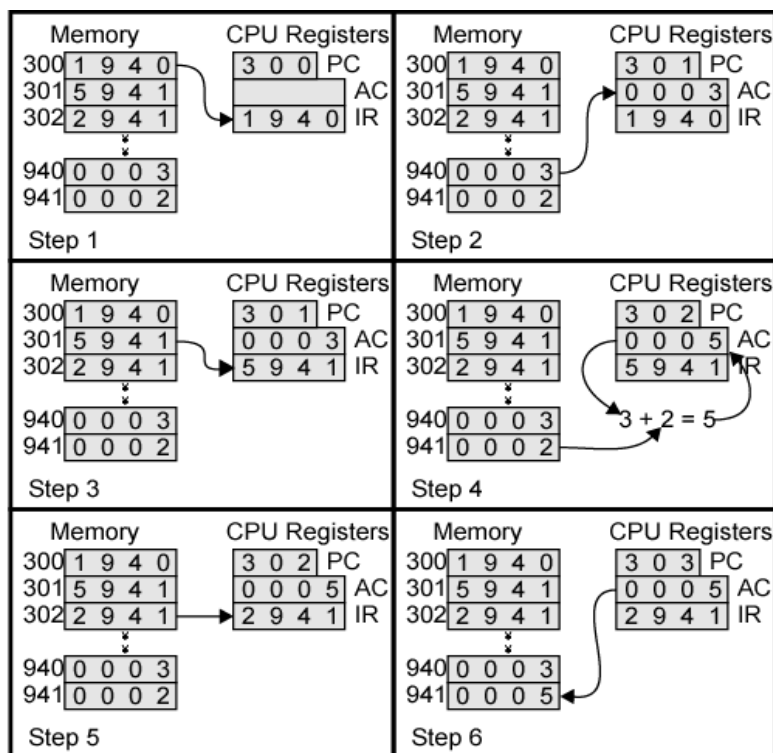


Figure 1. Example of Program Execution

2. When the instruction mix of a CPU in the values that are shown in the table below: [CO1, C2, Mark: 2+3]

Instruction type	Instruction execution time	Occurrence rate
Register to register operation	0.3 microsecond	30%
Register to /from memory operation	0.5 microsecond	50%
Unconditional branch	0.2 microsecond	20%

- a. What is the average executing time of one instruction?
 - b. What is the performance of CPU?
3. Consider two microprocessors having 16- and 32 bit-wide external data buses, respectively. The two processors are identical otherwise and their bus cycles take just as long. [CO1, C2, Mark: 2+2]
- a. Suppose all instructions and operands are four bytes long. By what factor do the maximum data transfer rates differ?
 - b. Repeat assuming that half of the operands and instructions are two-byte long.
4. Consider a 64-bit microprocessor whose bus cycle is the same duration as that of a 32-bit microprocessor. Assume that, on average, 40% of the operands and instructions are 64 bits long, 30% are 32 bits long, and 30% are only 16-bits long. Calculate the improvement achieved when fetching instructions and operands with the 64-bit microprocessor. [CO1, C3, Mark: 3]
5. A microprocessor has decrement memory direct instruction, which deletes 2 from the value in a memory location. The decrement instruction has five stages: fetch opcode (three bus clock cycles), fetch operand address (two cycles), fetch operand (two cycles), decrement 2 from operand (three cycles), and store operand (four cycles). What amount in percent will the duration of the instruction increase if we insert four bus wait states in each memory read and five bus wait states in memory write operation? [CO1, C3, Mark: 4]
6. Multiply the following two numbers using Booth's algorithm. [CO1, C3, Mark: 3]
The numbers are: 10110 and 11101