Chapter 12: Processor Structure and Function

Question 12.3

A microprocessor is clocked at a rate of 5 GHz.

a) How long is a clock cycle?

b) What is the duration of a particular type of machine instruction consisting of three clock cycles?

Solution a:

Frequency = 5GHz

Frequency means no of revolution per second.

One clock cycle means the time it takes to turn a transistor OFF and back ON again.

Means cycle time is time to complete 1 rotation.

5 GHz means 5 billion cycles (5000000000) per second.

So, in 1 second it makes $5*10^9$ rotations or cycles.

Thus $5*10^9$ rotation or cycles in 1 second

So, 1 Rotation takes 1/(5*10^{9} seconds = 0.20 nano second

Solution b.

3 cycles *0.20 ns =0.60 nano second

Question 12.4.

A microprocessor provides an instruction capable of moving a string of bytes from one area of memory to another. The fetching and initial decoding of the instruction takes 10 clock cycles. Thereafter, it takes 15 clock cycles to transfer each byte. The microprocessor is clocked at a rate of 10 GHz.

a) Determine the length of the instruction cycle for the case of a string of 64 bytes.

b) What is the worst-case delay for acknowledging an interrupt if the instruction is non interruptible?

c) Repeat part (b) assuming the instruction can be interrupted at the beginning of each byte transfer.

SOLUTION:

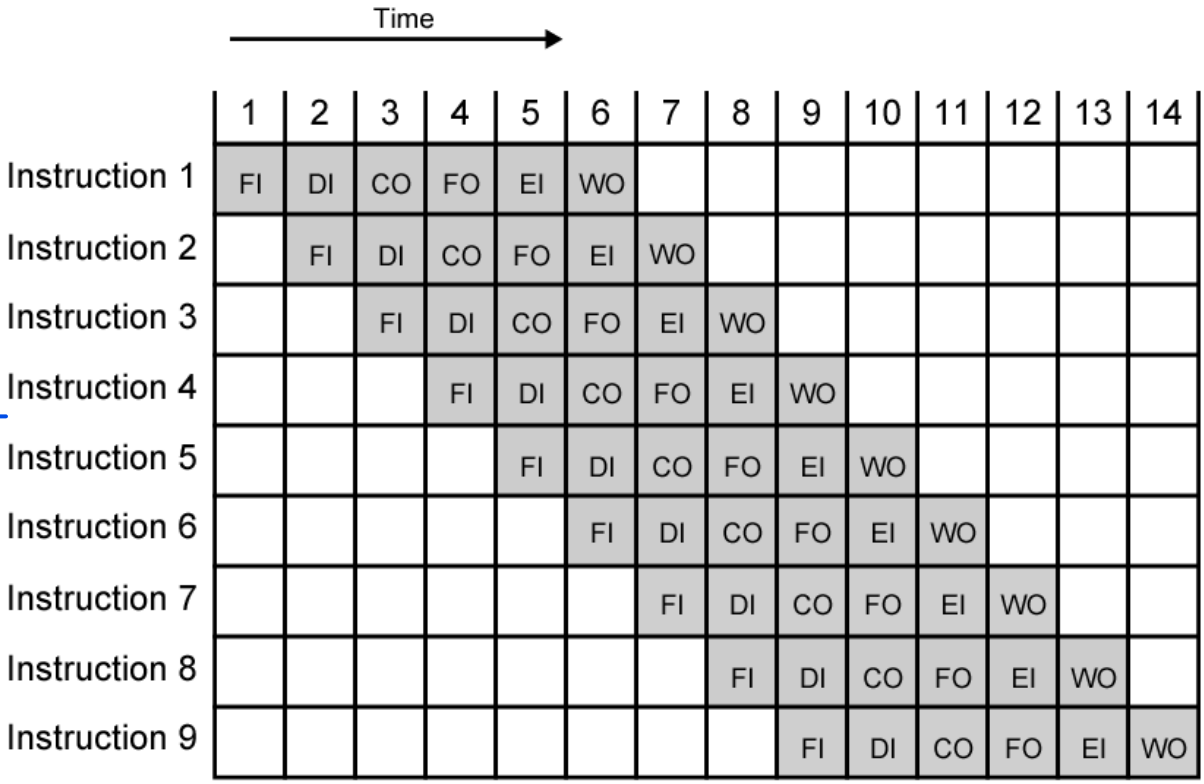
a) The length of a clock cycle is 0.1 ns.
The length of the instruction cycle for this case is [10+(15*64)]*0.1 = 97ns.

b) The worst-case delay is when the interrupt occurs just after the start of the instruction, which is 97 ns.

c) In this case, the instruction can be interrupted after the instruction fetch, which takes 10 clock cycles, so the delay is 10*0.1=1 ns. The instruction can be interrupted between byte transfers, which results in a delay of no more than 15 clock cycles *0.1= 1.5 ns. Therefore, the worst-case delay is 1.5 ns.

Question 12.7.

Consider the timing diagram of the following Figure. Assume that there is only a two-stage pipeline (fetch, execute). Redraw the diagram to show how many time units are now needed for four instructions.



SOLUTION:

TIME

INSTRUCTIONS	1	2	3	4	5
INS 1	F	E			
INS 2		F	E		
INS 3			F	E	
INS 4				F	E

Question 12.8

Assume a pipeline with four stages: fetch instruction (FI), decode instruction and calculate addresses (DA), fetch operand (FO), and execute (EX). Draw a diagram like Figure in Question 12.7 for a sequence of 7 instructions, in which the third instruction is a branch that is taken and in which there are no data dependencies.

SOLUTION:

TIME

BRANCH PENALTY

INSTRUCTIONS	1	2	3	4	5	6	7	8	9	10
I1	FI	DA	FO	EX						
I2		FI	DA	FO	EX					
I3			FI	DA	FO	EX				
I4				FI	DA	FO				
I5					FI	DA				
I6						FI				
I15							FI	DA	FO	EX

Question 12.10

A non-pipelined processor has a clock rate of 2.5 GHz and an average CPI (cycles per instruction) of 4. An upgrade to the processor introduces a five-stage pipeline. However, due to internal pipeline delays, such as latch delay, the clock rate of the new processor has to be reduced to 2 GHz.

a. What is the speedup achieved for a typical program?

b. What is the MIPS rate for each processor?

Solution:

a. Speedup = ExecutionTimeOld / ExecutionTimeNew

ExecutionTimeOld = CPIOld * CycleTimeOld

= CPIOld * CycleTimeOld

= 4 * 1/2.5 Nanoseconds

= 1.6 ns

CPInew can be assumed 1 on average for pipelining.

ExecutionTimeNew = CPInew * CycleTimenew

= 1 * 1/2 Nanoseconds

= 0.5 ns

Speedup = 1.6 / 0.5 = 3.2

b. Clock Rate (non-pipelined) = 2.5GHz

CPI= 4

Clock rate (pipe lined) =2GHZ

MIPS for non-pipelined:

MIPS = Clock rate / CPI

MIPS = 2500 MHz/4

MIPS=625

MIPS for pipelined:

CPI=1 because instructions are completed at the rate one per clock cycle.

MIPS = Clock rate / CPI

MIPS = 2000 MHz/1

MIPS = 2000