#### Problem 5.1

Consider dynamic RAM that must be given a refresh cycle 64 times per ms. Each refresh operation requires 150 ns. What percentage of the memory's total operating time must be given to refreshes?

#### **Solution:**

In 1 ms, the time devoted to refresh is 64 \* 150 ns = 9600 ns

1 ms = 1000000 ns

In 1000000 ns refreshing occur 9600 ns

In 1 ns refreshing occur (9600/1000000) ns

In 100 ns refreshing occur (9600 x 100) / 1000000 ns = 0.96 ns

Which is approximately 1%

## Problem 5.3

Assume that the access time is 60ns and the recharge time is 40ns.

- a) What is the memory cycle time? What is the maximum data rate this DRAM can sustain, assuming a 1-bit output?
- b) Constructing a 32-bit memory system using these chips yields what data transfer rate?

### **Solution a:**

Memory cycle time = (60 + 40) ns = 100 ns

100 ns = 1 bit

Therefore, the maximum data rate is 1 bit in every 100 ns,

$$10^{-7} s = 1 \text{ bit}$$

$$1 s = 10^7 \text{ bit}$$

100 NS = 1 bit

15 = 16 Mbgs

1 s = 10000000 bit

1 s = 10000 Kilobit

1 s = 10 Megabit

which is 10 Mbps

# **Solution b:**

If 1 bit in every 100ns then

For 32-bit memory system data rate is  $\frac{1}{2}$  32\* 10 Mbps = 320 Mbps

Which is 40 MB/s (MB/ second)