Problem 7.12:

A DMA module is transferring characters to memory using cycle stealing from a device transmitting at 9600 bps. The processor is fetching instructions at the rate of 1 million instructions per second (1 MIPS). By how much will the processor be slowed down due to the DMA activity?

Solution:

DMA module transferring characters at 9600 bps = 9600/8 Bps = 1200 Bps
Processor is fetching instructions at the rate = 1 MIPS (million instruction per second)
Slowdown = $1200*100/10^6$ = 0.12%

Problem 7.14:

Examination of the timing diagram of the 8237A indicates that once a block transfer begins, it takes three bus clock cycles per DMA cycle. During the DMA cycle, the 8237A transfers one byte of information between memory and I/O devices

a. Suppose we clock the 8237A at a rate of 5 MHz. How long does it take to transfer one byte?
b. What would be the maximum attainable data transfer rate?
c. Assume that the memory is not fast enough, and we have to insert two wait states per DMA cycle. What will be the actual data transfer rate?

a) At 5 MHz,
5 MHz means 5000000 cycles per second
So, 5000000 cycles take 1 second
1 cycle takes=1/5000000 sec = 0.2 μs

So, the one clock cycle takes 0.2 μs.
A transfer of one byte takes 3*0.2= 0.6μs because one DMA cycle takes three bus cycles

b) The data rate = 1/transfer rate = $1/(0.6 \times 10^{-6})$ =
=1.67 MB/s

0.6 μs needs to transfer 1 byte of data
0.6/1000000 sec needs to transfer 1 byte of data
So, 1 sec needs to transfer = 1* 1000000/0.6 =1666666.667 bytes=1666.667= 1.5894 MB of data

c) Two wait states add an addition = (0.2 + 0.2) μs = 0.4 μs,

So, that a transfer of one byte takes= (0.4μs+0.6μs) =1μs.
1 μs need to transfer 1 byte of data
1/1000000 sec is required to transfer 1 Byte
1 sec required to transfer=1000000 Byte=1 MB

The resulting datarate= $1/((0.6+0.4)\times10^{-6})=1/(1\times10^{-6})$ =1MB/s

Problem 7.15:

Assume that in the system of the preceding problem, a memory cycle takes 750 ns. To what value could we reduce the clocking rate of the bus without effect on the attainable data transfer rate?

Solution:

A DMA cycle could take as long as 750/1000= 0.75 μs without the need for wait states.

This corresponds to a clock period of **0.75/3 = 0.25 μs,** which in turn corresponds to a clock rate of 4 MHz.

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Problem 7.16:

A DMA controller serves four receive-only telecommunication links (one per DMA channel) having a speed of 64 Kbps each.

a. Would you operate the controller in burst mode or in cycle-stealing mode?
b. What priority scheme would you employ for the service of the DMA channels?

Solution:

a. Telecommunications links can operate continuously, so burst mode cannot be used, as this would tie up the bus continuously. Cycle-stealing is needed.

b. Because all 4 links have the same data rate, they should be given the same priority.

Problem: 7.17

A 32-bit computer has two selector channels and one multiplexor channel. Each selector channel supports two magnetic disks and two magnetic tape units. The multiplexor channel has two-line printers, two card readers, and T0 VDT terminals connected to it. Assume the following transfer rate:

Disk drive: 800 Kbytes/sec
Magnetic tape drive 200 Kbytes/sec
Line printer 6.6 Kbytes /sec
Card reader: 1.2 Kbytes/sec
VDT: 1 Kbytes/sec
Estimate the maximum aggregate I/O transfer rate in this system.

Selector selects one device at a time, Multiplexer for getting output from one or more than one device.
For Selector I/O transfer rate = maximum of (two magnetic disk and two magnetic tape units) = max (800, 200) =800KBps
For two selectors=800*2=1600 KBps
For Multiplexer I/O transfer rate = 2*6.6 + 2*1.2 +10*1 = 25.6Kbyte/sec
So, total maximum aggregate I/O transfer rate = 1600 + 25.6 =1625.6Kbyte/sec

Example: A DMA controller transfers 32-bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at a rate of 4800 characters per second. The CPU fetches and executing instructions at an average rate of one million instructions per second. By how much will the CPU be slowed down because of the DMA transfer?

Solution:

DMA controller transfers 32 bit(4 byte) words to memory(cycle stealing mode).
Device transmits 4800 character per second (1 character = 1 byte)
So, for 1 byte it will take 1 / 4800 sec.
Since the controller transfers 4 byte in cycle stealing mode, it will take 4 * (1 / 4800) = 1 / 1200 sec.
So 1200 characters will be transferred in cycle stealing mode and it is given that CPU is fetching and executing instructions at an average rate of one million instructions per second. Slow down or cycle wasted % in DMA transfer = (1200/1000000) * 100 = 0.12 %