

ALL the questions in here ?

TAG,SET,WORD,BLOCK TYPE:

1. A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte. Show the number of bits in each of the Tag, Block, and Word fields of the memory address and design the cache organization.
2. A TWO WAY-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses.
3. A set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses.
4. A two-way set-associative cache has lines of 64 bytes and a total size of 32 Kbytes. The 128-Mbyte main memory is byte addressable. Show the format of main memory addresses.
5. Show the format of A two-way set-associative cache has lines of 64 bytes and a total size of 16 Kbytes. The 128-Mbyte main memory is byte addressable. Show the format of main memory addresses.
6. A four-way set-associative cache has lines of 32 bytes and a total size of 16 KB. The 256-MB main memory is byte addressable. What is the format of main memory addresses?

Instructions and opcode

1. Consider a hypothetical 64-bit microprocessor having 64-bit instructions composed of two fields: the first two byte contains the opcode and the remainder the immediate operand or an operand address. a. What is the maximum directly addressable memory capacity (in bytes)? b. How many bits are needed for the program counter and the instruction register?
2. 3.3 Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address. a. What is the maximum directly addressable memory capacity (in bytes)? b. Discuss the impact on the system speed if the microprocessor bus has 1. a 32-bit local address bus and a 16-bit local data bus, or 2.

a 16-bit local address bus and a 16-bit local data bus. c. How many bits are needed for the program counter and the instruction register?

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Table mix of a CPU in the values

| Instruction type | Instruction execution time | Occurrence rate |
|------------------------------------|----------------------------|-----------------|
| Register to register operation | 0.3 microsecond | 30% |
| Register to /from memory operation | 0.5 microsecond | 50% |
| Unconditional branch | 0.2 microsecond | 20% |

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Problem 4.

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Performance of the CPU :

1. When a CPU operates at a clock frequency of 500MHz, requires an average of 5

CPI for executing one instruction, what is the performance (in MIPS) of the CPU?

2. A CPU operates at a clock frequency of 125 GHz, requires an average of 77 CPI for executing one instruction, **what** is the performance (in MIPS) of the CPU?

3. When a CPU operates at a clock frequency of 12.1GHz, requires an average of 17 CPI for executing one instruction, what is the performance (in MIPS) of the CPU?

4. When a CPU operates at a clock frequency of 100000 KHz, requires an average of 10 CPI for executing one instruction, what is the performance of the CPU?

5. When a CPU operates at a clock frequency of 3.5GHz, requires an average of 27 CPI for executing one instruction, what is the performance (in MIPS) of the CPU?

Instruction Stages Math:

1. A microprocessor has an increment memory direct instruction, which adds 3 to the value in a memory location. The instruction has five stages: fetch opcode (2 bus clock cycle), fetch operand address (4 bus clock cycle), fetch operand (8 bus clock cycle), add 3 to operand (5 clock cycle), and store operand (7 clock cycle).

a) By what amount in percent will the duration of the instruction increase if we insert **three bus wait states** in each memory read and **four bus wait states in memory write** operations?

b) Repeat assuming that the increment operation taken 20 clock cycles instead of 5 clock cycles.

2. A microprocessor has a decrement memory direct instruction, which subtracts 2 from the value in a memory location. The instruction has five stages: fetch opcode (3 bus clock cycle), fetch operand address (5 bus clock cycle), fetch operand (7 bus clock cycle), subtract 2 from operand (6 clock cycle), and store operand (4 clock cycle).

a) By what amount in percent will the duration of the instruction increase if we insert **two bus wait states in each memory read and four bus wait states in memory write operations?**

b) Repeat assuming that the decrement operation taken 12 clock cycles instead of 6 clock cycles.

3. A microprocessor has decrement memory direct instruction, which deletes 2 from the value in a memory location. The decrement instruction has five stages: fetch opcode (three bus clock cycles), fetch operand address (two cycles), fetch operand (two cycles), decrement 2 from operand (three cycles), and store operand (four cycles).

a. What amount in percent will the duration of the instruction increase if we **insert four bus wait states in each memory read and five bus wait states in memory write operation?**

TM, TC, CC, CM AND EFFECTIVE ACCESS TIME MATH

1. Consider a memory system with the following parameters: $T_c = 175 \text{ ns}$ $C_c = 10^{-3} \text{ \$/bit}$ $T_m = 1500 \text{ ns}$ $C_m = 10^{-4} \text{ \$/bit}$ a) What is the cost of 2.5 MB of main memory using cache memory technology? b) If the effective access time is 35% greater than the main memory access time, what is the hit ratio H ?

2. Consider a memory system with the following parameters: $T_c = 150 \text{ ns}$ $C_c = 10^{-6} \text{ \$/bit}$ Consider a memory system with the following parameters: $T_c = 150 \text{ ns}$ $C_c = 10^{-6} \text{ \$/bit}$ $T_m = 1500 \text{ ns}$ $C_m = 10^{-7} \text{ \$/bit}$ MByte of main memory?

a. What is the cost of 2 MByte of main memory?

b. What is the cost of 2.5 technology? b. What is the cost of 2.5 MByte of main memory using cache memory MByte of main memory using cache memory

c. If the effective access time is time, what is the hit ratio H ? c. If the effective access time is 25% greater than the main memory access

3. Consider a memory system with the following parameters:

$T_c = 160 \text{ ns}$ $C_c = 10^{-6} \text{ \$/bit}$

$T_m = 1100 \text{ ns}$ $C_m = 10^{-7} \text{ \$/bit}$

a) What is the cost of 3.5 MByte of main memory using cache memory technology?

b) If the effective access time is 3% greater than the main memory access time, what is the hit ratio H ?

Hit ratio miss ratio math :

1. Consider the hit ratio is 0.7 and the access times for cache memory and main memory are 150 ns and 1800 ns respectively, what is the average memory access time in ns for the CPU?

Refresh , Access Time AND Recharge math

1. Consider dynamic RAM that must be given a refresh cycle 64 times per ms. Each refresh operation requires 150 ns. What percentage of the memory's total operating time must be given to refreshes?

2. Assume that the access time is 60ns and the recharge time is 40ns.

a) What is the memory cycle time? What is the maximum data rate this DRAM can sustain, assuming a 1-bit output?

b) Constructing a 32-bit memory system using these chips yields what data transfer rate?

3. Assume that the access time is 120ns and the recharge time is 60ns.

a) What is the memory cycle time?

b) What is the maximum data rate this DRAM can sustain, assuming a 1-bit output?

c) Constructing a 64-bit memory system using these chips yields what data transfer rate?

4. Assume that the access time is 55 ns, and the recharge time is 35 ns.

a) What is the memory cycle time? What is the maximum data rate this DRAM can sustain, assuming a 2-bit output?

b) Constructing a 128-bit memory system using these chips yields what data transfer rate?

IF Maximum Memory Address

1. Consider a hypothetical microprocessor generating a 128-bit address (for example, assume that the program counter and the address registers are 128 bits wide) and having a 64-bit data bus.

a. What is the maximum memory address space that the processor can access directly if it is connected to a "128-bit memory"?

b. What is the maximum memory address space that the processor can access directly if it is connected to an "64-bit memory"?

2. Consider a hypothetical microprocessor generating a 16-bit address (for example, assume that the program counter and the address registers are 16 bits wide) and having a 16-bit data bus

a. What is the maximum memory address space that the processor can access directly if it is connected to a "16-bit memory"?

b. What is the maximum memory address space that the processor can access directly if it is connected to an "8-bit memory"?

3. Consider a hypothetical microprocessor generating a 32-bit address, assume that the program counter and the address register are 32-bit. Consider a hypothetical microprocessor generating a 32-bit address (for bits wide) and having 32-bit data bus.

a) What is the maximum memory address space that the processor can access directly if it is connected to a "16-bit memory"?

b) If an input and output instruction can specify a 16-bit I/O port number, how many 16-bit I/O ports can the microprocessor support? Explain. If an input and output instruction can specify a 16-bit I/O port number, how many 32-bit I/O ports can the microprocessor support? How many 32-bit I/O

Maximum data transfer rate :

1. Consider a 64-bit microprocessor, with a 64-bit external data bus, driven by an input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals four input clock cycles.

a) What is the maximum data transfer rate across the bus?

b) To increase its performance, would it be better to make its external data bus 128 bits or to double the external clock frequency supplied to the microprocessor? State any other assumptions you make and explain.

2. Consider a 64-bit microprocessor, with a 32-bit external data bus, driven by an input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals four input clock cycles. a) b) What is the maximum data transfer rate across the bus that this microprocessor can sustain, in bytes/s? To increase its performance, would it be better to make its external data bus 32 bits or to double the external clock frequency supplied to the microprocessor? State any other assumptions you make, and explain.

Improvements Operands and Instruction percentage :

1. Consider a 32-bit microprocessor whose bus cycle is the same duration as that of a 16-bit microprocessor. Assume that, on average, 20% of the operands and instructions are 32 bits long, 40% are 16 bits long, and 40% are only 8 bits long. Calculate the improvement achieved when fetching instructions and operands with the 32-bit microprocessor.

2. Consider a 64-bit microprocessor whose bus cycle is the same duration as that of a 32-bit microprocessor. Assume that, on average, 20% of the operands and instructions are 64 bits long, 40% are 32 bits long, and 40% are only 16 bits long. Calculate the improvement achieved when fetching instructions and operands with the 64-bit microprocessor.

Factor :

Consider two microprocessors having 16- and 32 bit-wide external data buses, respectively. The two processors are identical otherwise and their bus cycles take just as long.

- a. Suppose all instructions and operands are four bytes long. By what factor do the maximum data transfer rates differ?
- b. Repeat assuming that half of the operands and instructions are two-byte long.

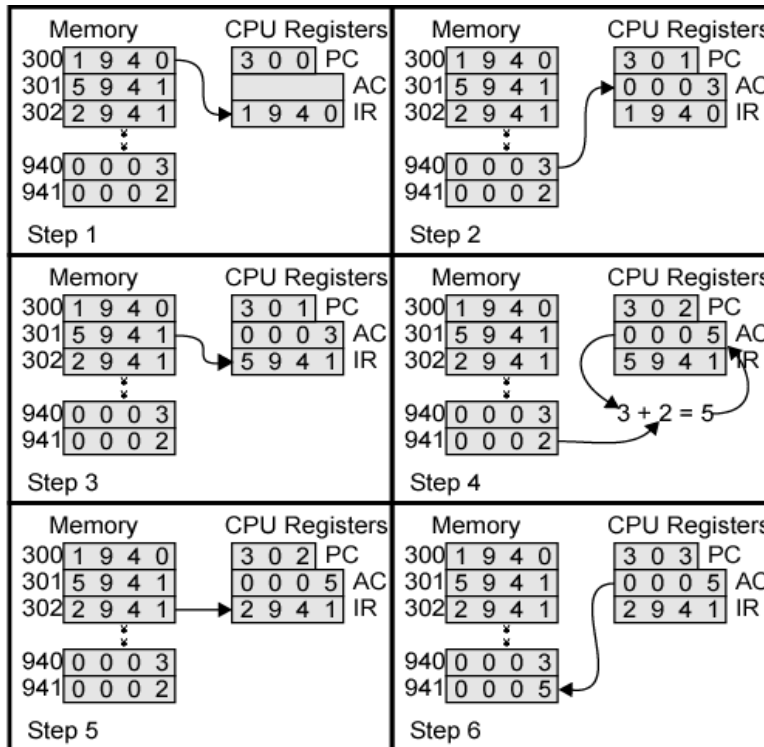
2. Consider two microprocessors having 8- and 16-bit-wide external data buses, respectively. The two processors are identical otherwise and their bus cycles take just as long.

- a. Suppose all instructions and operands are two bytes long. By what factor do the maximum data transfer rates differ?
- b. Repeat assuming that half of the operands and instructions are one-byte long.

Table instruction :

A program is run first on a 300MHz and then on a 400 MHz processor. The executed program consists of 1.5 million instructions, with the following instruction mix and clock cycle count. Instruction Type Instruction Count
Integer arithmetic Cycles per Instructions 250000 2 Data transfer 200000 3 Floating point 150000 3 Control transfer 40000 2 Determine the effective CPI and MIPS rate for both the cases.

LOAD,STORE,ADD



1. The hypothetical machine has two instructions: 0100 = Load AC from I/O 0101 = Store AC to I/O 0110 = Add AC to Memory In these cases, the 12-bit address identifies a particular I/O device. Show the program execution (using the format of Figure 1) for the following program: a) Load AC from device 21 b) c) Add contents of memory location 940 Store AC to device 26 Assume that the next value retrieved from device 21 is 7 and that location 940 contains a value of 13

2. The hypothetical machine has two instructions:

0001 = Load AC from I/O

0101 = Store AC to I/O

0010 = Add AC to Memory

In these cases, the 12-bit address identifies a particular I/O device. Show the program execution (using the format of Figure 1) for the following program:

- Load AC from device 17
- Add contents of memory location 940
- Store AC to device 20

Assume that the next value retrieved from device 17 is 8 and that location 940 contains a value of 6

3. The hypothetical machine has two instructions:

0100 = Load AC from I/O

0101 = Store AC to I/O

0110 = Add AC to Memory

In these cases, the 12-bit address identifies a particular I/O device. Show the program execution (using the format of Figure 1) for the following program:

- a) Load AC from device 14
- b) Add contents of memory location 940
- c) Store AC to device 17

Assume that the next value retrieved from device 14 is 16 and that location 940 contains a value of 20