# DESIGN AND ANALYSIS OF MASTER-SLAVE DATA FLIP-FLOP USING MULTI-THRESHOLD FINFET

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# DESIGN AND ANALYSIS OF MASTER-SLAVE DATA FLIP-FLOP USING MULTI-THRESHOLD FINFET

*A Project Report*
*submitted in partial fulfillment of the*
*requirements for the award of the degree of*

**Bachelor of Technology**
**in**
**Electronics and Communication Engineering**

**by**

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**INSTITUTE OF AERONAUTICAL ENGINEERING**
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**Dundigal, Hyderabad – 500 055, Telangana**

**May, 2023**

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**Date :**

# APPROVAL SHEET

This project report entitled **DESIGN AND ANALYSIS OF MASTER-SLAVE DATA FLIP-FLOP USING MULTI-THRESHOLD FINFET** by **Mr. S Sandeep Kumar, Ms. Bejugam Sangeetha, Mr. B Shiva Prabhas** is approved for the award of the Degree Bachelor of Technology in **Electronics and Communication Engineering**.

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**Place:**

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# Abstract

Because of its growing scale, CMOS technology's power loss can no longer be ignored. The multi-threshold approach, which employs significant threshold transistors in non-critical circuit channels to lower the circuit's total power loss, is one method for addressing leakages. In this work, a multi-threshold strategy and FinFET technology are used to build a master-slave data flip flop. Results are compared using only one threshold master slave data flip flop. It has been demonstrated that the flip flop's static and average electricity usage have fallen by 54% and 8.5%, respectively.

**Keywords**— Single threshold, Multi threshold, Master-slave data flip-flop, CMOS, FinFET, Substrate.

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# List of Abbreviations

| | |
|---|---|
| CMOS | Complementary Metal Oxide Semi-Conductor |
| VLSI | Very Large Scale Integration |
| VHDL | VSHIC Hardware Description Language |
| FPGA | Field Programmable Gate Array |
| CLB | Configurable Logic Block |
| LUT | Look-up Table |
| MOSFET | Metal-Oxide Semiconductor Field effect Transistor |
| FET | Field Effect Transistor |
| TTL | Transistor-Transistor Logic |

# Chapter-1
# Introduction

## 1.1 Introduction

Given that there are more portable electronic devices available on the market, the batteries ought to last longer. The ideal option in this situation would be to reduce the power usage of the electronic devices because adding more battery capacity makes the gadgets larger. Because both static and dynamic power consumptions are made up by CMOS transistors. It is easy to reduce the dynamic power by reducing the supply voltage since the dynamic power dissipation from Eqn 1 is directly proportional to the square of the supply voltage. However, because the channel current is inversely proportional to the power supply, doing so would slow down the gadget.

$$P_{Dynamic} \alpha CV^2_{DD}f \longrightarrow [1]$$

As technology advances, the channel length decreases, lowering the transistor threshold. The dynamic loss of power of the circuit may also drop now that the supply has been reduced, but due to the shorter channel length, the leaky power consumption increases. In order to solve the leakage power, the gate should now have more control over the channel current because we went to FinFETs because they have higher controllability of the channel current, which will limit leakages. Similar to MOSFETs, FinFETs are three-dimensional devices with gate terminals around the channel and raised source and drain structures above the substrate (see Figure 1.1).

Many fins may be included in a single FinFET device, and each of those fins will be protected by a separate gate terminal. The fin of a FinFET is the passageway between the source and drain. It may be applied to increase the FinFET's driving capability. The goal of this study is to design a sequential circuit with a data flip flop in FinFET 18nm technology utilising a multi threshold approach in order to decrease leakages without harming the circuit's performance. The findings have been compared to those of a single threshold data flip flop, and it is evident that using the multi threshold approach reduced the leakage power.

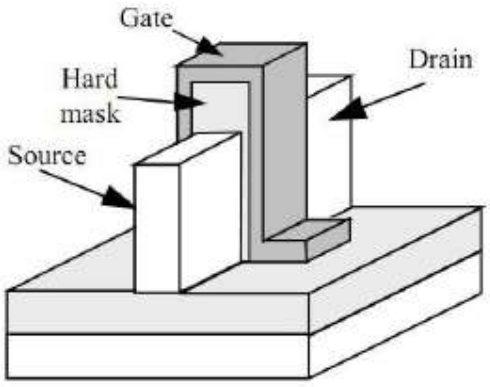


Figure 1.1: FinFET cross-section

## 1.2 Introduction to Vlsi

The electronics industry has grown tremendously over the past 20 years, mostly as a result of the rapid advancement of integration technologies, large-scale systems design, or, to put it another way, the advent of VLSI. Consumer electronics, telecommunications, and high-performance computing are just a few of the fields that are using integrated circuits rapidly and extensively. Typically, the required processing power (or, to put it another way, the intelligence) of these applications is what propels this discipline's rapid growth. Figure 1.2 summarises the major advancements in information technology during the following decades. The most sophisticated technologies already in use already give end users some processing power and mobility, such small bit-rate video and wireless communications.

This trend is anticipated to persist, which will have significant implications for the design of VLSI and systems. The increasing need for extremely high processing power and bandwidth (to handle real-time video, for example) is one of the most significant aspects of information services. The shift towards more personalised information services (as opposed to collective services like broadcasting) is another significant factor. Equipment must be both portable and intelligent in order to adapt to individual demands and give enhanced flexibility and mobility.

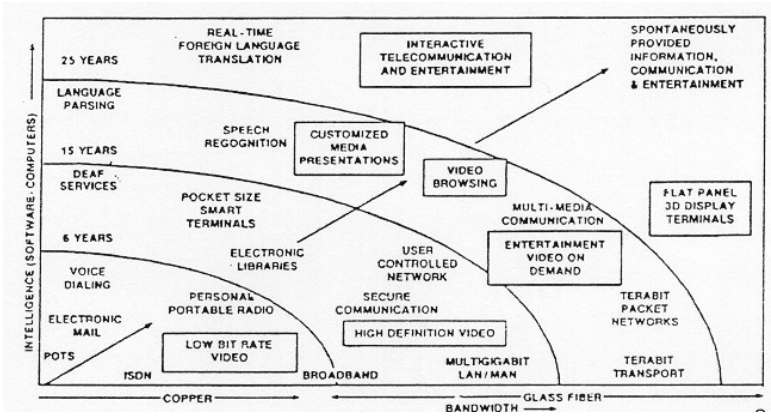


Figure 1.2: Prominent trends in Information Technologies

The demand to incorporate these functionalities in a compact system or package is growing as increasingly complex functions are needed in various data processing and communications devices. A measure of degree of integration, the number of logic gates, has been rapidly increasing since around three decades ago. This growth is mostly attributable to the rapid improvement of processor and communication technologies. The growth in logic complexity in integrated circuits over the past three decades is shown in Table 1.1, with each era's key turning points highlighted. To demonstrate the order-of-magnitude, the estimated circuit complexity in this case should only be seen as a few illustrative examples. A logic block may have ten to one hundred transistors, depending on the function.

Table 1.1: Evolution of integrated circuit logic complexity.

| **ERA** | **DATE** | **COMPLEXITY(number of logic blocks per chips)** |
|---|---|---|
| Single transistor | 1959 | Less than 1 |
| Unit logic(one gate) | 1960 | 1 |
| Multi-function | 1962 | 2-4 |
| Complex function | 1964 | 5-20 |
| Medium Scale Integration | 1967 | 20-200 |
| Large Scale Integration | 1972 | 200-2000 |
| Very Large Scale Integration | 1978 | 2000-20000 |
| Ultra Large Scale Integration | 1989 | 20000 |

The key takeaway from this is that logic complex per chip has been (and continues to be) growing exponentially. The following benefits are often offered by the monolithic integration of several functionalities on a single chip:

1. Less volume and area, and hence, compactness
2. Lower energy use
3. Fewer system-level testing needs
4. Greater dependability, primarily as a result of enhanced on-chip interconnects
5. Greater speed as a result of much shorter connecting distance
6. Considerable financial savings

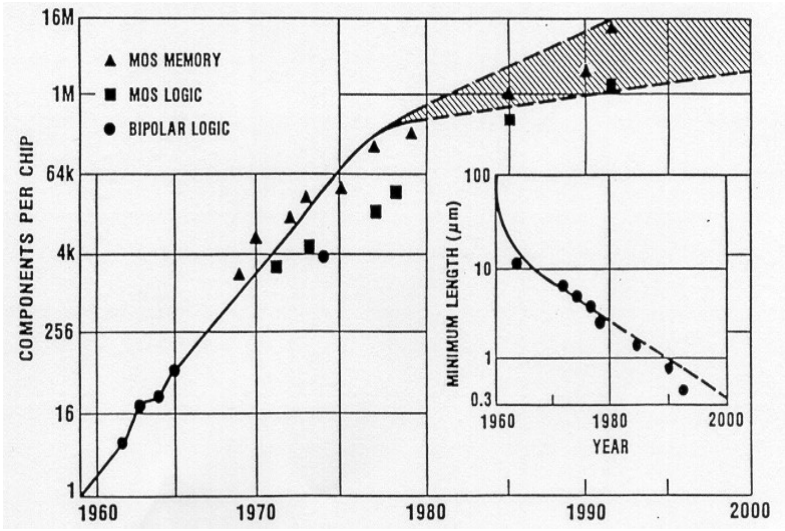


Figure 1.3: Early 1980s observations on the evolution of integration density and minimal feature size.

The present tendency of integration will thus probably last for a while. Improvements in the technology used to manufacture devices, notably the ongoing reduction of the minimum feature size (the smallest transistor or link that can be produced on a chip), promote this trend. Figure 1.3 shows the minimal feature size and previous and projected trends in chip complexity as of the early 1980s. In the year 2000, a minimum feature size of 0.3 microns was predicted. But real technology progress has far outpaced these forecasts. The first 64 Mbit DRAM and the INTEL Pentium CPU

chip, both with over 3 million transistors, were already in production by 1994, pushing the boundaries of integration density. As a result, integration density has exceeded estimates.

There is a notable disparity between memory chips and logic chips that must be taken into consideration when evaluating integrated circuit integration density. Beginning in 1970, Figure 1.4 depicts the advancement of chip integration for memory and logic devices. It is clear that in any given year, logic chips contain far fewer transistors than other types of semiconductors, mainly because complicated interconnects take up a lot of space on the chip. Memory circuits' high regularity makes it possible to integrate more cells while only using a small portion of the connection area.

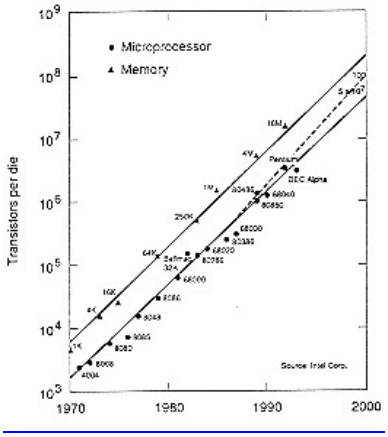


Figure 1.4: Level of integration for logic and memory chips through time

Logic circuits, such as those found in microprocessors and digital signal processors (DSP), may include a wide variety of functional units in addition to vast arrays of memory (SRAM) cells. Therefore, even if advanced memory chips contain certain intricate logic operations, it is considered that their design complexity is significantly higher than that of memory chips. The amount of transistors that must be integrated causes a nearly exponential rise in the difficulty of constructing a logic device. Design cycle time increases as a result of the delay between the beginning of chip fabrication and the delivery of mask-tape.

The chip development cycle must be short enough to allow for the maturation of chip production and quick distribution to users in order to fully employ the technology. Because of this, real logic integration frequently falls short of what is possible with

today's processing technology. To deal with the fast rising design complexity, sophisticated computer-aided design (CAD) tools and procedures have been created and are currently being used.

## 1.3 Vlsi Design Flow

The design process frequently has an evolutionary quality at certain phases. A specified set of requirements serves as the first step. The first design is made and compared to the requirements. The design must be modified if the requirements are not satisfied. The change in requirements and its effect analysis must be taken into consideration if an update is either impractical or too expensive. Most logic chips employ the Y-chart (originally proposed by D. Gajski) seen in Figure 1.5 to describe the design flow. On three different axes (domains), which resemble the letter Y, design activity is displayed.

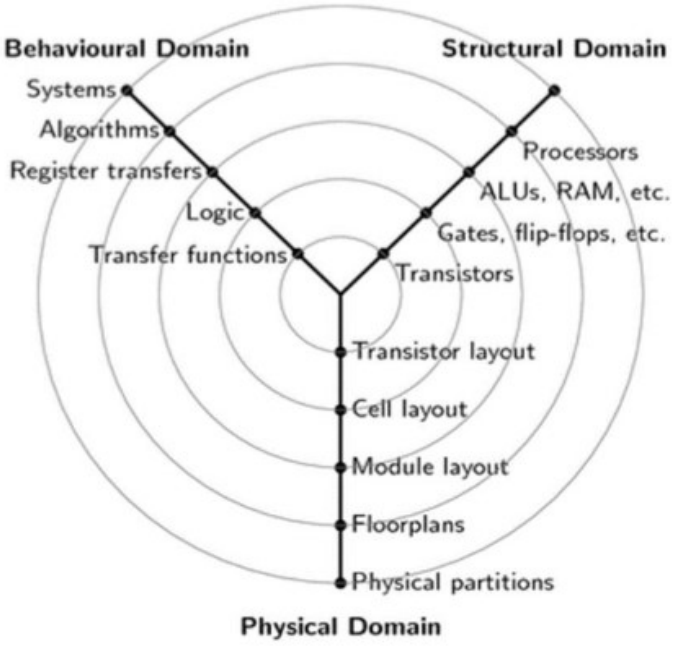


Figure 1.5: Three domains of a typical VLSI design flow (Y-chart depiction).

The three primary domains on the Y-chart are as follows:

1. Behavioral domain,
2. Structural domain,
3. Geometrical layout domain.

FSMs, which may be built using functional modules like registers and ALUs, are a popular technique for simulating the behaviour of digital circuits. Using a hardware description language like Verilog or VHDL to define the design at a lower level of abstraction is usually the next step once the behavioural design is finished. The various logic gates and connections that make up the design are defined here, along with their timing and power specifications. The next step is to synthesise the design into a set of digital signals that can be used to programme the semiconductor once it has been confirmed using simulation and other approaches.

To decrease the connection space and signal delays, modules are then automatically geometrically positioned onto the chip surface using CAD tools. The behavioural module is introduced at the start of the third evolution. Then, utilising leaf cells, numerous modules are constructed. Logic gates (leaf cells), which may be put and connected using cell placement & routing programme, are currently what define the semiconductor. After a thorough Boolean description of them, leaf cells and mask generation are implemented at the transistor level in the final development. Standard-cell-based design makes use of pre-made leaf cells that are kept in a library and used to build logic.

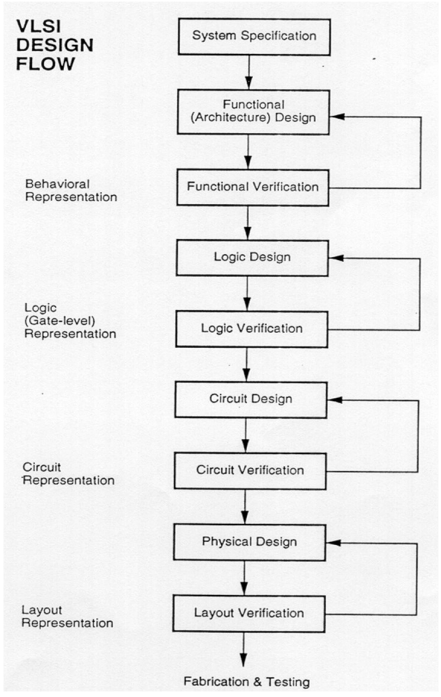


Figure 1.6: VLSI Design Flow chart

The VLSI design flow is depicted in a more condensed manner in Figure 1.6, taking into consideration the different representations or design abstractions, including behavioural, logical, circuit, and mask designs. Keep in mind that every phase of this procedure revolves on the verification of the design. Failure to thoroughly test a design in its early stages frequently results in substantial and pricy redesign at a later time point, lengthening the time to market.

There are actually a lot of back-and-forth modifications throughout the design process, notably between any two neighbouring phases and occasionally even pairings that are far apart, despite the fact that it has been simplified to look like a linear procedure. There isn't a completely unidirectional top-down design flow, despite the fact that it offers an excellent method for controlling the design process. Both top-down and bottom-up strategies must be used. For instance, it is entirely possible that the final chip layout might exceed the area limit of the available technology if a chip designer created an architecture without accurately anticipating the corresponding chip size.

To fit architecture inside the allowed area in such a case, it could be essential to remove some features and restart the design process. These modifications may need a significant change to the original specs. Thus, it is critical to quickly (bottom up) transfer low-level information to higher levels.

The sections that follow will go through the systematic methods of design and development that have been created over time to handle challenging hardware and software projects. Whatever the project's actual size, the foundations of structured design will increase the likelihood of success. Hierarchy, regularity, modularity, and locality are some of the traditional methods for simplifying IC design.

## 1.4 Design Hierarchy

The hierarchy technique, sometimes referred to as the "divide and conquer" strategy, calls for decomposing a module into smaller ones and then repeating the procedure on the smaller ones until the complexity of the bigger portions can be managed. This process is quite similar to how complex software programmes are split into ever-smaller pieces until subroutines with distinct functions, interfaces can created.

Three design categories for VLSI chips were introduced. An appropriate hierarchical structure may be specified for each section separately. The hierarchies in different domains must, however, be able to be easily mapped into one another for design simplicity.

Figure 1.7 provides a structural hierarchy demonstration by decomposing a CMOS four-bit adder into its component pieces. One-bit adders, single logic gates, and independent carry and sum circuits may all be created from the adder over time. At this lower level of the hierarchy, compared to the upper levels, it is much easier to create a basic circuit that implements a clearly defined Boolean function.

It is possible to break down a complicated system into its many important components, which will offer valuable direction for the actualization of these chip-based building blocks. Naturally, in order to produce a functional floorplan, the approximate form and size (area) of each sub-module should be estimated. In the area of physical description (geometrical layout), a four-bit adder is divided hierarchically into a floorplan. This adder model physically represents the exterior shape, input and output pin locations, and the capability of some signals (in this example, the carry signals) to go from one sub-block to another without the need for external routing.

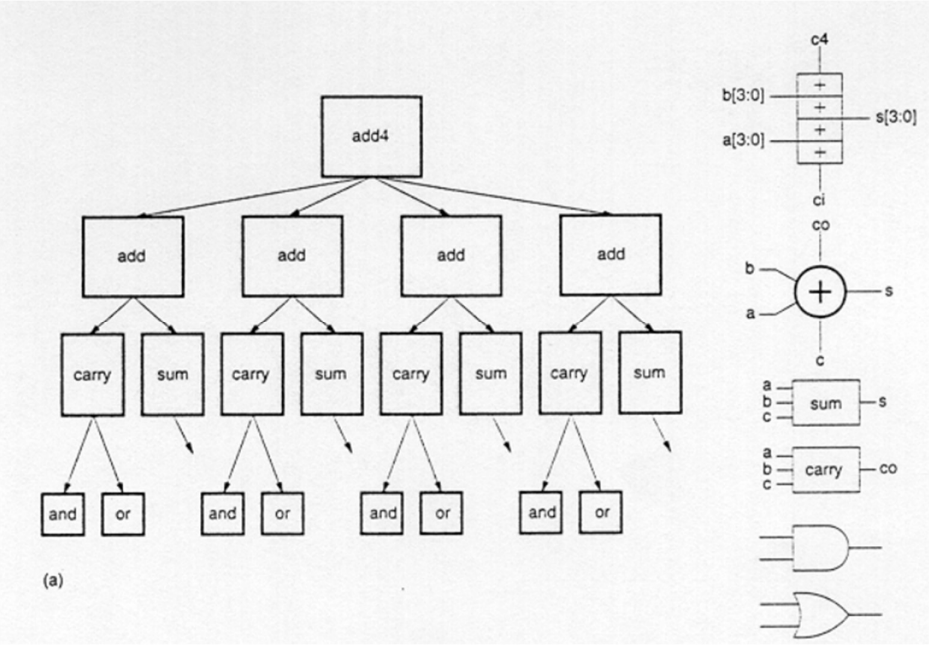


Figure 1.7: Four-bit adder circuit structural dissection, displaying the hierarchy all the way to the gate level.

## 1.5 Vlsi Design Styles

When implementing particular algorithms or logic functions on a device, a number of design strategies might be taken into consideration. Every design style has benefits and drawbacks of its own, so designers must choose wisely in order to provide functionality at a fair price.

### 1.5.1 Field programmable gate array (FPGA's)

Users can access fully completed FPGA chips that are ready for custom hardware programming to accomplish desired functionality. These chips contain programmable interconnects with hundreds or even more logic gates. With this design strategy, chips may be produced fast and economically, which is very useful for low-volume applications. I/O buffers, a collection of programmable logic blocks (CLBs), and programmable interconnect topologies make up the majority of FPGA devices. By programming RAM cells with output terminals attached to the gates of MOS pass transistors, the interconnects are configured. Figure 1.8 displays an FPGA from XILINX's complete design. Figure 1.9 provides a more in-depth look at the switch grids that are utilised for connection routing.

Figure 1.10 (model XC2000 from XILINX) depicts a basic CLB. It includes a look-up table, user-programmable multiplexers, an SR-latch, a clock input terminal, a clock signal terminal, four signal input terminals (A, B, C, and D). The truth table of the Boolean function is stored in the LUT, a digital memory. It may therefore produce any function with up to four variables or any combination of functions with three variables each. The control terminals for the multiplexers are not specifically depicted in Figure 1.10.

The CLB is made to allow for the programming of a wide range of logic operations to carry out various tasks. Additionally, more complicated CLBs have been developed to map complex functions. The behavioural specification of a device's functionality using a hardware description language, such as VHDL, is the first stage in the normal design cycle of an FPGA chip. Logic cells or circuits are then separated out of the final architecture (or technology-mapped). The chip design has been fully established at this point in terms of the easily available logic cells. The placement and

routing technique then designates the routing patterns between the logic cells in line with the netlist and allocates specific logic cells to FPGA sites (CLBs).

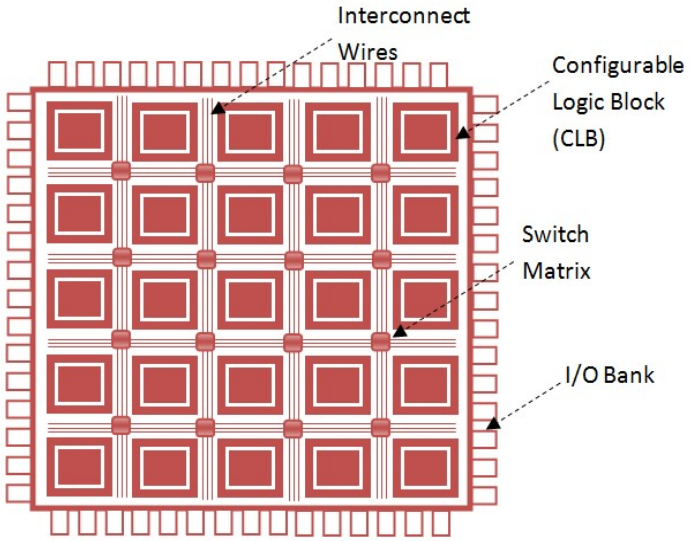


Figure 1.8: The design of Xilinx FPGAs

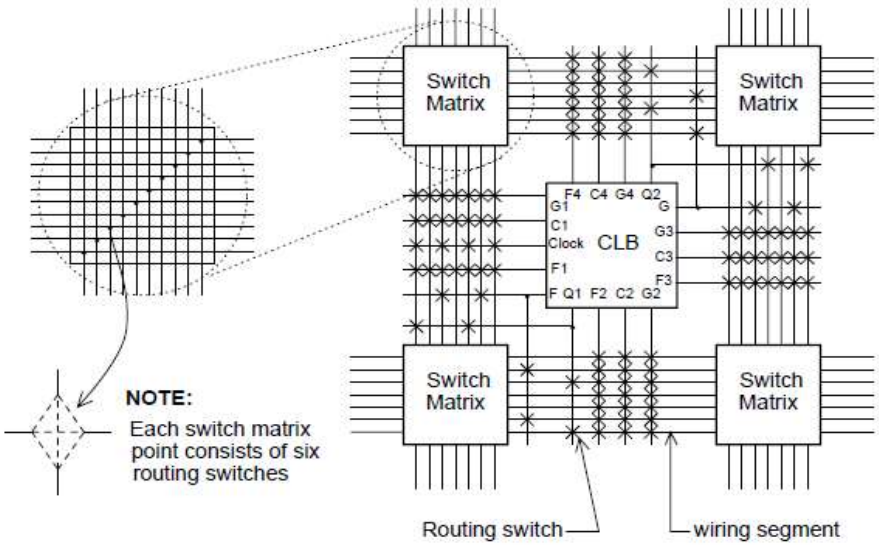


Figure 1.9: Switch matrix details, including interconnection routing between CLBs.

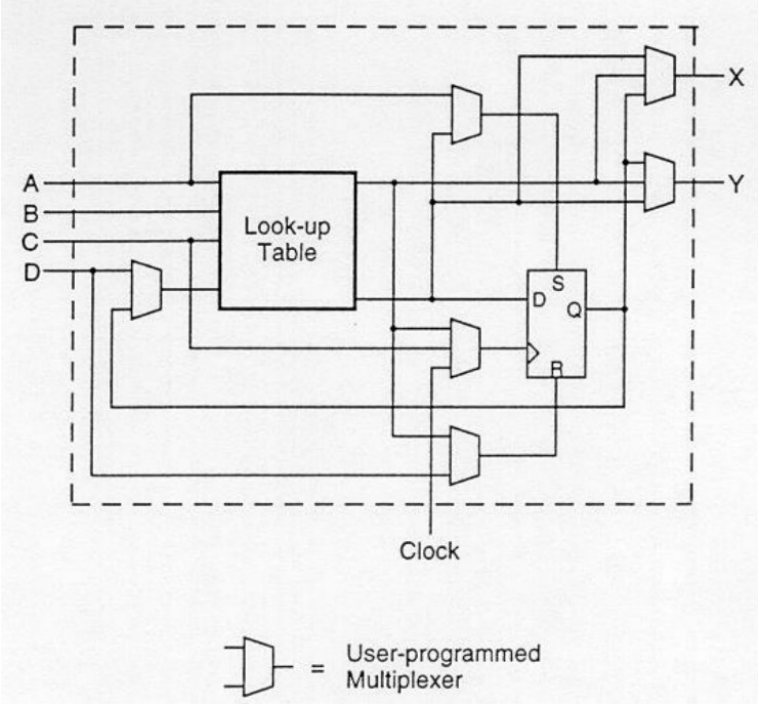


Figure 1.10: XC2000 CLB of the Xilinx FPGA.

Prior to downloading the design to programming an FPGA device, the performance of the design may be simulated and confirmed. As long as the chip is turned on or until fresh programming is completed, the chip's programming is still in effect. Most of the time, it is challenging to use the entire FPGA chip surface since some cell locations could be empty.

The key advantage of FPGA-based design is the quickest turnaround time, or the length of time required from the beginning of the design process until a functional device is ready. After the design is mapped onto a certain technology, a functioning prototype may be made accessible virtually instantly since the FPGA chip can be changed without necessitating any actual manufacturing procedures. For the same design, FPGA chips are frequently more expensive than alternative realisation choices (such as gate array or conventional cells), but they are a particularly attractive option for small-batch ASIC chip fabrication and fast prototyping.

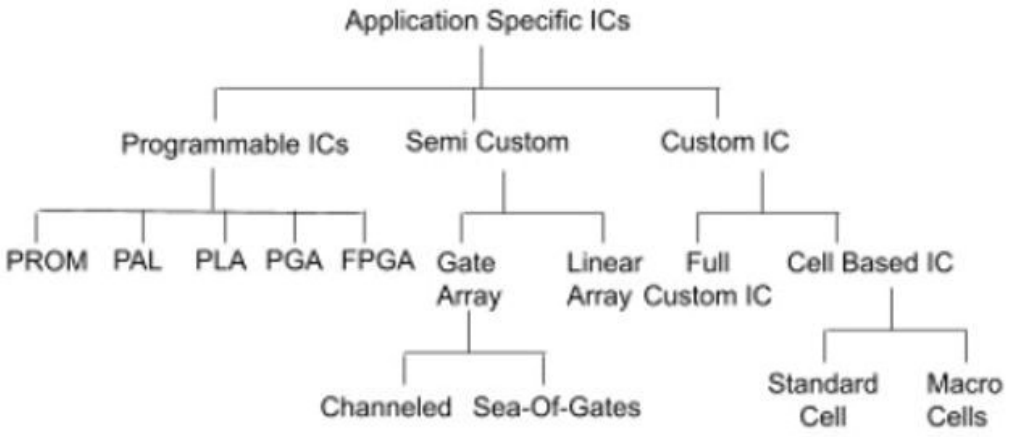


Figure 1.11: VLSI design styles

## 1.6 Existing Method

The source-to-drain channel current of a MOSFET is voltage-controlled and influenced by the gate control voltage, as is widely known. As technology advanced and channel length shrunk ever-further, leakages resulted as the gate's ability to regulate the channel current began to diminish. Many technologies, including FinFETs, have been created because it was challenging to manage the channel. In a FinFET, the gate has more control over the channel than in a CMOS device since it surrounds the channel, minimising leakages.

There are a number of phenomena that contribute to MOSFET leakage, including:

A little amount of charge leakage between the source and drain occurs when the gate control voltage is lower than the threshold voltage. gates open It is well knowledge that as devices get smaller, the gate oxide gets thinner. Gate leakages are as a result of electrons tunnelling between the gate oxide and substrate. The total number of device leakages may be impacted by a variety of unique situations.

Leakages are avoided using a variety of techniques, including transistor stacking, a sleep mode approach, the sleep keeper technique, low power retention strategy, and many more. Each of these approaches has benefits and drawbacks that might lead to a wider area and a longer response time.

# Chapter-2
# Literature Review

In [1] S. A. Tawfik and V. Kursun, Jan. 2011, described about unique independently-gated sequential circuits, work-function, and gate-drain/source overlap engineering are shown employing multi-threshold voltage (multi) FinFETs. The multi-sequential circuits are capable of reducing total active mode power consumption, clock power, and average leakage power by up to 55%, 29%, and 53%, respectively, while maintaining similar data stability and speed, when compared to single-threshold voltage (single-) tied-32 nm-gate FinFET technology. In addition, compared to circuits using single-tied-gate FinFETs, the novel sequential circuits provide an area decrease of up to 21%. It should be mentioned that synchronised integrated circuits (ICs) typically use static latches and flip-flops. [3] asserts that the clock subsystem, which accounts for 33% of power consumption in synchronous systems like high-speed microprocessors, has a substantial role. Therefore, brute-force sequential circuits with less complex circuitry and lower clock demands are needed for modern integrated circuits [3], [4]. This work offers novel, small, and clock-load-efficient FinFET latches and flip-flops. The development of multi-threshold voltage (multi-) tied-gate FinFET sequential circuits with lower power consumption than customary single-threshold voltage (single-) tied-gate FinFET circuits is the result of research into independent-gate bias, work-function engineering, and gate-drain/source overlap engineering. Sequential circuits using FinFET technology and a 32 nm gate were disclosed in a prior research by Medici [5].

IN [2] L. LI and J. HU, 2009, explained about Modern CMOS circuits must take leakage current's power cost into account since it is too crucial to ignore. Dual-threshold techniques can be applied to solve this problem by reducing leakage power. In particular, high-threshold transistors are used in non-essential lines to reduce leakage current while low-threshold transistors used in key channels of circuits improve performance. In order to reduce its leakage power, this work offers a revolutionary dual-threshold CMOS-based gearbox gate flip-flop. Simulated findings show that, in comparison to single-threshold transmission gate and gate-length biassing flip-flops, the proposed dual-threshold transmission gate flip-flop decreases leakage power by 40–

50% and power consumption by 20–30%. The suggested flip-flop is a great option for low-power VLSI designs needed for deep sub-micron integrated circuits. Reducing the use of power has been a critical factor in contemporary VLSI circuits as portable and wireless electronic device usage increases [1-3]. The loss of energy in CMOS digital circuitry consists of both dynamic and static elements. Because dynamic power is proportional to VDD squared, lowering the supply voltage VDD is the most efficient way to cut electrical usage when dynamic power is dominating. To maintain performance standards, transistor threshold voltage must also be adjusted when the supply voltage is decreased. In low-voltage and high-performance circuits, leakage current can unfortunately quickly grow due to this scaling, which is a serious problem. There are several methods for lowering the leakage power of sequential circuits. By using high-speed, low threshold voltage (VT) transistors for logic cells and low leakage, high VT devices for sleep transistors, MTCMOS (Multiple Threshold CMOS) technology offers both low leakage and high performance operation [4-6]. When the system is in the active state, however, the employment of sleep transistors can increase dynamic power and slow down logic cells. In order to solve this problem, the leaky feedback approach is used to keep an active channel on one rail when the system is in sleep mode [9]. The feedback balloon is a useful method for cutting leakage current, but because of the significant increase in dynamic power and area, it has a negative impact on performance. The gate-length biassing flip-flop was created on the premise that a minimal size inverter's gate length may be increased by 8nm to provide a 30% reduction leakage power with a 5% high in delay [7]. When the leakage power and latency are identical, however, the reduction in leakage power is constrained. For delay-constrained circuits, a novel flip-flop based on dual-threshold technology is suggested in this work. The suggested flip-flop reduces leakage current while retaining performance by employing high-threshold transistors in non-essential circuits and low-threshold transistors in important logic circuits.

In [3] A. K. Kuna, K. Kandpal and K. B. R. Teja, 2017, explained about the design of a low-power flip-flop utilising FinFET technology is the main topic of this study. An inverter was used as the foundational digital circuit to examine the properties of p-FinFETs and n-FinFETs in various combinations. The flip-flop was constructed using a multiplexer-based method for demonstrative purposes. Utilising the Predictive Technology Model (PTM) FinFET 32nm library, the designs were put into practise on

HSPICE. Due to its low power consumption and cheap cost per chip, CMOS technology has been a preferred option for electronic designers for a number of decades. The built-in flip-flops run at 0.9V and use 11.4 W of power. Due to the limits of CMOS technology, researchers are looking towards other device designs and materials such FinFETs, nanowires, and carbon nanotubes to continue the advancement of electronics [3]. By lowering leakage current, these technologies have the potential to improve device performance and minimise power usage. It could take some time for these technologies to become widely used in the electronics sector because there are still issues with production and design that need to be resolved. Nevertheless, the area of electronics is still relentlessly pursuing innovation and advancement, and new and interesting advancements are undoubtedly in store for the future. In fact, it takes a lot of money and research to create new technologies that solve the problems of minimising static power usage. Although there are several intriguing alternatives, like CNTFET, Tunnel FET, and MUGFET, their usability and scalability need to be assessed and improved. In addition, new industrial infrastructure must be built, which may be expensive and time-consuming. Therefore, in order to achieve the needed reductions in power consumption and performance, it is imperative to strike a balance between researching new technologies and improving the already-existing ones. The design of the flip-flop itself is then described while keeping in mind the special features of FinFET technology. Analysis is done on the effect that the flip-flop's fin width, gate length, and doping concentration have on its performance. The suggested FinFET-based flip-flop delivers a considerable decrease in leakage power when compared to a traditional CMOS flip-flop, according to simulation findings using the BSIM-CMG model. The FinFET-based flip-flop also provides better performance in terms of latency and power use. As a result, the future of FinFET technology holds enormous promise for less-power and good-performance applications.

In [3] D. S. Bhutada, 2016, explained about a possible method for low-voltage flip-flops is to use CPAL circuits. Complementary pass-transistor adiabatic logic flip-flop circuits with low voltage medium and quicker operation may be implemented using DTCMOS methods. The results show that CPAL with power-gating offers flip-flop functionality and boosts execution performance when the circuits are simulated using 180nm Tanner model technology and different supply voltages. Because it may minimise the number of transistors, the power-clock approach is very helpful for

constructing flip-flops for two phase sequential circuits. Designing digital circuits using adiabatic logic power consumption by reusing energy that would otherwise be lost in the form of wasted as heat. Adiabatic circuits work by recycling energy from a gate's output to its input. Energy used by a circuit during switching may be considerably reduced using this method, but it also adds complexity in the form of charge pumps and other energy recovery circuits. Adiabatic logic may greatly minimise dynamic power dissipation, which contributes significantly to overall power consumption in contemporary CMOS devices, which is one of its key advantages. Adiabatic circuits can improve performance and extend battery life in mobile devices and other low-power applications by lowering dynamic power dissipation. However, adiabatic logic is not without flaws. Adiabatic circuit implementation requires more complexity, which can lead to a bigger circuit area and longer design durations. Electrostatic discharge (ESD) and other reliability concerns can also become more likely when charge pumps and other energy recovery circuits are used at high voltages. Power clocks are used in this clocking technique and signal waveform; they are continually charged and discharged to reduce energy loss. By shutting off adiabatic units during idle states, the power-gating strategy further minimises dynamic and leakage power, resulting in overall energy savings. In high-performance applications where power dissipation is a substantial barrier, adiabatic circuits are particularly helpful. However, leakage dissipation in adiabatic circuits has also grown to be a crucial aspect to take into account as CMOS technology develops and threshold voltage drops. But these problems can be lessened and adiabatic circuits can still be used in low-power applications by using power-gating and other energy-saving methods. In adiabatic circuits, DTCMOS methods are utilised to reduce leakage current. Two threshold voltages are used in the DTCMOS technology to reduce leakage current. Through the use of dynamic node feedback mechanisms, the output node's static power loss may be decreased. Using this technique, the input stage receives the output node voltage after sensing it. The supply voltage for the following phase is then drawn from the feedback voltage of the output node. Furthermore, the power dissipation of the adiabatic circuits is decreased by using the diode clamp approach. In order to prevent overcharging of the power-clock generator, the diode clamp approach makes use of two diodes and a capacitor.

In [4] A. Kumar, Y. Kumar and D. Berwal 2016, explained about the flip-flop's suggested design makes use of a number of strategies to cut down on power usage and boost performance. The pulse generator control logic design uses an EXOR gate and an inverter chain to simplify the circuit and eliminate pointless switching, which lowers power consumption. Additionally tuned for power efficiency, the signal feed-through method speeds up charging and discharging along the crucial channel only when necessary. Multi-threshold CMOS technology also used lessen power loss. Less transistors are used in the pulse-generation circuit, which results in a more compact and power-efficient design. Overall, the suggested design offers an enhanced performance low power option. Designing low-power VLSI systems consequently requires minimising power consumption in the clock subsystem. This objective may be greatly advanced by the suggested dual edge-triggered, low power, multi-threshold CMOS-based flip-flop device. Power dissipation is decreased while performance is maintained thanks to the adoption of multi-threshold CMOS technology and an improved pulse generator control logic architecture. The suggested architecture is hence perfect for battery-operated portable devices that demand both great performance and low power consumption. The suggested design outperforms existing FF designs under study in terms of power-delay product performance, according to the findings of post-layout simulations based on CMOS 90-nm technology. Overall, it can be said that the suggested architecture represents a significant advancement towards the creation of low-power, high-performance VLSI systems for contemporary portable devices. The advantages and drawbacks of these numerous methods for building flip-flops vary in terms of speed, power consumption, and surface area. Compared to previous FF designs investigated, the proposed design in this study, which makes use of multi-threshold CMOS technology and optimised pulse generator control logic, has been demonstrated to have better power-delay product performance. Particularly in battery-operated portable devices where power economy is critical, the introduction of such energy-efficient FFs can dramatically lower the overall power consumption of VLSI systems. The requirement for low-power, high-performance VLSI systems will only increase as technology develops and device sizes get smaller, making the creation of energy-efficient FFs a crucial field of study. That's accurate. Double-edge-triggered flip-flops (DETFF) can function at half the frequency of SETFFs while still maintaining the same data throughput because they can store data on both rising and falling edges of clock.

Performance is enhanced and power consumption is reduced as a consequence. Modern microprocessors frequently employ DETFFs to provide excellent performance with little power consumption. Multi-Threshold CMOS, or MTCMOS, is a method for lowering sub-threshold leakage power in digital circuits. It operates by combining MOSFETs with high- and low-threshold voltages on a single chip, enabling selectable power gating of various circuitry. MTCMOS may dramatically lower overall power consumption while retaining circuit performance by utilising high-threshold voltage devices in regions with low switching activity and low-threshold voltage devices in regions with high switching activity.

This paper discusses techniques with several thresholds. In comparison to single threshold sequential circuits, the proposed multi-threshold method significantly reduces power consumption, average power, and clock power while maintaining about the same speed and data stability. The development of sequential circuits makes use of 32nm FinFET technology.

# Chapter – 3
# Methodology

## 3.1 Proposed Method

The first step of this study's research is examining FinFET technology and its many qualities in comparison to CMOS technology.

### 3.1.1 FinFET Technology

FinFET (Fin Field Effect Transistor) is a type of transistor that has become increasingly popular in the semiconductor industry due to its superior electrical performance compared to other types of transistors. The FinFET is a 3D transistor design that provides better control over current flow and allows for smaller, more power-efficient chips.

The FinFET transistor gets its name from the "fin" structure, which is a vertical, raised channel on the silicon substrate that acts as the transistor's gate. The fin is surrounded on three sides by a gate electrode, which is separated from the fin by a thin layer of insulating material.

The key advantage of the FinFET over the traditional planar transistor design is that it provides better control over the flow of electrons. The raised fin structure provides additional surface area for the gate electrode, allowing for better control of the channel and reducing leakage current. This improved control also results in faster switching speeds and lower power consumption.

FinFETs are a simple replacement for MOSFETs in the future due to the similarity in the production process. Dual gate transistors, or FinFETs, are essentially quasi-planer in nature. The single gate in a planar FET regulates the source-drain channel. Even when the gate is off, leak currents between the source and the drain occur due to this gate's poor electrostatic field management away from the channel surface near to the gate. In contrast, the transistor channel in a FinFET is a narrow, vertical fin, and the gate completely encircles the channel between the source and the drain. You may think of the FinFET segment as having several gates enclosing the thin channel. A

multiple gate can entirely exhaust the carrier channel. Better voltage control of the channel and thus better electrical properties result from this.

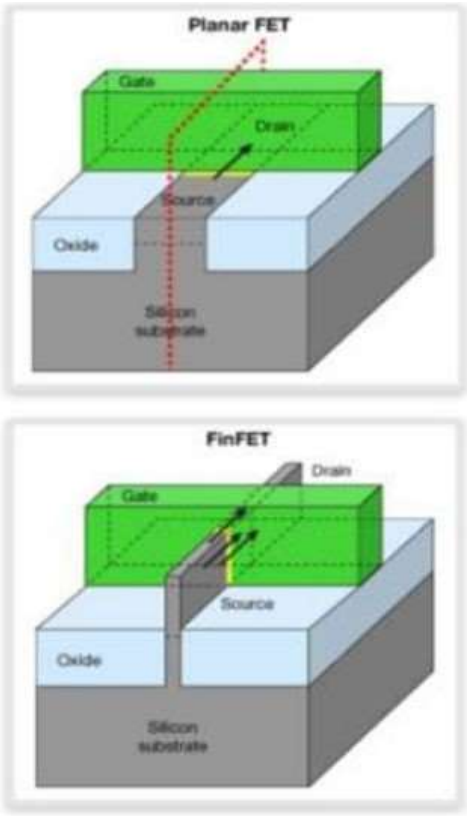


Figure 3.1: Planar FET, FINFET

### 3.1.2 Master-Slave Data Flip-Flop

Through the use of a master-slave flip-flop, a type of digital circuit, one piece of information may be saved. It is often employed in sequential logic circuits like counters, shift registers, and control circuits in digital electronics. The Master-Slave flip-flop is made up of the master and slave stages. The Master-Slave flip-flop has the advantage of being edge-triggered, which means that the output changes only at the rising or falling edge of the clock signal. This makes it more reliable and less prone to glitches and noise in the input signal.

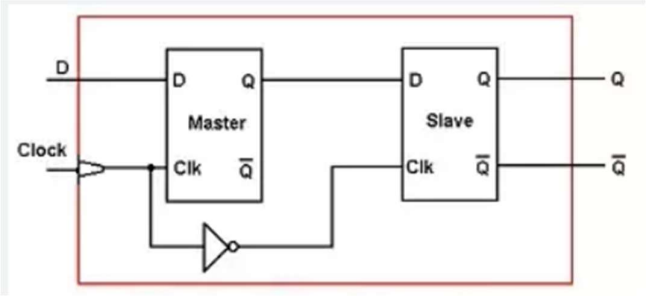


Figure 3.2: Master-Slave data flip-flop

## 3.2 Introduction to Verilog

A common hardware description language in the semiconductor and electrical design industries is Verilog HDL. At many levels of abstraction, including RTL (register-transfer level), gate-level, and behavioural levels, it is used to describe and simulate digital systems and circuits. ASIC design, FPGA prototyping, and digital signal processing are just a few of the many applications that Verilog HDL is appropriate for since it provides both behavioural and structural modelling. Along with other verification languages and tools, it is frequently used in the verification of digital and mixed-signal circuits.

### 3.2.1 Overview

Blocking assignments (=) in Verilog HDL are assessed sequentially, whereas non-blocking assignments (=) are examined simultaneously. This implies that non-blocking assignments enable more realistic modelling of hardware behaviour, whereas blocking assignments might result in race situations and unanticipated behaviour, especially in bigger systems. In addition, Verilog HDL has structures for defining the timing and behaviour of signals, including edge-triggered behaviour, events, and delays. These constructs are crucial for simulating the behaviour of electrical systems.

Verilog's language semantics enabled designers to provide a comparatively short and succinct description of complex circuits. For circuit designers who previously used graphical schematic capture software and custom-written software programmes to describe and simulate electrical circuits, this represented a significant productivity increase. Designers may build a thorough model of a circuit in Verilog and simulate it

in software, allowing them to find mistakes before incurring the cost of building a physical prototype. Verilog further made it simpler to make modifications to a design because the circuit description was in a text file that could be altered as opposed to a graphical schematic that required redecorating.

In addition, Verilog has special capabilities and techniques designed specifically for hardware description, such as the ability to define timing and delay, input/output port declarations, and module definitions and instantiation. Additionally, Verilog allows for the definition of unique functions and modules in addition to having built-in primitives for frequently used digital logic gates. Overall, Verilog is a valuable tool for hardware engineers since its syntax and semantics are adapted to the requirements of designing electrical circuits.

To be clear, Verilog is really regarded as a hardware description language (HDL), which is a specialised kind of language used for modelling and developing electrical circuits, although having certain features of a dataflow language. Verilog is not a true dataflow language in the sense that it does not depict a system as a collection of interconnected functional blocks, but it does allow for the description of a circuit's behaviour in terms of the flow of data across it. Instead, it represents the whole system as a group of linked hardware parts. The mix of concurrent and sequential statements in Verilog enables designers to succinctly and modularly describe the complicated behaviour of electrical systems.

Additionally, the 'reg' type is used in Verilog to define variables that may maintain a value over time and can be used to represent both state components (like flip-flops) and combinational logic. Unlike wires, registers have no associated strengths and may only have a value given to them within a procedural block (such as a "always" block). Depending on whether a flip-flop is positive-edge or negative-edge activated, a "reg" used to simulate a state element is often given a value on the rising edge or falling edge of a clock signal.

At the register-transfer level (RTL) abstraction level, synthesizable Verilog code defines a design's digital hardware functionality such that it may be translated into a gate-level netlist by synthesis tools. This netlist contains the design's digital logic as gates, registers, and interconnects that may be programmed into FPGAs or utilised to make ASICs. The quality of the Verilog code and the optimisations carried out by the

synthesis tools determine the quality of the netlist and the effectiveness of the final circuit.

## 3.3 History

### 3.3.1 Beginning

The first contemporary hardware description language was Verilog. During the winter of 1983/1984, Phil Moorby and Prabhu Goel came up with it. This procedure was referred to as "Automated Integrated Design Systems" as a hardware modelling language, but it was later renamed to "Gateway Design Automation" in 1985. In 1990, Cadence Design Systems bought Gateway Design Automation. The Verilog software from Gateway and Verilog-XL HDL simulator, which would eventually become the industry standard for Verilog logic simulators over the following ten years, are now fully owned by Cadence. Verilog was first designed to describe and enable simulation; synthesis functionality was added later.

### 3.3.2 Verilog-95

Cadence made the decision to openly standardise VHDL in response to the language's rising popularity at the time. Under the auspices of Open Verilog International (OVI), which is now known as Accellera, Cadence released Verilog into the public domain. Later, Verilog submitted to IEEE where it was accepted as IEEE Standard 1364-1995, also known as Verilog-95.

In order to complement their Spectre circuit simulator, Cadence Design Systems created Verilog-A, an analogue hardware description language. It is a subset of Verilog-AMS, a unified hardware description language for analogue and mixed-signal devices that combines the behavioural modelling components of Verilog-A, Verilog-D, and Verilog-AMS. By providing new constructs for defining mixed-signal systems that use both analogue and digital components, Verilog-AMS expands on Verilog-95.

### 3.3.3 Verilog-2001

A revision of the Verilog-95 standard, Verilog-2001 adds a number of new capabilities, such as generate constructs, user-defined jobs and functions, and new data types including bit vectors and structures. These additional characteristics greatly

increased the language's strength and versatility, enabling it to describe increasingly complicated digital systems.

User-defined primitives, improved testing capabilities, and greater support for reusable intellectual property (IP) blocks through the usage of generate blocks are additional features added to Verilog-2001. The always comb block, which makes it simpler to design and comprehend combinational logic, was also included in Verilog-2001. The ability to specify and utilise enumerated types is another important improvement that makes code easier to comprehend and maintain. Verilog-2001 also provides enhancements to the simulation and verification process, including as coverage analysis and assertions.

Similar to VHDL, Verilog-2001 contains a generate/endgenerate construct that allows for conventional case/if/else decision-making to control the instantiation of instances and statements. With the use of the generate/endgenerate commands, Verilog-2001 may create an array of instances with control over how each instance is connected to the others. File I/O has improved due to the installation of several extra system jobs. The usage of named parameter overrides, always @*, and header declarations for functions, tasks, and modules in the C style are just a few of the grammatical modifications that have been implemented to improve code readability.

### 3.3.4 Verilog-2005

The modelling analogue and mixed-signal systems is supported through Verilog-AMS (Analogue Mixed-Signal) extension. Additionally, it offers continuous-time and discrete-time signals, analogue and digital controllers, and device models for modelling analogue signals and systems at the system level. To overcome Verilog's limitations in simulating and modelling analogue and mixed-signal systems, Verilog-AMS was created. It is now a widely accepted standard for mixed-signal design and verification and has been adopted by several EDA tool providers.

### 3.3.5 System Verilog

Accellera, a standards body, created System Verilog, which became the first version to be standardised as IEEE Standard 1800-2005 in 2005. Later, in 2009, it was updated and became IEEE Standard 1800-2009. Although System Verilog does contain features from Open Vera and other hardware verification languages, it is a superset of

Verilog-2005. Constrained random testing, coverage analysis, assertions, and object-oriented programming techniques are a few of the significant new features added to System Verilog. In the semiconductor industry, the System Verilog language is frequently used for the design and verification of sophisticated digital systems.

The System Verilog language was developed by the IEEE and first became standardised in 2005. Assertions, coverage, and limited random testing are some of the extra verification capabilities added to System Verilog, a hardware description and verification language that builds on Verilog. The tools for higher-level design description in System Verilog additionally include class-based object-oriented programming techniques and interfaces. In the semiconductor sector, it is now often utilised for both design and verification.

A wide range of capabilities for design verification are offered by System Verilog, including potent structures for creating testbenches and confirming the accuracy of designs. Its HVL characteristics make it simpler to build extensive test environments by enabling higher-level, more abstract modelling of complicated test situations. It is also simpler to create and maintain test benches and designs over time due to the uniformity of the syntax across projects.

Typical HVL characteristics that set it apart from Hardware Description Languages like Verilog or VHDL include the following:

1. Constrained Random Testing (CRT): HVLs offer built-in capability for generating testbenches that create stimuli randomly and assess responses. Through the use of CRT, test scenarios may be developed automatically depending on particular restrictions, significantly expanding the coverage of the design being evaluated.
2. Functional Coverage: HVLs come with built-in support for creating coverage metrics that quantify how much of the design the testbench has actually exercised. This enables the designer to identify which elements of the design have been tried and which have not, allowing for more thorough testing.
3. Assertions: HVLs offer built-in capability for constructing assertions that determine whether or not specific conditions are true. These may be used to verify that the design being tested is valid and can aid in finding defects early in the design phase.

4. OOP: HVLs enable OOP ideas like inheritance, encapsulation, and polymorphism, which promote more modular and reusable programming. Complex testbenches may be easier to create and manage as a result.
5. Data Types: Complex data types like arrays, structures, and classes are supported natively by HVLs. This makes it simpler to create test cases that simulate intricate systems.
6. Integration with Simulation Tools: HVLs are intended to integrate easily with simulation tools, making test result analysis and troubleshooting simple.

All things considered, HVLs provide a more potent and adaptable technique to build test benches for confirming hardware designs and are a crucial instrument for assuring the calibre and dependability of contemporary electronic systems.

Advanced constructs are available in an HVL like System Verilog to build test benches that more accurately simulate a design's behaviour in real-world situations. By offering features. HVLs provide more effective and efficient verification as well as better debugging capabilities. With the aid of these characteristics, elaborate, extendable, reusable test benches may be created, increasing the productivity and efficiency of the verification process.

Coverage-driven verification (CDV) checks that all corner cases have been evaluated and that the design has been adequately tested. To cut down on verification time and effort while boosting design confidence, CDV combines automatic test creation, self-checking test benches, and coverage metrics. The design's test coverage is determined by the coverage metrics, and the findings are utilised to direct further testing. The built-in support for coverage metrics in System Verilog enables designers to generate and examine coverage data throughout simulation. The final design's quality and dependability are considerably increased when CDV methods are used in System Verilog.

# Chapter 4

# Implementation

## 4.1 FinFET Technology

MOSFETs are referred to as voltage-controlled devices because the voltage applied to the gate controls how much current flows in the channel between the source and drain. The gate's ability to control the channel current has, however, deteriorated due to technological developments and the ongoing reduction in channel length, which has led to leakage problems. FinFETs are one of the many devices that have been introduced to address this issue. When compared to CMOS, the FinFET gate has greater control over the channel because it surrounds it, which reduces leakage. MOSFETs are often used transistors in digital circuits, according to research literature, and memory chips or microprocessors frequently contain billions of them. The pros and cons of each technology are discussed as the paper compares and contrasts CMOS and FinFET. Future sections in this series will focus on specific features of FinFETs that set them apart from conventional MOS transistors. Scaling conventional MOSFET transistors has become more challenging as a result of the severe short channel effects, especially for dimensions below 32 nm. The narrowing of the width and length of MOS devices has resulted in decreased performance and increased average power consumption.

Many significant challenges have been satisfactorily resolved by the FinFET technology with the steady scaling of planar bulk CMOS. A FinFET is a multi-gate (MOSFET). The term "Fin Field Effect Transistor" was initially coined in 2001 by researchers at the University of California, Berkeley, including Professors Tsu-Jae King-Liu, Chenming Hu, and Jeffrey Bokor. It explains a non-planar double-gate transistor built on an SOI substrate. A thin silicon film is wrapped around a conductive channel to provide the appearance of a set of fins in the body of a FinFET. FinFETs have a lot of potential as bulk MOS transistor substitutes at the nanoscale. Notably, FinFETs are produced using methods that are quite similar to those that are employed to produce traditional MOS transistors. Due to their identical production processes, FinFETs may eventually succeed where MOSFETs once did. FinFETs are a member of the dual-gate transistor (DG) family. In a typical planar FET, the channel between the source and drain is controlled by a single gate.

Therefore, even when the gate is closed, leakage currents may still flow between the source and drain. The gate entirely encircles the channel between the source and drain in a FinFET, where the transistor channel resembles a slender, vertical fin. The FinFET structure is composed of several gates that surround the narrow channel. Multiple gates can be used to completely drain the carrier channel, improving electrical properties and enhancing voltage control.

## 4.2 Complementary Metal-Oxide Semiconductor

The basis for integrated circuits (ICs) in a range of applications, CMOS is one of the most widely utilised MOSFET technologies now in use. It is also still widely employed in the computer chip design industry. The robust noise immunity and low static power consumption of CMOS contribute significantly to its appeal. In CMOS devices, just the transistor switching operation uses a significant amount of power. Furthermore, CMOS devices do not generate thermal noise like other logic types like transistor-transistor logic (TTL). CMOS technology enables the integration of a large number of logic functions into a single chip. of a pull-down network of CMOS gates, n-type MOSFETs are stacked between the output and the low-voltage power supply. Instead of the load resistances found in NMOS logical gates, the pull-up and high-voltage network uses p-type MOSFETs. When both types of transistors (n and p) have their gates linked to the same input, the p-type MOSFET will turn on when the n-type MOSFET is off, and vice versa. As seen in the image below, the connection is set up so that one transistor is on and the other is off for each specific input pattern.

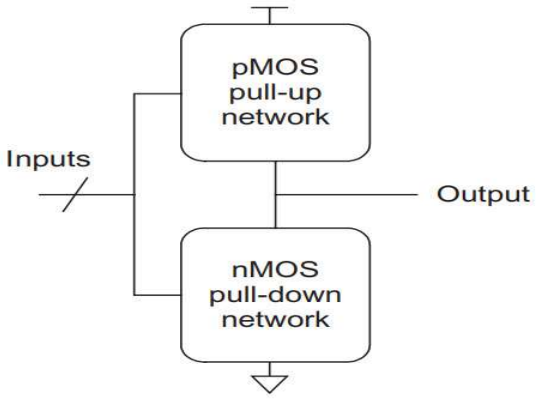


Figure 4.1: Schematic diagram of CMOS

The input resistance of CMOS inverters is quite high because of the features of the MOS transistor's gate, which performs as almost a perfect insulator and draws very little DC input current. As a result, when the input node of the inverter is merely linked to transistor gates, the input current is almost zero in the steady-state condition.

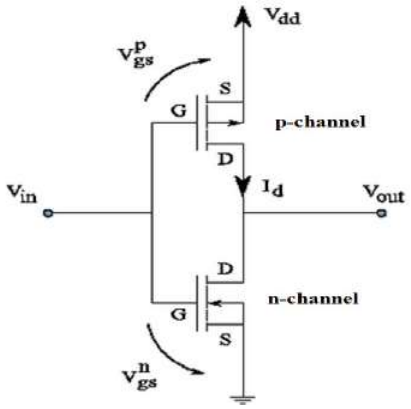


Figure 4.2: CMOS inverter

Hisamato et al. conceptualised the fully-depleted lean channel transistor (DELTA), the first iteration of FinFET technology, as a double-gate Silicon-On-Insulator (SOI) structure in 1989 [2]. A FinFET typically has a body surrounded by gates that are either shorted or independent on each side of the body on a silicon insulator substrate. FinFETs have two gates that can be used either separately or together. By adjusting the voltage on one gate, the threshold voltage can be controlled. By reducing leakage current and power dissipation, FinFET devices have the potential to boost performance because the front and rear gates can be regulated separately or concurrently.

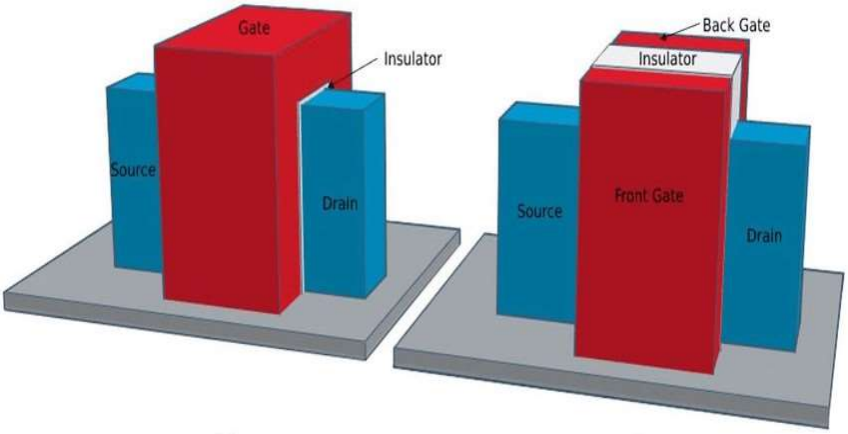


Figure 4.3: Short-Gate FINFET (b) Independent Gate FINFET

Three-terminal (3T) FinFETs are usually used to describe FinFETs with shorter gates, whereas four-terminal (4T) FinFETs are used to describe those with independent gates. Unlike 3T FinFETs, which have the gates physically shorted at both the front and the back, 4T FinFETs have the gates physically isolated from one another. 3T FinFETs have higher on-current (I_on) and off-current (I_off or subthreshold current) than 4T FinFETs. 4T FinFETs offer the option of applying different signals or voltages to both gates, in contrast to CMOS devices.

## 4.3 Multi Threshold Technique

The multi-threshold Technique, also known as the multi-Vt (Voltage threshold) technique, is used by integrated circuits to maximise power consumption and performance. It involves using transistors with different threshold voltage levels in the same circuit, allowing for better control over power consumption and performance trade-offs.

By using transistors with a range of threshold voltages, the circuit designer may selectively alter the power supply voltage to different circuit components. High-performance areas can run at a higher voltage to assure faster switching rates, while low-power zones can run at a lower voltage to conserve energy. In battery-operated devices and other applications where power efficiency is crucial, the multi-threshold approach is highly useful.

Leakage in MOSFETs is mostly caused by two fundamental processes:

Subthreshold Leakage: This is the current that flows through a MOSFET's channel even when the gate voltage is lower than the threshold voltage. It occurs as a result of quantum mechanically induced carrier tunnelling through thin gate oxide. Subthreshold leakage increases significantly when the transistor is in the off state or operating at low voltages.

Gate Leakage: Gate leakage is the current that flows through the gate terminal of a MOSFET. Gate oxide's poor ability to act as an insulator results in current leakage between the gate and channel. Gate leakage may occur directly via the gate oxide or indirectly by carrier diffusion from the source/drain regions into the gate.

These two leakage phenomena contribute most to the overall leakage current in MOSFETs. They might have a big impact on a device's performance and how much power it uses. Design techniques and technology improvements are employed to lower these leakages and boost than MOSFET efficiency.

## 4.4 Work Done

The investigation of FinFET technology and its numerous aspects is followed by a comparison with CMOS technology as the first step in this study's work. This investigation revealed that as technology is scaled back, leakage currents increase, increasing overall power consumption. It's important to keep in mind that a circuit's total power may be divided into three components:

1. Static power is the power consumed by the circuit when it is in a static or idle state, regardless of whether any inputs or outputs are actively changing. Static power is mostly caused by leakage currents such gate leakage and subthreshold leakage.
2. Dynamic power is the amount of energy required by the circuit during active switching transitions. Transistor gates must either charge or discharge load capacitances when signals change. Dynamic power consumption is inversely associated with supply voltage, load capacitance, and switching frequency.
3. Short circuit power is generated during the brief overlap period when both the PMOS and NMOS transistors are conducting current during switching transitions. This power element fluctuates in direct proportion to the supply voltage and short-circuit current.

Understanding and analysing these three power components is crucial for evaluating and optimising a circuit or system's total power consumption. By evaluating the features of FinFET technology and contrasting them with CMOS, the study seeks to assess the potential advantages and challenges related to FinFETs, particularly in terms of power efficiency and leakage reduction.

## 4.5 Software Requirement

The software used in this study for simulation and design execution is called Microwind. Using the well-known software tool Microwind, integrated circuits for digital, analogue, and mixed-signal applications may be created and simulated. It provides an easy user interface and a variety of tools for designing and studying electrical circuits at the transistor and layout levels.

Using Microwind, scientists and engineers model and build a variety of circuit elements, including MOSFETs and other semiconductor devices. Users may create circuit schematics, run simulations to check the behaviour of the circuit, and improve designs for performance, power consumption, and desired characteristics. Additionally, Microwind provides layout design tools that enable users to create physical circuit layouts and perform layout-level simulations.

The scheme covers a variety of manufacturing methods and technologies, including CMOS, FinFET, and SOI. It offers a full set of tools and libraries for building and simulating complex digital and analogue circuits, including logic gates, memory cells, and more.

Microwind is commonly used for research, training, and development in both academia and business. Due to its user-friendly interface and extensive features, it is a helpful tool for learning about and analysing semiconductor devices and circuits.

### 4.5.1 Software Implementation

This is the interface of the Microwind where the designing and the simulation of the electrical circuits can be done.

The step by step implementation of the project in the microwind is:

First open the DSCH3 file from microwind folder

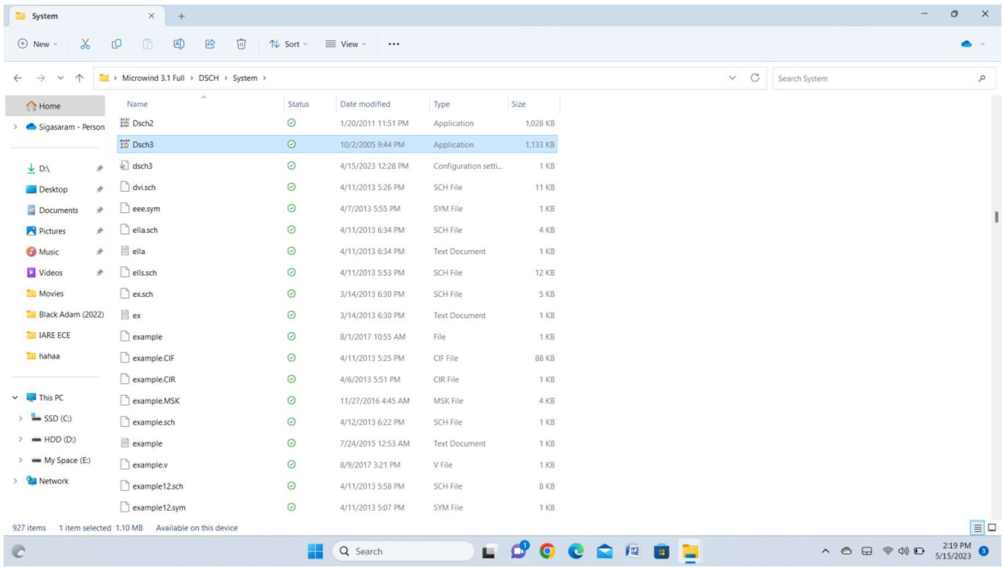


Figure 4.4: Opening the software

After Opening the dsch3 file from the microwind folder, it can view the following interface.

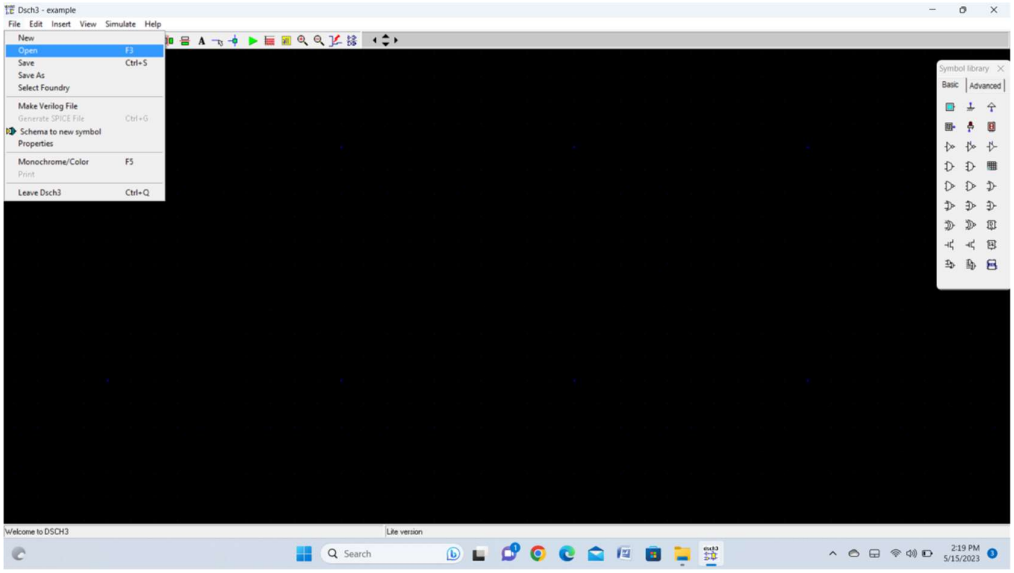


Figure 4.5: Software interface

Now open the schematic and implementing in the software as the schematic is already designed. Click on the file on the status bar and open the .sch file to implement.

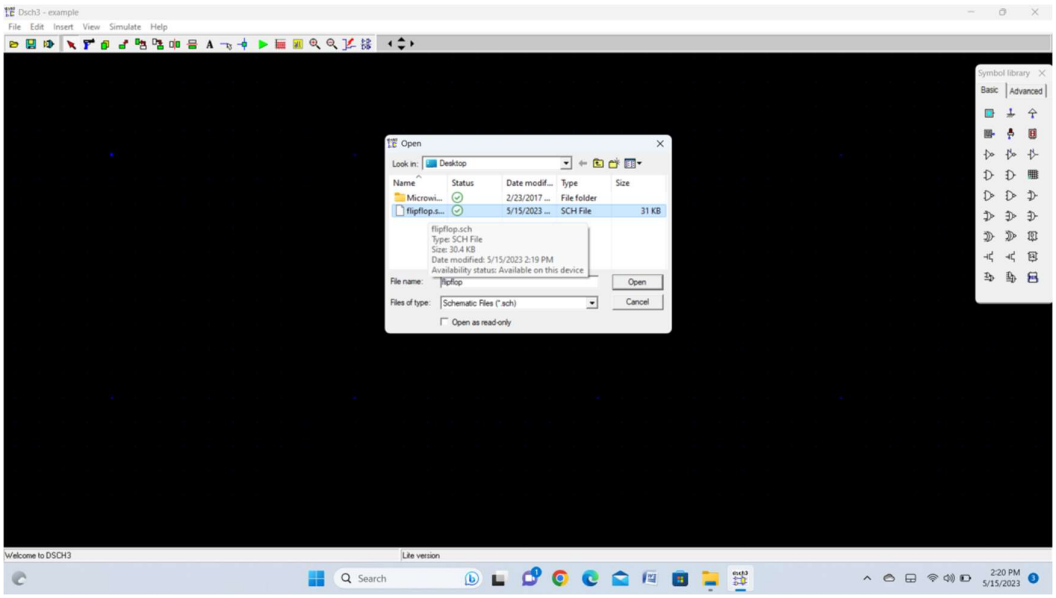


Figure 4.6: Opening the schematic

Then opens the project designs and the circuits, which consists of Master and Slave circuit, Master and Slave using NAND and NOR Gates, Multi-Threshold data Flip Flop schematic, single threshold data flip flop schematic and Master and Slave circuits using transistor switches.

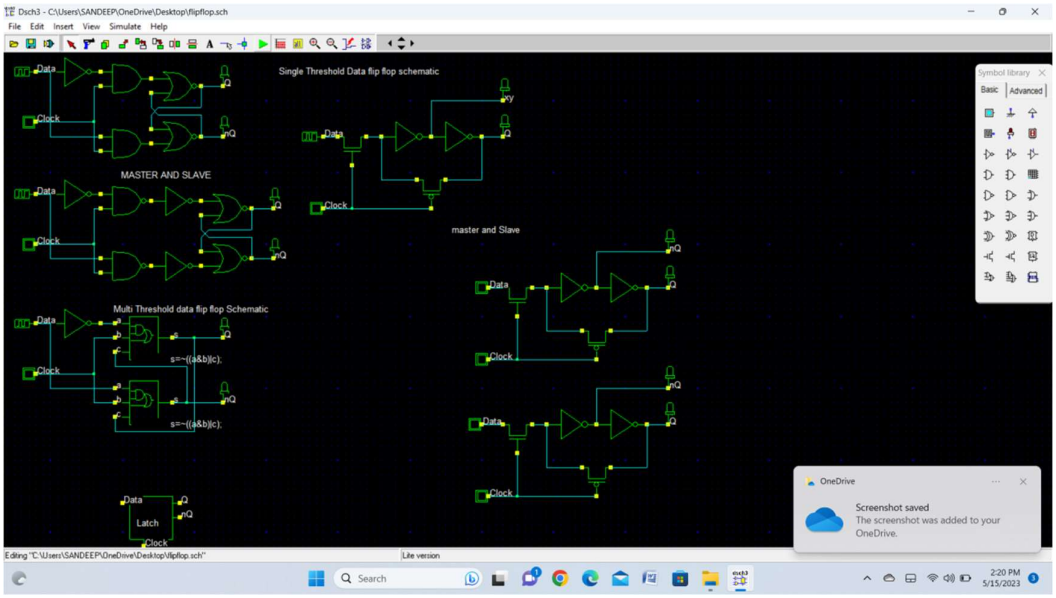


Figure 4.7: Circuits and designs

The above figure is about circuit designed in the .sch file, all circuits like master and slave circuit, and master and slave using NAND and NOR gates, Multi-Threshold data Flip Flop.

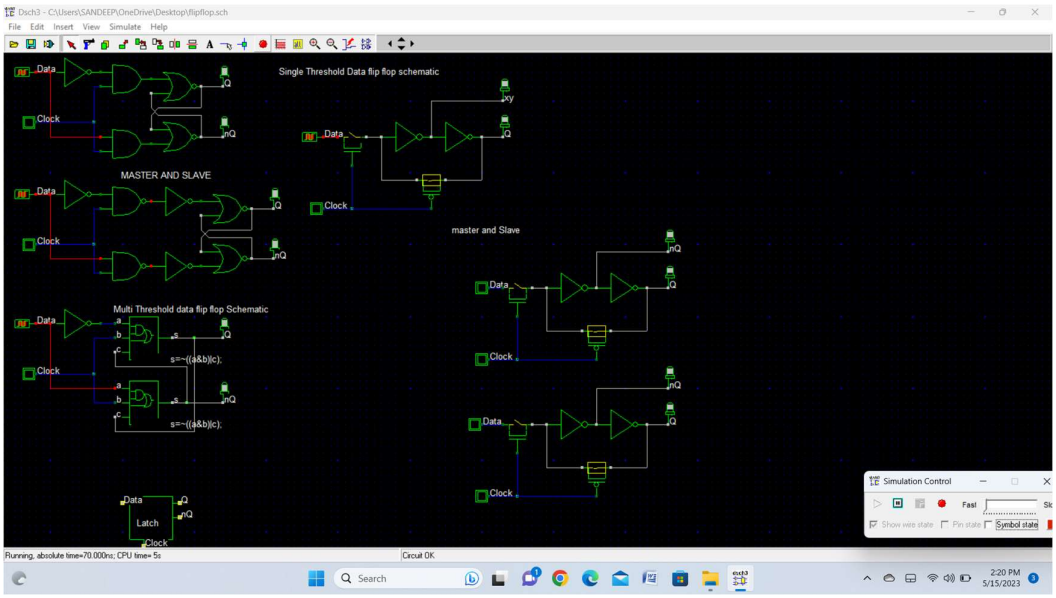


Figure 4.8: Circuits in run state

In the above figure the circuits are currently running and in active state. The data inputs are given in default and the clock has been initialized from low state.

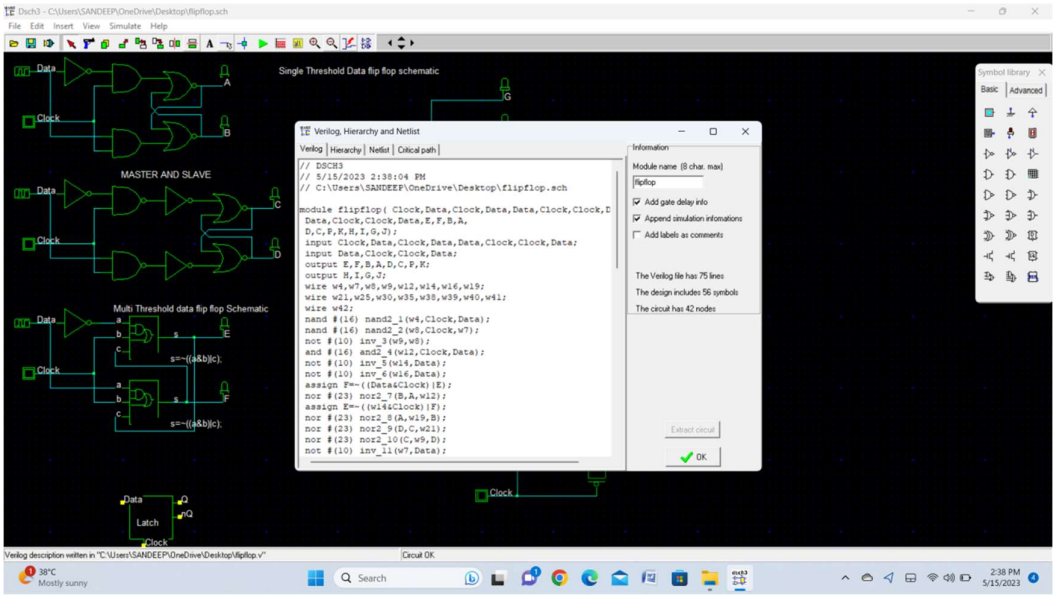


Figure 4.9: Configuring

The input and output waveforms of the circuits are observed above each circuit has a data and clock as input and the output are present and previous states. Now configure the schematic and create it as a verilog file for further use.

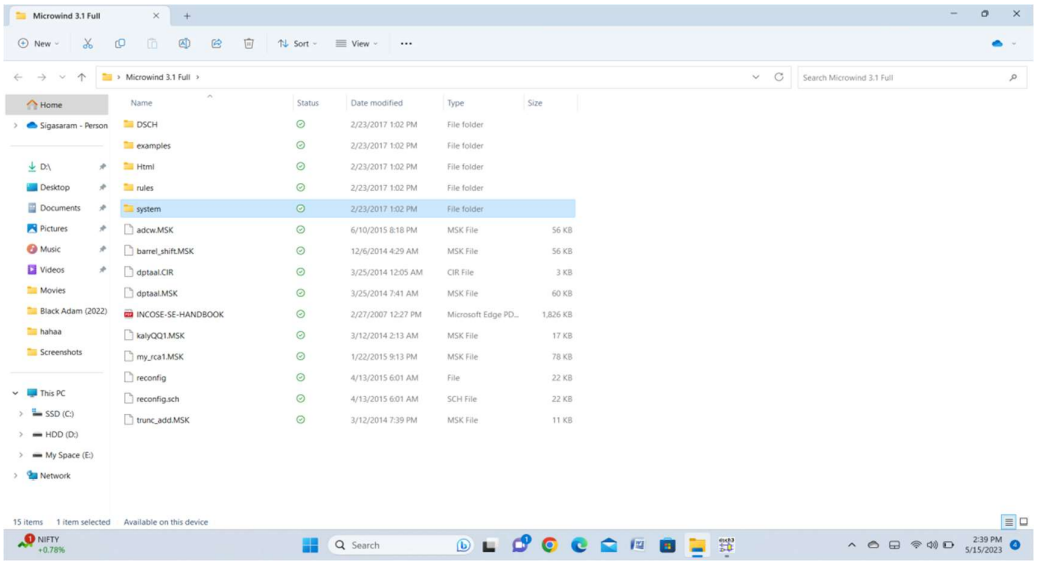


Figure 4.10: Select the System folder

Now for the layouts click on file from status bar and select ‘make verilog’ then open the file and click on ‘system’ folder.

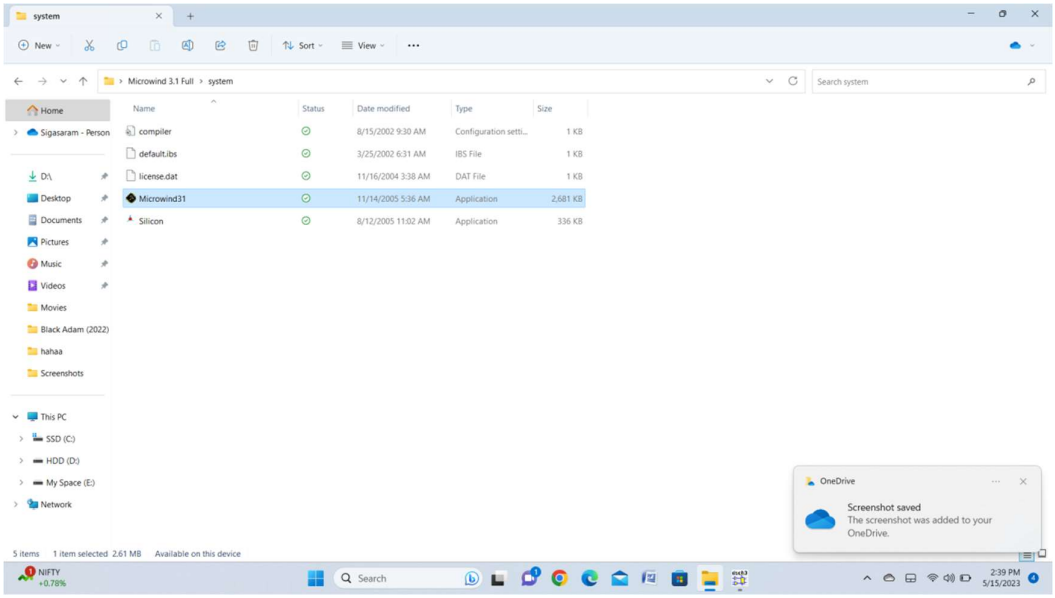


Figure 4.11: Open Microwind31 for layout designs

The above figure discuses about the opening of the microwind31 for the purpose of the layout design.

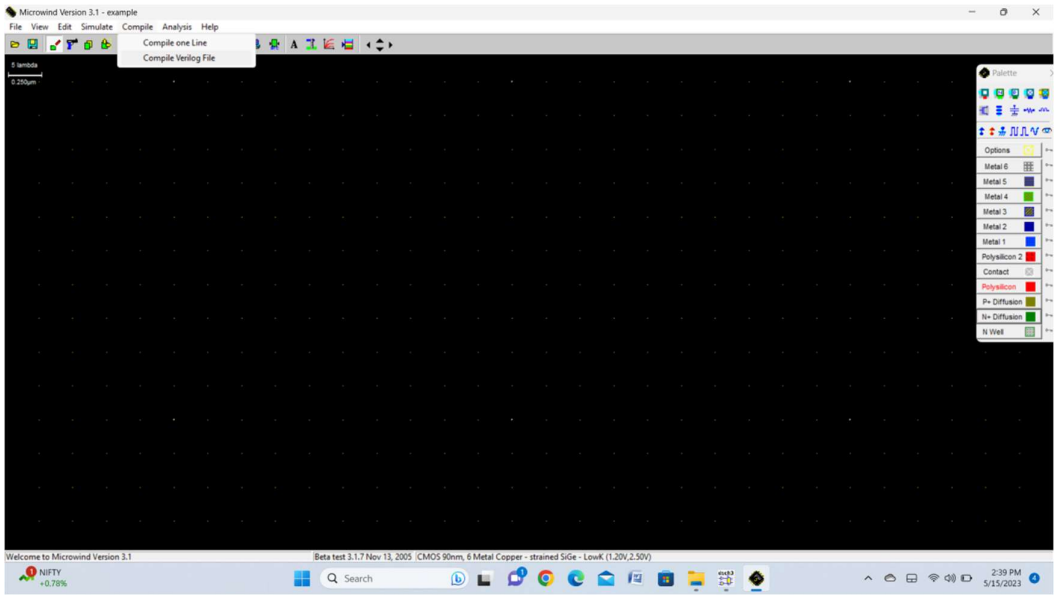


Figure 4.12: Open Compile

Now from status bar click on the compile tool then from it select the ‘Compile Verilog File’ to compile the .v file.

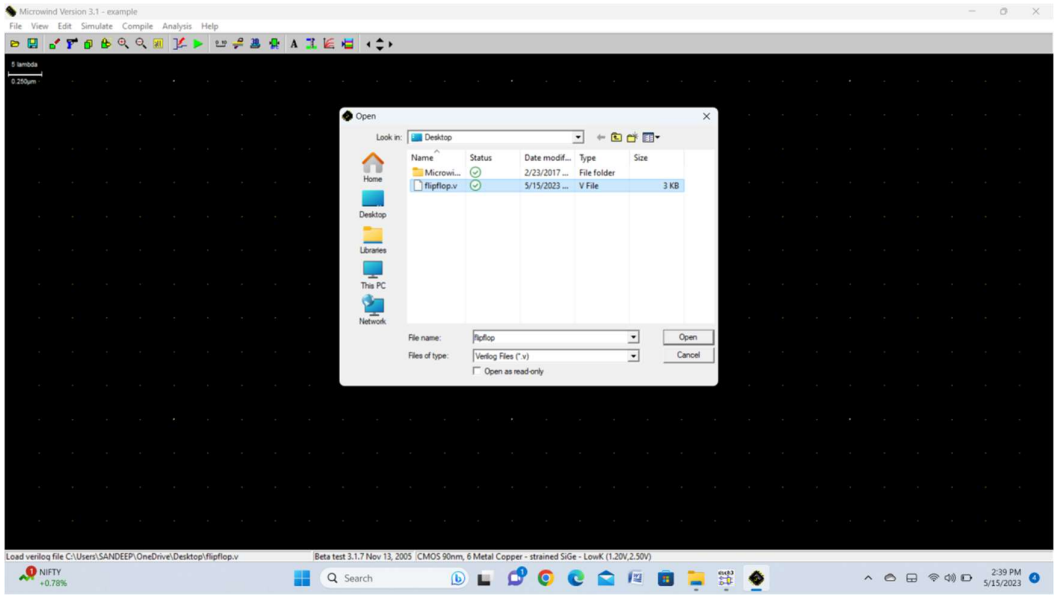


Figure 4.13: Select the Verilog file

Now pops up a window to select the Verilog file from the destination which is a .v file it contains the circuit design and schema.

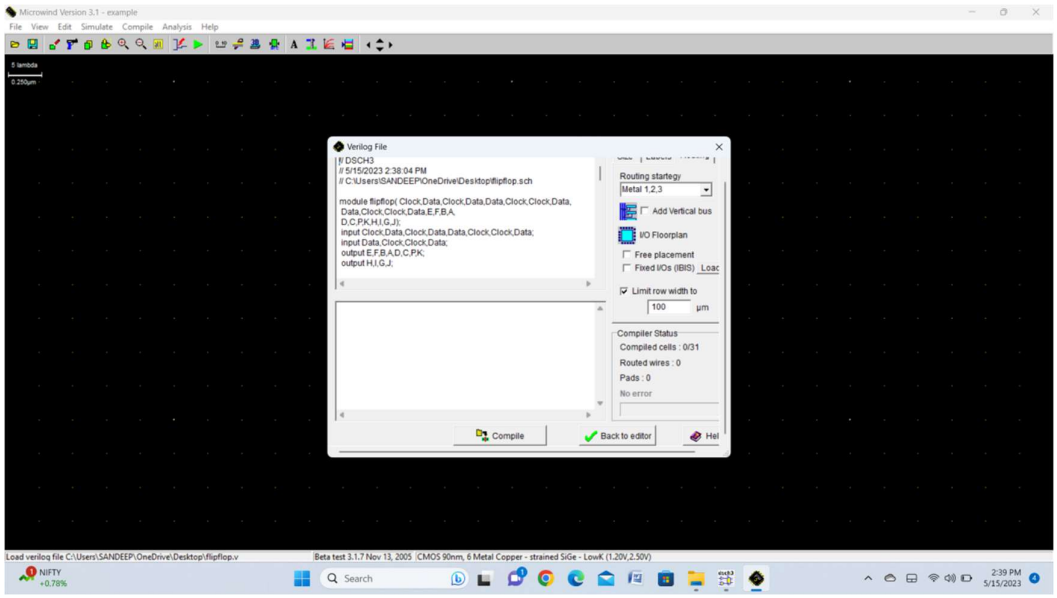


Figure 4.14: Verilog file compiling

Now we have the schema and after we run it, results of timing diagrams are obtained.

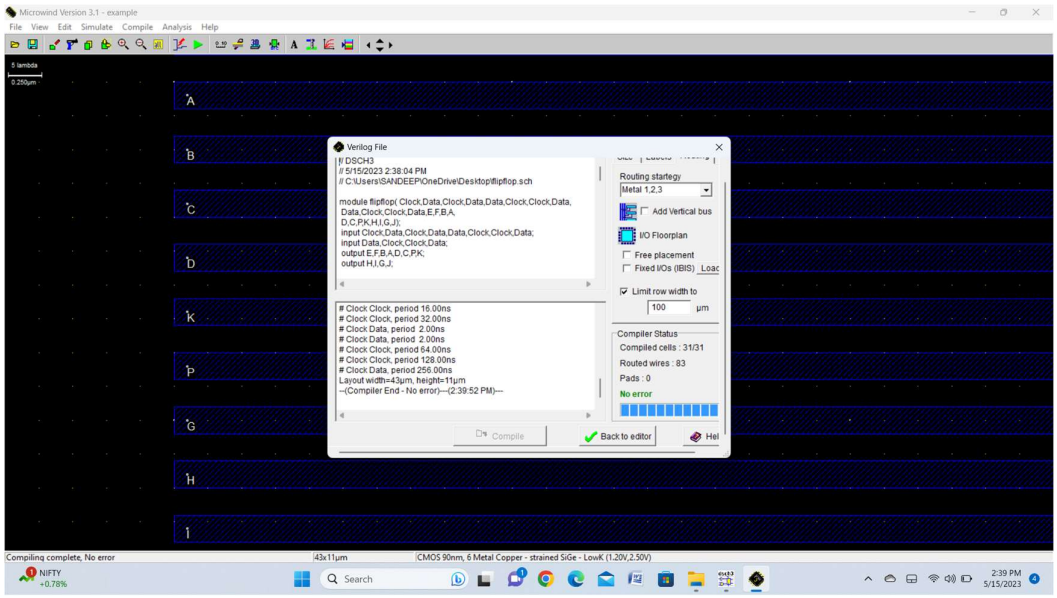


Figure 4.15: Schema compiling

The above figure is about the schema running in the background as a result eye diagram are obtained.

# Chapter – 5

# Results

The results obtained from the circuits run on Microwind contribute to the overall understanding and optimization of the designed circuits, facilitating advancements in microelectronics research and development. Below are the results obtained,

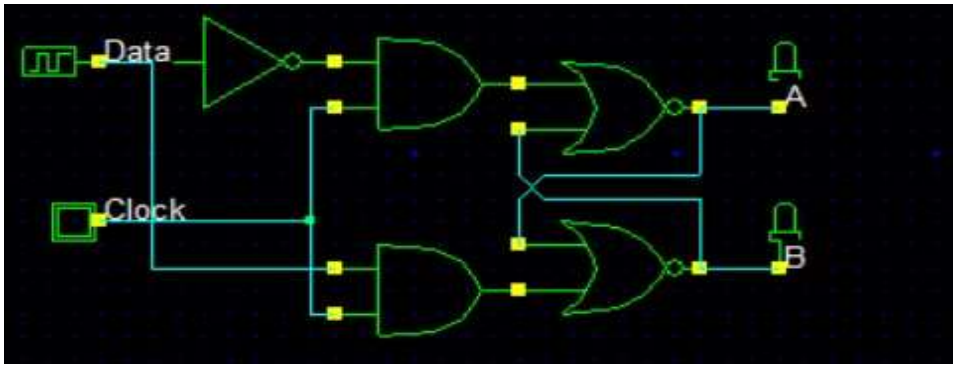


Figure 5.1: Master-slave data flip-flop

The above figure describes about the Master-slave data flip-flop using AND and NOR gates. When data is supplied, the system generates an output based on the previous state. However, when a clock signal is received because of an edge trigger, the system enters the current state and generates a new output based on the updated state.

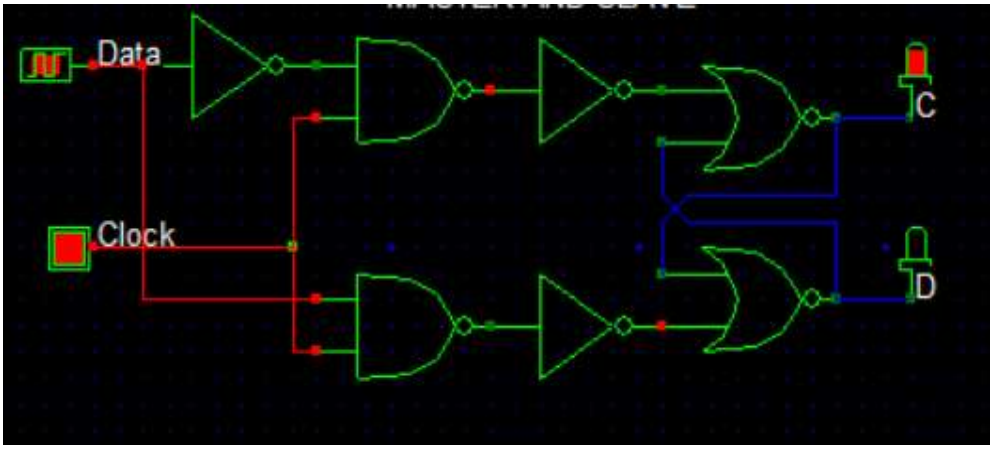


Figure 5.2: Master-slave data flip-flops using NOR and NAND gates

In the above master slave data flip flop is designed using NOR and NAND gates. The system produces an output depending on the prior state when data is presented. The system switches to the current state and produces a new output based on the updated state when a clock signal is received, however, as a result of an edge trigger.

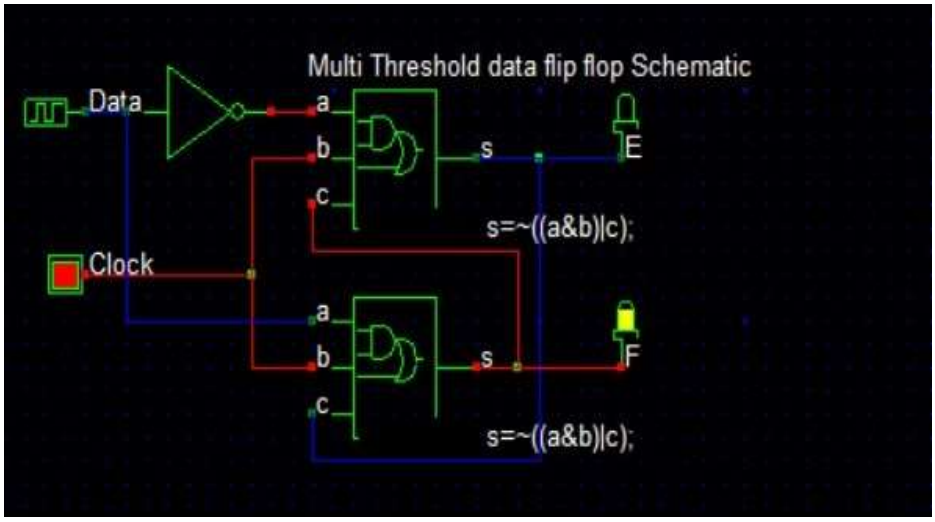


Figure 5.3: Multi-threshold data flip-flop

In the above figure a Multi-threshold data flip flop is designed using AND and OR gates, here we multiple thresholds to the circuit and examine each output. This gives the exact perfect output than the other circuits.

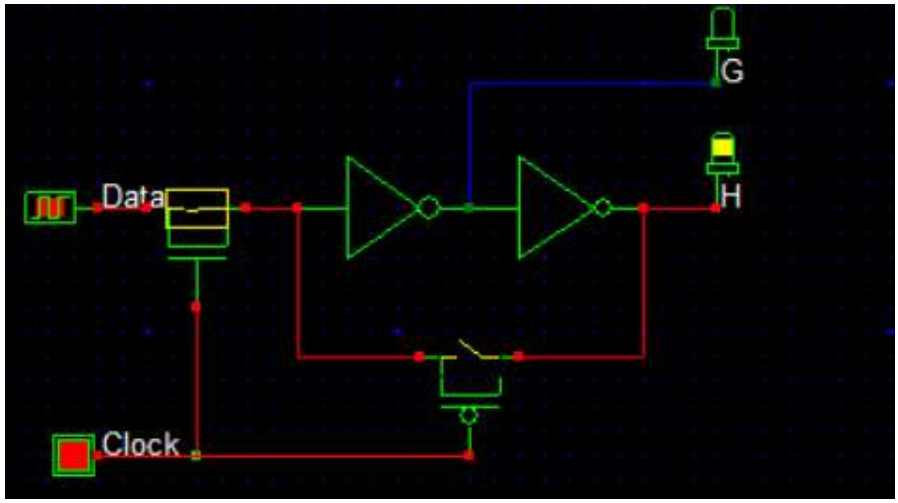


Figure 5.4: Single-threshold data flip-flop

The above circuits describes the single-threshold data flip-flop which is designed using transistor switches. Data is on then the transistor(nmos) turns to high state and the pmos transistor switch is low, previous state output is obtained. When clock is low the pmos transistor switch goes high and the present state output is obtained.

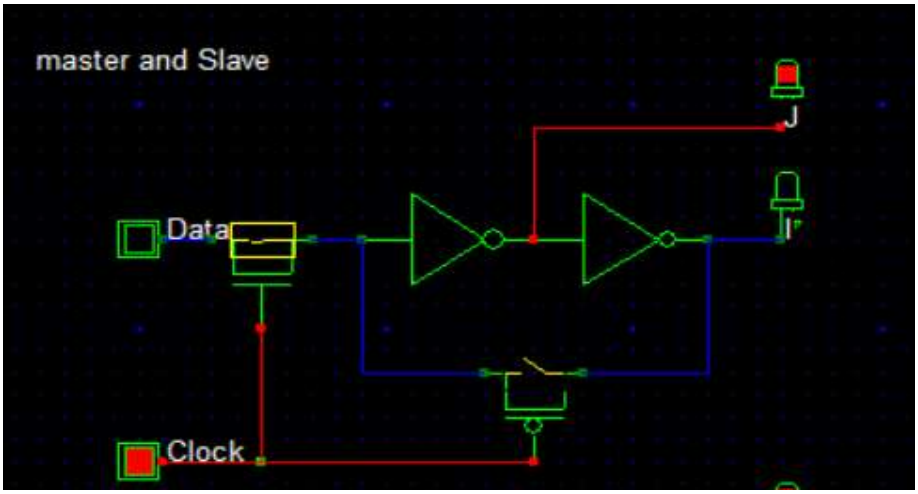


Figure 5.5: Master and slave circuits using transistor switches

The above circuits describes the Master and Slave data flip-flop which is designed using transistor switches. When data is on then the nmos transistor switch turns to high state and the pmos transistor switch is low, previous state output is obtained. When clock is low the pmos transistor switch goes high and the present state output is obtained.

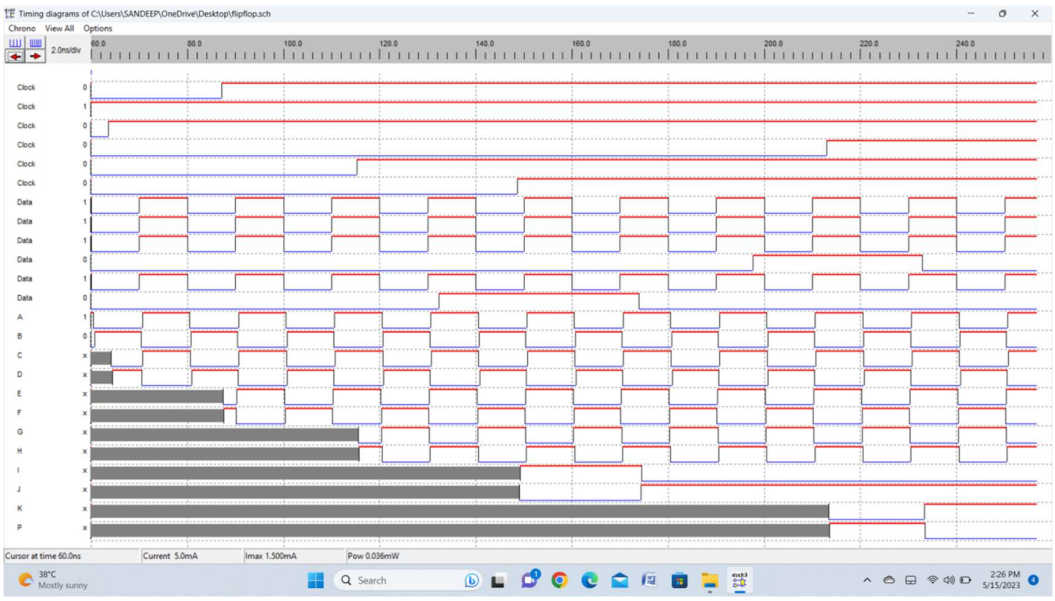

Figure 5.6: Timing diagram

The above figure describes the Timing diagram of the circuits designed, each data and clock signals are observed and the output waveforms are compared.

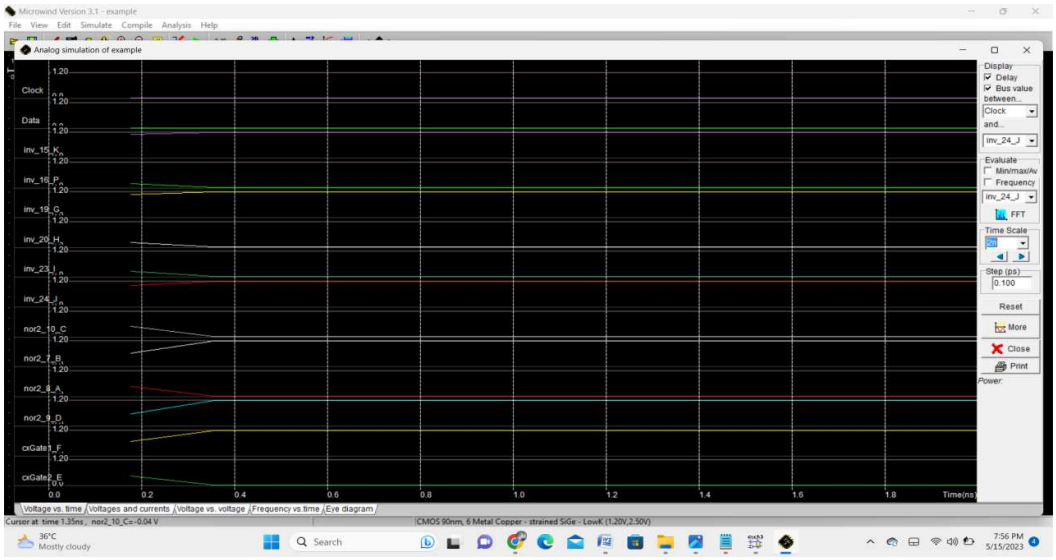


Figure 5.7: Voltage vs. Time

The above figure is about the timing diagram from the layout and describes about the voltage vs time parameters.

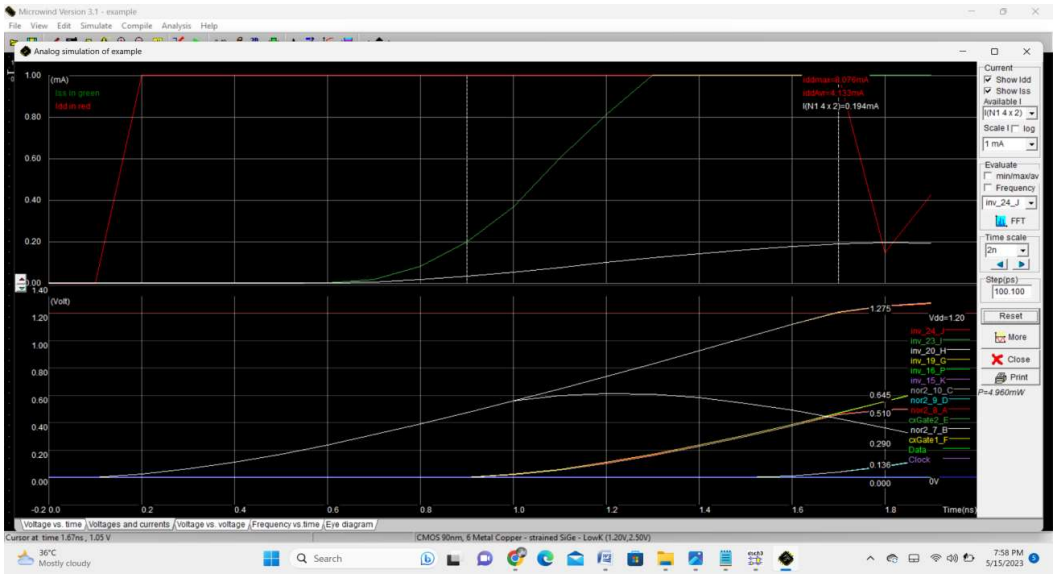


Figure 5.8: Voltage and Currents

The above figure is about the timing diagram for the parameters of the voltage vs currents.

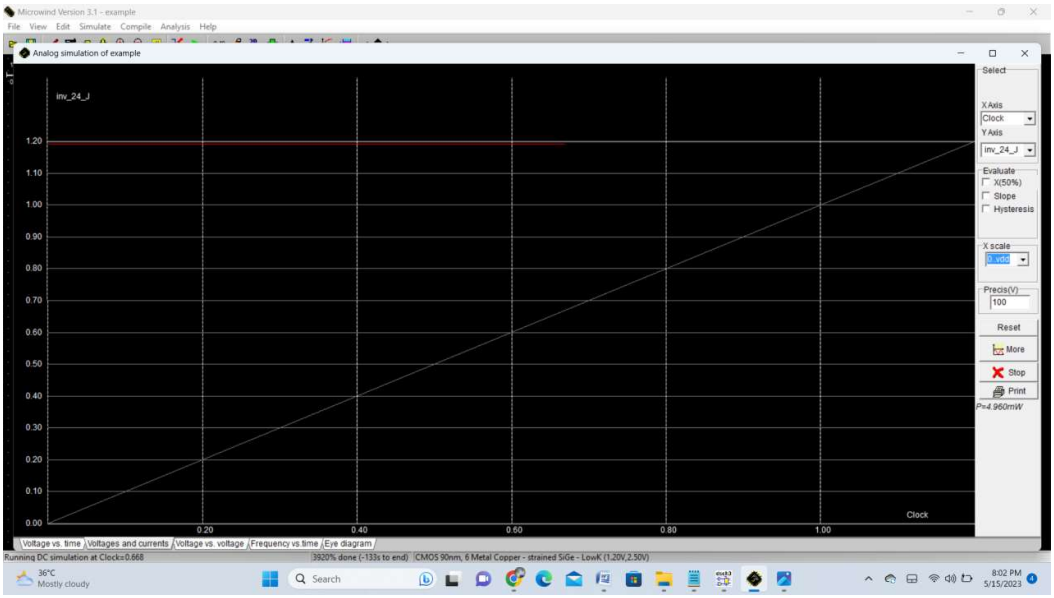


Figure 5.9: Voltage vs. Voltage

The above figure is about the timing diagram for the output parameter of the voltage vs voltage.

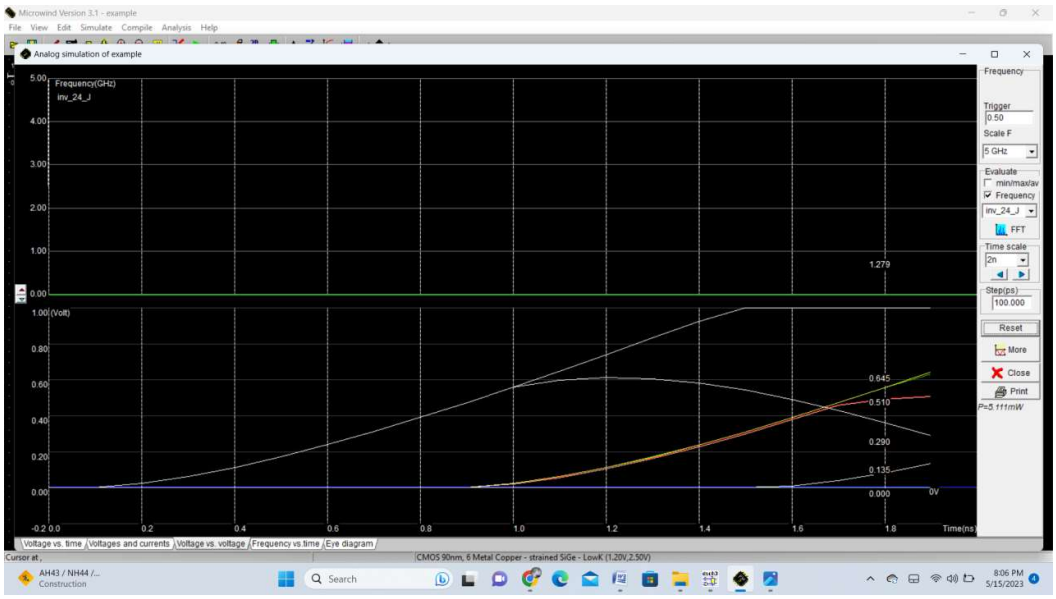


Figure 5.10: Frequency vs. Time

The above figure is the timing diagram for the output result of the parameter of the frequency vs time.

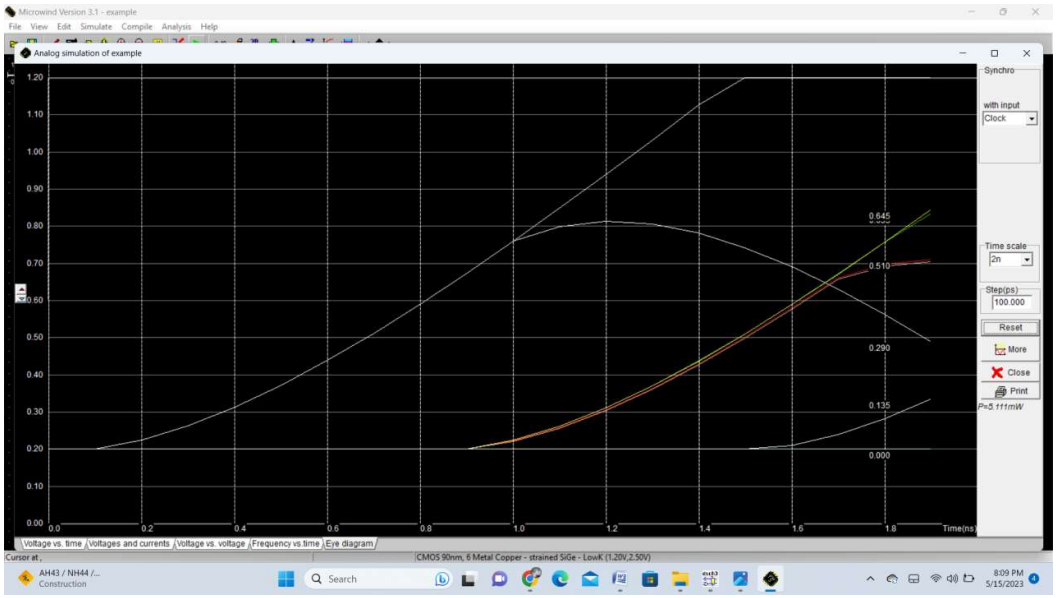


Figure 5.11: Eye diagram

The above figure is the eye diagram for the resultant output of the above parameter like voltage vs voltage vs current vs frequency etc.

# Chapter – 6
# Conclusion

A multi-threshold data flip-flop based on the FinFET 18nm electronic devices has been suggested as an alternative. The advantage of the recommended method is that it uses less energy while performing similarly as well as only one threshold data flip flop. Additionally, this study compares only one threshold data flip flops made with CMOS 45nm and FinFET 18nm technologies. While having a smaller channel length than CMOS technology, the static power dissipation of FinFET 18nm has increased. The simulations have been performed using Microwind simulation software.

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# Design and Analysis of Master Slave Data Flip Flop Using Multi Threshold FinFET


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***Abstract*— As CMOS technology gets smaller, it is no longer feasible to disregard the power loss it causes. The multi-threshold approach, which employs high threshold transistors in non-essential tasks circuit channels to mitigate the whole leakage power of the circuits, is one method for dealing with leakages. This research analyses the operation of a master - slave data flip flop constructed using multi threshold approach and FinFET technology to that of a flip-flop with a single threshold master slave. It has been demonstrated that the flip flop's static and average electrical usage have fallen by 54% and 8.5% respectively.**



***Keywords*— Multi-Threshold, FinFET, Master Slave data flip flop.**


## I. INTRODUCTION

As there are more portable electronic gadgets on the market, the batteries should last longer. The ideal option in this situation would be to reduce the power usage of the electronic devices because adding more battery capacity makes the gadgets larger. Because both static and dynamic power consumptions are made up by CMOS transistors. Because Eqn. 1 shows that the dynamic power dissipation is exactly proportional to the square of the supply voltage, reducing the supply voltage can reduce the dynamic power. However, because the channel current is inversely proportional to the power supply, doing so will make the gadget operate more slowly.

$$P_{Dynamic} \alpha CV^2_{DD}f \longrightarrow 1$$

As technology progresses, the transistor threshold falls as channel length increases. The circuit's dynamic power loss and supply have decreased, which has resulted in an increase in leaky power transfer. As a result, the gate should now have more control over the channel current to address the leakage power. We switched to FinFETs because of their improved channel current controllability, which would minimize leakages. In addition to elevated source and drain structures above silicon surface and gate terminals around the channel, FinFETs are three-dimensional devices that resemble MOSFETs(see figure 1).

A single FinFET device may have many fins, with a single gate terminal covering each fin. The channel that connects a FinFET's source and drain is referred to as its fin. It may be used to improve the driving performance of FinFET. In order to eliminate losses without diminishing the performance of the circuit, the aim of this study is to build a sequential data flip flop in FinFET 18nm technology. In comparison to findings obtained using a one threshold data flip flop, the results demonstrate that the power loss has decreased when the multi threshold approach has been applied.

## II. LITERATURE REVIEW

Sherif A,[1] Threshold-based strategies are covered in this article. In comparison to single threshold sequential circuits, the recommended multi-threshold approach significantly reduces the use of electricity, average power, and clock power while maintaining about the same speed and data stability. Sequential circuits are built using the 32nm FinFET manufacturing technology.

Linfeng Li,[2] The transmission gate-based directed master slave flip flop is implemented in this study, which also discusses the available low power solutions, their benefits, and their drawbacks. A high threshold transistor is used in the noncritical circuit to reduce leakage power, and it is also discussed how the multi threshold technique is preferable than other technique.

Ashok Kumar Kuna,[3] The properties of n-FinFET, p-FinFET are examined in this essay. In terms of transistor sizing and particular ideal design choices, both the simplest circuit, an inverter, and a sequential circuit data flip flop employing multiplexers were extensively explored. It is all hypothetical for 32nm FinFET technology.

Dhiraj kumar s. Bhutada,[4] It has been found that the suggested technique significantly lowers the dual threshold CMOS method's power consumption. In this study, complementary pass-transistor adiabatic logic (CPAL), which is utilized to create circuits employing dual threshold CMOS technology, is represented by low voltage flip flops.

Ashih Kumar,[5] Using the multi threshold technique, a low power dual edge triggered flip flop was developed in this study and implemented on CMOS devices with a channel length of 90nm. The following are the circuit's key characteristics: Low power dissipation is achieved using the simplest method, the multi threshold CMOS approach. Speeding up charging and discharging along the essential path is accomplished using the signal feed through technique.

James T,[6] This work highlights the need for a method to keep the performance of static and dynamic combinational circuits while reducing the leakage power caused by the continuously decreasing gate channel. By introducing a novel implanted dual-applied domino logic, several issues, such as sleep transistor sizing, are addressed.

Liqiong Wei,[7] This study also tackles the necessity of preventing transistor leakages by outlining an algorithm for choosing a threshold transistor in a circuit. Leakages are observed to be reduced by 20% to 50% as a result of this. According to the results of the literature review, there is always work to be done in the field of low power, and FinFETs are the emerging technology because of its advantages over CMOS technology. The sequential circuit's FinFET implementation is what we employ in this study.

## III. EXISTING FRAMEWORK

The source-to-drain channel current of a MOSFET is voltage-controlled and influenced by the gate control voltage, as is common knowledge. As technology advanced and channel length shrunk ever-further, the gate's ability to regulate the channel current began to wane, resulting in leakages.

Several devices, including FinFETs, have been introduced since it was challenging to take control of the channel. Here in a FinFET, the channel is encircled by the gate, giving it more control over the channel than in a CMOS device and reducing leakages.

There are a number of phenomena that contribute to MOSFET leakage, including:

Subthreshold leakage, which is a tiny amount of charge leakage between the source and drain, occurs when the gate control voltage is lower than the threshold voltage. a gate leak As we are aware, the gate oxide gets thinner as devices scale down. Gate leakages are the consequence of electrons tunnelling between the gate oxide and surface as a result of this. The total number of device leaks is also affected by a number of different situations.

Transistor stacking, a sleep mode method, the sleep keeper technique, low power retention technique, and many other strategies are used to prevent leakages. Each of these methods has advantages and limitations of their own, which may result in a larger area and a longer response time.

## IV. PROPOSED FRAMEWORK

The first step of this study's research is examining FinFET technology and its many qualities in comparison to CMOS technology.

FINFET TECHNOLOGY

FinFET is a type of transistor that has become increasingly popular in the semiconductor industry due to its superior electrical performance compared to other types of transistors. The FinFET is a 3D transistor design that provides better control over current flow and allows for smaller, more power-efficient chips.

The FinFET transistor gets its name from the "fin" structure, which is a vertical, raised channel on the silicon substrate that acts as the transistor's gate. The fin is surrounded on three sides by a gate electrode, which is separated from the fin by a thin layer of insulating material.

The key advantage of the FinFET over the traditional planar transistor design is that it provides better control over the flow of electrons. The raised fin structure provides additional surface area for the gate electrode, allowing for better control of the channel and reducing leakage current. This improved control also results in faster switching speeds and lower power consumption.

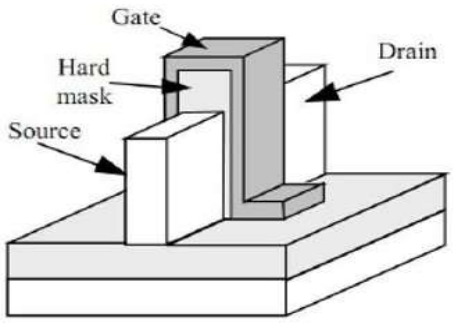



Figure 1. FinFET cross-section

FinFETs are a simple replacement for MOSFETs in the future due to the similarity in the production process. Dual gate transistors, or FinFETs, are essentially quasi-planer in nature. The single gate in a planar FET regulates the source-drain channel. Even when the gate is off, leak currents between the source and the drain occur due to this gate's poor electrostatic field management away from the channel surface near to the gate. In contrast, the transistor channel in a FinFET is a narrow, vertical fin, and the gate completely encircles the channel between the source and thedrain. You may think of the FinFET segment as having several gates enclosing the thin channel.

A multiple gate can entirely exhaust the carrier channel. Better voltage control of the channel and thus better electrical properties result from this.

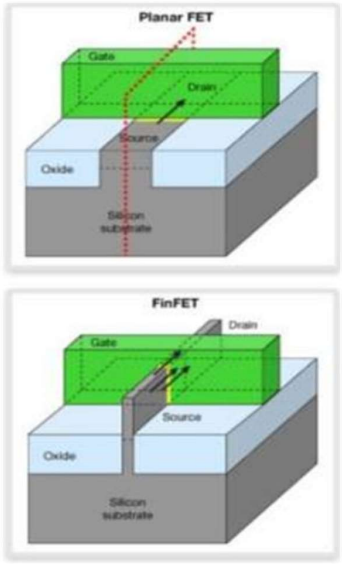



Figure 2. Planar FET, FINFET

MASTER-SLAVE DATA FLIP-FLOP

Through the use of a master-slave flip-flop, a type of digital circuit, one piece of information may be saved. It is often employed in sequential logic circuits like counters, shift registers, and control circuits in digital electronics. The Master-Slave flip-flop is made up of the master and slave stages.

The Master-Slave flip-flop has the advantage of being edge-triggered, which means that the output changes only at the rising or falling edge of the clock signal. This makes it more reliable and less prone to glitches and noise in the input signal.

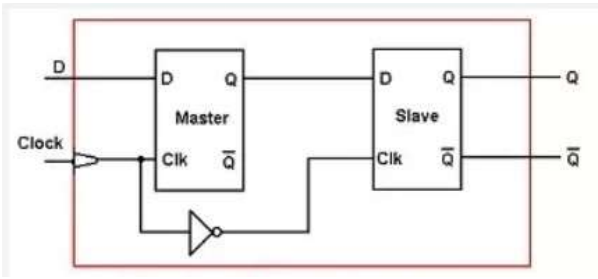



Figure 3. Master-Slave data flip-flop

## V. RESULTS

we are designing the circuit master slave data flip flop using multi-threshold data flip-flop in microwind software. we have compared the outputs of multi-threshold and single-threshold master-slave data flip-flops using various logic gates and transistors.

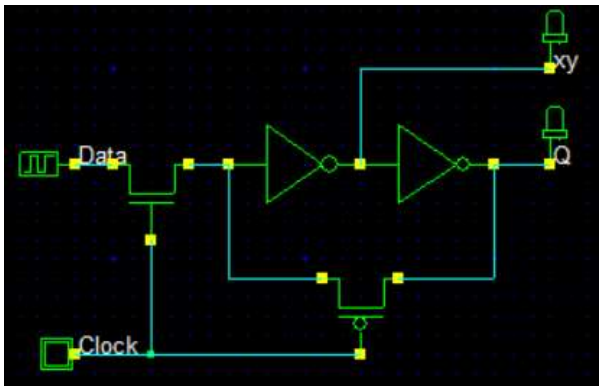



Figure 4.Single threshold multi data flip flop

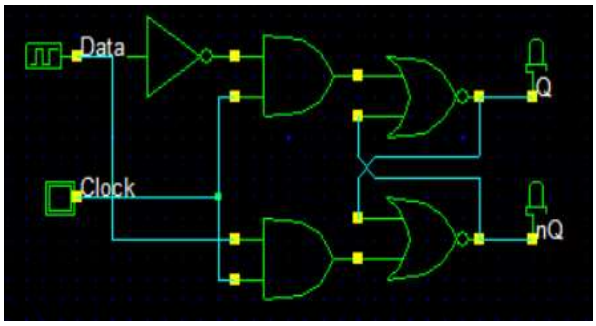



Figure 5. Master Slave Data flip flop

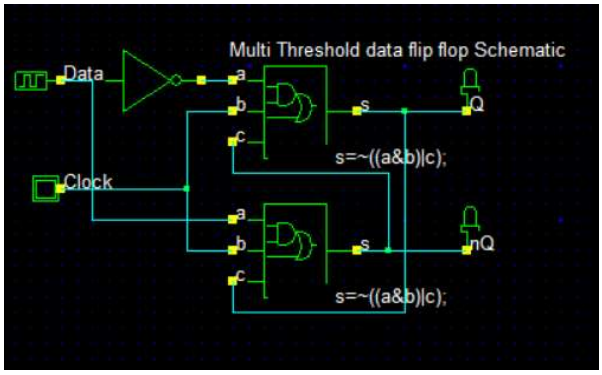



Figure 6. Multi Threshold data flip flop

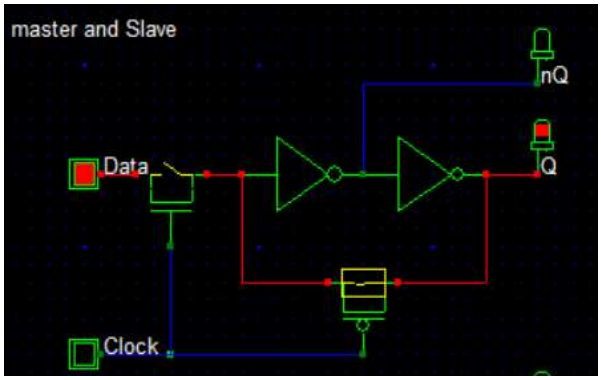
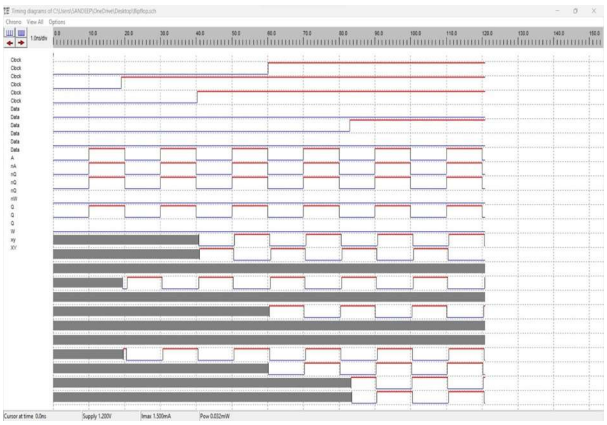



Figure 7. Master slave using transistors

TIMING DIAGRAMS



## V. CONCLUSION

A multi-threshold data flip-flop based on the FinFET 18nm electronic devices has been suggested as an alternative. The advantage of the recommended method is that it uses less energy while performing similarly as well as only one threshold data flip flop. Additionally, this study compares only one threshold data flip flops made with CMOS 45nm and FinFET 18nm technologies. While having a smaller channel length than CMOS technology, the static power dissipation of FinFET 18nm has increased. The simulations have been performed using Microwind simulation software.

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