ASIC Implementation of Horn & Schunck Optical Flow Algorithm

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I. Introduction

The main objective of the project is to implement the Horn and Schunck optic flow algorithm on hardware. The design flow includes Chisel code with testbench and contract verification, verilog RTL simulation, synthesis, place-and-route and gate-level simulation. By going through the flow and the assisting of PrimeTime, we could analyze power, area, performance in this design. To achieve real-time optic flow, the performance should not be traded by other metrics, like power and area. Architectural design would be discussed to optimize power and area consumption.

II. Optical Flow Algorithm

Optic flow provides valuable information on the motion of objects from frame to frame. The basic idea is to calculate the spatial and temporal difference between image frames. The approach to determine the optic flow vectors have been classified into two groups: gradient based and the segmentation method. In this project, we adopt Horn and Schunck algorithm, which is the first to describe the technique directly. *E(x,y,t)* represents the brightness of the pixel (x,y) (spatial) in the t (temporal) image. By the meeting the requirements that the brightness patten of the image must remain constant, we can derive that: $E_x u + E_y v + E_t = 0$, where *u* and *v* are the velocities of pixels in each direction.

The equations to derive the velocities are listed below:

$$u = \bar{u} - R_x = \bar{u} - \frac{P_x}{D}, \text{where } P_x = E_x P,\ D = \alpha^2 + E_x{}^2 + E_y{}^2$$

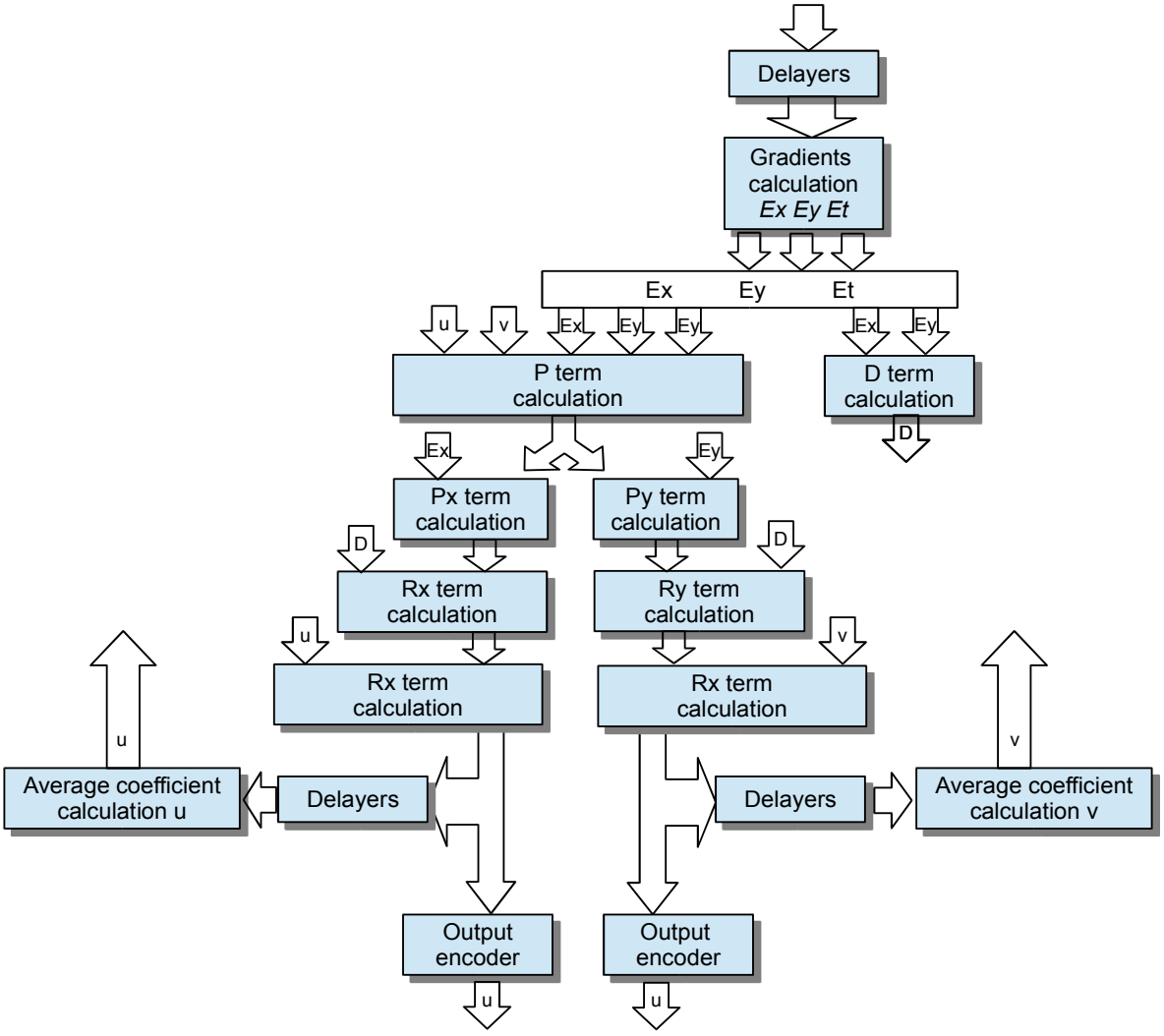
$$v = \bar{v} - R_y = \bar{v} - \frac{P_y}{D}, \text{where } P_y = E_y P,\ P \equiv (E_x \bar{u} + E_y \bar{v} + E_t)$$

The average coefficient of velocity, *u* and *v*, can be calculated by convolution with a mask. Using the mask proposed by Horn and Schunck, *u* and *v*, are defined as:

$$\bar{u}_{i,j} = \frac{1}{6}(u_{i-1,j} + u_{i,j+1} + u_{i+1,j} + u_{i,j-1}) + \frac{1}{6}(u_{i-1,j-1} + u_{i-1,j+1} + u_{i+1,j+1} + u_{i+1,j-1})$$

$$\bar{v}_{i,j} = \frac{1}{6}(v_{i-1,j} + v_{i,j+1} + v_{i+1,j} + v_{i,j-1}) + \frac{1}{6}(v_{i-1,j-1} + v_{i-1,j+1} + v_{i+1,j+1} + v_{i+1,j-1})$$

By the algorithm and all the equations above, we are able to build a hardware to implement real-time optic flow detection. The flow chart is shown below:



III. ASIC Implementation Proposal

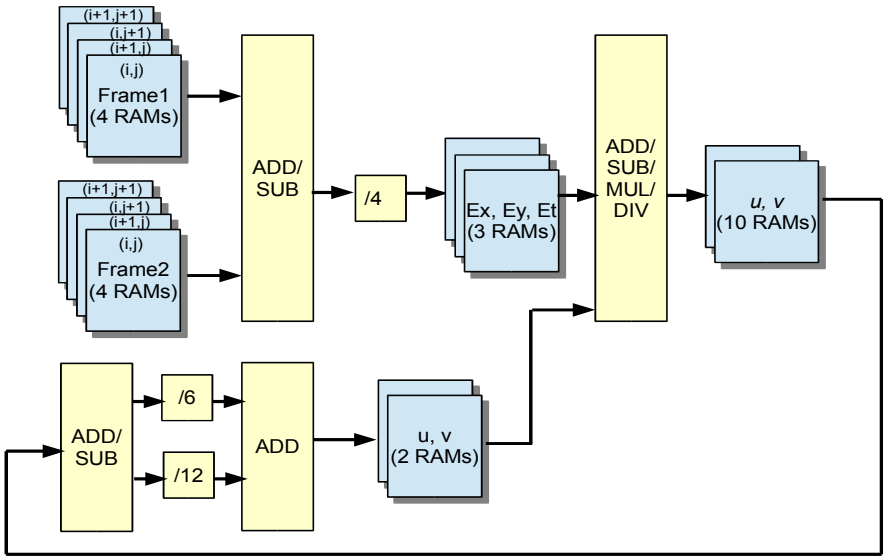
In this project, we would instantiate the Horn and Schunck algorithm using 32nm Synopsys educational PDK. The target specifications are listed below:

- Frame size: 720*480 pixels
- Frame rate: 60 frame/s
- Throughput: 20250 Kpixel/s

To lower the energy consumption, which is our main design objective, we want to investigate several architectural approaches. We would explore the tradeoffs between area and power in the proposed architecture design space.

- Parallel computing blocks for pixel block operations will be examined in order to maintain our targeted frame rate under a lower operating voltage.
- Multi-VT design scheme will also be included to reduce leakage power consumption.
- RAM blocks will be further utilized to reach our low-power design objective.

The block diagram of ASIC implementation with memories and arithmetic blocks is shown below.



IV. Project Timetable

10/04/12	Initial Project Proposal Presentation
10/11/12	Define all the signals and define all the functional blocks
10/18/12	Design sub-blocks and the testbenches
10/25/12	(Presentation)
11/01/12	Finish all functional blocks
11/08/12	(Presentation)
11/15/12	Connecting all modules and test with contract
11/22/12	Power/area/delay analysis
11/29/12	Design Wrap up
12/07/12	Final Project Presentation
12/12/12	Final Project Report

References

[1] Berthold K. P. Horn and Brian G. Schunck, “Determining Optical Flow”
[2] Jose L. Martin, Aitzol Zuloaga, Carlos Cuadrado, Jesus Lazaro, Unai Bidarte, “Hardware implementation of optical flow constraint equation using FPGAs,” Computer Vision and Image Understanding, 2005, pp. 426-490.
[3] Mohammad Reza Balazadeh Bahar and Ghader Karimian, “High Performance Implementation of the Horn and Schunck Optical Flow Algorithm on FPGA,” 20th Iranian Conference on Electrical Engineering, 2012, pp. 736-741.