

IMX7ULP-EVK-SOM

## Table of Content

## Revision History

Rev.	Code	Date	Description
A		2016/9/1	First Release
A1		2016/9/12	1. Change the connection of LL from VDD_3v3 to PMC_3V3; 2. Use Y2 to generate 32.768K for WIFI module, as PTB8 is dedicated for QSPIA_SS0 during booting;
A2		2016/12/11	1. Add J7 for Battery Input; 2. Correct the circuit of Q4; 3. Add pull up resistor R215 for PF1550 WDI; 4. Add D16 to reduce the power supply for U14; 5. Change U8 to PPF2124 to eliminate the reverse current; 6. Change U11, U13 to SN74LVCZG126DCTR to reduce current leakage; 7. Add C15 on U15 to increase the soft start time; 8. Change C143, C145 to 22uF as workaround for VSYS drop; Add C226, C227 100uF as workaround for VSYS drop; Add D17 as backup workaround for VSYS drop; 9. Add TP92 for CLKOUT_A7; 10. Route PTB0(CLKOUT_M4) to Base Board as MCLK input workaround; 11. Add R224 to isolate VDD_HSIC from VDD_1V2 for current measurement; 12. Add R228 to isolate PMIC_VDDIO from PMC_1V8 for current measurement; 13. Add R221-R223 for ONOFF/PMIC_ON_REQ workaround; 14. Change DDR_SW_EN# from PTC1 to PTB6, let M4 control the power for LPDDR3;
A3		2017/03/11	1. Change U20 WIFI/BT Module to LBEE5KLIPJ, QCA9377 based; 2. Change USB connector to Type C, and CC logic circuits; > USB_OVG_DOG#(PTC16,USB_CCSLE#(PTC11),USB_NFT#(PTC12)); 3. Change USB_OTG_ID from PTC8 to PTC13, as B0 changes the pinmux table; 4. Remove C226, C227 100uF, which were for PF1550 workaround; 5. Change WIFI_BT power control and wakeup signals to M4 domain, then even A7 is shut down, WIFI/BT Module could still run > BT_REG_ON#(PTA15),WL_REG_ON#(PTA14),BT_HOST_WAKE#(PTB7),WL_HOST_WAKE#(PTA3); > RTC_CLK#(PTB14); 6. Change PMIC_INT# from PTB7 to PTB11; 7. Change VOL- from PTB11 to PTA28, VOL+ from PTB14 to PTA3(LLWU_P1); 8. Change BATL_ADC_EN from PTA3 to PTA12; 9. Change SW1 Boot Switch to support Lower Boot and Single/Dual Boot;
B		2017/12/20	1. Remove R221, R222, R223, as B0 fixed the ONOFF polarity issue; 2. Add U21 and related circuit to solve the unaccurate threshold issue for power switching; 3. Change VOL- to PTA13, as PTA28 is occupied by JTAG;
B1		2018/01/31	1. Optimize the power switching circuit; 2. Change U2 LPDDR3 part from NT6CL256T32BQ-H2 to NT6CL256T32CQ-H1; 3. Add optional VDD_1V8 connection for eMMC VCCQ;
B2		2018/07/25	1. Add R270 and DNP R207 to bypass load switch (U5), for we cannot power off NVCC_DRAM_SW in VLLS mode; 2. Change R173 from DNP to populate for there is no pull up resistor on tamper detect pin in battery mode; 3. Add R271 and C241 to meet the requirement for USB Type-C test; 4. Add R272, R273, R274, C242 and Q14, DNP R129 and C242. Using USB_OTG_ID pin to enable load switch for VBUS; 5. Change R213.Pad2 from RF_ANT to RF_ANTO;



Microcontroller Product Group

**Encountech Product Group**

Austin, TX 78735-8598

ICAP Classification: CP- IIQ: A PUBL:

卷之三

I.MX7ULP-EVK\_SOM

**Title and Box History:**

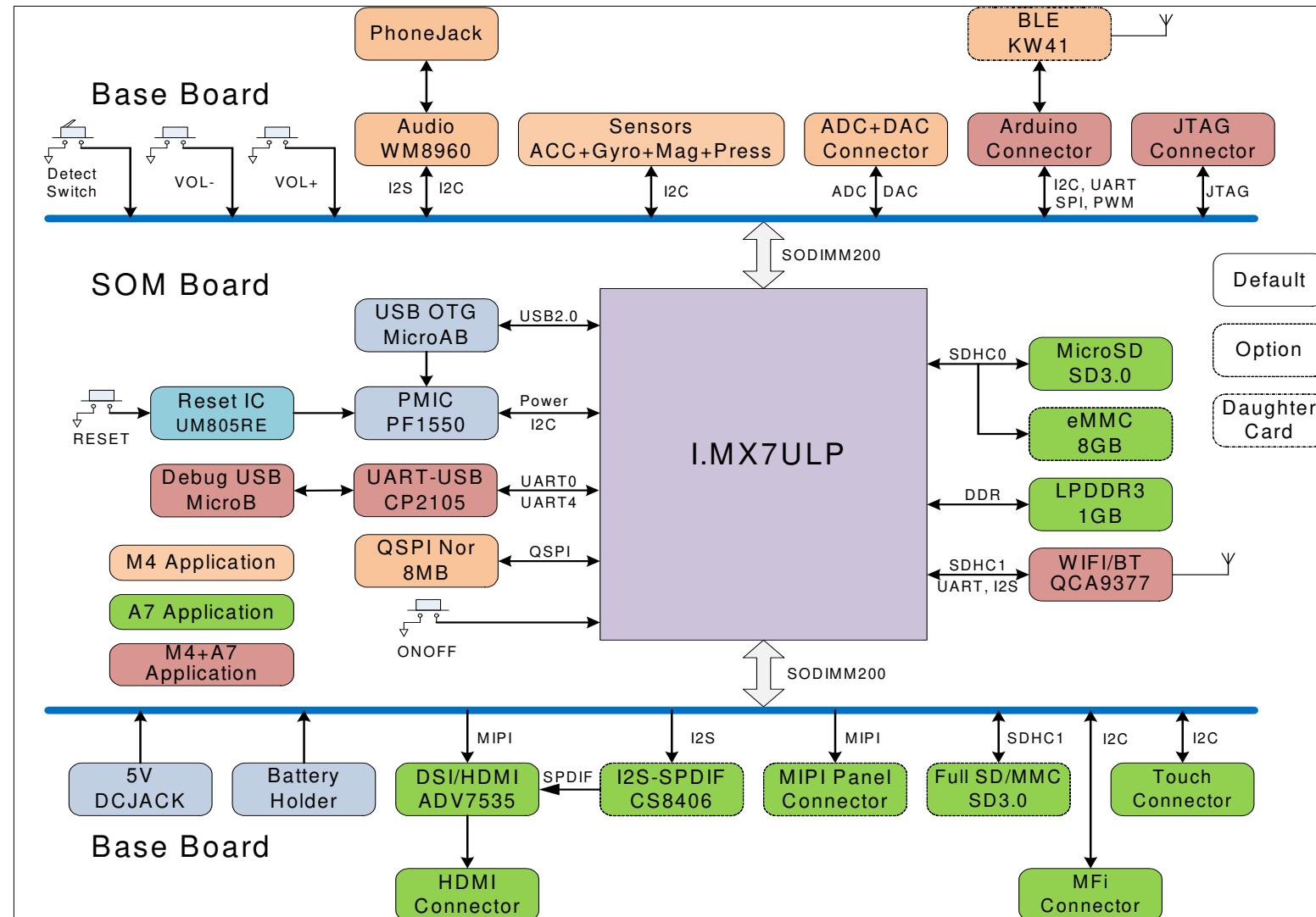
## Title and Rev History

SCH-29163 PDF: SPF-29163

Wednesday September 11 2018

1

# i.MX7ULP EVK Block Diagram



Microcontroller Product Group

6501 William Cannon Drive West  
Austin, TX 78735-8598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

ICAP Classification: CP: IUO: A PUBL:

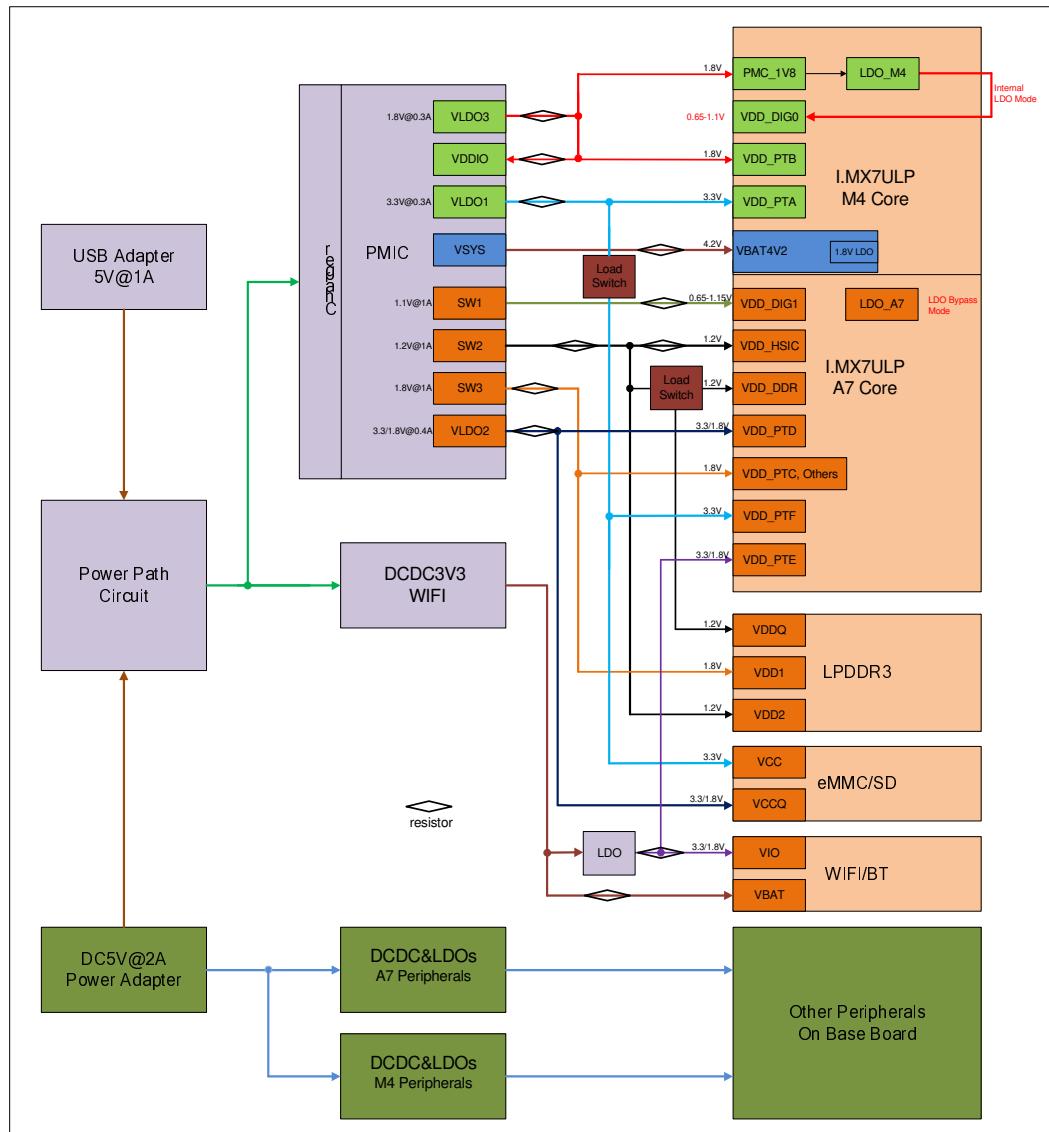
Designer: <Designer> Drawing Title: **i.MX7ULP-EVK\_SOM**

Drawn by: <DrawnBy> Page Title: **Block Diagram**

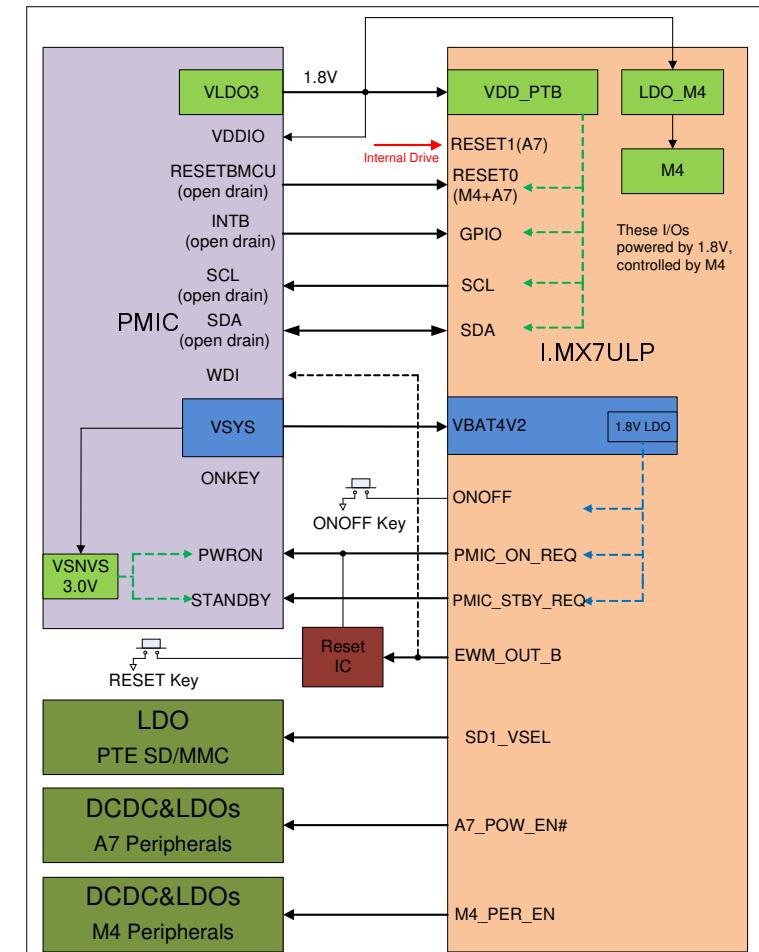
Approved: <Approver> Size A3 Document Number: SCH-29163 PDF: SPF-29163 Rev B2

Date: Wednesday, July 25, 2018 Sheet 2 of 18

## Power Distribution Diagram



## Power Control Diagram



**Microcontroller Product Group**  
6501 William Cannon Drive West  
Austin, TX 78735-8598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

ICAP Classification: CP: IUO: A PUB: I.MX7ULP-EVK\_SOM

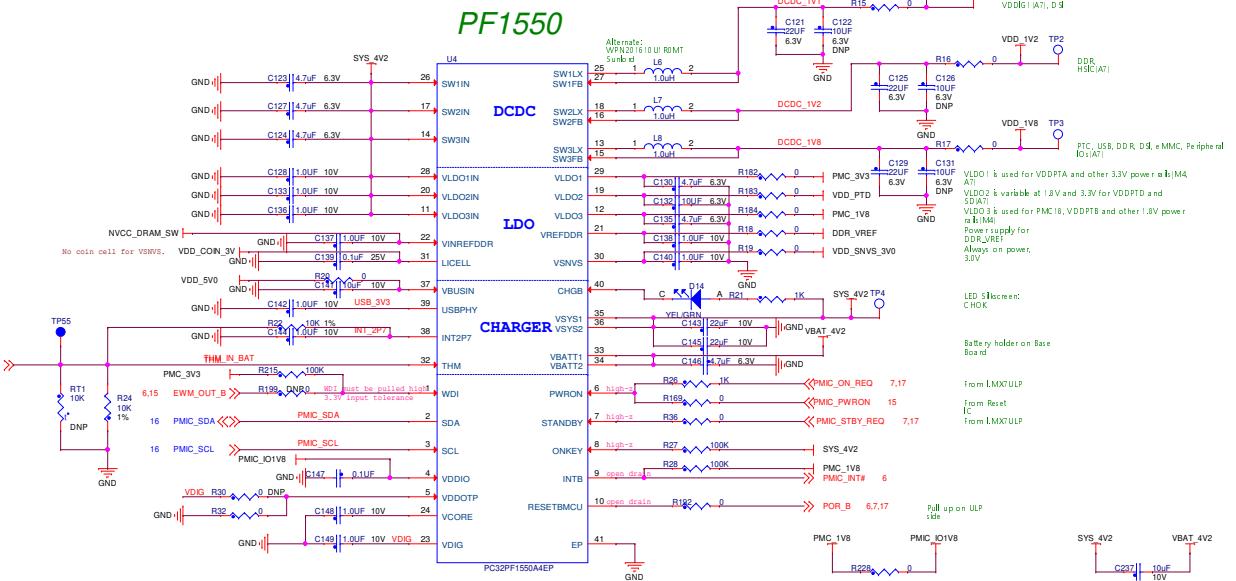
Designer: <Designer> Drawing Title: **Power Distribution Diagram**

Drawn by: <DrawnBy> Page Title:

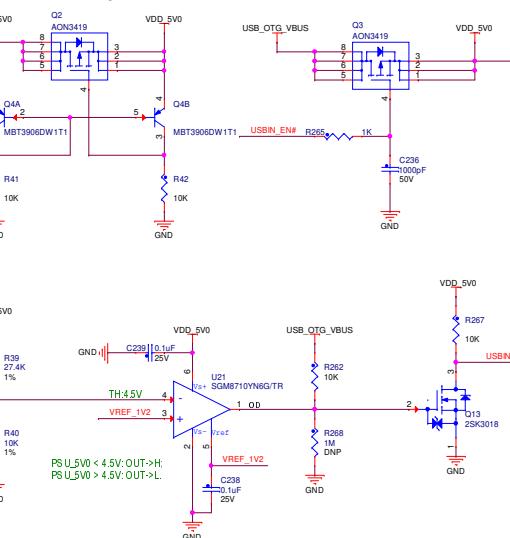
Approved: <Approver> Size A3 Document Number: SCH-29163 PDF: SPF-29163 Rev B2

Date: Wednesday, July 25, 2018 Sheet 3 of 18

# *System PMIC*

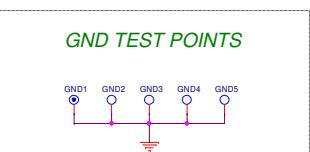


## *Dual Input Power Path Control*

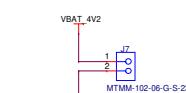


**Note:** When Wall Adapter is not present or <4.5V, the path of USB Input to Charger IC is always enabled; When Wall Adapter is present and >4.5V, the path of USB Input to Charger IC is blocked.

## **GND TEST POINTS**



### *Battery Test Points*



PF1550 Power Outputs Sequence						
Regulator	Voltage /V	Name	Power Sequence	Block	Current (mA)	Note
SW1	1.1	VDD_V1	4	A7	1000	
SW2	1.2	VDD_V2	1	A7, PTD, R3	1000	
SW3	1.8	VDD_VB	2	A7	1000	
VDDQ1	3.3	PVC_3V3	1	M4, A7	300	
VDDQ2	3.3/1.8	VDD_PTD	2	A7	400	Data w/ 3.3V PTD, SD/EMMC
VLD03	1.8	PVC_1VB	1	M4	300	
VSNSV	3.0	BDV_SNVS_3V0	0	SNVS	2	Always on
VSYS	4.2	SYS_4V2	0	Charge	1500	SYS w/ 4.2V Power Output
VBATTT	4.2	VBAT_4V2	0	Charge	1000	Battery
VREFDDR	0.6	DDR_VREF	3	A7	10	Dependent on VINREFDDR

#### SYSTEM POWER RAIL

Voltage / V	Ref ID Name	Block	Generated By	Current Capability (mA)	NOTES
5.0	PSU_5V0	DC5V	Power Adp per	2000	From Base Board
	USB_OTG_VBUS	USB	USB Adp per	1500	Could be Input or Output
4.2	VDD_9V0	Charger	PSU_5V0/ USB_OTG_VBUS	2000	
	SYS_4V2	RESET	VDD5V0	1500	
3.6	VBAT_4V2	Charger	SYS_4V2	1000	
	VDD_VBAT_4V2	S NS	VBAT_4V2	2	
3.3	VDD_3V6	WIFI	VDD5V0	1000	
	WIFI_VBAT	WIFI	SYS_4V2	300	
3.1/1.8	VDD_ANA33	ADC	PMC_3V3	50	
	VSD_3V3	SD	VDD_3V3	100	
3.3/1.8	A7_PFB_3V3	Peripheral	PSU_5V0	1000	A7 Peripheral on Base Board
	M4_PFB_3V3	Peripheral	PSU_5V0	300	M4 Peripheral on Base Board
3.3/1.8	VDD_PTDO	SD/EMMC/PTDO	PF1150 VDD_3V3	400	3.3V/LVCMOS usable
	VDD_DIO	WIFIS_DIO/PTE	External 1.8V	400	3.3V/LVCMOS usable
3	VDD_3VNS_3V0	PMIC_SINA	PF1150 SW5	2	3.0V fixed
	PMC_VDDIO				
1.8	PMC_1V8	PMIC M4 Core PIL IOREF PTB QSPI	PF1150 VDD_3V3	300	PMIC_VDDIO VDD_PTB VDD_PMC18_DIG0 VDD_PMC18 VDD_PIL VDD_IOREF
	VDD_ANA18	ADC	PMC_1V8	10	
1.5	VDD_1V8	DDR USB DSI PTC	PF1150 SW3	1000	VDD0_DDR VDD1_ISI88 VDD_DS18 VDD_PTC DDR_VDD1
	VDD_VBAT_1V8	S NS	U7	2	
1.2	A7_PFB_1V8	Peripheral	A7_TER_3V3	100	A7 Peripheral on Base Board
	M4_PFB_1V8	Peripheral	M4_TER_3V3	100	M4 Peripheral on Base Board
1.1	LDO_VDD1P5	WIFI	WIFI_VBAT	300	
	VDD_1V2	DDR HSIC	PF1150 SW2	400	DDR_VDDCA DDR_VDQ2 VDD_HSIC
1.0	NVCC_DRAM_3V	DDR	VDD_1V2	400	UDP_VDD_DDR DDR_VDDQ
	A7_CORE				DDR_DIG1
1.1	VDD_1V1	I2C_A7 DSI	PF1150 SW1	400	VDD_PMC1C12_06G1 VDD_PMC1C12_06G1_CA
	VDD_DIG0	M4 Core	I2C_M4	50	VDD_DIG0 VDD_PMC1C12_DIG0_CAP
1.0	ADC_VREF	ADC	ADC_VREF	10	



---

Microcontroller Product Group

Proprietary to NXP and shall not be used for engineering design.

ICAP Classification: CP: IUO: A PUBI

IMX7ULP-EVK SOM

e: System RMIC

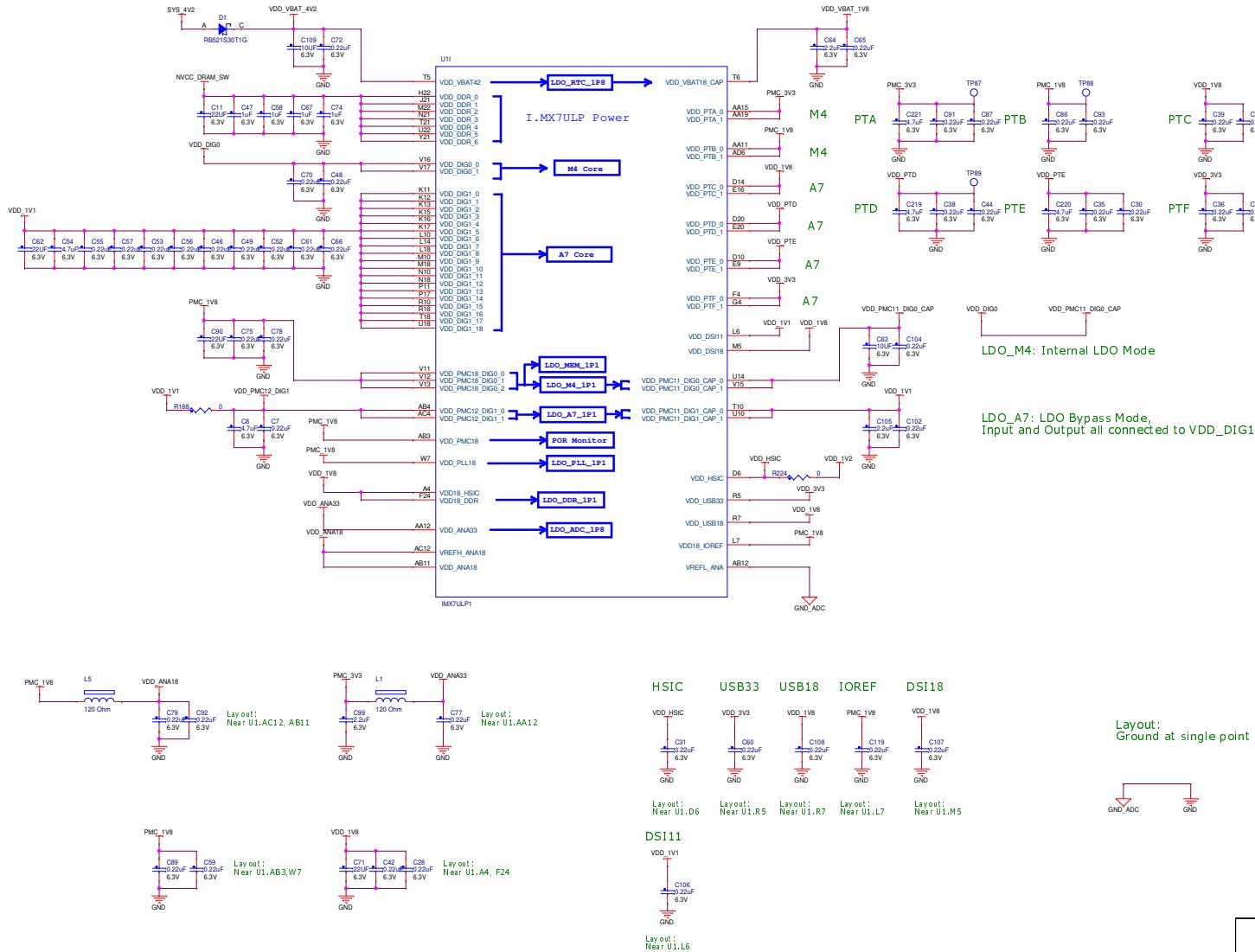
---

System PMIC

SCH-29163 PDF: SPF-29163

Wednesday, June 12, 2019 | Sheet 4 of 18

## *IMX7ULP Power*

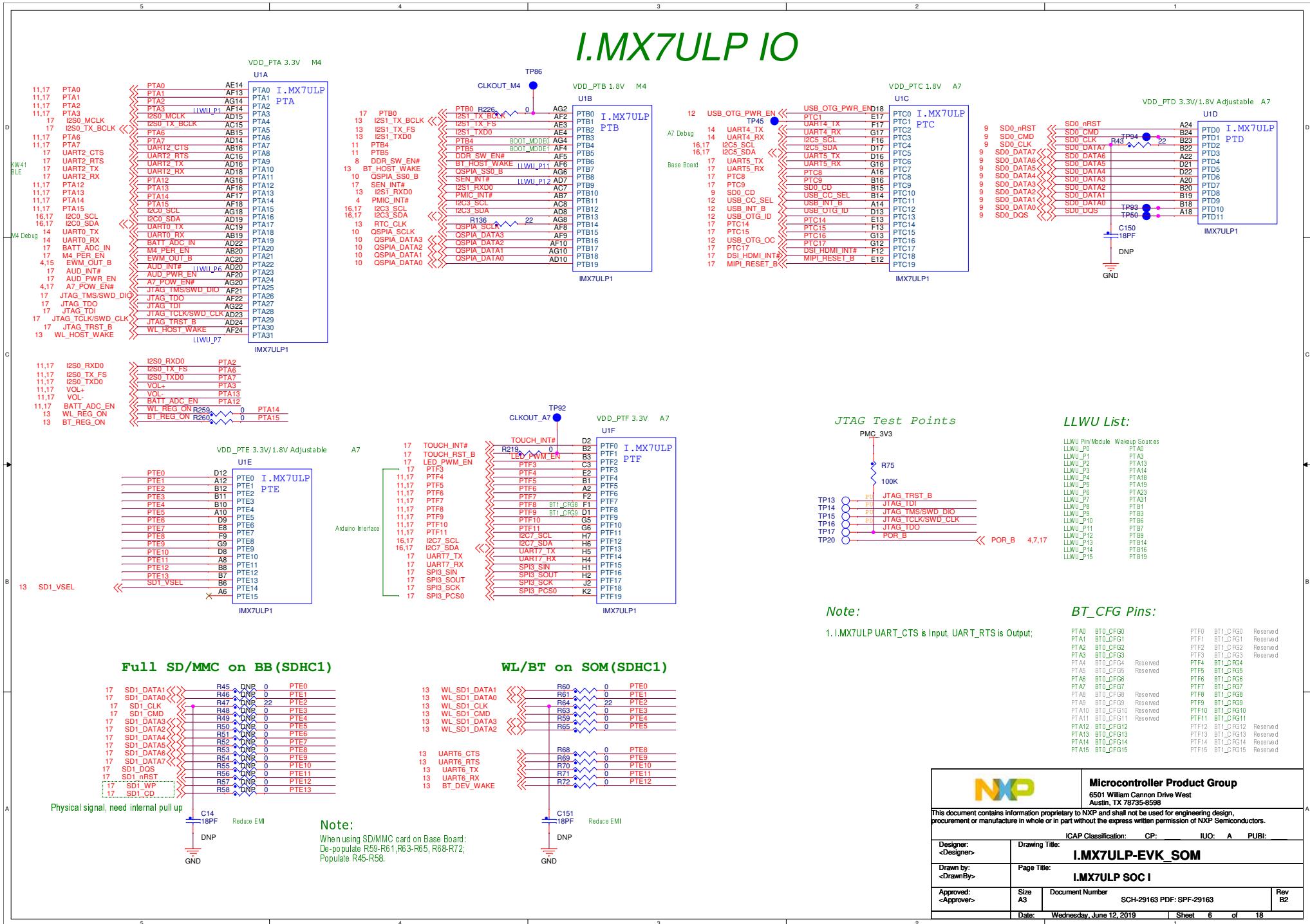


LDO\_A7: LDO Bypass Mode,  
Input and Output all connected to VDD\_DIG

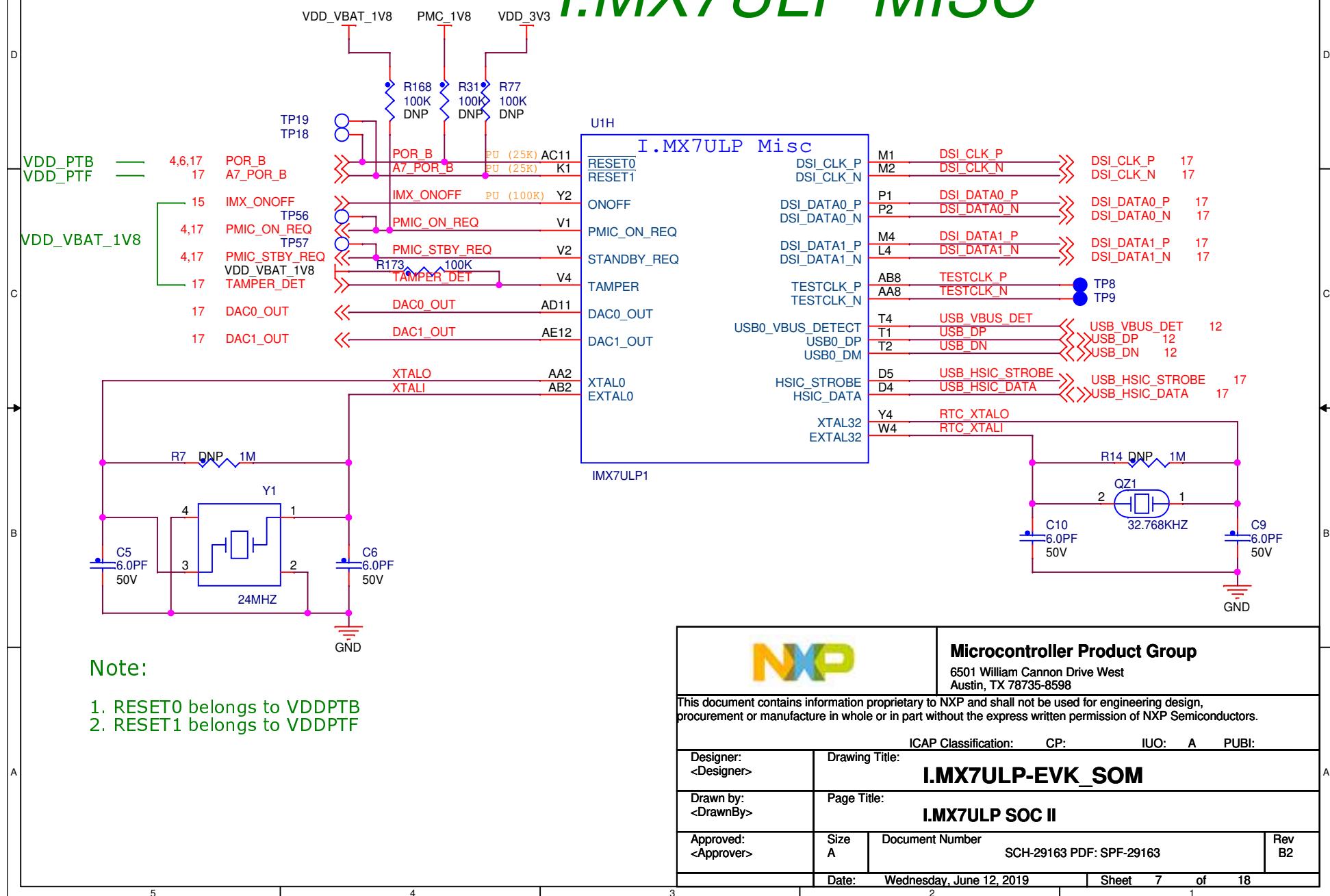
Layout:  
Ground at single point

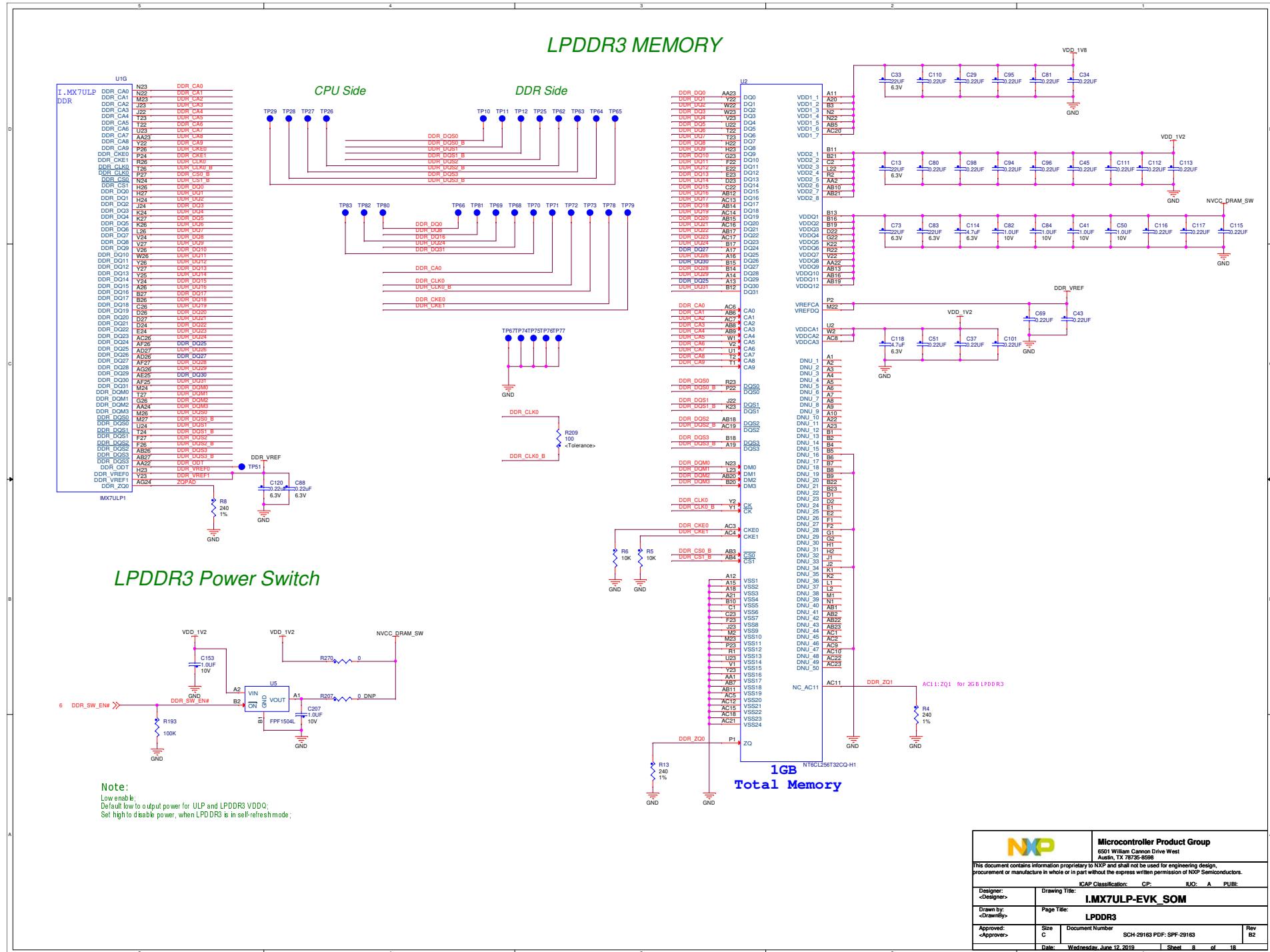
		Microcontroller Product Group			
		6501 William Cannon Drive West Austin, TX 78730-8500			
<p>This document contains information proprietary to NXP Semiconductors. It is intended solely for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.</p>					
ICAP Classification:		CP-	ILO:	A	PUBL:
Designer:	Drawing Title:	<b>LMX7ULP-EVK_SOM</b>			
<Designer>					
Review by:	Page Title:	<b>LMX7ULP Power</b>			
<Reviewer>					
Approved:	Size	Document Number			
<Approver>	A2	SCN-29163 PDF: SPF-29163	Rev B2		
Date:	Wednesday, June 29, 2016				
	I	Sheet	5	of	18

# I.MX7ULP IO

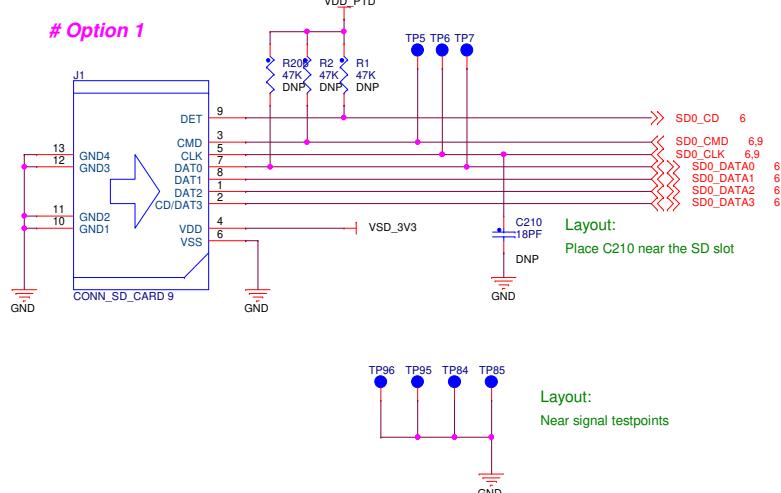


# I.MX7ULP MISC

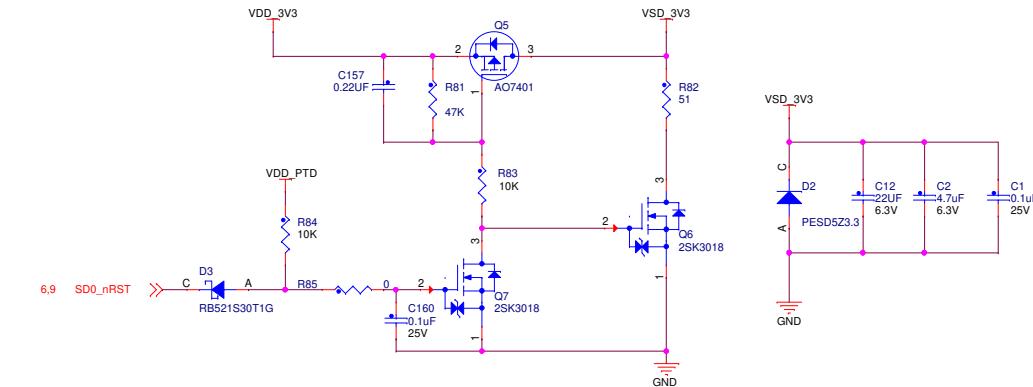




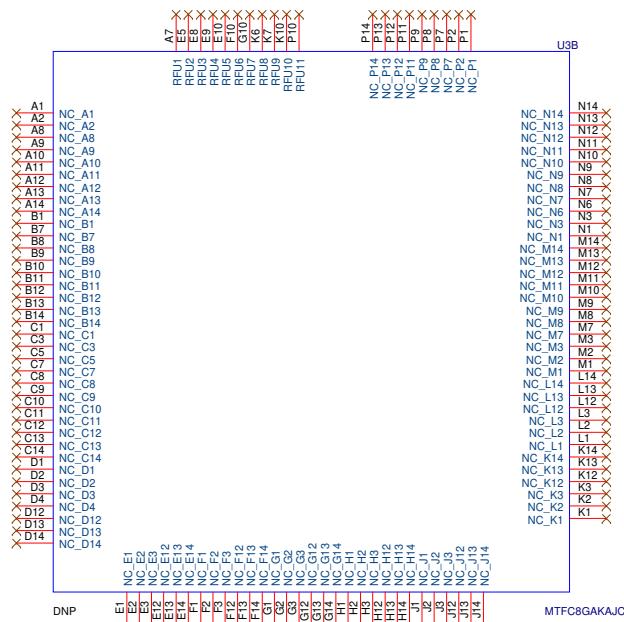
## MicroSD Push-Push Socket(Default)



## Power Switch for SD3.0

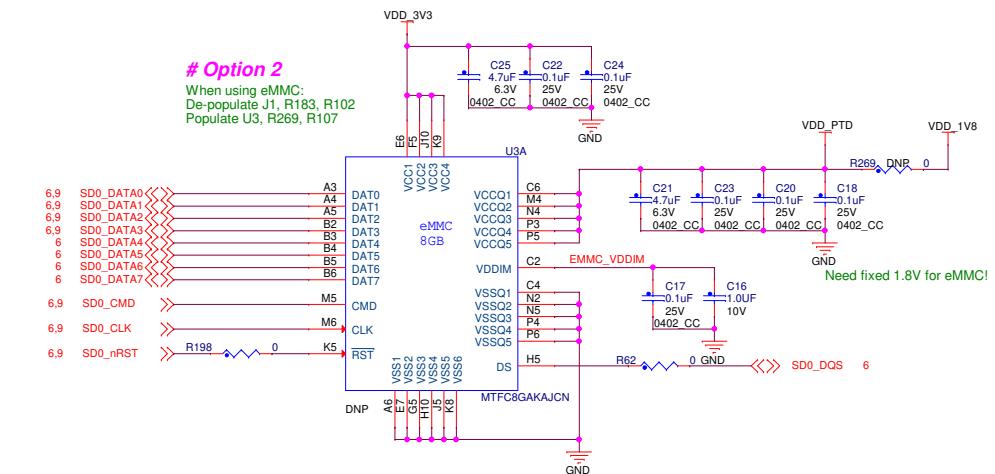


## eMMC 5.0 Footprint



### # Option 2

When using eMMC:  
De-populate J1, R183, R102  
Populate U3, R269, R107



Microcontroller Product Group

6501 William Cannon Drive West  
Austin, TX 78735-8598

ICAP Classification: CP: IUO: A PUBI:

I.MX7ULP-EVK\_SOM

Drawn by: <DrawnBy>

Page Title: SD & eMMC

Approved: <Approver>

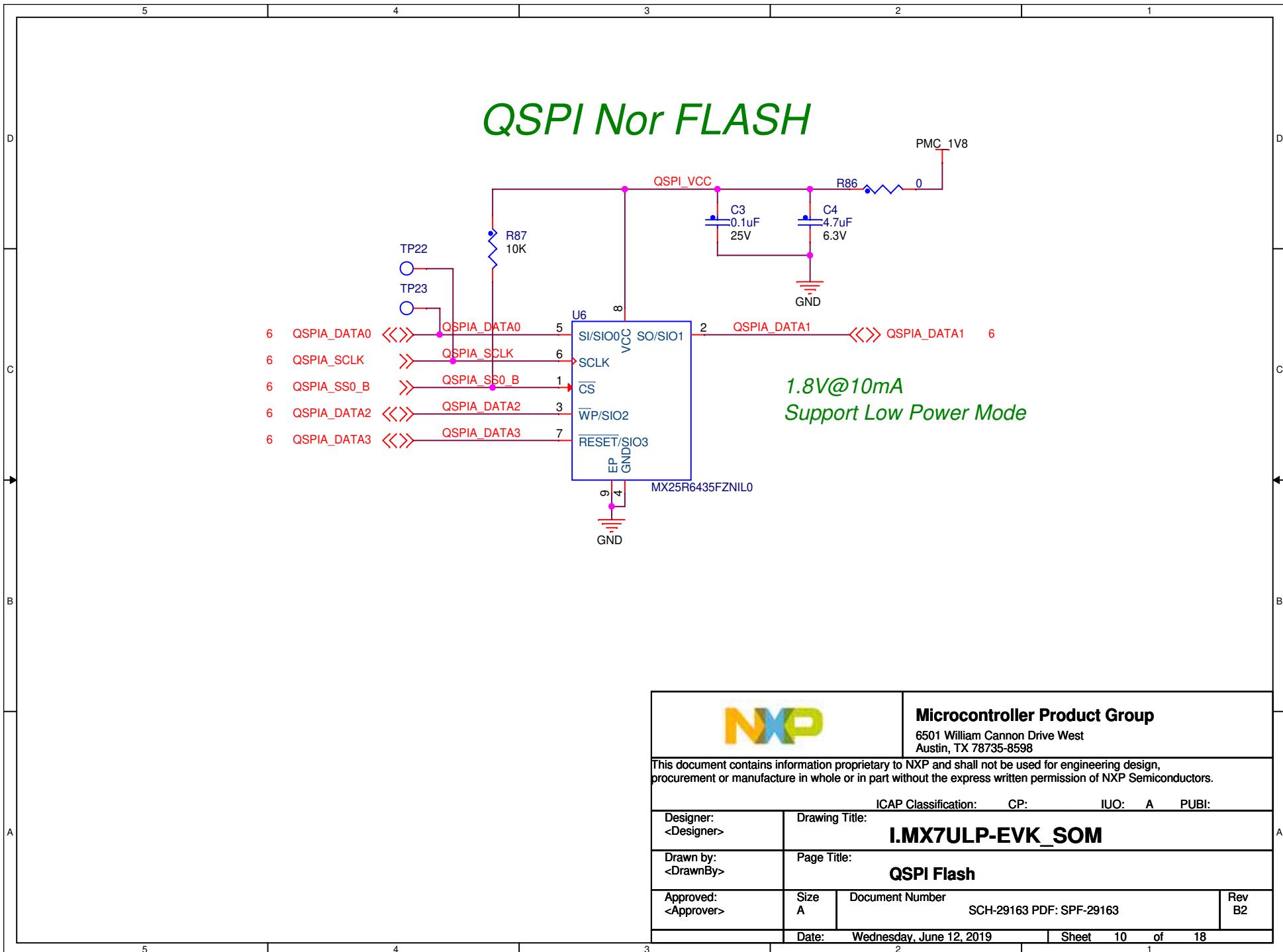
Size: A3

Document Number: SCH-29163 PDF: SPF-29163

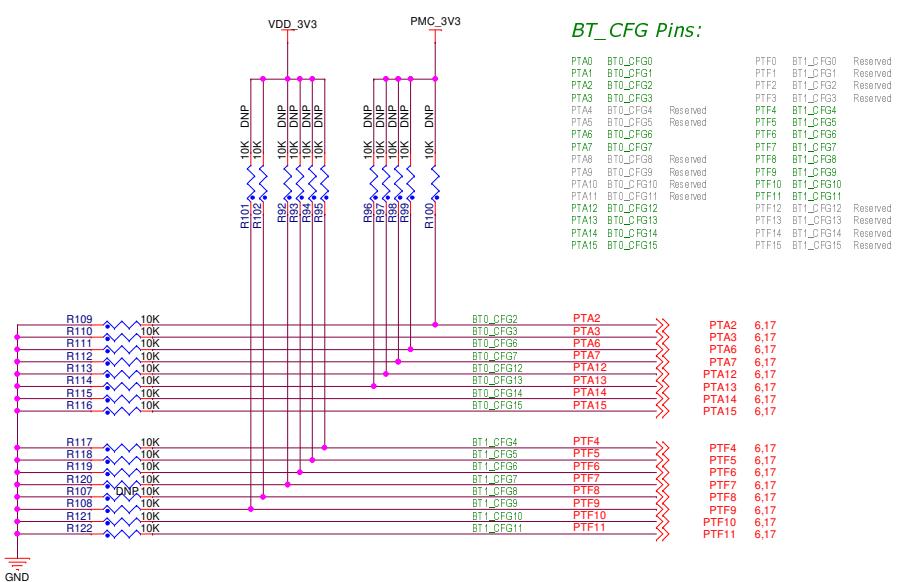
Rev: B2

Date: Wednesday, June 12, 2019

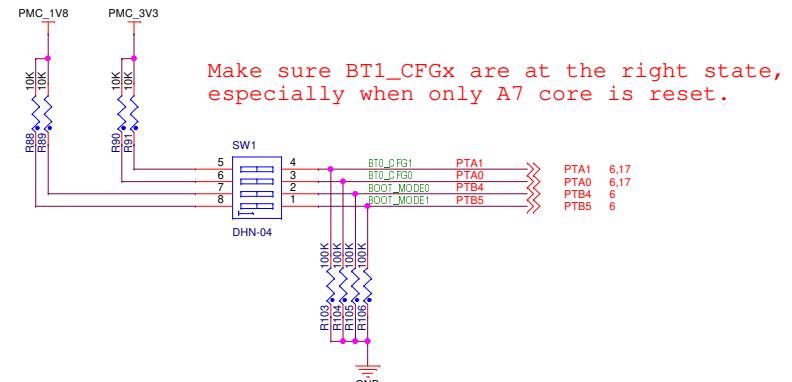
Sheet: 9 of 18



## Boot Configuration



## Boot Switch



Note:  
i) 1001 as default

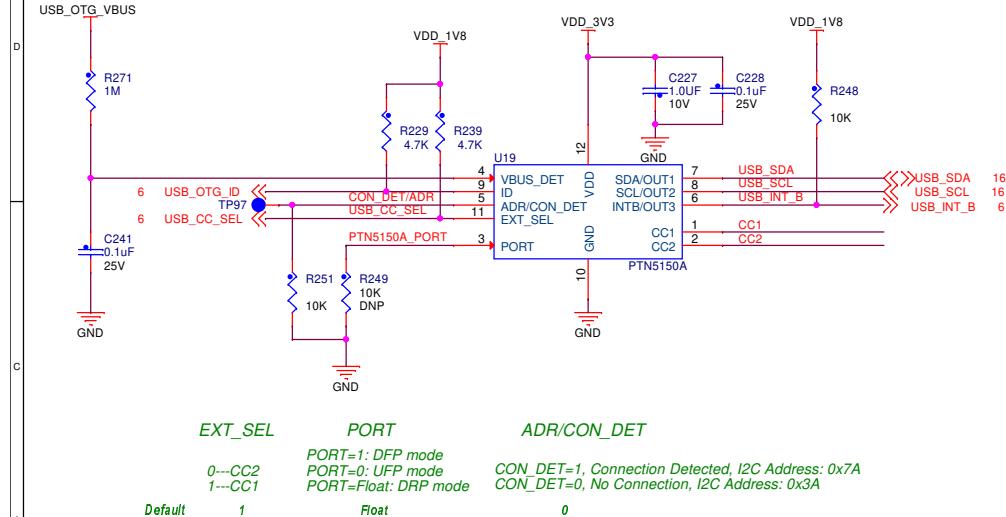
## FUSE MAP

0	0	0	0	0	0	0	0	0	1	0
<b>TYPE</b>	<b>BT0_CFG15</b>	<b>BT0_CFG14</b>	<b>BT0_CFG13</b>	<b>BT0_CFG12</b>	<b>BT0_CFG7</b>	<b>BT0_CFG6</b>	<b>BT0_CFG3</b>	<b>BT0_CFG2</b>	<b>BT0_CFG1</b>	<b>BT0_CFG0</b>
QSPI	QSPI instance 00 - QSPI0 Others - reserved	QSPI device type 00 - 3B read supported 01 - Hyperflash 1.8V 10 - Hyperflash 3.0 11 - 4B read supported	External OSC Freq Selection 00 - 24Mhz 01 - 30Mhz 10 - 19.2 Mhz 11 - 26Mhz (Not supported by ROM in ULP1 TO1.0)	M4 boot interface 0 - QSPI Others- reserved	Infinit-Loop (Debug USE only) 0 - Disable 1- Enable	Dual Boot 0- Boot from eMMC/SD 1- Boot from A7/eMMC/SD and M4/QSPI	LP Boot 0- No Low Power Boot 1 = Boot from M4 with A7 on demand			
SD/eSD										
MMC/eMMC										

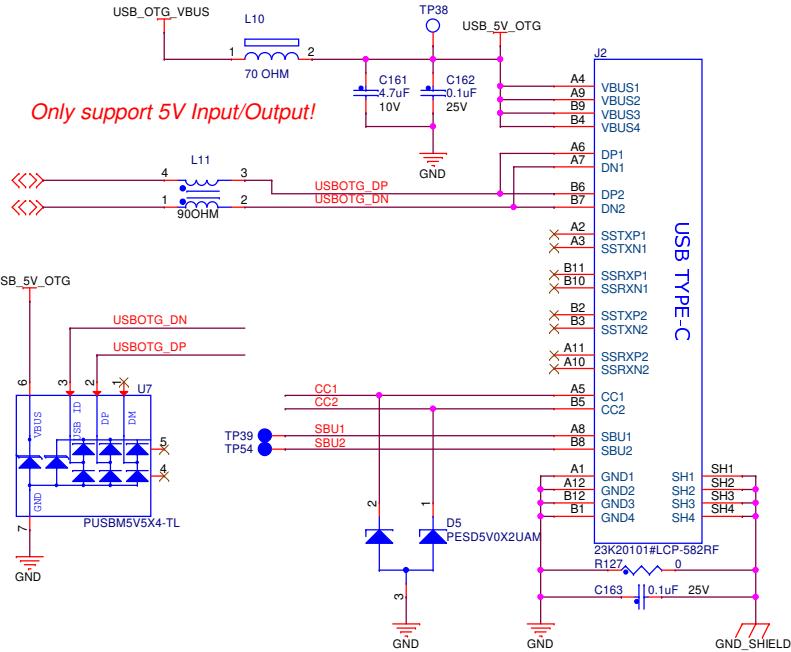
0	0	0	1	0	0	0	0	0
<b>TYPE</b>	<b>BT1_CFG11</b>	<b>BT1_CFG10</b>	<b>BT1_CFG9</b>	<b>BT1_CFG8</b>	<b>BT1_CFG7</b>	<b>BT1_CFG6</b>	<b>BT1_CFG5</b>	<b>BT1_CFG4</b>
QSPI	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SD/eSD	A7 boot interface 000 - USDHCO 001 - USDHCI others - reserved	USDHC device type 0 - eMMC 1 - SD	SD Speed 000 - Normal 001 - High Others - Reserved	SD Loopback Clock Source Sel for SDR50 and SDR104 only '0' - through SD pad '1' - direct	Bus width 00 - 4 bit 01 - 8 bit 10 - 4 bit DDR 11 - 8 bit DDR	Speed 0 - Normal 1 - High	eMMC fast boot 0 - disable 1 - enable	
MMC/eMMC								

<b>NXP</b>	<b>Microcontroller Product Group</b>
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.	
ICAP Classification:	CP: IUO: A PUBL:
<Designer>	Drawing Title:
<DrawnBy>	Page Title:
Approved: <Approver>	Size A3 Document Number SCH-29163 PDF: SPF-29163 Rev B2
Date: Wednesday, June 12, 2019	Sheet 11 of 18

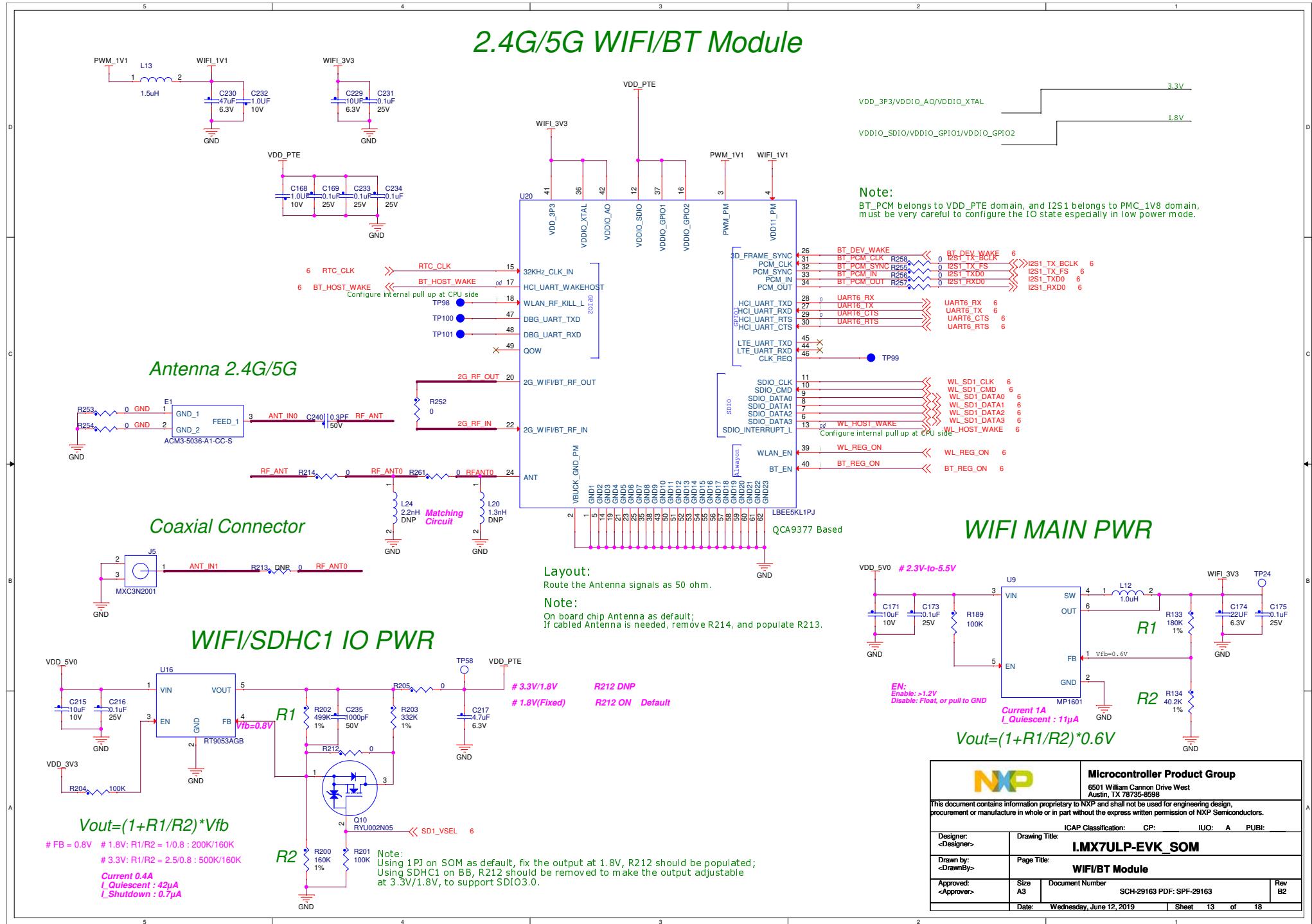
## CC Logic Control



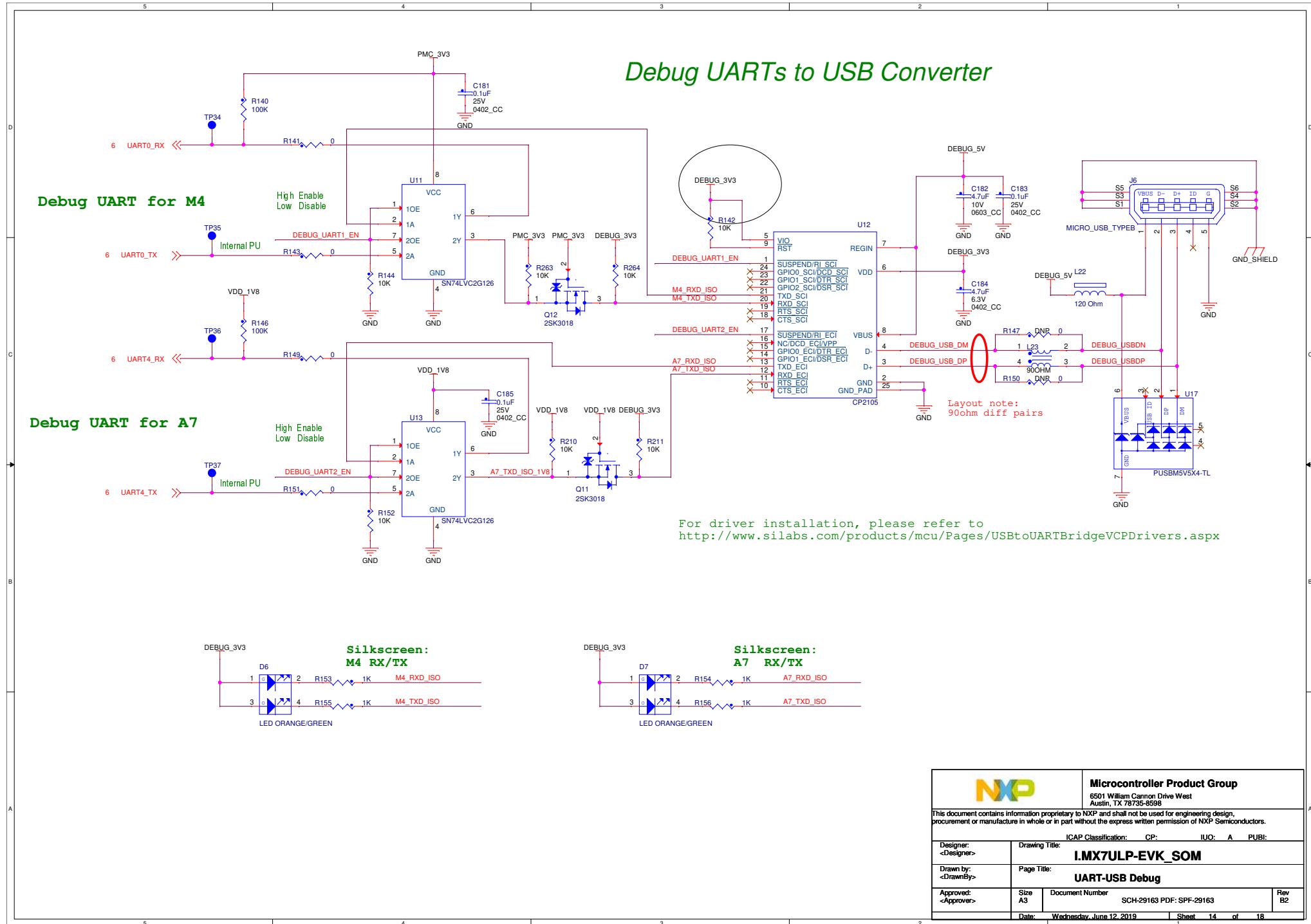
## USB TYPE-C Port



# 2.4G/5G WIFI/BT Module



# Debug UARTs to USB Converter



**Microcontroller Product Group**  
6501 William Cannon Drive West  
Austin, TX 78735-8598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

ICAP Classification: CP: IUO: A PUBI:

I.MX7ULP-EVK\_SOM

Drawn by: <Designer>

Drawn by: <DrawnBy>

Approved: <Approver>

Date: Wednesday, June 12, 2019

Size A3

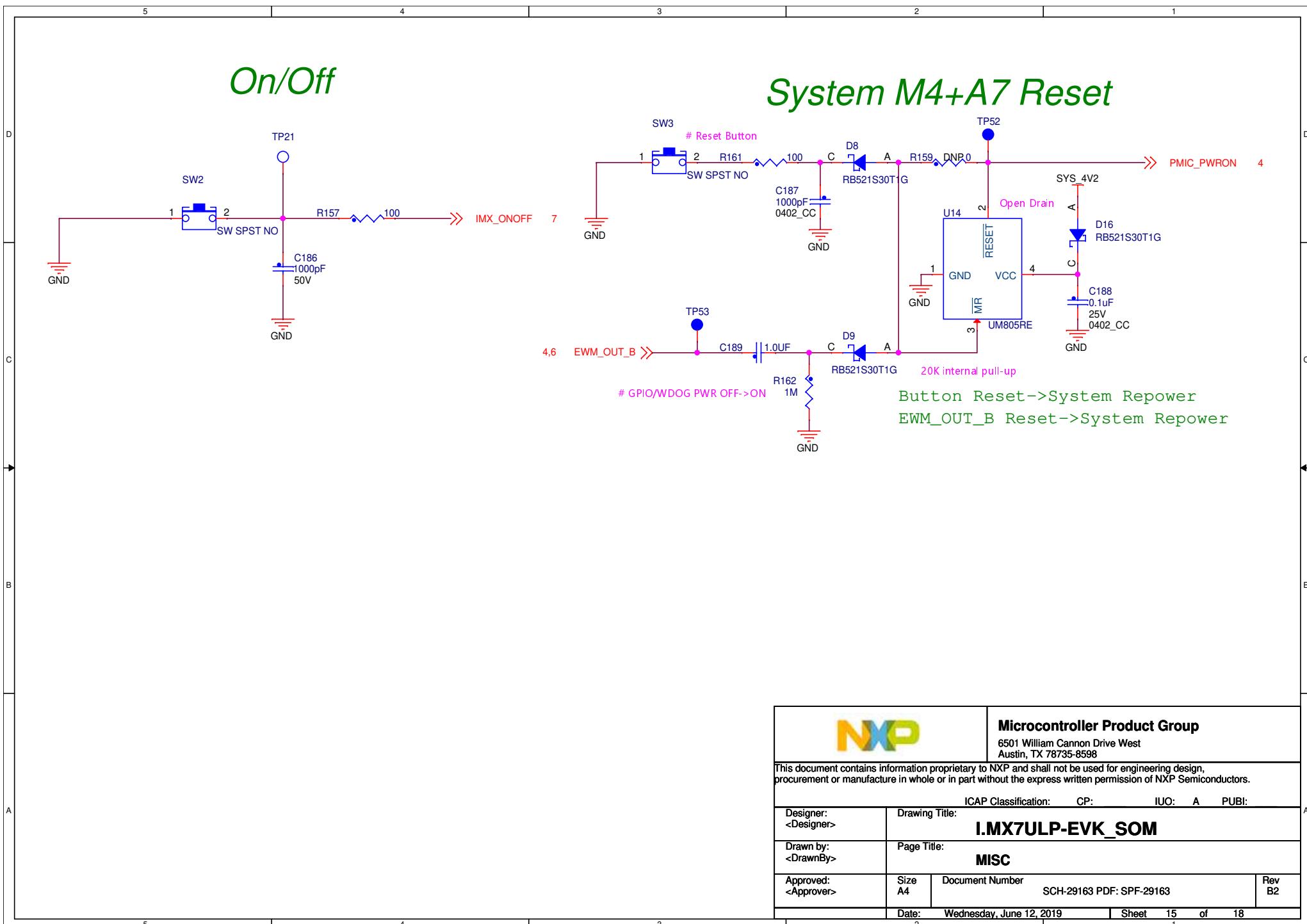
Document Number SCh-29163 PDF: SPF-29163

Rev B2

Sheet 14 of 18

*On/Off*

*System M4+A7 Reset*



**Microcontroller Product Group**

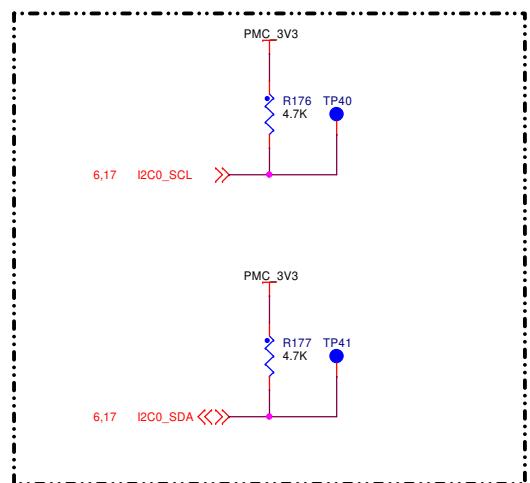
6501 William Cannon Drive West  
Austin, TX 78735-8598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

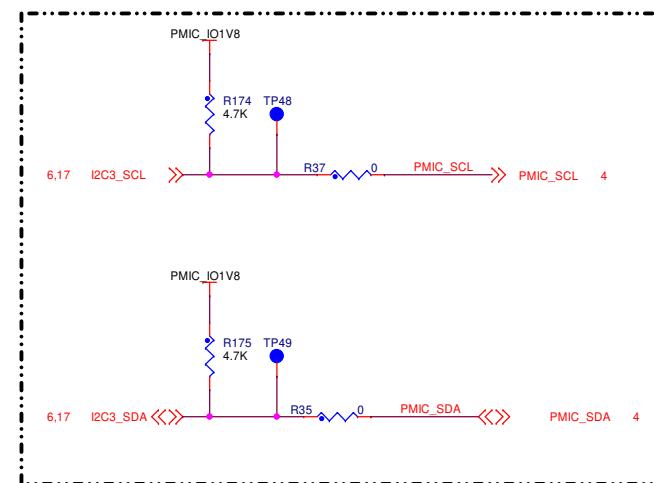
ICAP Classification: CP: IUO: A PUBLI: A

Designer: <Designer>	Drawing Title: <b>I.MX7ULP-EVK_SOM</b>		
Drawn by: <DrawnBy>	Page Title: <b>MISC</b>		
Approved: <Approver>	Size A4	Document Number SCH-29163 PDF: SPF-29163	Rev B2
	Date: Wednesday, June 12, 2019	Sheet 15	of 18

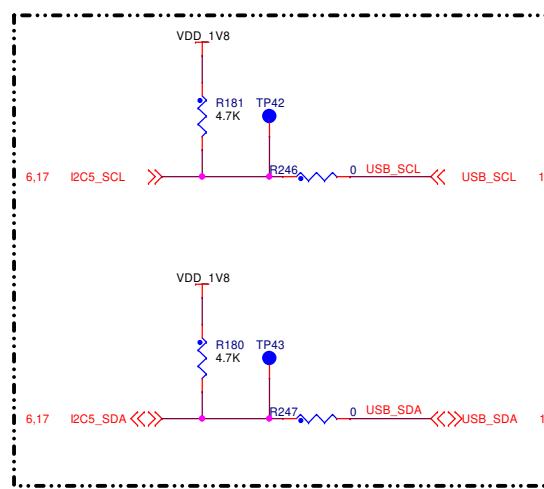
*I2C0(M4, 3.3V)*



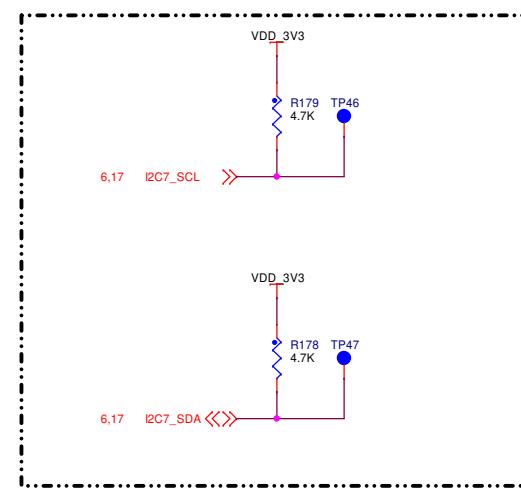
*I2C3(M4, 1.8V)*



*I2C5(A7, 1.8V)*

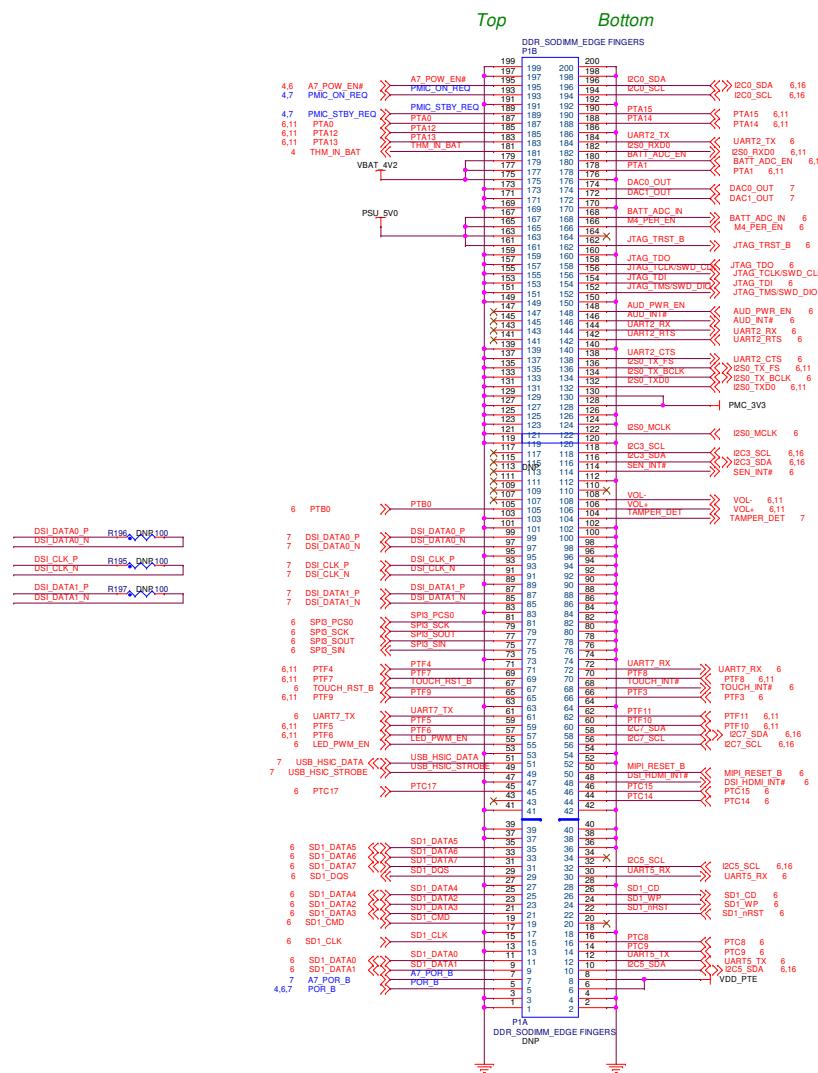


*I2C7(A7, 3.3V)*



<b>Microcontroller Product Group</b> 6501 William Cannon Drive West Austin, TX 78735-8598	
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.	
Designer: <Designer>	Drawing Title: <b>I.MX7ULP-EVK_SOM</b>
Drawn by: <DrawnBy>	Page Title: <b>I2C</b>
Approved: <Approver>	Size B Document Number SCH-29163 PDF: SPF-29163 Rev B2
Date: Wednesday, June 12, 2019	Sheet 16 of 18

## *SODIMM 200 Golden Finger*



**Microcontroller Product Group**  
6501 William Cannon Drive West

Austin, TX 78735-8598

**ICAP Classification:** CP: **IUO:** A **PUBL**

ewing Title: LMX7ULP-EVK SO

Page Title: **SPU COMMUNES**

CPU-SODIMM200

Document Number SCH-2916

de: Wednesday, June 12, 2019

1

## i.MX7ULP Board IOMUX



Microcontroller Product Gr

ation proprietary to NXP and shall not be used for engineering design.

© 2007 NXP Semiconductors N.V. All rights reserved. Reproduction in whole or in part without the express written permission of NXP Semiconductors N.V. is prohibited.

ICAP Classification: CP: IUO: A PUE

Drawing Title: IMX7U B-EVK Schematic

IMX7ULP-EVK\_SUM

## IOMUX

Document Number

SCH-29163 PDF: SPF-29163

Date: Wednesday, July 25, 2018

1