Homework Assignment 08

(Due 2:10pm, Mar. 25, email to daehyun.kim@wsu.edu or turn in hardcopies)

In this homework, we will learn how to use sub-circuits in HSpice. Subckts enable hierarchical designs (and you will also need to use subckts for Lab 3).

1. Download the following file.

    wget https://eecs.wsu.edu/~daehyun/teaching/2022_EE434/hw/subckt.sp

2. Open it in a text editor. The netlist file is self-explanatory, so you can just read it and find out how to define and use subckts. Run it and see the waveforms. (You will need the 45nm_PTM_HP_v2.1.pm file from hw07).

3. Homework problem (100 points)

Make an HSpice netlist and simulate it for the following logic:

$$Y = A \cdot B + C \cdot D$$

- Available input: A, B, C, D
- V_{DD}: 1V
- Transistor length: 45nm (for all the NFETs and PFETs).
- Define a subckt for a two-input AND gate.
    - Transistor width: 100nm (for NFETs) and 75nm (for PFETs) in the NAND part. 50nm (for NFETs) and 75nm (for PFETs) in the inverter part.
- Define a subckt for a two-input OR gate.
    - Transistor width: 50nm (for NFETs) and 150nm (for PFETs) in the NOR part. 50nm (for NFETs) and 75nm (for PFETs) in the inverter part.
- Then, instantiate two AND gates and one OR gate using the subckt definitions to implement the given logic.
- Load capacitance: 10fF (just add a capacitor between the output node and the ground)
- Use the following input waveforms (notice that your node names match my node names).

VA nA 0 PWL 0p 0 200p 0 210p Vsup 1n Vsup 1.01n 0 2.5n 0 2.51n Vsup

VB nB 0 PWL 0p 0 400p 0 410p Vsup 1n Vsup 1.01n 0 2.5n 0 2.51n Vsup

VC nC 0 PWL 0p 0 1.2n 0 1.21n Vsup 2n Vsup 2.01n 0 2.5n 0 2.51n Vsup

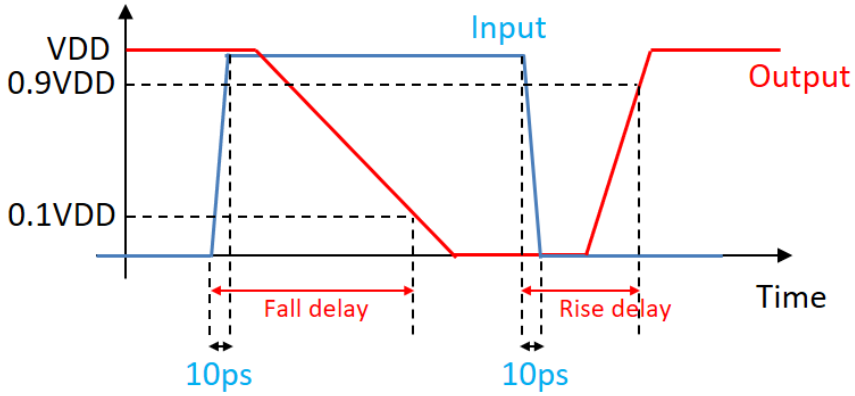
VD nD 0 PWL 0p 0 1.4n 0 1.41n Vsup 2n Vsup 2.01n 0 2.5n 0 2.51n Vsup

.tran 1p 3.2n

- Note: There are three rising edges.

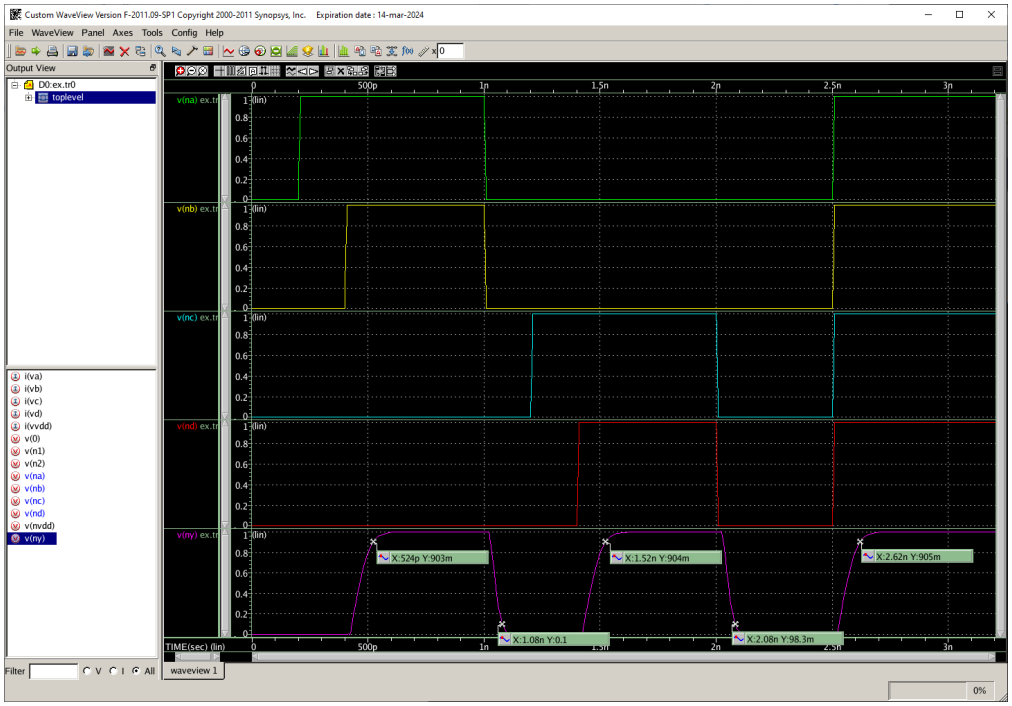
- First: B goes high 200ps after A goes high.
- Second: D goes high 200ps after C goes high.
- Third: All the four signals go high all at the same time.
- For the first and second ones, the rise delay should be measured between the time the slower signal starts going high and the time the output reaches 0.9*VDD.
- For the third one, the rise delay is just the time difference between the time any input signal starts switching and the time the output reaches 0.9*VDD.

- **Submit**
  - HSpice netlist file (.sp)
  - Signal waveforms (show all the waveforms of A, B, C, D, and Y in a single waveform snapshot (see below))
  - Two fall delay values (write down in your report)
  - Three rise delay values (write down in your report)
- Note: The rise or fall delay is measured as shown below:



- Example report

Waveform



Rise delays: 124ps, 120ps, 120ps