Consistent Modelling of I-V and C-V Behaviour of GaN HEMTs in Presence of Trapping

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***Abstract*— Charge trapping in Gallium Nitride (GaN) based high electron mobility transistors (HEMTs) is known to change the I-V behaviour of these devices. Trapping also changes the C-V behaviour of the device. In this paper, for the first time, we present a physics-based compact model which captures the I-V and the C-V characteristics of the device in presence of trapping effects consistently with I-V and C-V modelled using the same set of model formulations and physical model parameters. The developed model shows excellent agreement to the measured data. The importance of a consistent I-V and C-V model is also shown.**

***Keywords*— Gallium-nitride (GaN), high electron mobility transistor (HEMT), charge trapping, pulsed I-V, pulsed S-parameters.**

I. Introduction

Over the past decades, it has been well documented [1]–[4] that GaN HEMTs are considered to be excellent candidates for both high-frequency and high-power applications. This is attributed to material properties such as: high electron mobility, high breakdown voltage, wide bandgap etc. [5], [6]. However, it is well known that this technology suffers from charge trapping effects. The so-called "trap centers" are a deep-level defect which have been linked to such causations as: non-stabilised growth processes, dislocations due to lattice mismatch, surface states and buffer dopants [2], [5]–[8]. Trapping has been shown to degrade the device performance.

The effect that the trap centers have on the current-voltage (I-V) characteristics has been extensively studied and there exist several types of models (empirical [9], physics-based compact [1], [10] and TCAD models [11]) which can capture the influence that the trap centers have on such characteristics as; DC drain current and trans-conductance. To a lesser extent, the repercussions of trap centers on the capacitance-voltage (C-V) characteristics have been investigated [12], [13] where there are very few models in existence which can model the effect of trap centers on the intrinsic device capacitances. Typically I-V and C-V behaviour are modelled with separate sets of formulations and parameters, i.e., inconsistently. However, the same set of trap centers affect both I-V and C-V behaviour. Thus, in order to accurately model the trapping effects in an AlGaN/GaN HEMT, both I-V and C-V characteristics need to be modelled with the same set of formulations and parameters, i.e., consistently. Here for the first time, this work will illustrate the importance of a trap model which is congruent between both the I-V and C-V characteristics.

For a device which has the intended use for high-frequency (RF) circuit design, a typical figure of merit (FOM), f_T, known as the cut-off or transit frequency, is used to quantify the performance of the device as it represents the frequency at which the small-signal current gain is equal to unity and hence the output is AC shorted. An approximation of f_T can be considered as

$$f_T \approx \frac{g_m}{(2\pi(C_{gs}+C_{gd}))}. \tag{1}$$

Thus, f_T is linked to both I-V and C-V characteristics of the device. Similarly, with the application of the device being for high-power circuit design there is an importance placed upon the non-linear distortion characteristics when considering power amplifiers (PAs), where the dominant sources of distortion are; AM-AM conversion, dominated by g_m non-linearity and AM-PM conversion, dominated by non-linear capacitors. As trapping impacts both I-V and C-V behaviour, a consistent model capturing both I-V and C-V behaviour is required. This will be further illustrated through simulations of a model which is consistent between I-V/C-V characteristics and placed in comparison to an inconsistent model, where "inconsistent" means a model which neglects the effects that the trap centers have on the C-V characteristics while still capturing the effects on the I-V behaviour.

II. Trapping Effects in GaN HEMTs

In an AlGaN/GaN HEMT, the density of the two-dimensional electron gas (2-DEG) at the heterostructure interface is prone to decrease in response to the capture of electrons by the deep level defects which may be present at any one or more of four locations: the surface passivation layer, the AlGaN barrier, the GaN buffer layer, and/or the AlGaN/GaN hetero-interface. By carrying out pulsed I-V and pulsed S-parameter measurements, the trapping mechanisms can be distinguished from the self-heating effects (SHE). One of the more common trapping effects is known as current collapse, which embodies phenomena such as the gate- and drain-lag effects. Bias conditions which produce a strong vertical, possibly even horizontal, electric field along with a high leakage current result in the capture of free electrons in the 2-DEG channel. In addition to the extensively studied impact of trapping effects on I-V behaviour of the device, the

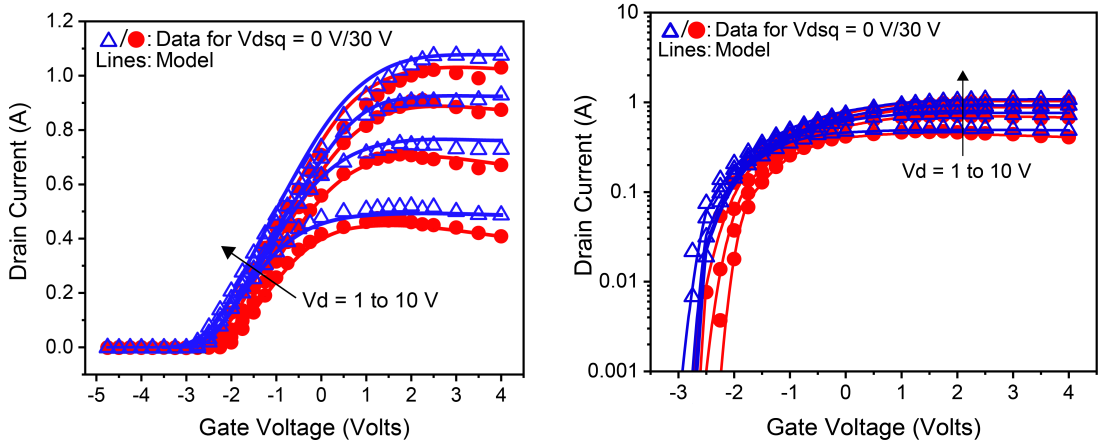

Fig. 1. Drain current versus gate voltage measured data and model for two different quiescent drain voltages (V_{dsq} = 0 V and 30 V) and quiescent gate voltage (V_{gsq} = -4.5 V) is constant. Vd = 1, 2, 4 and 10 V (a) lin-lin plot; (b) log-lin plot

trapping of charges in different regions of the device naturally impacts its C-V behaviour too. For instance, the change in the threshold or cut-off voltage due to trapping shifts the gate-bias from which C_{gs} starts to increase in $C_{gs}-V_{gs}$ characteristics. The change in I-V and C-V behaviour should then be self-consistently modelled to capture the device realistically. We present our methodology to do so in the next section.

III. Modelling Approach

In order to identify and quantify the effects of trapping on I-V and C-V characteristics, pulse measurements at different quiescent bias conditions of drain-voltage (V_{dsq}) were performed on an AlGaN/GaN HEMT device with a gate length of $0.25\,\mu m$ and a total gate width of $1.0\,mm$. We focus on the V_{dsq} points as a change in V_{gsq} is known to have very little impact on device characteristics. We measure the device such that it is biased to be in a low stress state with V_{dsq} = 0 V and a high stress state with V_{dsq} = 30 V for a fixed V_{gsq} = -4.5 V.

Fig. 1 and Fig. 2 depict the measurement and modelling results for the pulsed I-V characterisation where it can be seen that the device is experiencing well-known effects due to trapping. The increase in cut-off or threshold-voltage (VOFF) as well as decrease in on-state current at high V_{dsq} are clearly visible.

Fig. 6 depicts the gate-source intrinsic capacitance versus gate voltage, which has been extracted from the pulsed S-parameter measurements, where it can be seen that the increase in cut-off voltage is consistent between both the I-V and C-V characteristics. Similarly, it can also be seen that when the device is subject to high stress (V_{dsq} = 30 V) a large change in device behaviour is apparent as seen in Fig. 1 and Fig. 6 (red traces). The high off-state capacitance is due to a source-terminated field plate ("shield") on top of the gate. This is in agreement with the theory that by introducing dopants into the GaN buffer layer that deep level acceptor-trap centers are formed causing modulation in the 2-DEG channel. These observations are crucial in the development of modelling the trapping behaviour of the device under test (DUT).

Recent developments in the field of surface potential based compact models have reported [1] the accuracy of modelling the dynamic trapping effects with respect to I-V characteristics. This is done by means of adopting the Shockley-Read-Hall (SRH) based trap model [14] in unification with the Advanced SPICE Model for GaN HEMTs (ASM-GaN-HEMT) [10]. The trapped charges generate a "trap potential" which is then used to influence particular I-V related parameters of the ASM-GaN-HEMT model, such as VOFF, U0, UA, etc. This modelling approach can be summarised in Fig. 3.

The modification which the trapping model makes on the I-V parameters here is in agreement to the parameters presented in [1], where the deviation in the cut-off voltage and degradation in channel mobility are captured and accounted for. Here we also find that the sub-threshold behaviour of the device also changes due to trapping effects and we model this

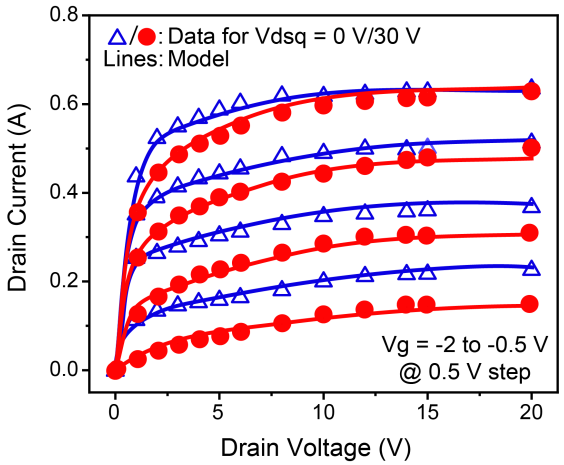

Fig. 2. Drain current versus drain voltage measured data and model for two different quiescent drain voltages (V_{dsq} = 0 V and 30 V) and quiescent gate voltage (V_{gsq} = -4.5 V) is constant

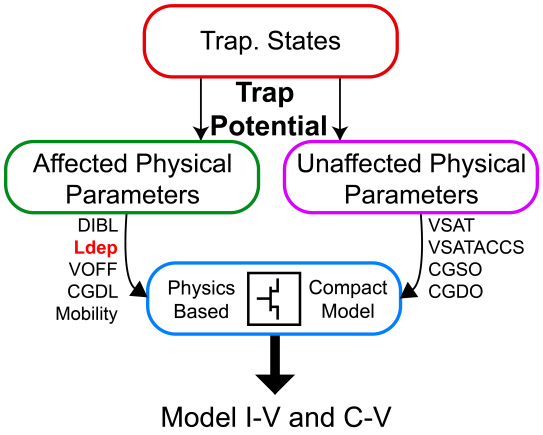

Fig. 3. Simplified flow diagram of how the trap model is used in conjuction with the transistor model

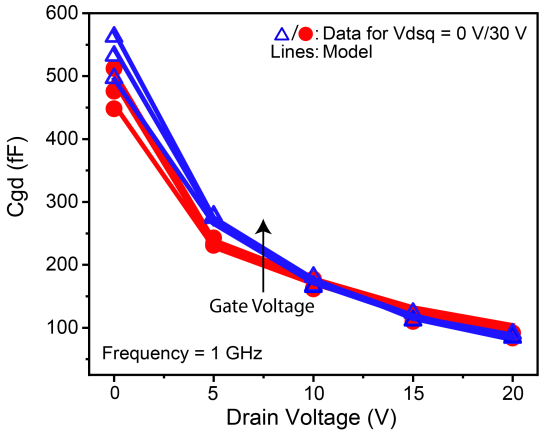

Fig. 4. Gate-drain capacitance versus drain voltage for the two quiescent bias conditions. Where V_{gsq} = -4.5 V and V_g = -2.5 V to -0.5 V

behaviour as highlighted by the semi-log plot shown in Fig. 1. The cut-off voltage is found to degrade from -2.6 V for V_{dsq} = 0 to -1.96 V for V_{dsq} = 30 V. Low-field carrier mobility is found to degrade by approximately 40% from V_{dsq} = 0 to V_{dsq} = 30 V.

Next, we investigate if the modelling of the impact of trapping on I-V behaviour consistently captures C-V behaviour too as the ASM-GaN-HEMT model has a self-consistent I-V and C-V model. We find that this is indeed the case for low drain voltage conditions for both V_{dsq}'s. This is shown in Fig. 6a. However, for high drain bias voltages the change in depletion charge due to trapping needs to be accounted for.

The charge equation used in the ASM-GaN-HEMT model is as follows [10],

$$Q_g = \frac{C_g LW}{(V_{go} - \psi_m + V_{th})}\left[V_{go}^2 + (1/3)\left(\psi_d^2 + \psi_s^2 + \psi_d\psi_s\right) - V_{go}\left(\psi_d + \psi_s - V_{th}\right) - V_{th}\psi_m\right], \quad (2)$$

where C_g is the gate capacitance per unit area, L is the total gate length, W is the total gate width, $V_{go} = V_{gs} - V_{OFF}$, V_{OFF} being the cut-off voltage, $\psi_m = (\psi_d + \psi_s)/2$; ψ_d and ψ_s are the surface potential values at the drain and source, respectively and V_{th} is the thermal voltage.

The capacitances in the ASM-GaN-HEMT model are modelled as derivatives of terminal charges, which are as follows [15],

$$C_{gs} = -\frac{\partial Q_g}{\partial V_s}, \quad (3) \qquad C_{gd} = -\frac{\partial Q_g}{\partial V_d}. \quad (4)$$

[10] states that the derivation of (2) is achieved by neglecting the effects of velocity saturation on charge carriers. However, for more aggressive GaN devices, such effects can not be neglected. Thus, it is proposed that the gate charge equation is split into two regions as follows,

$$Q_{g_{total}} = Q_g(\psi_s) + Q_{dep}, \quad (5)$$

where $Q_{g_{total}}$ is the total gate charge, $Q_g(\psi_s)$ is the charge in the 2-DEG channel with ψ_s being the surface-potential, and Q_{dep} is the depletion region charge. Where $Q_g(\psi_s)$ adheres to (2) and the depletion region charge is given by,

$$Q_{dep} = \frac{L_{dep} \cdot I_{DS}}{v_{car}}, \quad (6)$$

where L_{dep} is the length of the depletion region, I_{DS} is the drain-current and v_{car} is the carrier velocity.

With an increase in V_{ds}, the electric field in the access region is larger and there is a significant depletion region present. The amount of depletion region length is dependent on the amount of trapped charges as they can cause depletion. This causes an increase in L_{dep} with increasing V_{dsq}, where this effect has been investigated in [16]. After accounting for this additional change in the model with V_{dsq} we were able to model C-V behaviour for various Vd's and for the two different V_{dsq}'s consistently with the I-V model as shown in Fig. 4.

This work adopts the concept presented in [1], with the I-V modelling results depicted in Fig. 1 and 2; which are in excellent agreement to the measured data. However, with the application of high-frequency circuit design in mind for the DUT, the influence that the dynamic trapping effects have on

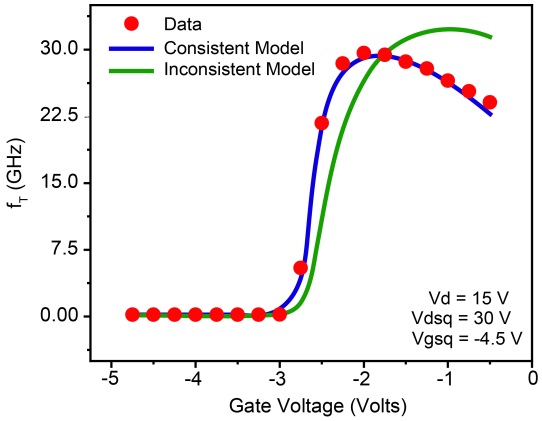

Fig. 5. Comparison of the intrinsic transit frequency (f_T) of the 0.25 µm AlGaN/GaN HEMT between a consistent model (blue trace) which accounts for the trapping effects in both I-V and C-V characteristics against an inconsistent model (green trace) which only accounts for trapping effects related to I-V characteristics

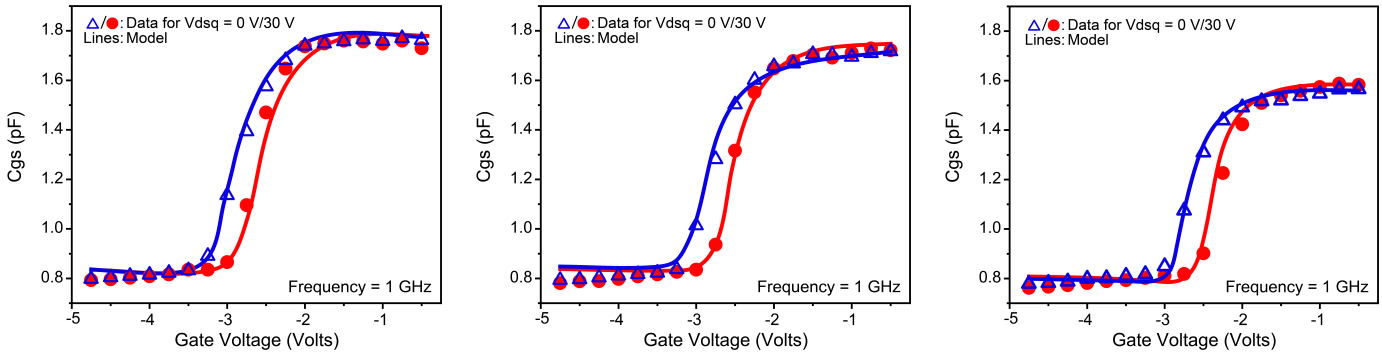

Fig. 6. Gate-source capacitance versus gate voltage for the two quiescent bias conditions. V_{gsq} = -4.5 V for all plots: (a) Vd = 0 V; (b) Vd = 10 V; (c) Vd = 20 V

not only the I-V characteristics but also the C-V behaviour and the consistency of the model between the two becomes of great importance. Next, we highlight the importance of consistently modelling the impact of trapping effects on both I-V and C-V characteristics of the device. A comparison between an inconsistent model which neglects the C-V characteristics and a consistent model is depicted in Fig. 5. Careful consideration of the two models presented in Fig. 5 illustrates the importance of a charge trapping model being consistent between both I-V and C-V characteristics. Observing the inconsistent model (green trace) in Fig. 5, while it is able to capture the influence that the trapping effects have on the I-V data, it is evident that this is not adequate for an accurate representation of the DUT's C-V behaviour.

IV. Conclusion

The influence that dynamic trapping effects have on both the I-V and C-V characteristics of a AlGaN/GaN HEMT has been presented. The importance of how the trap effects being consistent between such characteristics has been illustrated through means of analysis and demonstration. A physics-based compact model has been adopted to model the effects of trapping on the I-V behaviour. The model has been extended to model the effects of trapping on the C-V behaviour using the same set of formulations and parameters such that the model is consistent between the I-V and C-V behaviour of an AlGaN/GaN HEMT.

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