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Technical Note – TN mipi1

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Subject CRUVI for the 4-lane CSI2 Camera

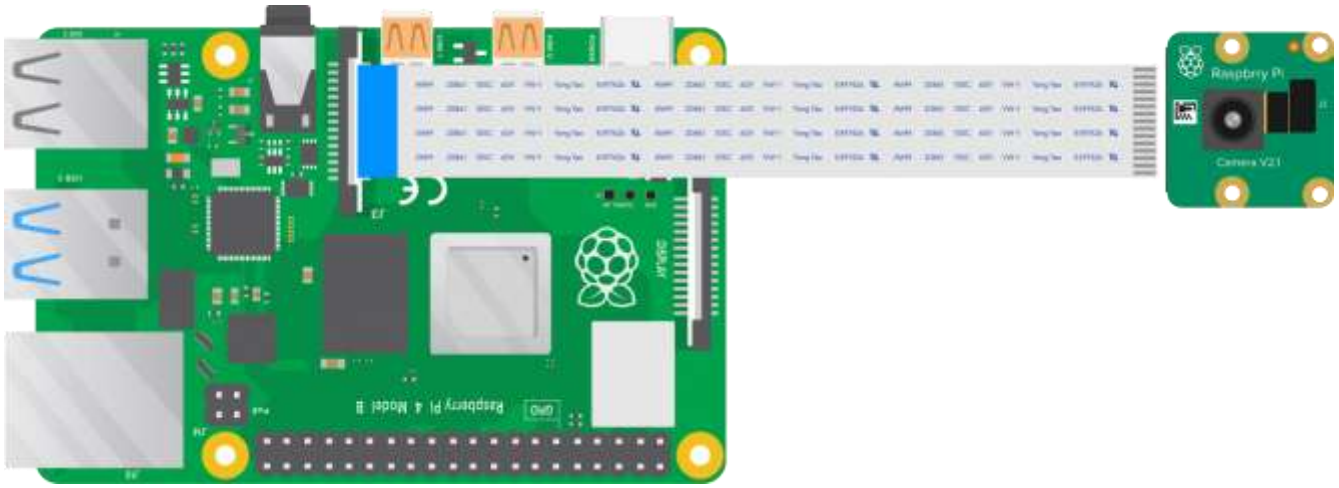
Objective Compatibility with RPi5 cameras on one side,
and Trenz TEB0707-02 Carrier Card with TE0711-01 FPGA SOM on the other

Background info

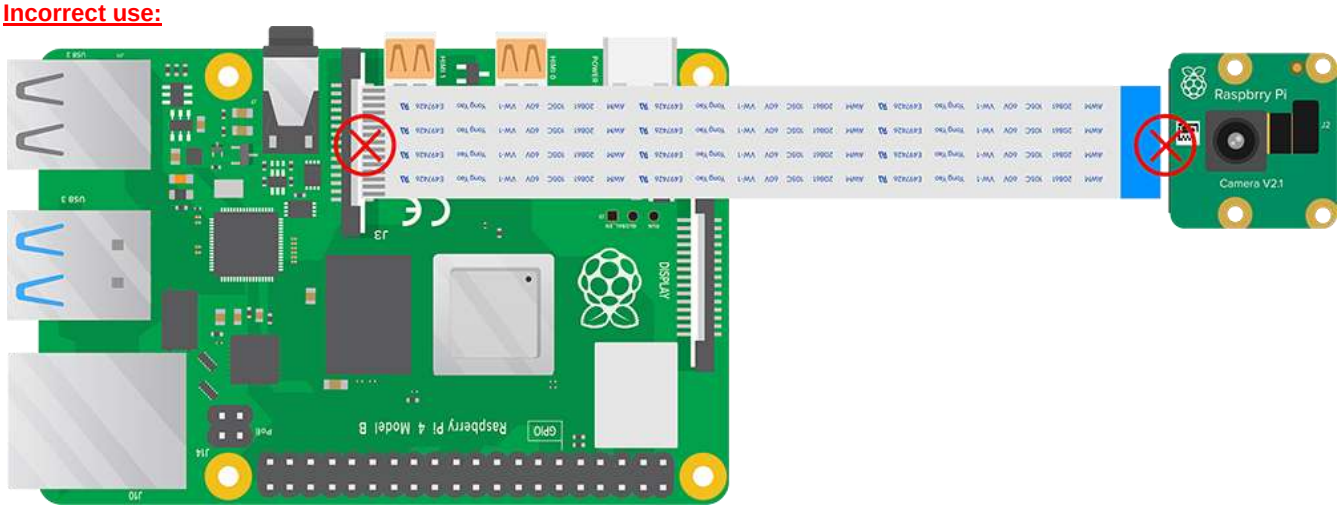
The camera connectors found on most of the previous models of Raspberry Pi were FFC (or even FPC) 15pin@1mm (15mm total, PN=SFW15R-2STE1LF) for up to 2-lane CSI imagers. Also known as "**Standard**" MIPI connector, this end-to-end-system was designed for the **OPPOSITE CONTACT CABLE**, such as illustrated below.

1) "Standard" 15pin@1mm CSI connectivity. Note cable reversal.

Correct use:

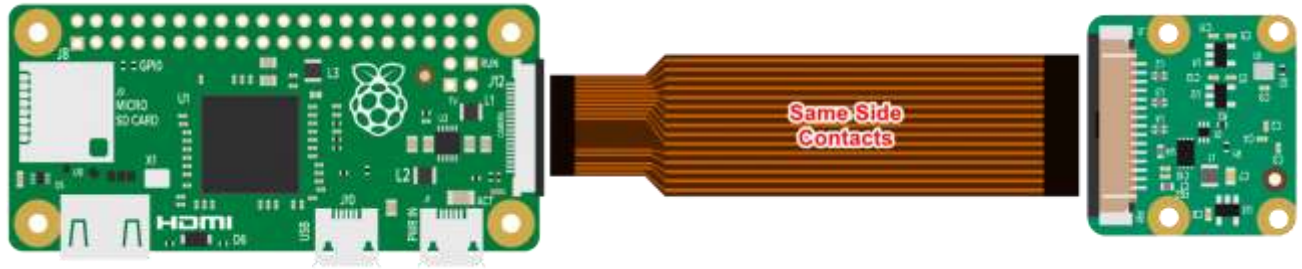


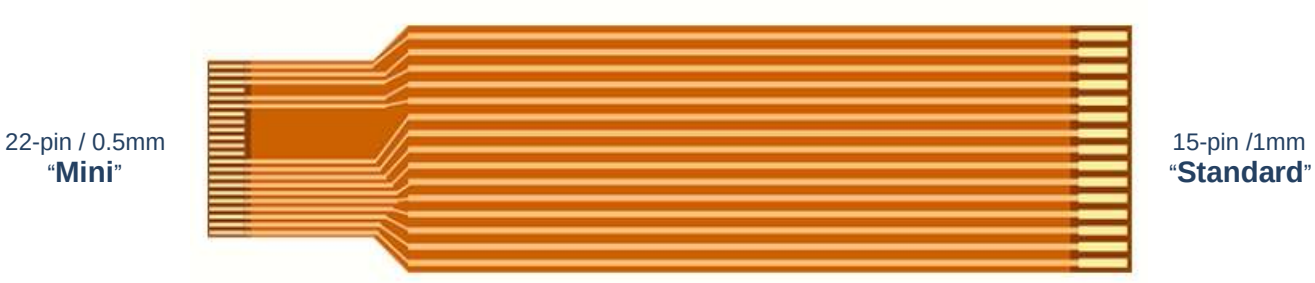
Incorrect use:



Starting with RPi5, this has changed to 22pin@0.5mm (11mm total, PN=54548-2271) for up to 4-lane HD cameras. Also known as "**Mini**" connector, this end-to-end system was designed for the **SAME CONTACT CABLE**. Part of the reason for making this change was to reduce the chance of misconnects shown in the second illustration of "Standard" system.

2) Hybrid system, with 22pin@0.5mm "*Mini*" on one end, and 15pin@1mm "*Standard*" on the other





Contacts are now on the same side of cable. The cable in this case also adapts the width and pin pitch. Despite featuring more pins, which are now denser, the new "*Mini*" connection is on the narrower side of the adapter cable.

3) Complete "Mini" system. Contacts are on the same side of the cable, exactly like on the Hybrid system (*)

However, the current CRUVI connector design is assuming the use of "*Opposite Contacts*" "*Mini*" cable. While such cables exist and can be purchased separate from the camera, they are not a norm. Indeed, the cable that comes with 4-lane IMX283 camera does not have "*Opposite Contacts*".

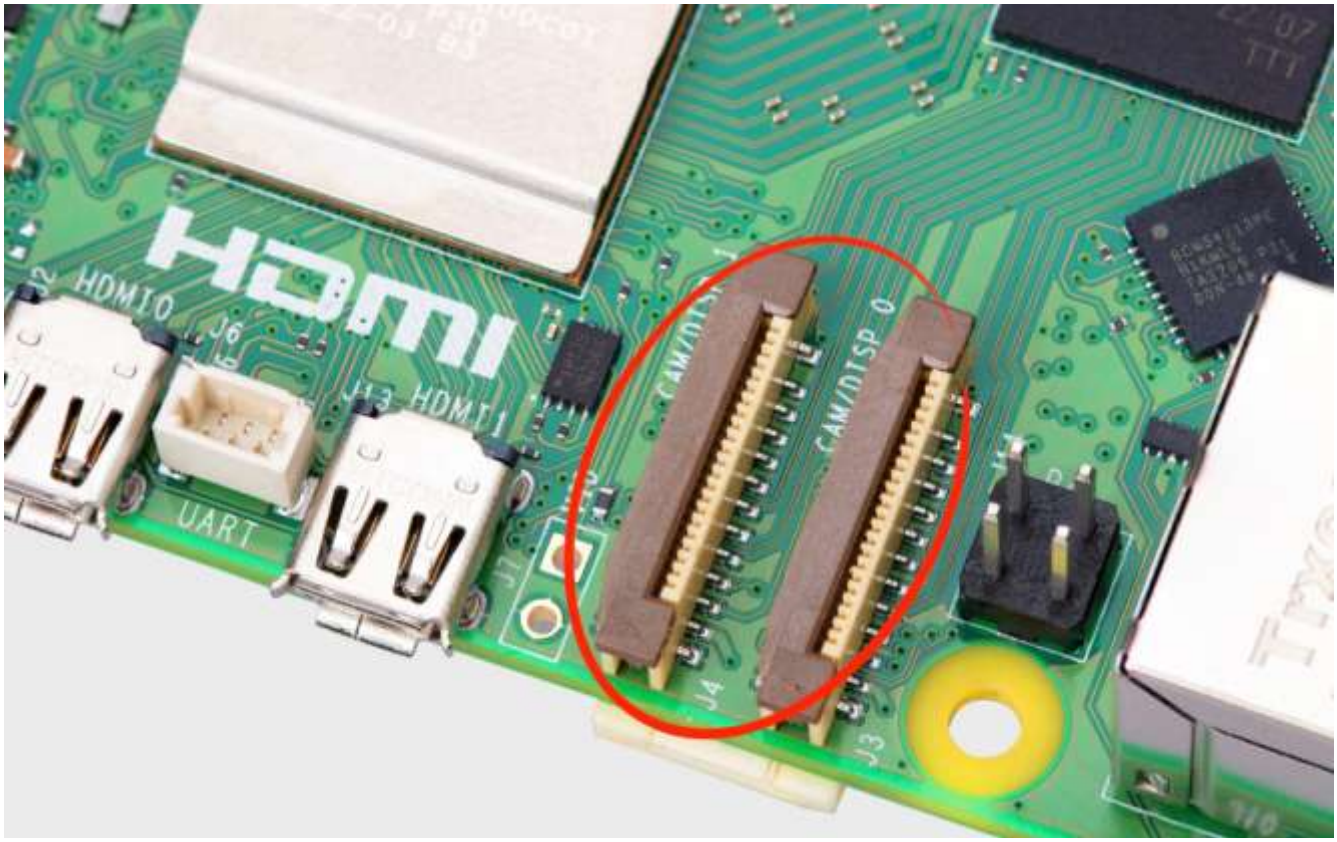
- **The use of incorrect cable results in a direct short of the 3.3V camera supply**.

Another, though less critical issue with the current CRUVI connector, is the signal mapping towards Trenz Carrier Card, which connects camera I2C pins to the on-board CPLD. This means that, for the SOM FPGA to get to camera I2C, the user needs to alter the CPLD program. While doable, this incurs unnecessary work and complications.

(*) Not to be mistaken, this discussion is for the **serial MIPI** CSI type of interfaces. There are also non-MIPI camera interfaces. One of the most popular is **DVP24**, which is a 24-pin parallel interface, with 0.5mm pin pitch. DVP stands for *Digital Video Port*. The DVP is not subject to *Mobile Industry Processor Interface* (MIPI) licensing limitations. Being parallel, the DVP is much simpler to work with, but cannot match the MIPI data throughput. DVP is therefore not suitable for imagers with high resolution and high frame rates.

Connector Pinout towards 4-lane Camera

The rule to apply is very simple: The camera side of CRUVI connector must be pinned exactly like the RPi5 MIPI connector.



The RPi5 pin assignment for MIPI connector is shown in *Table1* below. The corresponding connector on the camera side is also illustrated.

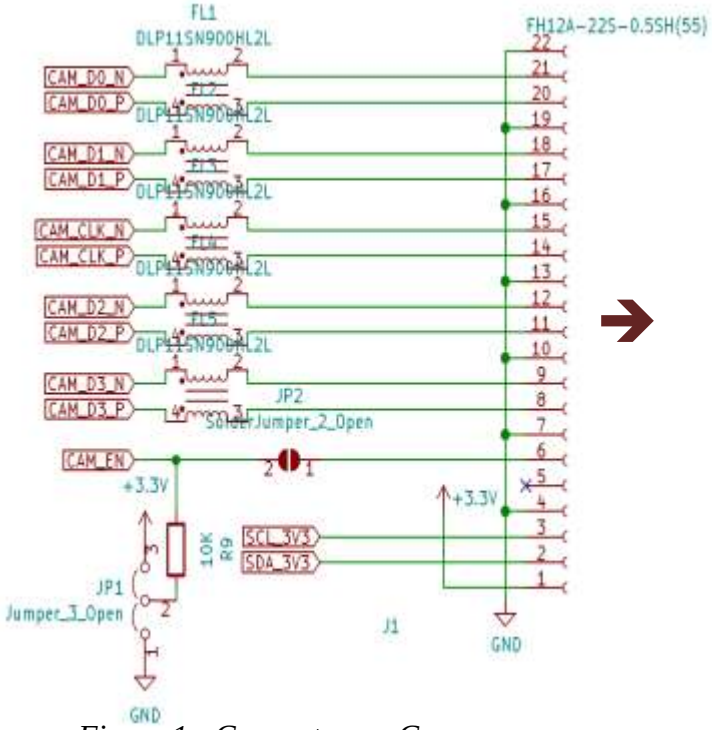


Figure 1 - Connector on Camera

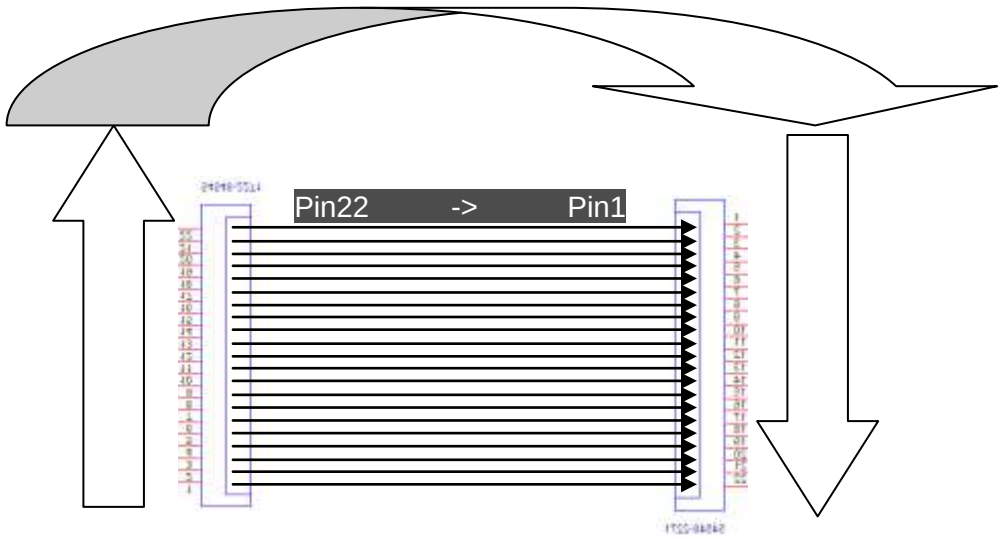
Pin	Name	Type	Description
1	GND	Ground	Power Ground
2	CAM_D0_N	RPi5 Input	Pixel Data Lane0 Negative
3	CAM_D0_P	RPi5 Input	Pixel Data Lane0 Positive
4	GND	Ground	Power Ground
5	CAM_D1_N	RPi5 Input	Pixel Data Lane1 Negative
6	CAM_D1_P	RPi5 Input	Pixel Data Lane1Positive
7	GND	Ground	Power Ground
8	CAM_CK_N	RPi5 Input	Pixel Clock Output Form Sensor Negative
9	CAM_CK_P	RPi5 Input	Pixel Clock Output Form Sensor Positive
10	GND	Ground	Power Ground
11	CAM_D2_N	RPi5 Input	Pixel Data Lane2 Negative
12	CAM_D2_P	RPi5 Input	Pixel Data Lane2 Positive
13	GND	Ground	Power Ground
14	CAM_D3_N	RPi5 Input	Pixel Data Lane3 Negative
15	CAM_D3_P	RPi5 Input	Pixel Data Lane3 Positive
16	GND	Ground	Power Ground
17	POWER-EN	RPi5 Output	Power Enable
18	LED-EN	I/O	LED Enable/XCLK
19	GND	Ground	Power Ground
20	SCL	RPi5 Output	SCCB serial interface clock input
21	SDA	RPi5 I/O	SCCB serial interface data I/O
22	VCC	Power	3.3V Power Supply

Table 1 – Connector on RPi5 Board (=CRUVI)

Note the pinout inversion from Camera to RPi5 Board. This comes from the combination of:

(1) 180-degree rotated connectors and
(2) "*Same Contact*" cable.

This connector rotation on the "*Standard*" system is compensated by the "*Opposite Contact*" cable. The "*Mini*" system however, by using "*Same Contact*" cable, counts on the RPi5 board for this compensation.



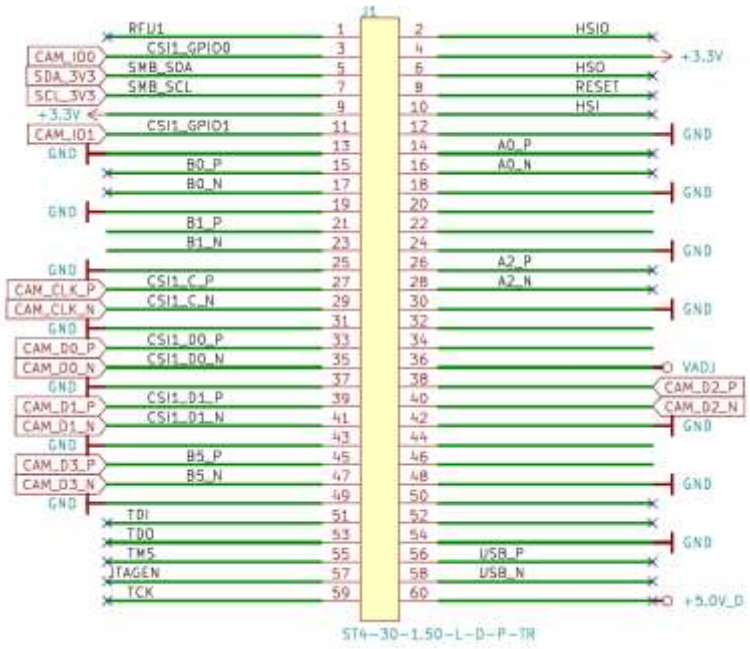
Camera => Same-Contact Cable => RPi5

Connector Pinout towards Trenz Carrier board (CRUVI connector)

Requirements:

1) No connection is to be fed through CPLD. All camera lines must have direct wiring to SOM FPGA
2) High-speed Clock pair should connect directly to LVDS FPGA Clock Capable (CC) pin
3) High-speed Data links should connect to LVDS FPGA pins in the same banks as the Clock / CC pin
   - If possible, place Data in the close proximity of Clock, ideally with Clock right in the middle
4) If possible, find the pinout that adheres to these rules for all 3 CRUVI locations on the Carrier Card

Current J1 CRUVI Pinout:



Connectivity Analysis:

CR00041				TEB0707				TEB0711		
From Camera 22-pin/0.5mm FFC		J1 CRUVI connector		J10 CRUVI connector		JB2 connect-or		JM2 connector		FPGA Bank 35
pin	signal	pin		pin	signal	pin		pin	signal	pin
20	SCL_3V3	39		39	CA_B4_P	37		38	B35_L23_N	K1
21	SDA_3V3	41		41	CA_B4_N	35		36	B35_L23_P	K2
17	POWER_EN_3V3	45		45	CA_B5_P	31		32	B35_L5_P	E6
18	LED_EN_3V3 (not used)	47		47	CA_B5_N	33		34	B35_L5_N	E5
9	CAM_CLK_P	40		40	CA_A4_N	55		56	B35_L12_P	E3 (MRCC)
8	CAM_CLK_N	38		38	CA_A4_P	57		58	B35_L12_N	D3 (MRCC)
3	CAM_D0_P	21		21	CA_B1_P	76		75	B35_L7_P	C4
2	CAM_D0_N	23		23	CA_B1_N	78		77	B35_L7_N	B4
6	CAM_D1_P	16		16	CA_A0_N	65		66	B35_L18_P	F1
5	CAM_D1_N	14		14	CA_A0_P	67		68	B35_L18_N	E1
12	CAM_D2_P	22		22	CA_A1_N	61		62	B35_L17_P	H1
11	CAM_D2_N	20		20	CA_A1_P	63		64	B35_L17_N	G1
15	CAM_D3_P	32		32	CA_A3_P	45		46	B35_L13_P	F4
14	CAM_D3_N	34		34	CA_A3_N	47		48	B35_L13_N	F3
			<->				<->			VADJ or 3.3V

Notes:

1) Camera I2C is kept separately from I2C for CRUVI-optional ID EEPROM

2) Pay attention to voltage levels between FPGA (VADJ) and Camera I2C and POWER_EN, which are 3.3V

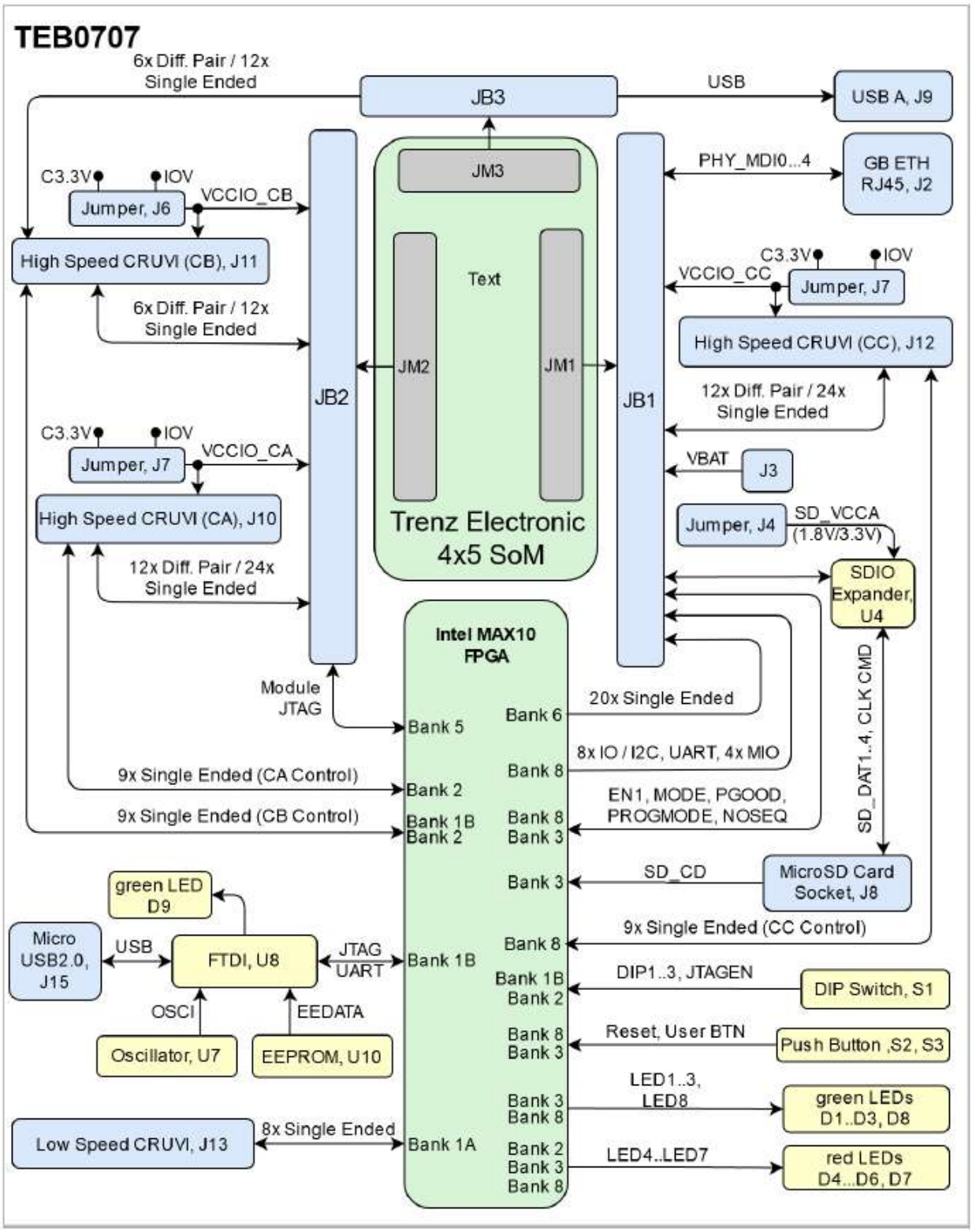
These 2 connectors are hermaphroditic. ODD pin numbers on the SOM are connected to EVEN pin numbers on the Carrier, and vice versa

Conclusion:

The proposed pinout supports two CSI CRUVIs in the system:

1) **Yimin 4-lane** in the TEB0707 **J10** position (FPGA Bank 35)
2) VHDPlus 2-lane in the TEB0707 J12 position (FPGA Bank 15)
3) We recommend eliminating optional CRUVI ID EEPROM

Addendum – **Trenz Carrier Card Block Diagram**



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