SONY

Diagonal 15.86 mm (Type 1) CMOS Image Sensor with Square Pixel for Color Cameras

IMX283EQJ-C

Description

The IMX283EQJ-C is a diagonal 15.86 mm (Type 1) CMOS image sensor with a color square pixel array and approximately 20.30 M effective pixels. 12-bit digital output makes it possible to output the signals of approximately 20.30 M effective pixels with high definition for shooting still pictures.
It also operates with three power supply voltages: analog 2.9 V, digital 1.2 V and 1.8 V, and achieves low power consumption.
Furthermore, it realizes 12-bit digital output for shooting high-speed and high-definition moving pictures by horizontal and vertical addition and subsampling. Realizing high-sensitivity, low dark current, this sensor also has an electronic shutter function with variable storage time.
In addition, this product is designed for use in consumer use digital still camera and consumer use camcorder. When using this for another application, Sony does not guarantee the quality and reliability of the product.
Therefore, don't use this for applications other than consumer use digital still camera and consumer use camcorder.
In addition, individual specification change cannot be supported because this is a standard product.
Consult your Sony Semiconductor Solutions Corporation sales representative if you have any questions.

Features

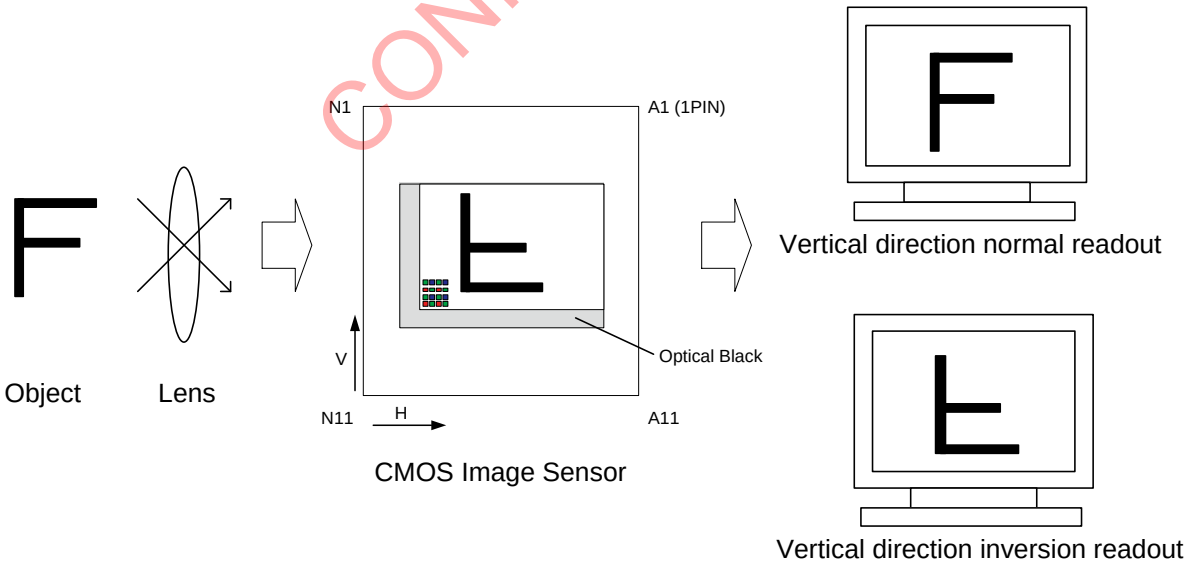
- ◆ CMOS active pixel type pixels
- ◆ Input clock frequency 6 to 27 MHz
- ◆ MIPI Specifications (CSI-2 high-speed serial interface)
- ◆ All-pixel scan mode
  Horizontal/vertical 2/2-line binning mode
  Horizontal/vertical 3/3-line binning mode
  Vertical 2/9 subsampling binning horizontal 3 binning mode
  Vertical 2/19 subsampling binning horizontal 3 binning mode
  Vertical 2 binning horizontal 2/4 subsampling mode
- ◆ High-sensitivity, low dark current, no smear, excellent anti-blooming characteristics
- ◆ Vertical and horizontal arbitrary cropping function
- ◆ Variable-speed shutter function (minimum unit: 1 horizontal period)
- ◆ Low power consumption
- ◆ H driver, V driver and I^2C communication circuit on chip
- ◆ CDS/PGA on chip: Gain +27 dB (step pitch 0.1 dB)
- ◆ 9-bit/10-bit/12-bit A/D conversion on chip
- ◆ R, G, B primary color mosaic filters on chip
- ◆ 118-pin high-precision ceramic package

Device Structure

- ◆CMOS image sensor
- ◆Image size
  Diagonal 15.86 mm (Type 1)
- ◆Total number of pixels
  5592 (H) × 3710 (V) approx. 20.75 M pixels
- ◆Number of effective pixels
  - Type1 approx. 20.30 M pixels use : 5496 (H) × 3694 (V) approx. 20.30 M pixels
  - Type 1/1.4 approx. 8.42 M pixels use : 3872 (H) × 2174 (V) approx. 8.42 M pixels
- ◆Number of active pixels
  - Type1 approx. 20.30 M pixels use : 5496 (H) × 3672 (V) approx. 20.18 M pixels diagonal 15.86 mm
  - Type 1/1.4 approx. 8.42 M pixels use : 3872 (H) × 2168 (V) approx. 8.39 M pixels diagonal 10.65 mm
- ◆Number of recommended recording pixels
  - Type1 approx. 20.30 M pixels use : 5472 (H) × 3648 (V) approx. 19.96 M pixels aspect ratio 3:2
  - Type 1/1.4 approx. 8.42 M pixels use : 3840 (H) × 2160 (V) approx. 8.29 M pixels ratio 16:9
- ◆Chip size
  16.226 mm (H) × 12.654 mm (V) (include scribe area)
- ◆Unit cell size
  2.40 µm (H) × 2.40 µm (V)
- ◆Optical black
  Horizontal (H) direction : Front 48 pixel, rear 0 pixel
  Vertical (V) direction : Front 16 pixels, rear 0 pixel
- ◆Substrate material
  Silicon

Optical Black Array and Readout Scan Direction

(Top View)



Note) Arrows in the figure indicate scanning direction during normal readout in the vertical direction.

Optical Black Array and Readout Scan Direction

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage 1	V_{ADD} *1	–0.3 to +3.3	V
Supply voltage 2	V_{DDD1} *2	–0.5 to +2.0	V
Supply voltage 3	V_{DDD2} *3	–0.5 to +3.3	V
Input voltage (Digital)	V_I	–0.3 to V_{DDD2} + 0.3	V
Output voltage (Digital)	V_O	–0.3 to V_{DDD2} + 0.3	V
Guaranteed operating temperature	T_{OPR}	–10 to +75	˚C
Storage guarantee temperature	T_{STG}	–30 to +80	˚C
Performance guarantee temperature	T_{SPEC}	–10 to +60	˚C

Recommended Operating Conditions

Item	Symbol	Rating	Unit
Supply voltage 1	V_{ADD} *1	2.9 ± 0.1	V
Supply voltage 2	V_{DDD1} *2	1.2 ± 0.1	V
Supply voltage 3	V_{DDD2} *3	1.8 ± 0.1	V
Input voltage (Digital)	V_I	–0.1 to V_{DDD2} + 0.1	V
Output voltage (Digital)	V_O	–0.1 to V_{DDD2} + 0.1	V

*1 V_{ADD}: V_{DD}SUB, V_{DD}HVS, V_{DD}HCM1 to 2, V_{DD}HPX, V_{DD}HDA1 to 2, V_{DD}HCP (2.9 V power supply)
*2 V_{DDD1}: V_{DD}LCN1 to 6, V_{DD}LSC1 to 2, V_{DD}LPA, V_{DD}LPL1 to 3, V_{DD}LIF (1.2 V power supply)
*3 V_{DDD2}: V_{DD}MIO (1.8 V power supply)

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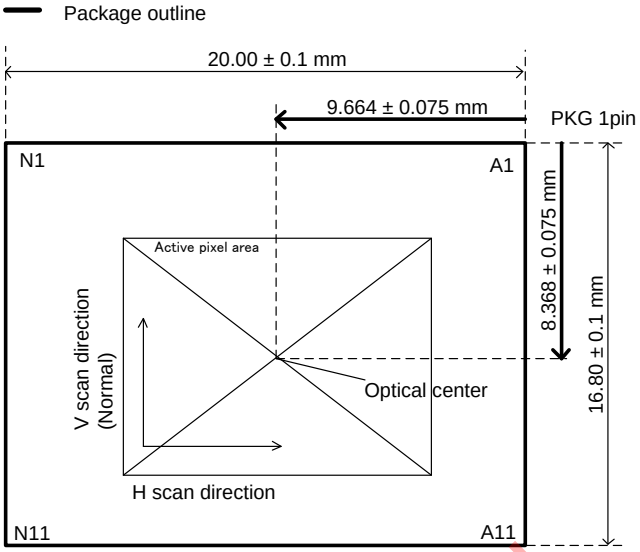
General-0.0.9

Contents

Optical Center

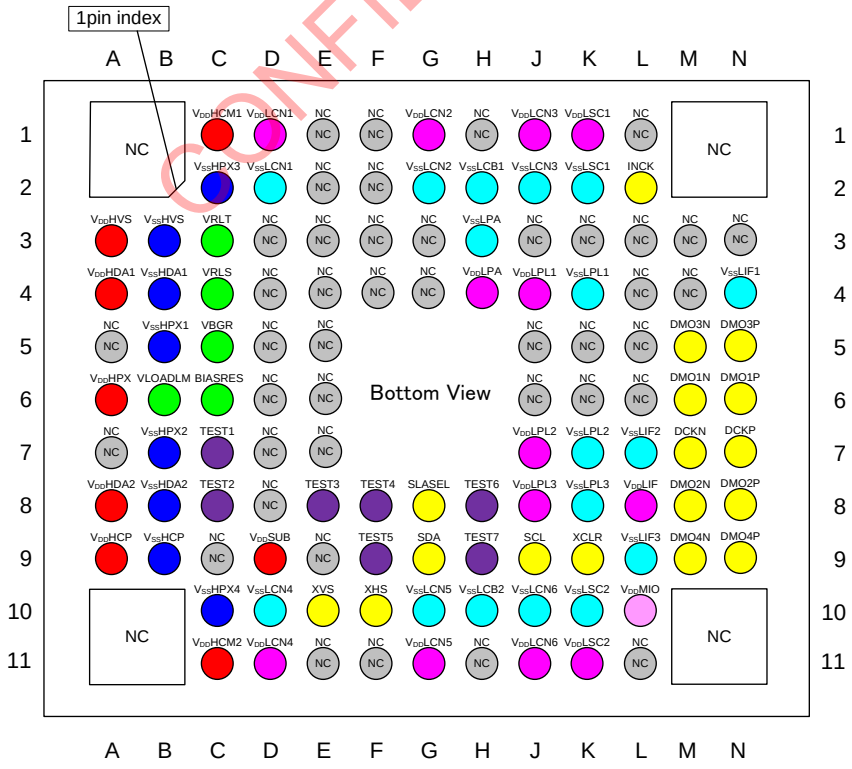
(Top View)



Optical Center

Pin Configuration

(Bottom View)



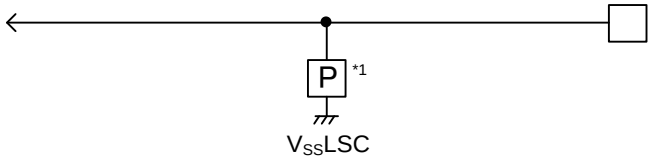
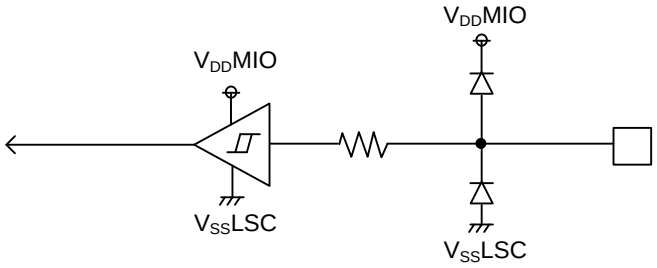
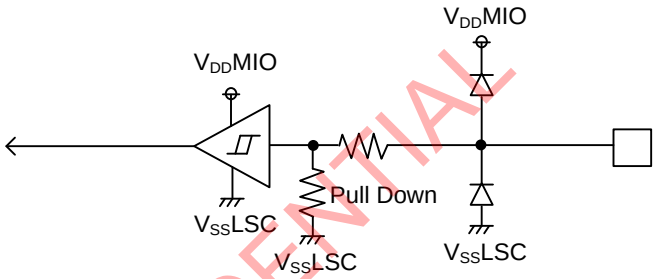
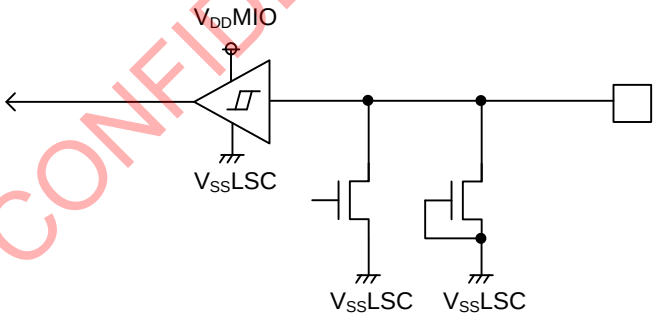
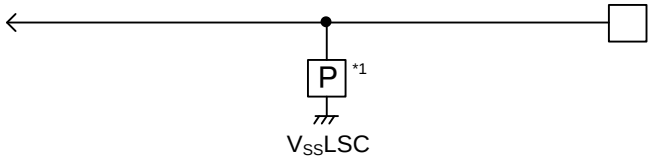
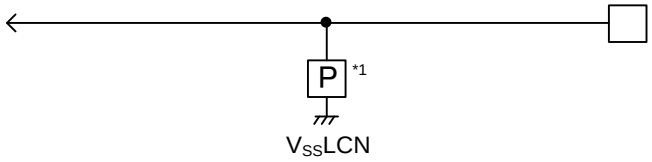
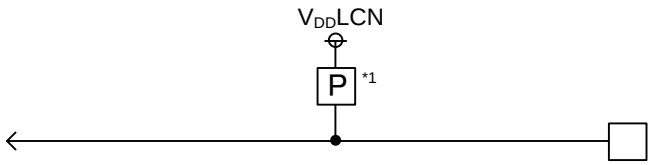
Pin Configuration

Pin Description

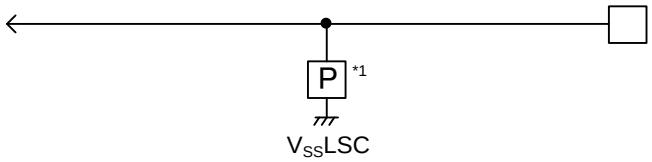
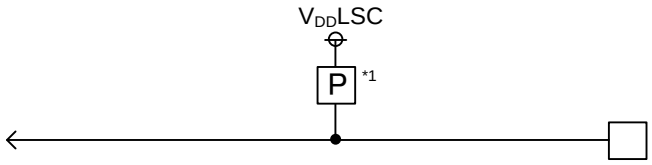
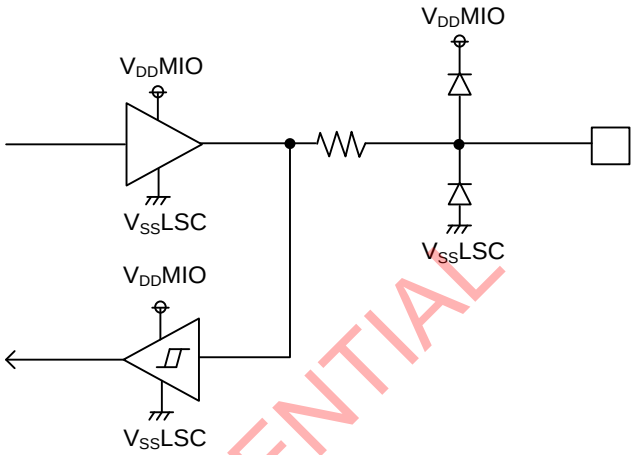
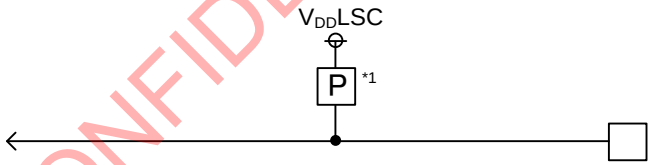
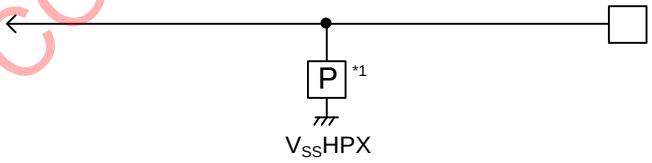
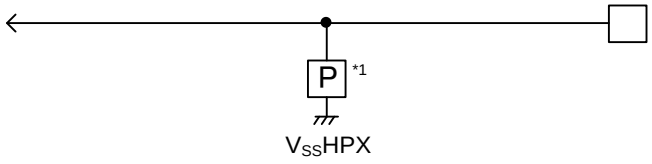
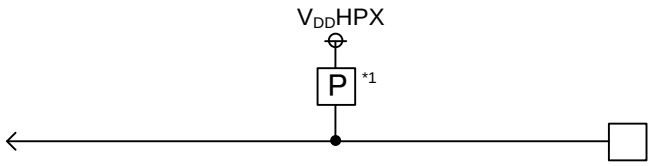
Pin No.	Symbol	I/O	A/D	Pin description	State in Standby mode	Remarks
A3	V_{DD}HVS	Power	A	Analog power supply (2.9 V)	—	
A4	V_{DD}HDA1	Power	A	Analog power supply (2.9 V)	—	
A6	V_{DD}HPX	Power	A	Analog power supply (2.9 V)	—	
A8	V_{DD}HDA2	Power	A	Analog power supply (2.9 V)	—	
A9	V_{DD}HCP	Power	A	Analog power supply (2.9 V)	—	
B3	V_{SS}HVS	GND	A	Analog GND (2.9V)	—	
B4	V_{SS}HDA1	GND	A	Analog GND (2.9V)	—	
B5	V_{SS}HPX1	GND	A	Analog GND (2.9V)	—	
B6	VLOADLM	O	A	Capacitor connection	Pull-down	
B7	V_{SS}HPX2	GND	A	Analog GND (2.9V)	—	
B8	V_{SS}HDA2	GND	A	Analog GND (2.9V)	—	
B9	V_{SS}HCP	GND	A	Analog GND (2.9V)	—	
C1	V_{DD}HCM1	Power	A	Analog power supply (2.9 V)	—	
C2	V_{SS}HPX3	GND	A	Analog GND (2.9V)	—	
C3	VRLT	O	A	Capacitor connection	Pull-down	
C4	VRLS	O	A	Capacitor connection	Pull-down	
C5	VBGR	O	A	Capacitor connection	Hi-Z	
C6	BIASRES	O	A	Test	Hi-Z	Leave open. (No connection)
C7	TEST1	O	A	Test	Hi-Z	Leave open. (No connection)
C8	TEST2	O	A	Test	Hi-Z	Leave open. (No connection)
C10	V_{SS}HPX4	GND	A	Analog GND (2.9V)	—	
C11	V_{DD}HCM2	Power	A	Analog power supply (2.9 V)	—	
D1	V_{DD}LCN1	Power	D	Digital power supply (1.2 V)	—	
D2	V_{SS}LCN1	GND	D	Digital GND (1.2 V)	—	
D9	V_{DD}SUB	Power	A	Analog power supply (2.9 V)	—	
D10	V_{SS}LCN4	GND	D	Digital GND (1.2 V)	—	
D11	V_{DD}LCN4	Power	D	Digital power supply (1.2 V)	—	
E8	TEST3	I	D	Test	—	Leave open. (No connection)
E10	XVS	O	D	Vertical sync signal output	—	
F8	TEST4	I	D	Test	—	Leave open. (No connection)
F9	TEST5	O	D	Test	Low Level	Leave open. (No connection)
F10	XHS	O	D	Horizontal sync signal output	—	
G1	V_{DD}LCN2	Power	D	Digital power supply (1.2 V)	—	
G2	V_{SS}LCN2	GND	D	Digital GND (1.2 V)	—	
G8	SLASEL	I	D	Slave address control	Pull-down	
G9	SDA	I/O	D	I^2C communication data input/output	—	
G10	V_{SS}LCN5	GND	D	Digital GND (1.2 V)	—	
G11	V_{DD}LCN5	Power	D	Digital power supply (1.2 V)	—	
H2	V_{SS}LCB1	GND	D	Digital GND (1.2 V)	—	
H3	V_{SS}LPA	GND	D	Digital GND (1.2 V)	—	
H4	V_{DD}LPA	Power	D	Digital power supply (1.2 V)	—	
H8	TEST6	O	D	Test	Low Level	Leave open. (No connection)
H9	TEST7	I	D	Connect to 1.8 V power supply	—	
H10	V_{SS}LCB2	GND	D	Digital GND (1.2 V)	—	

Pin No.	Symbol	I/O	A/D	Pin description	State in Standby mode	Remarks
J1	V_{DD}LCN3	Power	D	Digital power supply (1.2 V)	—	
J2	V_{SS}LCN3	GND	D	Digital GND (1.2 V)	—	
J4	V_{DD}LPL1	Power	D	Digital power supply (1.2 V)	—	
J7	V_{DD}LPL2	Power	D	Digital power supply (1.2 V)	—	
J8	V_{DD}LPL3	Power	D	Digital power supply (1.2 V)	—	
J9	SCL	I	D	I^2C communication clock input	—	
J10	V_{SS}LCN6	GND	D	Digital GND (1.2 V)	—	
J11	V_{DD}LCN6	Power	D	Digital power supply (1.2 V)	—	
K1	V_{DD}LSC1	Power	D	Digital power supply (1.2 V)	—	
K2	V_{SS}LSC1	GND	D	Digital GND (1.2 V)	—	
K4	V_{SS}LPL1	GND	D	Digital GND (1.2 V)	—	
K7	V_{SS}LPL2	GND	D	Digital GND (1.2 V)	—	
K8	V_{SS}LPL3	GND	D	Digital GND (1.2 V)	—	
K9	XCLR	I	D	Reset pulse input	—	
K10	V_{SS}LSC2	GND	D	Digital GND (1.2 V)	—	
K11	V_{DD}LSC2	Power	D	Digital power supply (1.2 V)	—	
L2	INCK	I	D	Input clock	—	
L7	V_{SS}LIF2	GND	D	Digital GND (1.2 V)	—	
L8	V_{DD}LIF	Power	D	Digital power supply (1.2 V)	—	
L9	V_{SS}LIF3	GND	D	Digital GND (1.2 V)	—	
L10	V_{DD}MIO	Power	D	Digital power supply (1.8 V)	—	
M5	DMO3N	O	D	Digital MIPI output	Low Level	Data Lane 3 connection
M6	DMO1N	O	D	Digital MIPI output	Low Level	Data Lane 1 connection
M7	DCKN	O	D	Digital MIPI output	Low Level	Clock Lane connection.
M8	DMO2N	O	D	Digital MIPI output	Low Level	Data Lane 2 connection
M9	DMO4N	O	D	Digital MIPI output	Low Level	Data Lane 4 connection
N4	V_{SS}LIF1	GND	D	Digital GND (1.2 V)	—	
N5	DMO3P	O	D	Digital MIPI output	Low Level	Data Lane 3 connection
N6	DMO1P	O	D	Digital MIPI output	Low Level	Data Lane 1 connection
N7	DCKP	O	D	Digital MIPI output	Low Level	Clock Lane connection.
N8	DMO2P	O	D	Digital MIPI output	Low Level	Data Lane 2 connection
N9	DMO4P	O	D	Digital MIPI output	Low Level	Data Lane 4 connection

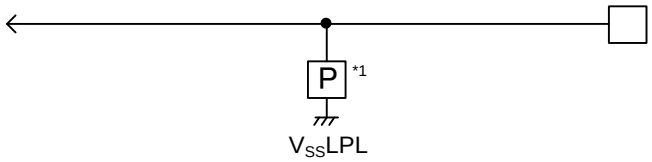
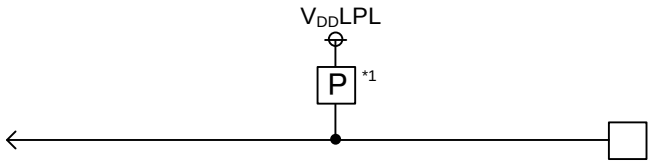
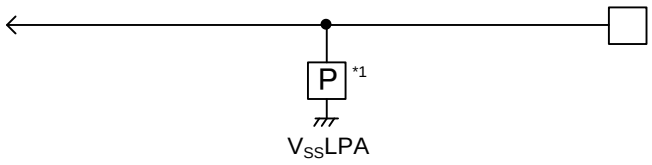
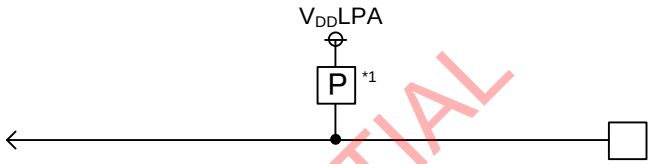
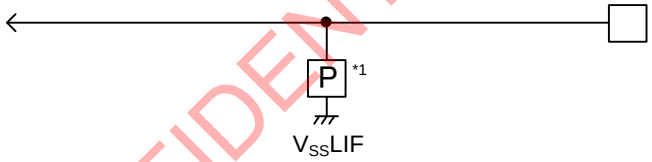
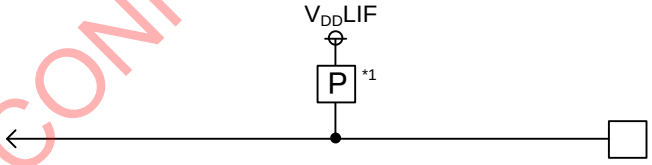
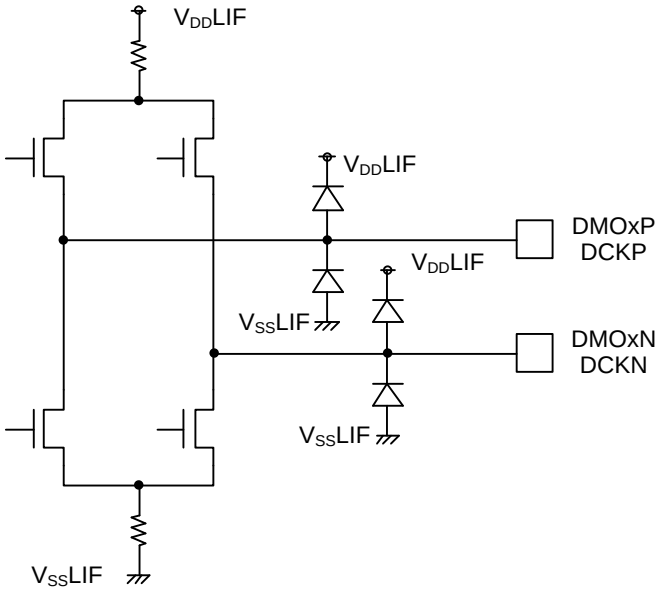
I/O Equivalent Circuit Diagram

Symbol	Equivalent circuit
V_{DD}SUB	
XCLR INCK	
SLASEL	
SDA SCL	
V_{DD}MIO	
V_{DD}LCN1 to 6	
V_{SS}LCN1 to 6	

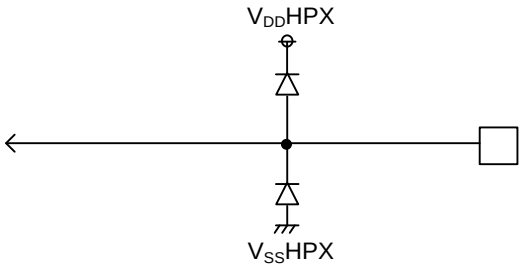
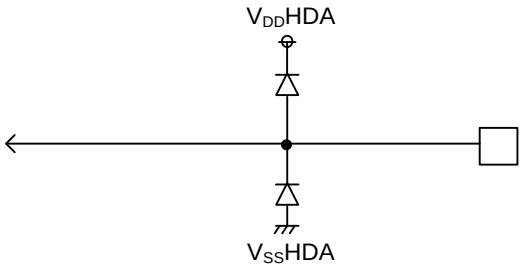
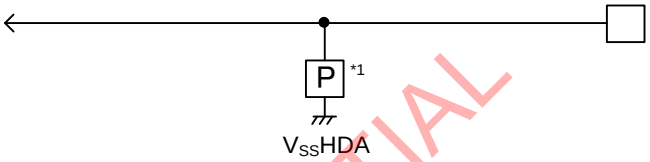
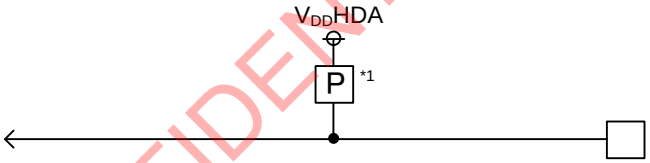
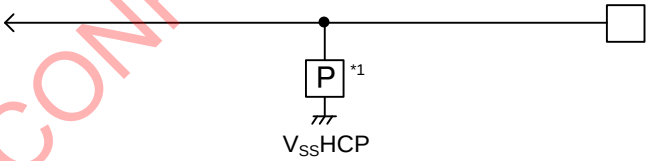
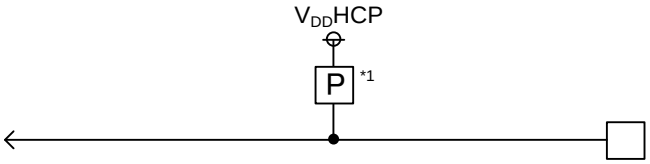
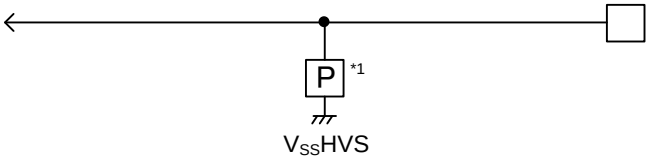
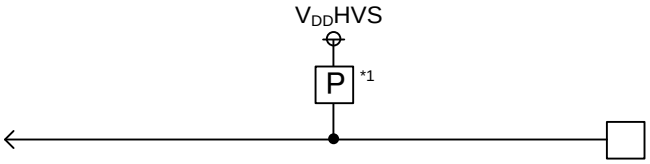
☐ External pins

Symbol	Equivalent circuit
V_{DD}LSC1 to 2	
V_{SS}LSC1 to 2	
XHS XVS	
V_{SS}LCB1 to 2	
V_{DD}HCM1 to 2	
V_{DD}HPX	
V_{SS}HPX1 to 4	

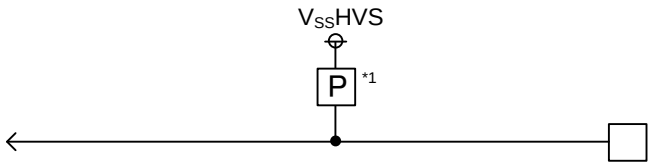
☐ External pins

Symbol	Equivalent circuit
V_{DD}LPL1 to 3	
V_{SS}LPL1 to 3	
V_{DD}LPA	
V_{SS}LPA	
V_{DD}LIF	
V_{SS}LIF1 to 3	
DMOxP (x = 1to 4) DMOxN (x = 1 to 4) DCKP DCKN	

□ External pins

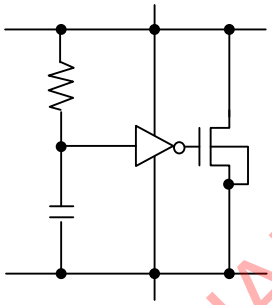
Symbol	Equivalent circuit
VLOADLM	
VBGR	
V_{DD}HDA1 to 2	
V_{SS}HDA1 to 2	
V_{DD}HCP	
V_{SS}HCP	
V_{DD}HVS	
V_{SS}HVS	

□ External pins

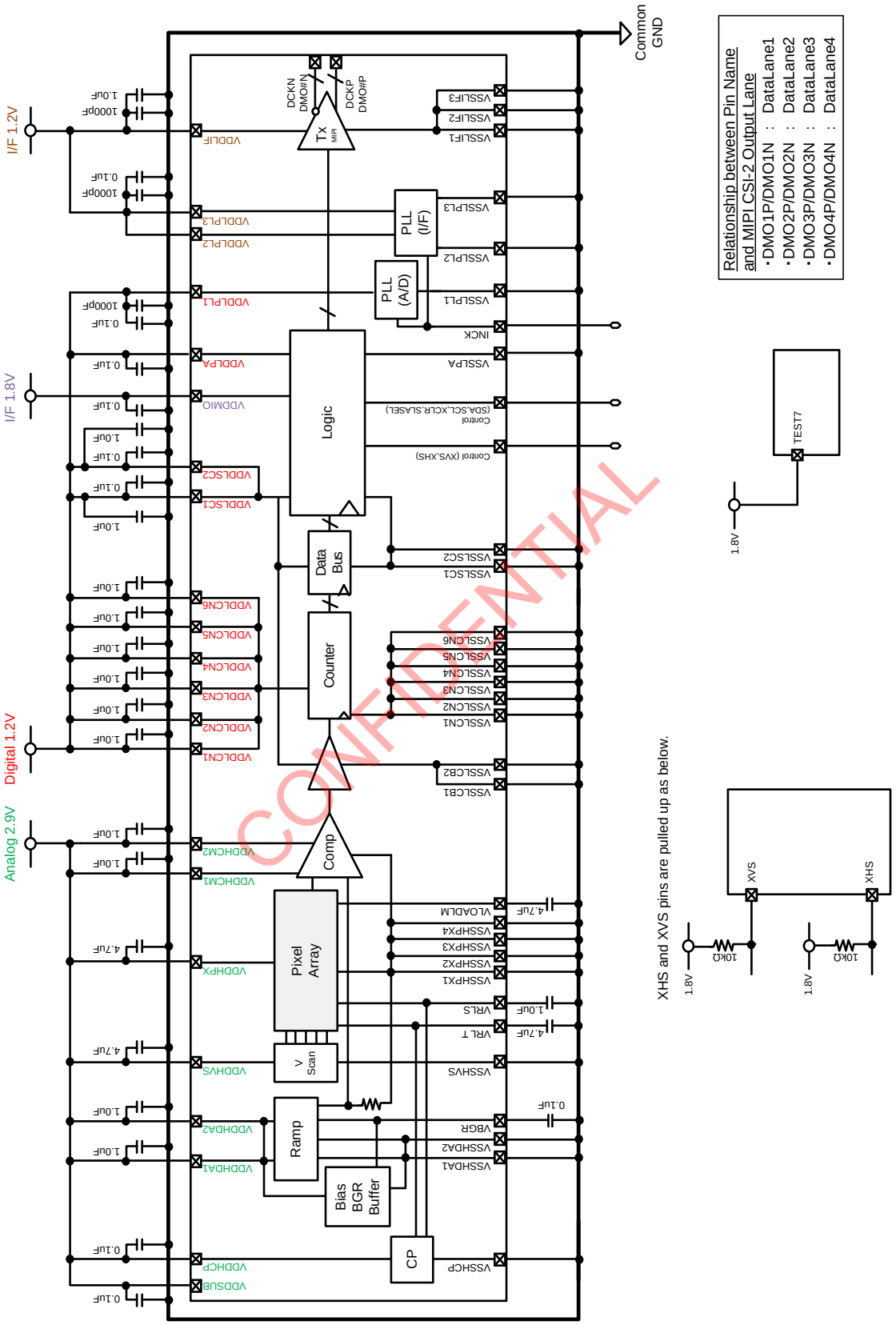
Symbol	Equivalent circuit
VRLT VRLS	

□ External pins

Description of Special Symbol

Symbol	Equivalent circuit
	

Peripheral Circuit



Peripheral Circuit

Electrical Characteristics

1. DC Characteristics

Current Consumption and Gain Variable Range

(V_{ADD} = 3.0 V, V_{DDD1} = 1.3 V, V_{DDD2} = 1.9 V, Tj = 60 ˚C, Reference Gain (0 dB)
All pixel scan mode (MODE0), 21.98 frame/s)

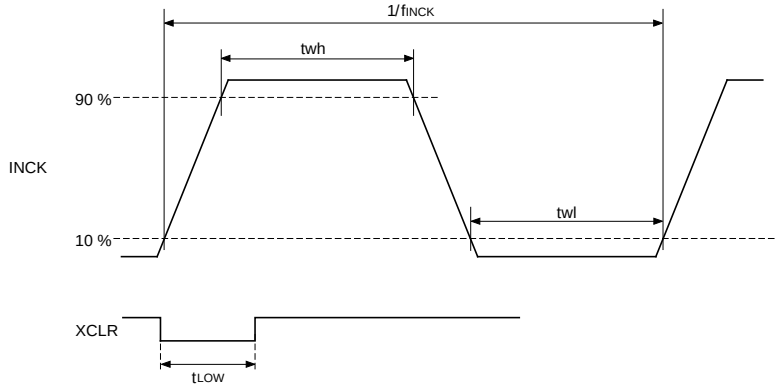
Item	Symbol	Min.	Typ.	Max	Unit	Remarks
Current consumption (Analog)	I_{ADD}	—	—	150	mA	
Current consumption (Digital1)	I_{DDD1}	—	—	260	mA	
Current consumption (Digital2)	I_{DDD2}	—	—	0.1	mA	
Standby current (Analog)	I_{ADDSTB}	—	—	70	μA	In the dark
Standby current (Digital1)	$I_{DDD1STB}$	—	—	11.5	mA	In the dark
Standby current (Digital2)	$I_{DDD2STB}$	—	—	15	μA	In the dark
PGA gain variable range	PGAG	0	—	27	dB	

Supply Voltage and I/O Voltage

Item		Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Analog	V_{DD}SUB, V_{DD}HCM1 to 2, V_{DD}HVS, V_{DD}HPX, V_{DD}HDA1 to 2, V_{DD}HCP	V_{ADD}	2.80	2.90	3.00	V
	Digital1	V_{DD}LCN1 to 6, V_{DD}LSC1 to 2, V_{DD}LPL1 to 3, V_{DD}LPA, V_{DD}LIF	V_{DDD1}	1.10	1.20	1.30	V
	Digital2	V_{DD}MIO	V_{DDD2}	1.70	1.80	1.90	V
Digital input voltage		SDA, SDL	V_{IH1}	0.7 × V_{DDD2}	—	V_{DDD2} + 0.1	V
			V_{IL1}	–0.1	—	0.3 × V_{DDD2}	V
		XCLR, INCK, SLASEL	V_{IH2}	0.7 × V_{DDD2}	—	V_{DDD2} + 0.1	V
			V_{IL3}	–0.1	—	0.3 × V_{DDD2}	V
Digital output voltage		XHS, XVS	V_{HVOUT}	—	V_{DDD2}		V

2. AC Characteristics

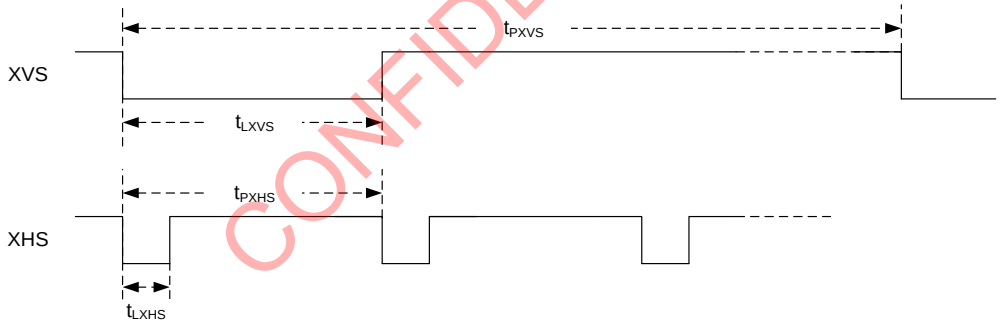
INCK, XCLR



INCK, XCLR

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	6	—	27	MHz	
INCK Low level pulse width	twl	5	—	—	ns	
INCK High level pulse width	twh	5	—	—	ns	
Clock duty	—	40	50	60	%	
XCLR Low level pulse width	t_{LOW}	100	—	—	ns	

XHS, XVS (Output)

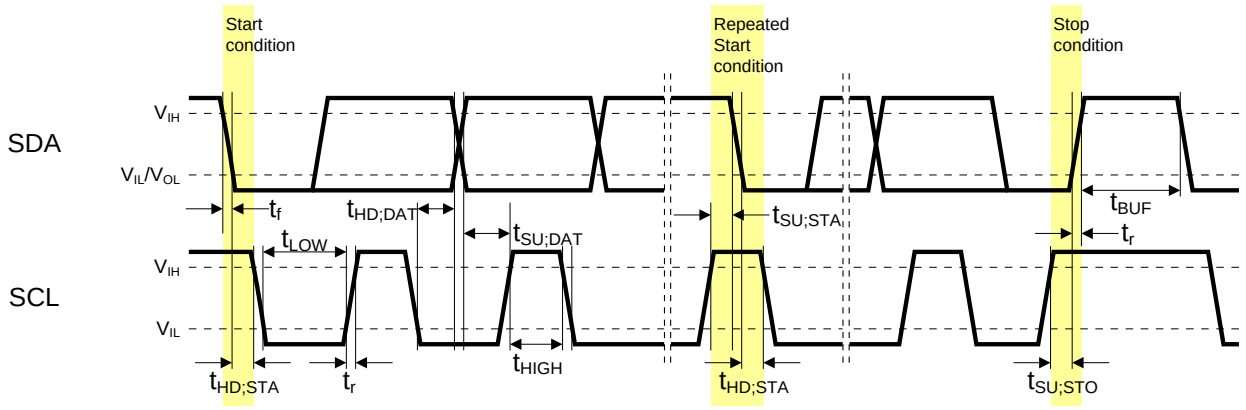


XHS, XVS Output

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XHS Low level pulse width	t_{LXHS}		222		ns	16 clk@72MHz
XHS pulse period	t_{PXHS}		HMAX[*1]		clk@72MHz	
XVS Low level pulse width	t_{LXVS}		t_{PXHS}		clk@72MHz	
XVS pulse period	t_{PXVS}		HMAX[*1] × VMAX[*2]		clk@72MHz	

[*1] The value set as HMAX (address 3036h, bit [7:0] and address 3037h, bit [7:0])
[*2] The value set as VMAX (address 3038h, bit [7:0], address 3039h, bit [7:0] and address 303Ah, bit [3:0]).

I²C Communication



I²C Communication

I²C Specification

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Low level input voltage	V_{IL}	−0.1	—	0.3 × V_{DDD2}	V	
High level input voltage	V_{IH}	0.7 × V_{DDD2}	—	V_{DDD2} + 0.1	V	
Low level output voltage	V_{OL}	0	—	0.2 × V_{DDD2}	V	V_{DDD2} < 2 V, Sink 3 mA
Output fall time	tof	—	—	250	ns	Load 10 pF to 400 pF, 0.7 × V_{DDD2} to 0.3 × V_{DDD2}
Input current (SCL, SDA, XCLR, INCK)	Ii	-10	—	10	µA	0.1 × V_{DDD2} to 0.9 × V_{DDD2}
Input capacitance of SCL / SDA	Ci	—	—	10	pF	

I²C AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	0	—	400	kHz
Hold time (Start Condition)	$t_{HD;STA}$	0.6	—	—	µs
Low period of the SCL clock	t_{LOW}	1.3	—	—	µs
High period of the SCL clock	t_{HIGH}	0.6	—	—	µs
Set-up time (Repeated Start Condition)	$t_{SU;STA}$	0.6	—	—	µs
Data hold time	$t_{HD;DAT}$	0	—	0.9	µs
Data set-up time	$t_{SU;DAT}$	100	—	—	ns
Rise time of both SDA and SCL signals	t_r	—	—	300	ns
Fall time of both SDA and SCL signals	t_f	—	—	300	ns
Set-up time (Stop Condition)	$t_{SU;STO}$	0.6	—	—	µs
Bus free time between a STOP and START Condition	t_{BUF}	1.3	—	—	µs

DCKP / DCKN, DMO

Detailed explanation of CSI-2 interface is in following two documents, "MIPI Alliance Standard for Camera Serial Interface2(CSI-2) Version 1.1" and "MIPI Alliance Specification for D-PHY Version 1.1".
Four data output Lanes are applied from MIPI Alliance Standard for Camera Serial Interface2(CSI-2) Version 1.1.

Spectral Sensitivity Characteristics

(Excludes lens characteristics and light source characteristics)

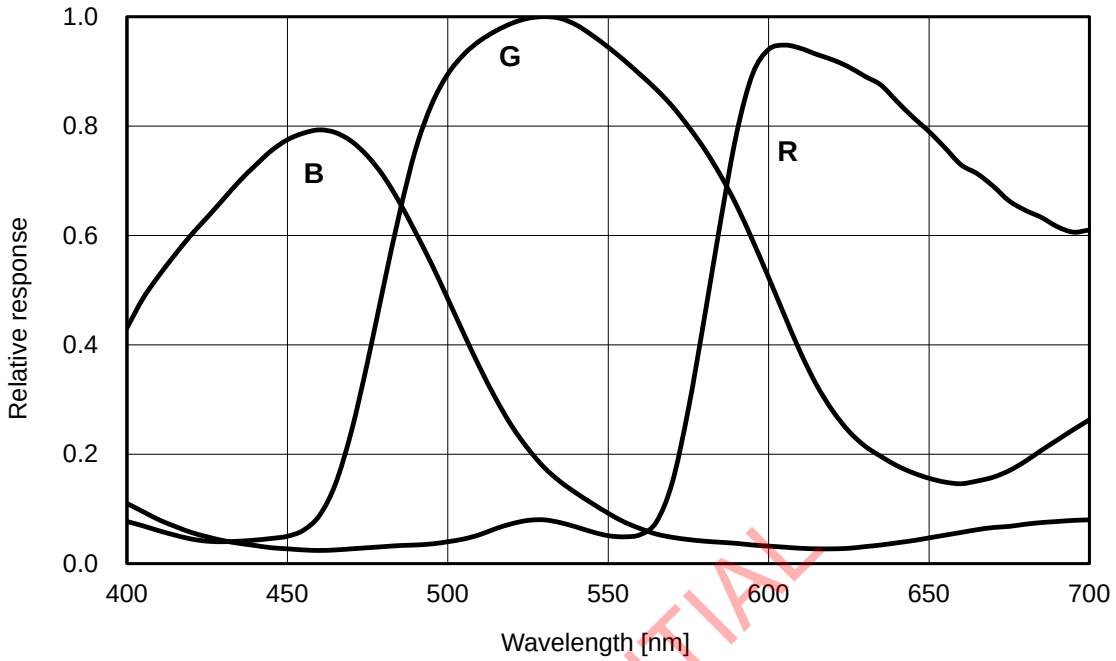


Image Sensor Characteristics

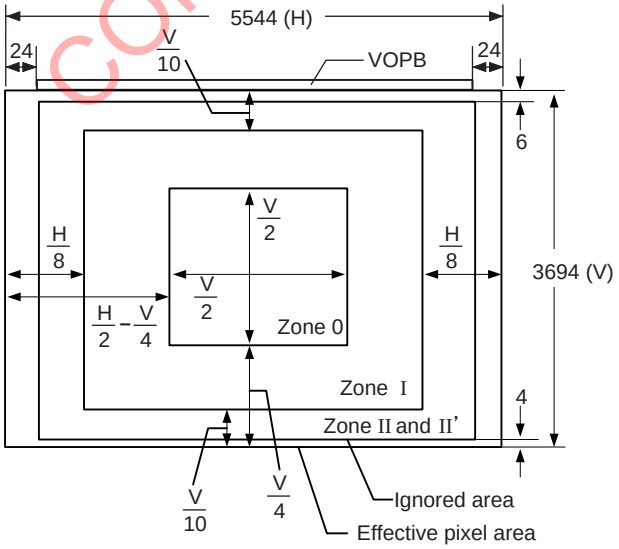
(V_{ADD} = 2.9 V, V_{DDD1} = 1.2 V, V_{DDD2} = 1.8 V, Tj = 60 ˚C, 19.98 frame/s, Reference Gain (0 dB))

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity		Sg	1501	1874	2247	digit*1	1	1/30 s integration conversion value Zone 0
Sensitivity ratio	R	Rr	36	—	62	%	1	Zone 0
	B	Rb	35	—	55	%	1	
Saturation signal		Vsat	3824	—	—	digit*1	2	Zone 0 to II’
Video signal shading		SHg	—	—	37	%	3	Zone 0 and I (the figure below)
			—	—	54			Zone 0 to II’ (the figure below)
Dark signal		Vdt	0	—	0.85	digit*1	4	1/30 s integration conversion value Zone 0 to II’
Dark signal shading		ΔVdt	0	—	1.2	digit*1	5	1/30 s integration conversion value Zone 0 to II’
Dark signal difference		VdOB	-0.41	—	0.41	digit*1	6	1/30 s integration conversion value Zone 0 to II’
Line crawl R		Lcr	-3.8	—	3.8	%	7	Zone 0 to II’
Line crawl B		Lcb	-3.8	—	3.8	%		

*1 Shows digit when 12-bit output. 1 digit ≈ 0.2465 mV when 12-bit output (1 digit ≈ 0.9858 mV when 10-bit output).

1. Zone Definition of Image Sensor Characteristics

Zone definition of image sensor characteristics and reference position during dark signal measurement are shown below.



Zone Definition of Image Sensor Characteristics and Reference Position during Dark Signal Measurement

Image Sensor Characteristics Measurement Method

1. Measurement Conditions

(1) In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
(2) In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the Gr/Gb channel signal output or the R/B channel signal output of the measurement system.

2. Color Coding of this Image Sensor and Readout

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb represent the G signal on the same line as the R and B signals, respectively. The Gb signal and B signal lines and the R signal and Gr signal lines are output successively.

Gb	B	Gb	B
R	Gr	R	Gr
Gb	B	Gb	B
R	Gr	R	Gr

Color Coding Diagram

3. Definition of Standard Imaging Conditions

◆ Standard imaging condition I:
Use a pattern box (luminance: 706 cd/m^2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

◆ Standard imaging condition III:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens (exit pupil distance –31.5 mm) with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. G sensitivity, Sensitivity ratio
Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/80.03 s, measure the Gr, Gb, R and B signal outputs (VGr, VGb, VR and VB) at the center of the screen which is zone 0, and substitute the values into the following formula

VG = (VGr + VGb) / 2
Sg = VG × 80.03/30 [digit]
Rr = VR/VG × 100 [%]
Rb = VB/VG × 100 [%]

2. Saturation signal
Set the measurement condition to the standard imaging condition II. Adjust the luminous intensity to 20 times the intensity with the average value of the G (= (Gr + Gb)/2) signal output, 469 digit when 10-bit output (1874 digit when 12-bit output). Measure the minimum values of the Gr, Gb, R and B signals when shooting in rolling shutter mode.

3. Video signal shading
   Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the G signal output is 469 digit when 10-bit output (1874 digit when 12-bit output). Then measure the maximum value (Gmax [digit]) and the minimum value (Gmin [digit]) of the G signal output, and substitute the values into the following formula.

   - When 10-bit output
     SHg = (Gmax – Gmin)/469 × 100 [%]
   - When 12-bit output
     SHg = (Gmax – Gmin)/1874 × 100 [%]

4. Dark signal
   Measure the average value (Vdt [digit]) of the signal output in zone 0 to zone II' in the light-obstructed state. Define the average value of the signal output accumulated in 1 frame period (t1v) as Vdt1V and the average value of the signal output accumulated in the shortest period (1H period: t1h) as Vdt1H, and then substitute the values into the following formula.

   Vdt = (Vdt1V – Vdt1H)/(t1v – t1h)/30 [digit]

5. Dark signal shading
   Following the item 4, measure the maximum value (Vdmax [digit]) and minimum value (Vdmin [digit]) of the dark signal output, and substitute the values into the following formula.

   ΔVdt = Vdmax – Vdmin [digit]

6. Dark signal difference
   Following the item 5, measure the average value of the dark signal output (VdOB [digit]) in zone 0 to zone II' using the optical black (vertical direction VOPB area) level as a reference.

7. Line crawl
   Set the measurement condition to the standard imaging condition III. After adjusting the average value of the G (= (Gr + Gb)/2) signal output when inserting G filter to 469 digit when 10-bit output (1874 digit when 12-bit output), measure the average values of the Gr and Gb signal output (GGr, GGb).
   After adjusting the average value of the R signal output when inserting R filter to 469 digit when 10-bit output (1874 digit when 12-bit output), measure the average values of the Gr and Gb signal output (RGr, RGb).
   Substitute the values into the following formula.

   Lcr = {RGr – (GGr/GGb) × RGb}/[{RGr + (GGr/GGb) × RGb}/2] × 100 [%]

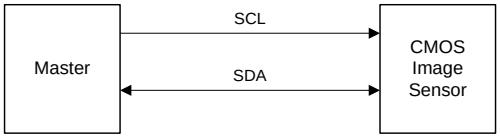
   Then, after adjusting the average value of the B signal output when inserting B filter to 469 digit when 10-bit output (1874 digit when 12-bit output), measure the average values of the Gr and Gb signal output (BGr, BGb).
   Substitute the values into the following formula.

   Lcb = {BGb – (GGb/GGr) × BGr}/[{BGb + (GGb/GGr) × BGr}/2] × 100 [%]

Setting Registers Using I²C Communication

Description of Setting Registers When Using I²C Communication

The serial data input order is MSB-first transfer. The table below shows the various data types and descriptions.



Pin connection of serial communication

The slave address is selectable by pin connection of SLASEL.

SLAVE Address

SLASEL (Pin No. G8)	Slave address							
	MSB							LSB
Low or NC	0	0	1	1	0	1	0	R / W[*1]
High	0	0	1	0	0	0	0	R / W[*1]

[*1] R/W is data direction bit

R / W

R / W bit	Data direction
0	Write (Master → Sensor)
1	Read (Sensor → Master)

Pin Connection of Serial Communication Operation Specifications When Using I²C Communication

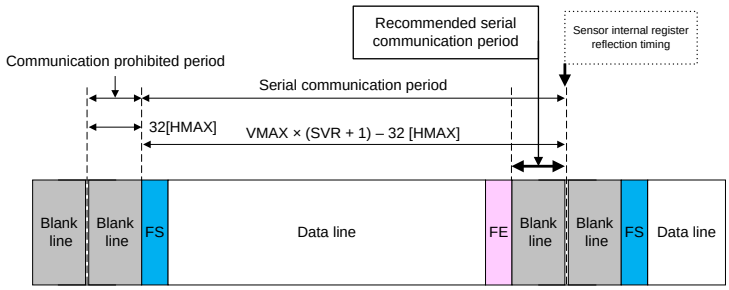
The pin connection of serial communication method conforms to the Camera Control Instance (CCI). CCI is an I²C fast-mode compatible interface, and the data transfer protocol is I²C standard.
This pin connection of serial communication circuit can be used to access the control-registers and status-registers of the sensor.

I²C pin description

Symbol	Pin No.	Remarks
SCL	J9	Serial clock input
SDA	G9	Serial data communication

Register Communication Timing When Using I²C Communication

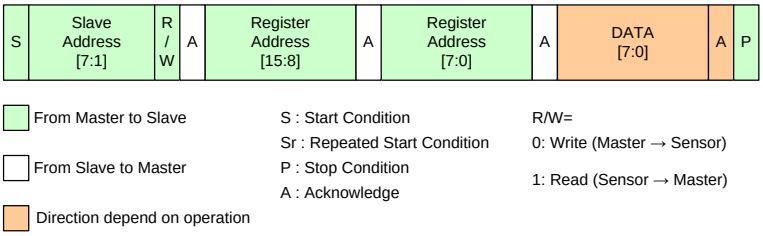
In I²C communication system, register setting can be performed during the period when communication is from the following figure “VMAX × (SVR + 1) − 32[HMAX]”.
Perform I²C communication within “FS of next frame − 32[HMAX]” period (recommended serial communication period) after FE period end to prevent noise. However, for non-picture frames in which noise is ignored (immediately after power-on or immediately after switching the drive mode, etc.), then register communication can be performed other than during the recommended serial communication period of those frames.



Register Communication Timing When Using I²C Communication

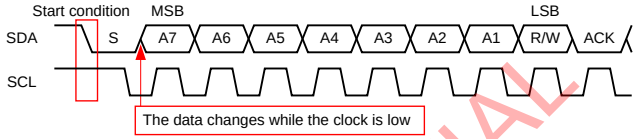
I²C Communication Protocol

I²C serial communication supports a 16-bit register address and 8-bit data message type.

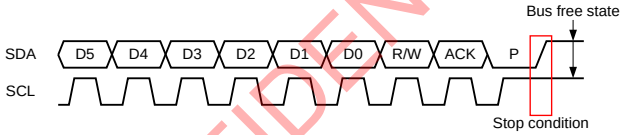


I²C Communication Protocol

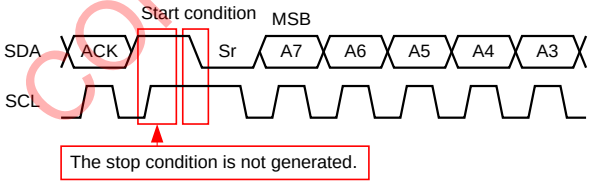
Data is transferred serially, MSB first in 8-bit units. After each data byte is transferred, A (Acknowledge) is transferred. Data is transferred at the clock cycle of SCL. SDA can change only while SCL is Low, so the SDA value must be held while SCL is High. The Start condition is defined by SDA changing from High to Low while SCL is High. When the Stop condition is not generated in the previous communication phase and Start condition for the next communication is generated, that Start condition is recognized as a Repeated Start condition.



Start Condition

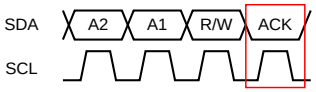


Stop Condition



Repeated Start Condition

After transfer of each data byte, the Master or the sensor transmits an Acknowledge and release (does not drive) SDA.



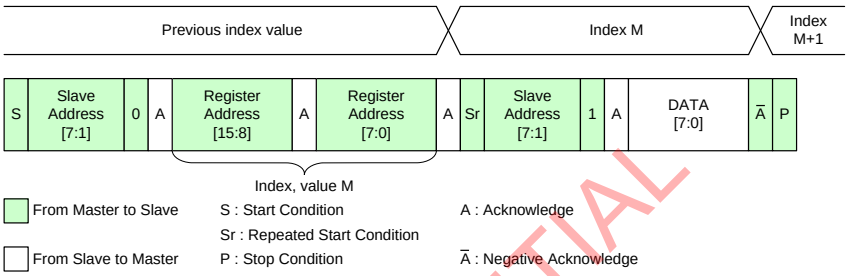
Acknowledge

Register Write and Read

This sensor supports to four read operations and two write operations.
In addition, INCK signal must be driven during the I^2C serial communication period.

Single Read from Random Location

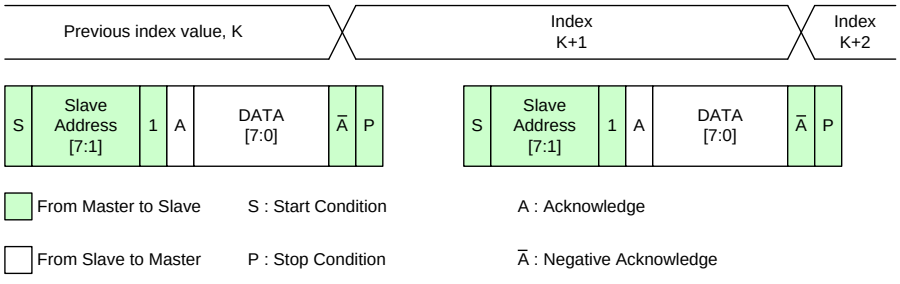
The sensor has an index function that indicates which address it is focusing on. In reading the data at an optional single address, the Master must set the index value to the address to be read. For this purpose it performs dummy write operation up to the register address. The upper level of the figure below shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the start condition. The Start Condition is generated without generating the Stop Condition, so it becomes the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the index address data on SDA. After the Master receives the data,it generates a Negative Acknowledge and the Stop Condition to end the communication



Single Read from Random Location

Single Read from Current Location

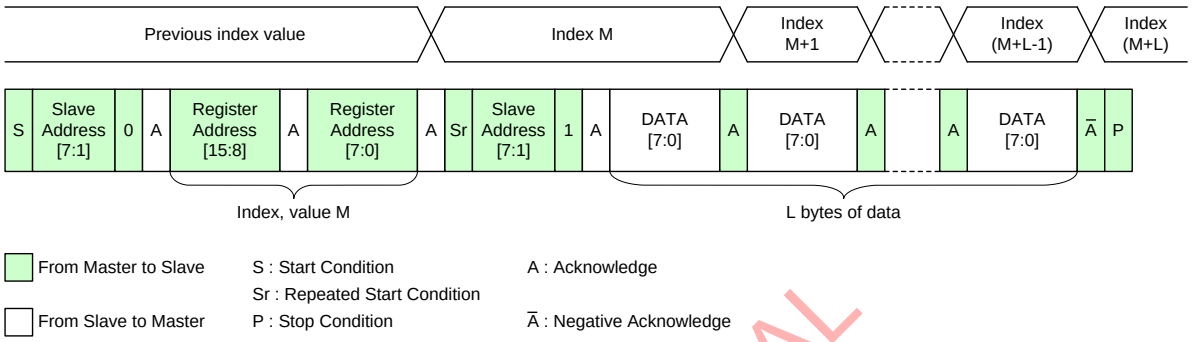
After the slave address is transmitted by a write request, that address is designated by the next communication and the index holds that value. In addition, when data read/write is performed, the index is incremented by the subsequent Acknowledge/Negative Acknowledge timing. When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after Acknowledge. After receiving the data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication, but the index value is incremented, so the data at the next address can be read by sending the slave address with a read request.



Single Read from Current Location

Sequential Read Starting from Random Location

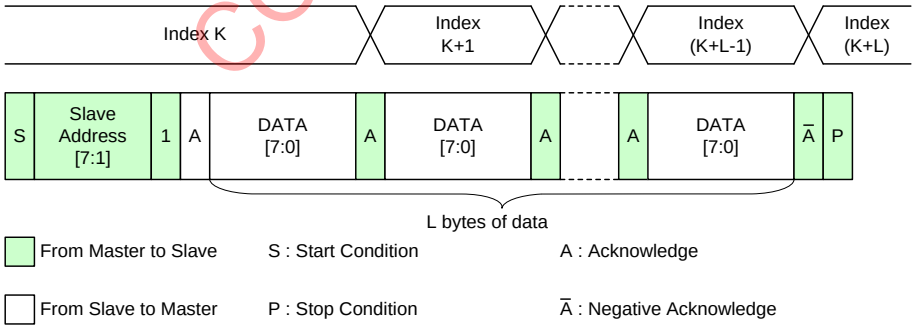
In reading data sequentially, which is starting from an optional address, the Master must set the index value to the start of the addresses to be read. For this purpose, dummy write operation includes the register address setting. The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Random Location

Sequential Read Starting from Current Location

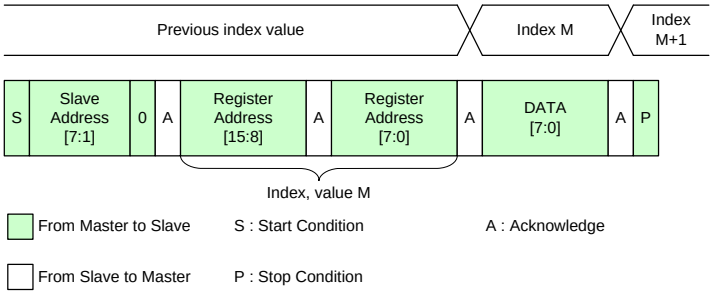
When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after the Acknowledge. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Current Location

Single Write to Random Location

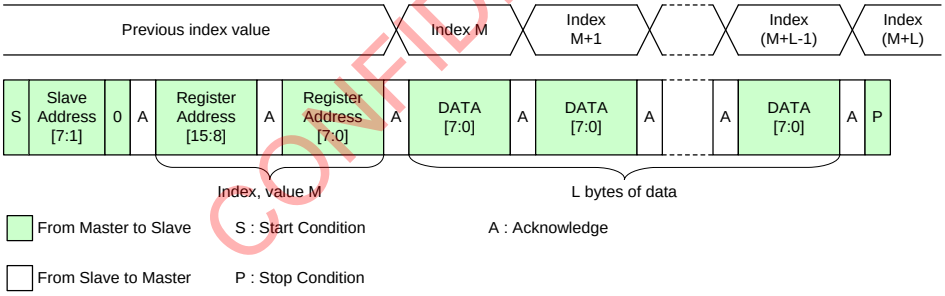
The Master sets the sensor index value to M by designating the sensor slave address with a write request, and designating the address (M). After that the Master can write the value in the designated register by transmitting the data to be written. After writing the necessary data, the Master generates the Stop Condition to end the communication.



Single Write to Random Location

Sequential Write Starting from Random Location

The Master can write a value to register address M by designating the sensor slave address with a write request, designating the address (M), and then transmitting the data to be written. After the sensor receives the write data, it outputs an Acknowledge and at the same time increments the register address, so the Master can write to the next address simply by continuing to transmit data. After the Master writes the necessary number of bytes, it generates the Stop Condition to end the communication.



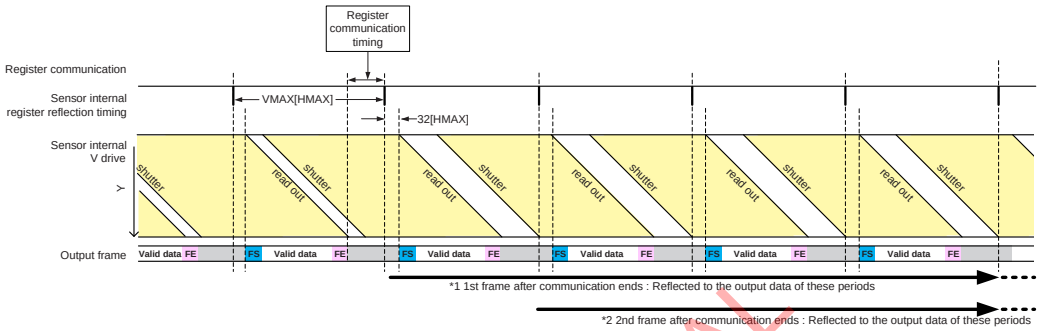
Sequential Write Starting from Random Location

Register Value Reflection Timing to Output Data

The register values established by register communication are reflected to the output data at the following timings.

Reflection timing	Explanation
*1 1st frame after communication ends	The communication contents are reflected to the output data from 1st frame after communication ends.
*2 2nd frame after communication ends	The communication contents are reflected to the output data from 2nd frame after communication ends.
Immediately	The communication contents are reflected immediately.

For which reflection timing of each register, see “Register Map” on pages 30 to 31.



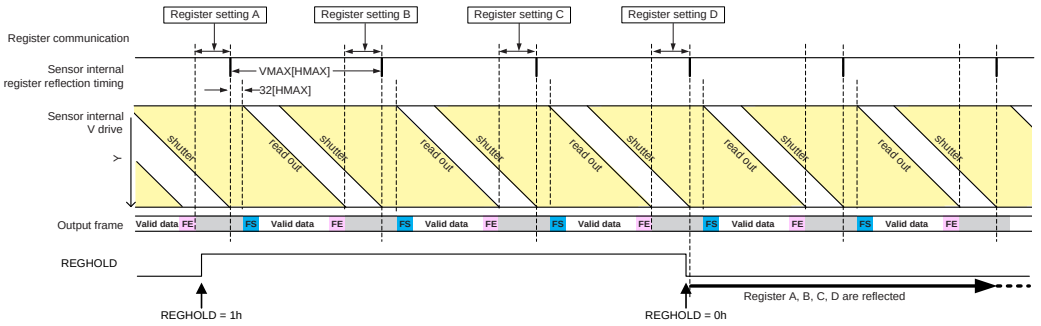
Register Value Reflection Timing to Output Data

Register Hold Setting

Register setting can be transmitted with divided to several frames and it can be reflected globally at a certain frame by the register REGHOLD for the registers of which reflection timing is frame unit (*1 and *2).
Registers are set when REGHOLD = 1h, and REGHOLD is set to “0h” during communication period just before the frame the registers are reflected from.
Register hold function is invalid for the registers of which reflection timing is immediately. Therefore these registers are reflected immediately when even though REGHOLD = 1h.

REGHOLD Setting

Name	Address	Bit	Register value	Function
REGHOLD	303Fh	[0]	0h	Normal communication Reflecting register setting when register settings are held
			1h	Register setting hold



Example of REGHOLD operation

Register Map

Address	Bit assign-ment	Default value	Reflection timing	Register name	Function	Remarks
3000h	[0]	1h	Immediately	STANDBY	0h: Normal operation 1h: Overall standby	Setting range: 0h to 1h
	[1]	1h	Immediately	STBLOGIC	0h: Normal operation 1h: Digital circuit standby other than serial communication block	Setting range: 0h to 1h
	[2]	0h	Immediately	STBMIPI	0h: Normal operation 1h: CSI-2 standby	Setting range: 0h to 1h
	[3]	1h	Immediately	STBDV	0h: Normal operation 1h: Frequency demultiplier standby	Setting range: 0h to 1h
	[4]	0h	Immediately	SLEEP	Low power consumption drive in exposure time	Setting range: 0h to 1h
	[7:5]	0h			—	Set the default value.
3001h	[3:0]	0h			—	Set the default value.
	[4]	0h	*1	CLPSQRST	When changing form 0h to 1h: Resets the internal clamp circuit operation mode	Setting range: 0h to 1h After the reset, the value is automatically returned to 0h.
	[7:5]	0h			—	Set the default value.
3003h	[7:0]	37h	*1	PLSTMG08	Drive pulse timing setting 08	Set to 77h
3004h	[7:0]	1Eh	*1	MDSEL1	Mode select 1	Set the value according to each readout mode register setting.
3005h	[7:0]	18h	*1	MDSEL2	Mode select 2	Set the value according to each readout mode register setting.
3006h	[7:0]	10h	*1	MDSEL3	Mode select 3	Set the value according to each readout mode register setting.
3007h	[7:0]	00h	*1	MDSEL4	Mode select 4	Set the value according to each readout mode register setting.
3008h	[0]	0h	*1	SMD	0h: Rolling shutter 1h: Global reset shutter	Setting range: 0h to 1h
	[7:1]	00h			—	Set the default value.
3009h	[7:0]	0000h	*2	SVR	Specifies the integration shutdown vertical period	Setting range: 0000h to FFFFh
300Ah	[7:0]					
300Bh	[0]	0h	*2	MDVREV	0h: Vertical direction normal readout 1h: Vertical direction inversion readout	Setting range: 0h to 1h
	[3:1]	0h			—	Set the default value.
	[4]	0h	*1	HTRIMMING_EN	Horizontal arbitrary cropping enable	Setting range is shown in “Description of Registers”
	[7:5]	1h			—	Set the default value.
300Fh	[7:0]	000h	*1	VWINPOS	Start position of vertical arbitrary cropping (two’s compliment)	Setting range is shown in “Description of Registers”
3010h	[3:0]					
	[7:4]	0h			—	Set the default value.
3011h	[7:0]	000h	*1	VWIDCUT	Width of vertical arbitrary cropping	Setting range is shown in “Description of Registers”
3012h	[2:0]					
	[7:3]	00h			—	Set the default value.
3013h	[7:0]	0000h	*1	MDSEL7	Mode select 7	Set the value according to each readout mode register setting.
3014h	[7:0]					
302Fh	[7:0]	04D2h	*1	Y_OUT_SIZE	Mode setting	Set the value according to each readout mode register setting.
3030h	[4:0]					
	[7:5]	0h			—	Set the default value.
3031h	[7:0]	04D6h	*1	WRITE_VSIZE	Mode setting	Set the value according to each readout mode register setting.
3032h	[4:0]					
	[7:5]	0h			—	Set the default value.
3033h	[5:0]	04h	*1	OB_SIZE_V	Mode setting	Set the value according to each readout mode register setting.
	[7:6]	0h			—	Set the default value.

Address	Bit assign-ment	Default value	Reflection timing	Register name	Function	Remarks
3036h	[7:0]	011Ch	*1	HMAX	Horizontal drive period length	Setting range is shown in ”Description of Registers”
3037h	[7:0]					
3038h	[7:0]	01081h	*1	VMAX	Vertical drive period length	Setting range is shown in ”Description of Registers”
3039h	[7:0]					
303Ah	[3:0]					
	[7:4]	0h			—	Set the default value.
303Bh	[7:0]	0007h	*2	SHR	Specifies the integration start horizontal period	Setting range is shown in “Description of Registers”
303Ch	[7:0]					
303Fh	[0]	0h	Immediately	REGHOLD	Register setting hold function	Setting range is shown in ”Register Value Reflection Timing to Output Data”
	[7:1]	00h			—	Set the default value.
3042h	[7:0]	000h	*1	PGC	Analog gain setting	Setting range: 000h to 7A5h
3043h	[2:0]					
	[7:3]	00h			—	Set the default value.
3044h	[1:0]	0h	*1	DGAIN	Digital gain setting 0h: 0dB, 1h: +6dB: 2h +12dB 3h: +18dB	Setting range: 0h to 3h
	[7:2]	00h			—	Set the default value.
3047h	[7:0]	32h	Immediately	BLKLEVEL	Digital black level offset setting	Setting range: 00h to FFh 10-bits readout mode: 1 digit/1h 12-bits readout mode: 4 digit/1h
3058h	[7:0]	00E0h	*1	HTRIMMING_START	Horizontal cropping start position	Setting range is shown in “Description of Registers”
3059h	[4:0]					
	[7:5]	0h			—	Set the default value.
305Ah	[7:0]	1018h	*1	HTRIMMING_END	Horizontal cropping end position +1	Setting range is shown in “Description of Registers”
305Bh	[4:0]					
	[7:5]	0h			—	Set the default value.
30F6h	[7:0]	0000h	Immediately	MDSEL18	Mode select 18	Set the value according to each readout mode register setting.
30F7h	[7:0]					
3105h	[0]	1h	Immediately	XMSTA	Master mode operation 0h: Master mode start 1h: Master mode stop	Refer to the ”Standby Cancel Sequence”
	[7:1]	00h			—	Set the default value.
3107h	[1:0]	3h	Immediately	SYNCDRV	XHS/XVS pulse output enable 2h :XHS/XVS is output 3h :XHS/XVS is Hi-Z	Refer to the ”Standby Cancel Sequence” when using XHS/XVS output
	[7:2]	28h			—	Set the default value.
320Bh	[7:0]	03h	Immediately	STBPL	00h: Normal operation 03h: PLL standby	Refer to the ”Standby Cancel Sequence” Setting range : 00h to 03h
36AAh	[7:0]	01h	Immediately	PLSTMG02	Drive pulse timing setting 02	Set to 00h
36C1h	[7:0]	01h	Immediately	PLRD1	Input clock frequency setting register	Setting range is shown in ”Description of Registers”
36C2h	[7:0]	00A0h	Immediately	PLRD2	Input clock frequency setting register	Setting range is shown in ”Description of Registers”
36C3h	[7:0]					
36F7h	[7:0]	01h	Immediately	PLRD3	Input clock frequency setting register	Setting range is shown in ”Description of Registers”
36F8h	[7:0]	80h	Immediately	PLRD4	Input clock frequency setting register	Setting range is shown in ”Description of Registers”

1. Description of Register

Total Standby Control

All sensor operation is stopped and the standby mode that reduces power consumption is established by setting the overall standby control register STANDBY to “1h”.
(Standby mode is established immediately after reset.)
The serial communication block operates even in standby mode, so standby mode can be canceled by setting “0h” in the STANDBY register.

STANDBY Setting

Name	Address	Bit	Register value	Function
STANDBY	3000h	[0]	0h	Normal operation
			1h	Overall standby

Digital Circuit Standby Control

When power-on, set the digital circuit standby control register STBLOGIC according to the standby cancel sequence. This register is valid only when STANDBY = 0h.

STBLOGIC Setting

Name	Address	Bit	Register value	Function
STBLOGIC	3000h	[1]	0h	Normal operation
			1h	Digital circuit standby other than serial communications block

CSI-2 Standby Control

CSI-2 can be standby by CSI-2 standby register STBMIPI.

STBMIPI Setting

Name	Address	Bit	Register value	Function
STBMIPI	3000h	[2]	0h	Normal operation
			1h	CSI-2 standby

Frequency Demultiplier Standby Control

When power-on, set the frequency demultiplier standby control register STBDV according to the standby cancel sequence. This register is valid only when STANDBY = 0h.

STBDV Setting

Name	Address	Bit	Register value	Function
STBDV	3000h	[3]	0h	Normal operation
			1h	Frequency demultiplier standby

Sleep

SLEEP register reduces the power consumption during the integration time. See “Low Power Consumption Drive in Integration Time When Using Rolling Shutter Operation” and “Low Power Consumption Drive in Exposure Time When Using Global Reset Shutter Operation”.

SLEEP Setting

Name	Address	Bit	Register value	Function
SLEEP	3000h	[4]	0h	Normal operation
			1h	Circuit standby

Clamp Reset

The internal clamp circuit operation status is reset by the clamp reset register CLPSQRST. Make this setting according to the recommended sequence during power-on or when canceling standby mode.
This register automatically returns to “0h” after the reset process, so there is no need to write “0h”.

CLPSQRST Setting

Name	Address	Bit	Register value	Function
CLPSQRST	3001h	[4]	Changed from 0h to 1h	Resets the internal clamp circuit operation status

Vertical Direction Readout Inversion

The direction of vertical readout order can be set by the vertical direction readout inversion register MDVREV. See “Optical Black Array and Readout Scan Direction” for details of readout image.

MDVREV Setting

Name	Address	Bit	Register value	Function
MDVREV	300Bh	[0]	0h	Vertical direction normal readout
			1h	Vertical direction inversion readout

Input Frequency Setting

The input clock frequency can be set arbitrarily by setting input clock setting register PLRD1, PLRD2, PLRD3 and PLRD4.
Set this registers according to the recommended sequence during power-on or when canceling standby mode.

Input Frequency Setting Registers

Name	Address	bit	Function
PLRD1 [7:0]	36C1h	[7:0]	Input clock frequency setting register
PLRD2 [7:0]	36C2h	[7:0]	
PLRD2 [15:8]	36C3h	[7:0]	
PLRD3 [7:0]	36F7h	[7:0]	
PLRD4 [7:0]	36F8h	[7:0]	

PLRD1 to PLRD4 Setting

		Register value			
		PLRD1	PLRD2	PLRD3	PLRD4
Input clock frequency [MHz][*1]	6	00h	00F0h	00h	C0h
	12	01h	00F0h	01h	C0h
	18	01h	00A0h	01h	80h
	24	02h	00F0h	02h	C0h

[*1] Consult your Sony sales representative concerning other input frequency settings.

Vertical Arbitrary Cropping

By setting VWIDCUT, VWINPOS, MDSEL3 and MDSEL4 registers of vertical arbitrary cropping, arbitrary cropping in vertical direction can be performed. Set the MDSEL 3 and MDSEL 4 registers according to the readout drive mode. See “Vertical Arbitrary Cropping Function” on page 65 for details.

VWINPOS, VWIDCUT Setting

Name	Address	Bit	Function
VWINPOS [7:0]	300Fh	[7:0]	Start position of vertical arbitrary cropping (two's complement)
VWINPOS [11:8]	3010h	[3:0]	
VWIDCUT [7:0]	3011h	[7:0]	Width of vertical arbitrary cropping
VWIDCUT [10:8]	3012h	[2:0]	

Horizontal Arbitrary Cropping

Arbitrary cropping in horizontal direction can be enabled by setting horizontal arbitrary cropping enable register HTRIMMING_EN, and arbitrary cropping in horizontal direction can be performed by designating cropping position of horizontal direction to setting cropping position of horizontal direction register HTRIMMING_START and HTRIMMING_END. See “Horizontal Arbitrary Cropping Function” on page 68 for details.

HTRIMMING_EN, HTRIMMING_START, HTRIMMING_END Setting

Name	Address	Bit	Function
HTRIMMING_EN	300Bh	[4]	Horizontal arbitrary cropping enable
HTRIMMING_START [7:0]	3058h	[7:0]	Horizontal cropping start position
HTRIMMING_START [12:8]	3059h	[4:0]	
HTRIMMING_END [7:0]	305Ah	[7:0]	Horizontal cropping end position +1
HTRIMMING_END [12:8]	305Bh	[4:0]	

Horizontal Drive Period Length and Vertical Drive Period Length

When using CSI-2, Horizontal drive period length (Unit: Number of 72MHz clock) and vertical drive period length (Unit: Number of horizontal drive period) can be set by horizontal drive period length setting register HMAX and vertical drive period length setting register VMAX.

HMAX, VMAX Setting

Name	Address	Bit	Register value	Function
HMAX [7:0]	3036h	[7:0]	Setting range is shown in ”Description of Registers”	Horizontal drive period length
HMAX [15:8]	3037h	[7:0]		
VMAX [7:0]	3038h	[7:0]	Setting range is shown in ”Description of Registers”	Vertical drive period length
VMAX [15:8]	3039h	[7:0]		
VMAX [19:16]	303Ah	[3:0]		

Calculating formula of vertical drive period (1 frame) is shown below.

Vertical drive period length [s] = VMAX value × (SVR value + 1) × HMAX value/ (72×10^6)

See “Horizontal/Vertical Operation Period in Each Readout Drive Mode” on pages 52 and 63 for setting range of HMAX and VMAX in each readout mode, and example of standard setting.

Analog Gain

The analog gain value can be set by setting the analog gain register PGC. Set the lower 8 bits and the upper 3 bits, for total of 11 bits.

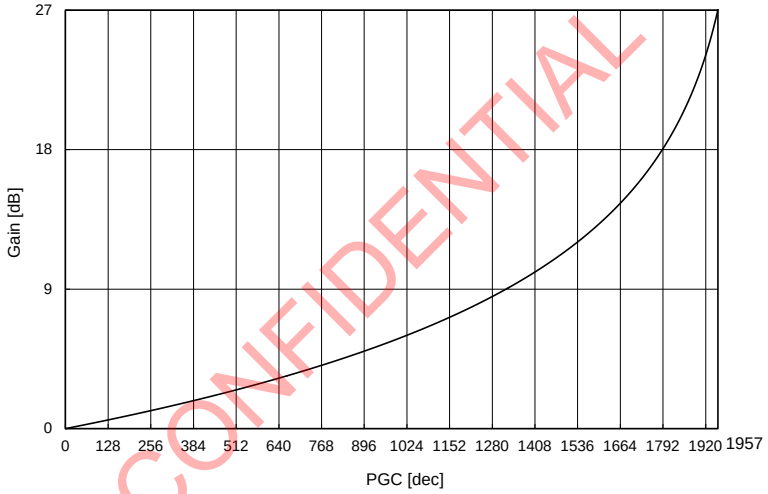
PGC Setting

Name	Address	Bit	Register value	Function
PGC [7:0]	3042h	[7:0]	0h to 7A5h (0d to 1957d)	Analog gain setting
PGC [10:8]	3043h	[2:0]		

In addition, the figure below shows the relationship between the register setting value and the gain value. When the register setting value is “0h (0d)”, the gain value is 0 dB (minimum settable value), and when “7A5h (1957d)”, the gain value is approximately 27 dB (maximum settable value).

Relation Formula

Gain [dB] = –20log{(2048 – PGC [10:0]) /2048}



Relationship between Register Setting Value and Set Gain Value

Digital Gain

The digital gain applied to the data after pixel binning can be set by the digital gain setting register DGAIN.

DGAIN Setting

Name	Address	Bit	Register value	Function
DGAIN [1:0]	3044h	[1:0]	0h	Digital gain setting value = 0 dB
			1h	Digital gain setting value = +6 dB
			2h	Digital gain setting value = +12 dB
			3h	Digital gain setting value = +18 dB

Digital Black Level Offset

The black level offset applied to the data after digital gain processing by the DGAIN register is set by the digital black level offset setting register BLKLEVEL.
Note that the offset unit changes according to the readout drive mode.
When the output data length is 10-bit output, increasing the register setting value by 1h increases the black level by 1 digit. When the output data length is 12-bit output, increasing the register setting value by 1h increases the black level by 4 digits.

BLKLEVEL Setting

Name	Address	Bit	Register value	Function
BLKLEVEL [7:0]	3047h	[7:0]	00h to FFh	Digital black level offset setting

PLL Standby Control

When power-on, set the PLL standby control register STBPL according to the standby cancel sequence. This register is valid only when STANDBY = 0h.

STBPL Setting

Name	Address	Bit	Register value	Function
STBPL	320Bh	[7:0]	00h	Normal operation
			03h	PLL standby

Master Mode Operation Control

When power-on, set the master mode operation control register XMSTA according to the standby cancel sequence. This register is valid only when STANDBY = 0h.

XMSTA Setting

Name	Address	Bit	Register value	Function
XMSTA	3105h	[0]	0h	Master mode start
			1h	Master mode stop

Readout Drive Mode

The readout drive mode of this sensor can be switched by setting the readout drive mode register MDSEL1 to 4, 7, 18, Y_OUT_SIZE, WRITE_VSIZE, OB_SIZE_V, HMAX, VMAX, vertical arbitrary cropping registers and horizontal arbitrary cropping registers. When changing the mode, make the setting according to “Register Settings for Each Readout Drive Mode” on pages 39 to 42.

Readout Drive Pulse Timing

When power-on, set the readout drive pulse timing registers, PLSTMG02 and 08, which are shown in the following table as the initialization registers. See the standby cancel sequence for timing of sending.

PLSTMG Setting

Name	Address	Bit	Register value
PLSTMG08	3003h	[7:0]	Set t0 77h
PLSTMG02	36AAh	[7:0]	Set to 00h

2. Register Setting for Each Readout Drive Mode

The register setting for each readout drive mode available with this sensor is shown in the table below. These registers should be change according to the mode to use. Set the register to the following value.

2-1. When Using Type 1 Approx. 20.30 M Pixels (3:2)

Description of Register Setting for Each Readout Drive Mode

Address	Bit assignment	Register name	Readout mode No. *1									
			0	1	1A	1S	2	2A	3	4	5	6
3004h	[7:0]	MDSEL1	04h	04h	04h	04h	0Dh	0Dh	1Eh	29h	2Dh	18h
3005h	[7:0]	MDSEL2	03h	01h	01h	41h	11h	11h	18h	18h	18h	21h
3006h	[7:0]	MDSEL3	10h	00h	20h	20h	50h	70h	10h	30h	10h	00h
3007h	[7:0]	MDSEL4	00h	00h	50h	50h	00h	50h	00h	50h	00h	09h
3009h	[7:0]	SVR	According to exposure time (See “Frame Rate Adjustment”)									
300Ah	[7:0]											
300Bh	[0]	MDVREV	0h: vertical direction normal /1h: inverted									
	[3:1]		0h									
	[4]	HTRIMMING_EN	1h	1h	1h	1h	1h	1h	1h	1h	1h	1h
	[7:5]		1h									
300Fh	[7:0]	VWINPOS	000h	000h	092h normal / F6Eh inverted	0A2h normal / F5Eh inverted	000h	047h normal / FB9h inverted	000h	009h normal / FF7h inverted	000h	000h
3010h	[3:0]											
	[7:4]		0h									
3011h	[7:0]	VWIDCUT	000h	000h	123h	144h	000h	08Fh	000h	011h	000h	000h
3012h	[2:0]											
	[7:3]		00h									
3013h	[7:0]	MDSEL7	0000h	0000h	0000h	1000h	0000h	0000h	0000h	0000h	0000h	0000h
3014h	[7:0]											
302Fh	[7:0]	Y_OUT_SIZE	0E6Eh	0E6Eh	0C28h	0BE6h	0732h	0614h	04D2h	017Ah	00C6h	0614h
3030h	[4:0]											
	[7:5]		0h									
3031h	[7:0]	WRITE_VSIZE	0E7Eh	0E7Eh	0C38h	0BF6h	0736h	0618h	04D6h	017Eh	00CAh	0618h
3032h	[4:0]											
	[7:5]		0h									
3033h	[5:0]	OB_SIZE_V	10h	10h	10h	10h	04h	04h	04h	04h	04h	04h
	[7:6]		0h									

Address	Bit assignment	Register name	Readout mode No. [*1]									
			0	1	1A	1S	2	2A	3	4	5	6
3036h	[7:0]	HMAX	Setting horizontal drive period length (72MHz clock unit)[*2]									
3037h	[7:0]											
3038h	[7:0]	VMAX	Setting vertical drive period length (unit: HMAX ×72MHz clock)[*2]									
3039h	[7:0]											
303Ah	[3:0]											
	[7:4]		0h									
303Bh	[7:0]	SHR	According to exposure time (See “Integration Time in Each Readout Drive Mode”)									
303Ch	[7:0]											
3058h	[7:0]	HTRIMMING_START	0078h	0078h	0078h	0290h	0078h	0078h	0078h	0078h	0078h	0078h
3059h	[4:0]											
	[7:5]		0h									
305Ah	[7:0]	HTRIMMING_END	15F0h	15F0h	15F0h	0E68h	15F0h	15F0h	15F0h	15F0h	15F0h	15F0h
305Bh	[4:0]											
	[7:5]		0h									
30F6h	[7:0]	MDSEL18	(invalid)			1098h	(invalid)					
30F7h	[7:0]											

[*1] See “Readout Drive Modes” on page 43 for details of readout mode No.

[*2] See “Horizontal/Vertical Operation Period in Each Readout Drive Mode” on page 52 and “ Frame Rate Adjustment” on pages 53 for setting range of HMAX and VMAX in each readout mode, and example of standard setting.

2-2. When Using Type 1/1.4 Approx. 8.42 M Pixels (16:9)

Description of Register Setting for Each Readout Drive Mode

Address	Bit assign ment	Register name	Readout mode No. *1
			1
3004h	[7:0]	MDSEL1	30h
3005h	[7:0]	MDSEL2	41h
3006h	[7:0]	MDSEL3	00h
3007h	[7:0]	MDSEL4	00h
3009h	[7:0]	SVR	According to exposure time (See “Frame Rate Adjustment”)
300Ah	[7:0]		
300Bh	[0]	MDVREV	0h: vertical direction normal /1h: inverted
	[3:1]		0h
	[4]	HTRIMMING_EN	1h
	[7:5]		1h
300Fh	[7:0]	VWINPOS	000h
3010h	[3:0]		
	[7:4]		0h
3011h	[7:0]	VWIDCUT	000h
3012h	[2:0]		
	[7:3]		0h
3013h	[7:0]	MDSEL7	0000h
3014h	[7:0]		
302Fh	[7:0]	Y_OUT_SIZE	087Eh
3030h	[4:0]		
	[7:5]		0h
3031h	[7:0]	WRITE_VSIZE	0886h
3032h	[4:0]		
	[7:5]		0h
3033h	[5:0]	OB_ZIVE_V	08h
	[7:6]		0h
3036h	[7:0]	HMAX	Setting horizontal drive period length (72MHz clock unit) *2
3037h	[7:0]		
3038h	[7:0]	VMAX	Setting vertical drive period length (unit: HMAX ×72MHz clock) *2
3039h	[7:0]		
303Ah	[3:0]		
	[7:4]		0h

Address	Bit assign ment	Register name	Readout mode No. *1
			1
303Bh	[7:0]	SHR	According to exposure time (See “Integration Time in Each Readout Drive Mode”)
303Ch	[7:0]		
3058h	[7:0]	HTRIMMING _START	00ECh
3059h	[4:0]		
	[7:5]		0h
305Ah	[7:0]	HTRIMMING _END	100Ch
305Bh	[4:0]		
	[7:5]		0h
30F6h	[7:0]	MDSEL18	(invalid)
30F7h	[7:0]		

*1 See “Readout Drive Modes” on page 43 for details of readout mode No.

*2 See “Horizontal/Vertical Operation Period in Each Readout Drive Mode” on page 63 and “ Frame Rate Adjustment” on pages 63 for setting range of HMAX and VMAX in each readout mode, and example of standard setting.

Readout Drive Modes

1. Readout Drive Modes

The table below describes the readout drive modes that can be used to operate this sensor.
All of the modes listed in the table below support vertical direction inversion operation (MDVREV = 0h/1h).

1-1. Description of Readout Drive Modes

(1) When Using Type 1 Approx. 20.30 M Pixels (3:2)

Readout Mode No.	Readout drive mode	Mode description
0	All-pixel scan mode (12-bit)	All pixels are readout with 12-bit output. This mode can be used together with the global reset shutter function according to the SMD register setting.
1	All-pixel scan mode (10-bit)	All pixels are readout with 10-bit output. This mode can be used together with the global reset shutter function according to the SMD register setting.
1A	All-pixel scan mode (10-bit) 16:9 cropping	All pixels are readout with 10-bit output. (16:9 cropping) This mode can be used together with the global reset shutter function according to the SMD register setting.
1S	All-pixel scan mode (10-bit) Square cropping	All pixels are readout with 10-bit output. (Square cropping) This mode can be used together with the global reset shutter function according to the SMD register setting.
2	Horizontal/vertical 2/2-line binning (horizontal and vertical weighted binning)	Horizontal and vertical direction 2-line weighted binning readout of pixels of the same color (See the image of binning.)
2A	Horizontal/vertical 2/2-line binning 16:9 cropping (horizontal and vertical weighted binning)	Horizontal and vertical direction 2-line weighted binning readout of pixels of the same color (16:9 cropping) (See the image of binning.)
3	Horizontal/vertical 3/3-line binning	Horizontal and vertical direction 3-line binning readout of pixels of the same color (See the image of binning.)
4	Vertical 2/9 subsampling binning horizontal 3 binning cropping	2 of 9 lines in the vertical direction at the all-pixel scan area (cropping) are added. Then, 3 pixels of the same color in the horizontal direction are added and output. (See the image of binning.)
5	Vertical 2/19 subsampling binning horizontal 3 binning	2 of 19 lines in the vertical direction at the all-pixel scan area (cropping) are added. Then, 3 pixels of the same color in the horizontal direction are added and output. (See the image of binning.)
6	Vertical 2 binning horizontal 2/4 subsampling 16:9 cropping (vertical weighted 2 binning)	Add 2 lines with weighting in the vertical direction at the all-pixel scan area (16:9 cropping) and 2 of every 4 lines in the horizontal direction are output. (See the image of binning.)

(2) When Using Type 1/1.4 Approx. 8.42 M Pixels (16:9)

Readout Mode No.	Readout drive mode	Mode description
1	All-pixel scan mode (10-bit)	All pixels are readout with 10-bit output. This mode can be used together with the global reset shutter function according to the SMD register setting.

1-2. Imaging Conditions in Each Readout Drive Mode

(1) When Using Type 1 Approx. 20.30 M Pixels (3:2)

Readout mode No.	Imaging conditions					
	Number of MIPI output lanes [lane]	Number of A/D conversion bits [bit]	RAW10/ RAW12	Number of horizontal recording pixels	Number of vertical recording pixels	Number of recording pixels
0	4	12	RAW12	5472	3648	Approximately 19.96 M Pixels
1	4	10	RAW10	5472	3648	Approximately 19.96 M Pixels
1A	4	10	RAW10	5472	3078	Approximately 16.84 M Pixels
1S	4	10	RAW10	3000	3000	9.00 M pixels
2	4	10	RAW12	2736	1824	Approximately 4.99 M Pixels
2A	4	10	RAW12	2736	1538	Approximately 4.21 M Pixels
3	4	9	RAW12	1824	1216	Approximately 2.22 M Pixels
4	4	9	RAW12	1824	370	Approximately 0.67 M Pixels
5	4	9	RAW12	1824	190	Approximately 0.35 M Pixels
6	4	10	RAW10	2736	1538	Approximately 4.21 M Pixels

(2) When Using Type 1/1.4 Approx. 8.42 M Pixels (16:9)

Readout mode No.	Imaging conditions					
	Number of MIPI output lanes [lane]	Number of A/D conversion bits [bit]	RAW10/ RAW12	Number of horizontal recording pixels	Number of vertical recording pixels	Number of recording pixels
1	4	10	RAW10	3840	2160	Approximately 8.29 M Pixels

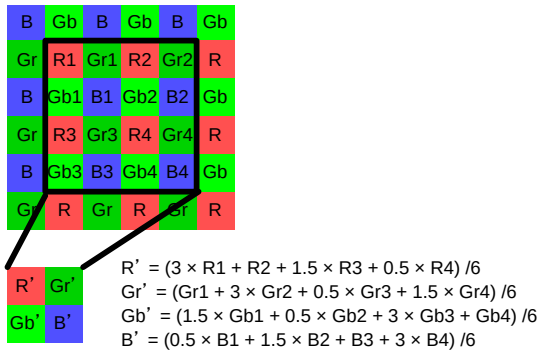
2. Relationship between Arithmetic Processing and the Number of Output Bits in Each Readout Drive Mode

The table below shows the relationship between the A/D conversion resolution, number of binning pixels, internal arithmetic processing, and number of output bits in each readout mode.
Note that the number of output bits differs in each mode. In addition the number of output bits is 10 bits. So the weight of 1 digit is 4 times greater than during 12-bit output.

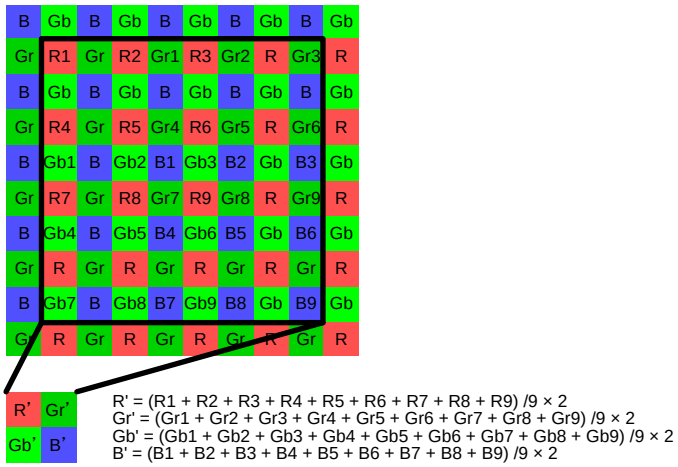
Relationship between Arithmetic Processing and the Number of Output Bits in Each Readout Drive Mode

Readout mode No.	A/D conversion resolution	Vertical pixel processing	Horizontal pixel processing	Total Number of binning pixels	Internal arithmetic processing	Number of output bits
0	12 bits	—	—	—	—	10 bits + 2 bits *1
1	10 bits	—	—	—	—	10 bits
1A						
1S						
2	10 bits	2 binning	2 binning	4 pixels	3/6, 1.5/6, 1/6, 0.5/6 (weighted binning *3)	10 bits + 2 bits *2
2A						
3	9 bits	3 binning	3 binning	9 pixels	2/9	10 bits + 2 bits *2
4	9 bits	2/9 subsampling binning	3 binning	6 pixels	1/3	10 bits + 2 bits *2
5	9 bits	2/19 subsampling binning	3 binning	6 pixels	1/3	10 bits + 2 bits *2
6	10 bits	2 binning	2/4 subsampling	2 pixels	3/4, 1/4 (weighted binning *3)	10 bits

*1 A/D conversion is performed with a resolution 4 times that of 10-bit A/D conversion, and the results are output in 12 bits regarded as a 10-bit integer item and a 2-bit decimal item.
*2 Division is performed by internal arithmetic processing, then the results are output in 12 bits with the integer item in the upper 10 bits and the decimal item in the lower 2 bits.
*3 See “Binning Image” diagram on pages 45 to 46 for details of weighted binning.

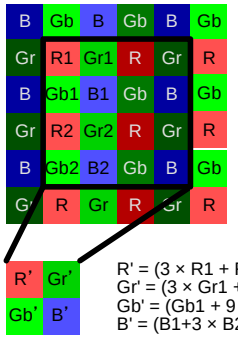


Horizontal/Vertical 2/2-line Binning
(horizontal and vertical weighted binning)
Binning Image

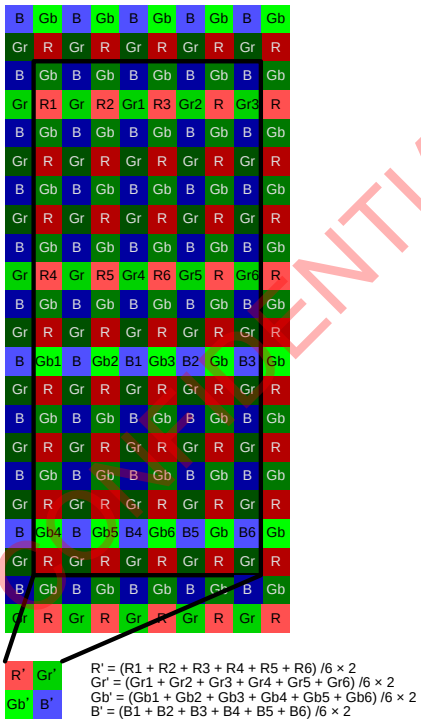


Horizontal/Vertical 3/3-line Binning
Binning Image

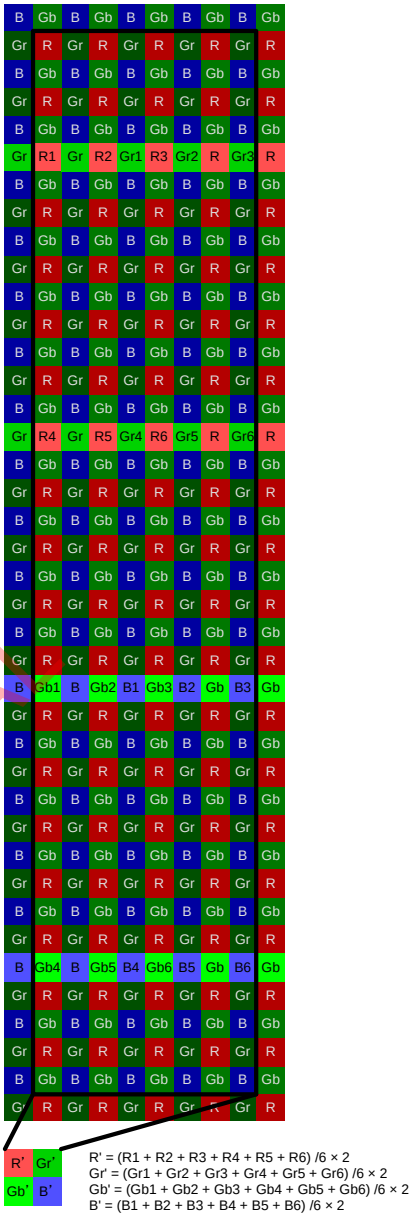
Note) White letters in the diagram indicate pixels which are not read out.



Vertical 2 Binning
Horizontal 2/4 Subsampling
(Vertical Weighted Binning)
Binning Image



Vertical 2/9 Subsampling binning
Horizontal 3 Binning
Binning Image



Vertical 2/19 Subsampling binning
Horizontal 3 binning
Binning Image

Note) White letters in the diagram indicate pixels which are not read out.

Image Data Output Format

Frame Format

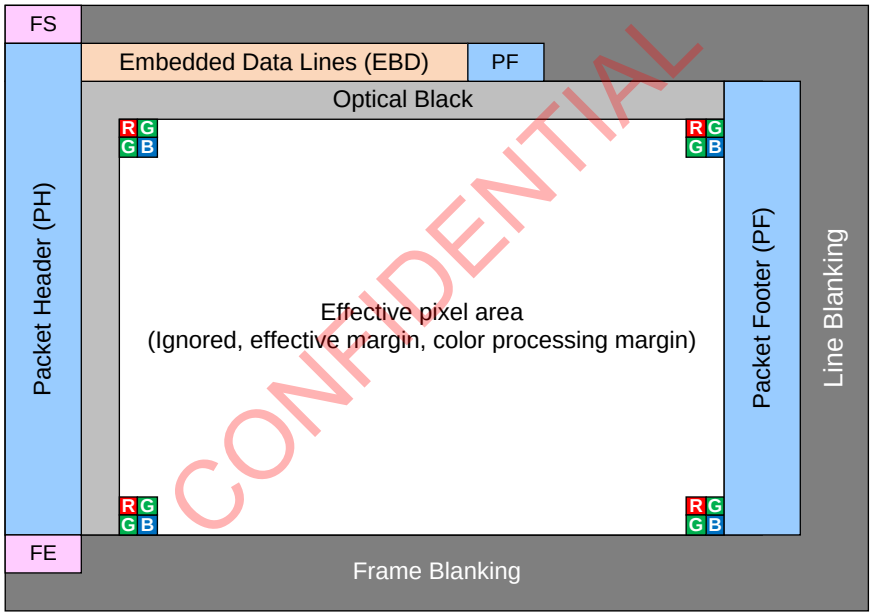
Each line of each image frame is output like the General Frame Format to CSI-2. The settings for each packet header are shown below.

DATA Type

Header [5:0]	Name	Description
00h	Frame Start Code	FS
01h	Frame End Code	FE
12h	Embedded Data	Embedded data
2Bh	RAW10	When output data bit length is 10-bits
2Ch	RAW12	When output data bit length is 12-bits
37h	Optical Black Data	Vertical Optical Black line data

Frame Structure

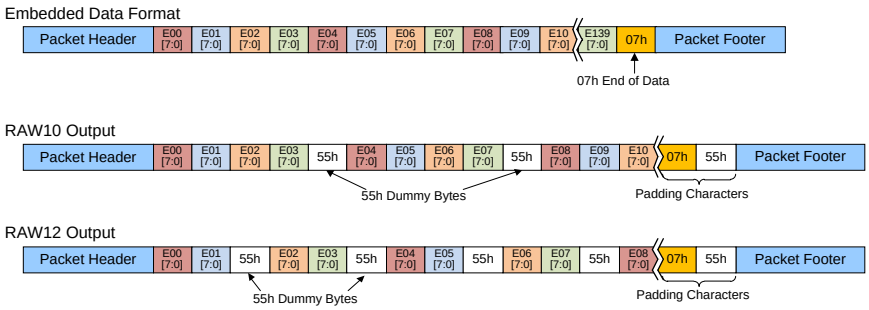
The figure below shows the image frame structure.



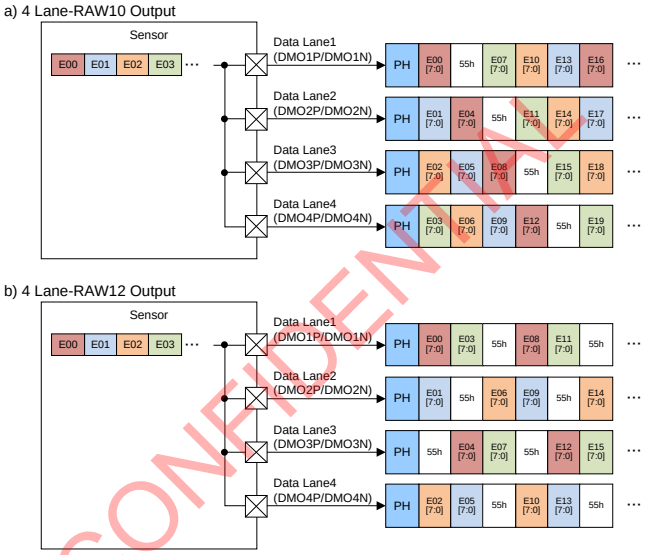
Frame Structure

Embedded Data Line

The Embedded data line is output in a line following the sync code FS.
In RAW10 mode, 55h dummy bytes are inserted after outputting 4 bytes of data each.
In RAW12 mode, 55h dummy bytes are inserted after outputting 2 bytes of data each.



The each format of 4 Lane is shown below.



Output Format of Embedded 4 Lane

Specific Output

Output timing	bit	Transfer data	Description
E00 to E05	[7:0]	—	(Ignored)
E06	[0]	SMD	
	[7:1]	—	(Ignored)
E07	[7:0]	PGC	
E08	[2:0]		
	[7:3]	—	(Ignored)
E09	[7:0]	SHR	
E10	[7:0]		
E11	[7:0]	SVR	
E12	[7:0]		
E13 to E14	[7:0]	—	(Ignored)
E15	[3:0]	DGAIN	
	[4]	MDVREV	
	[7:5]	—	(Ignored)

Output timing	bit	Transfer data	Description
E16	[7:0]	BLKLEVEL	
E17 to E24	[7:0]	—	(Ignored)
E25	[0]	HTRIMMING_EN	
	[7:1]	—	(Ignored)
E26	[7:0]	HTRIMMING_START	
E27	[4:0]		
	[7:5]	—	(Ignored)
E28	[7:0]	HTRIMMING_END	
E29	[4:0]		
	[7:5]	—	(Ignored)
E30	[7:0]	—	(Ignored)
E31	[7:0]	VWINPOS	
E32	[3:0]		
	[7:4]	—	(Ignored)
E33	[7:0]	VWIDCUT	
E34	[2:0]		
	[7:3]	—	(Ignored)
E35 to E139	[7:0]	—	(Ignored)

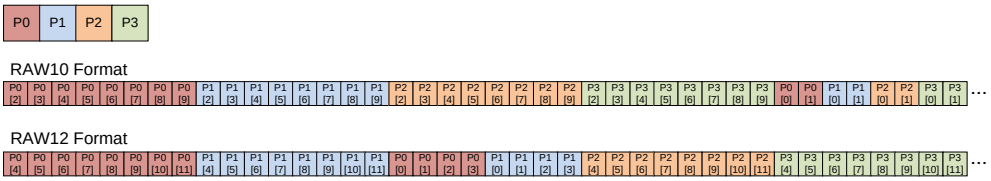
CSI-2 serial Output Setting

The output formats of this sensor support the following modes.

CSI-2 serial data output 4 Lane, RAW10 and RAW12

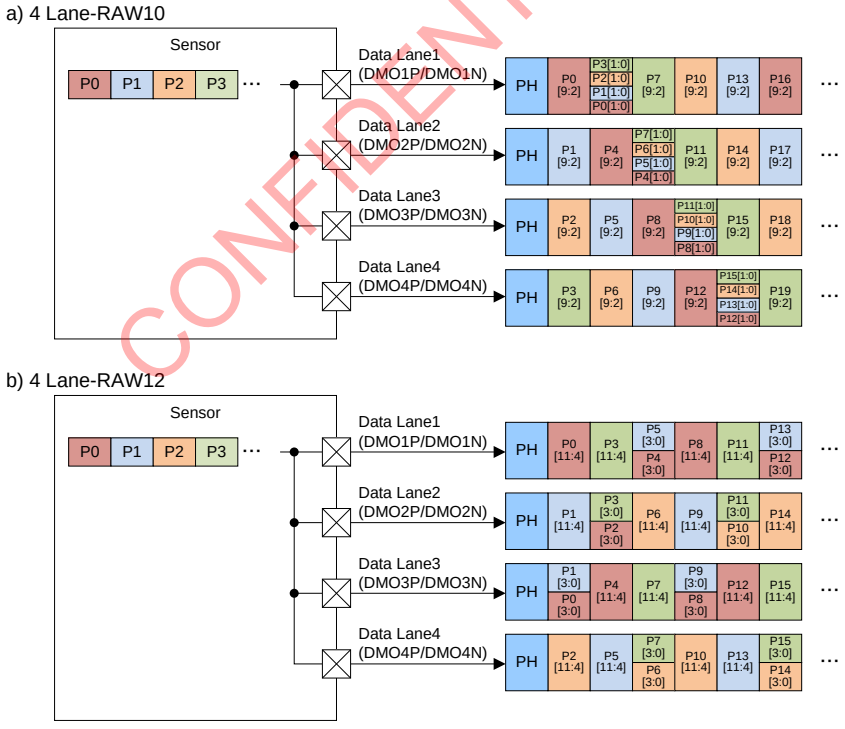
The image data is output from the CSI-2 output pin. The DMO1P/DMO1N are called the Lane1 data signal, the DMO2P/DMO2N are called the Lane2 data signal, the DMO3P/DMO3N are called the Lane3 data signal and the DMO4P/DMO4N are called the Lane4 data signal. In addition, the clock signals are output from DCKP/DCKN of the CSI-2 pins.
In 4 Lane mode, data is output from Lane1, Lane2, Lane3 and Lane4.
The bit rate maximum value is 1.440 Gbps/Lane.

The formats of RAW10 and RAW12 are shown below.



Example of formats of RAW10 and RAW12

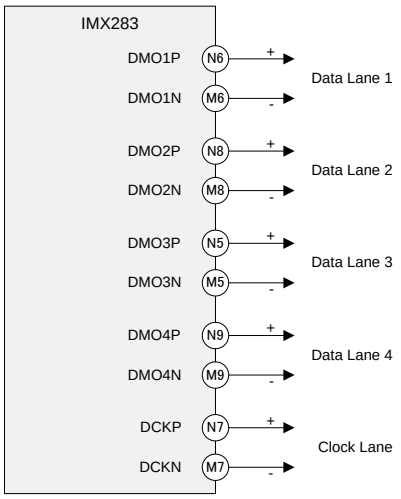
The each format of 4 Lane are shown below.



Output Format of 4 Lane

MIPI Transmitter

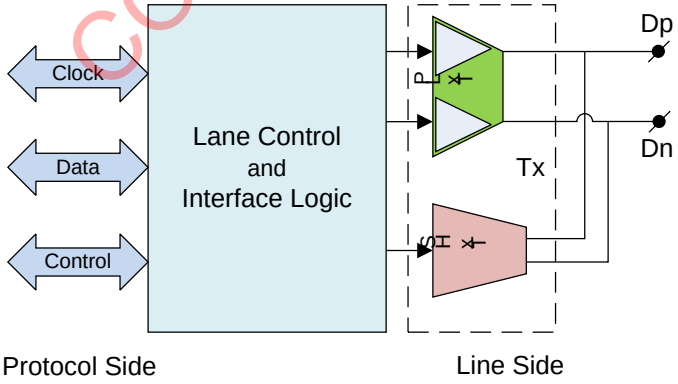
Output pins (DMO1P to DMO4P, DMO1N to DMO4N, DCKP, DCKN) are described in this section.



Relationship between Pin Name and MIPI Output Lane

The pixel signals are output by the CSI-2 High-speed serial interface.
See the MIPI Standard
・MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.1
・MIPI Alliance Specification for D-PHY Version 1.1

The CSI-2 transfers one bit with a pair of differential signals. The transmitter outputs differential current signal after converting pixel signals to it. Insert external resistance in differential pair in a series or use cells with a built-in resistance on the Receiver side. When inserting an external resistor, as close as possible to the Receiver.
The differential signals maintain a constant interval and reach the receiver with the shortest wiring length possible to avoid malfunction. The maximum bit rate of each Lane are 1.440Gbps/Lane.



Universal Lane Module Functions

Detailed Specification of Each Mode

1. When Using Type 1 Approx. 20.30 M Pixels (3:2)

1-1. Horizontal/Vertical Operation Period in Each Readout Drive Mode

Horizontal Operation Period in Each Readout Drive Mode

Readout mode No.	Horizontal operation period (Number of pixels conversion)						HMAX register minimum value
	Front OB area	Front ignored area of effective pixels	Front effective margin for color processing	Recommended recording pixels	Rear effective margin for color processing	Rear ignored area of effective pixels	
0	96	0	12	5472	12	0	887
1	96	0	12	5472	12	0	745
1A	96	0	12	5472	12	0	745
1S	96	0	16	3000	16	0	544
2	48	0	6	2736	6	0	362
2A	48	0	6	2736	6	0	362
3	32	0	4	1824	4	0	284
4	32	0	4	1824	4	0	362
5	32	0	4	1824	4	0	362
6	48	0	6	2736	6	0	364

Vertical Operation Period in Each Readout Drive Mode

Readout mode No.	Number of lines per vertical operation period (output data 1H conversion)						VMAX register minimum value
	Front OB area	Front ignore area of effective pixels	Front effective margin for color processing	Recommended recording pixels	Rear effective margin for color processing	Rear ignored area of effective pixels	
0	16	12	12	3648	12	10	3793
1	16	12	12	3648	12	10	3793
1A	16	6	12	3078	12	4	3203
1S	16	12	12	3000	12	4	3081
2	4	4	6	1824	6	2	3840
2A	4	4	6	1538	6	2	3300
3	4	4	6	1216	6	2	4200
4	4	2	2	370	2	2	828
5	4	2	2	190	2	2	440
6	4	4	6	1538	6	2	3296

1-2. Frame Rate Adjustment

The formula for frame rate calculation is shown below.

Frame rate [frame/s] = (72 x 10^6) / {HMAX register value × VMAX register value × (SVR register value + 1) }

The frame rate can be changed by changing HMAX and VMAX register values as long as these are set to minimum value or larger. HMAX changes the line blanking period. VMAX changes the frame blanking period.
The examples of setting for each readout drive mode are shown in the table below. Set HMAX and VMAX considering ISP image processing time.
The vertical sync signal XVS can be subsampled inside the sensor according to the SVR register. When using SVR = 1h, the frame rate becomes half. See pages 70 to 74 “Electronic Shutter Timing” for details.

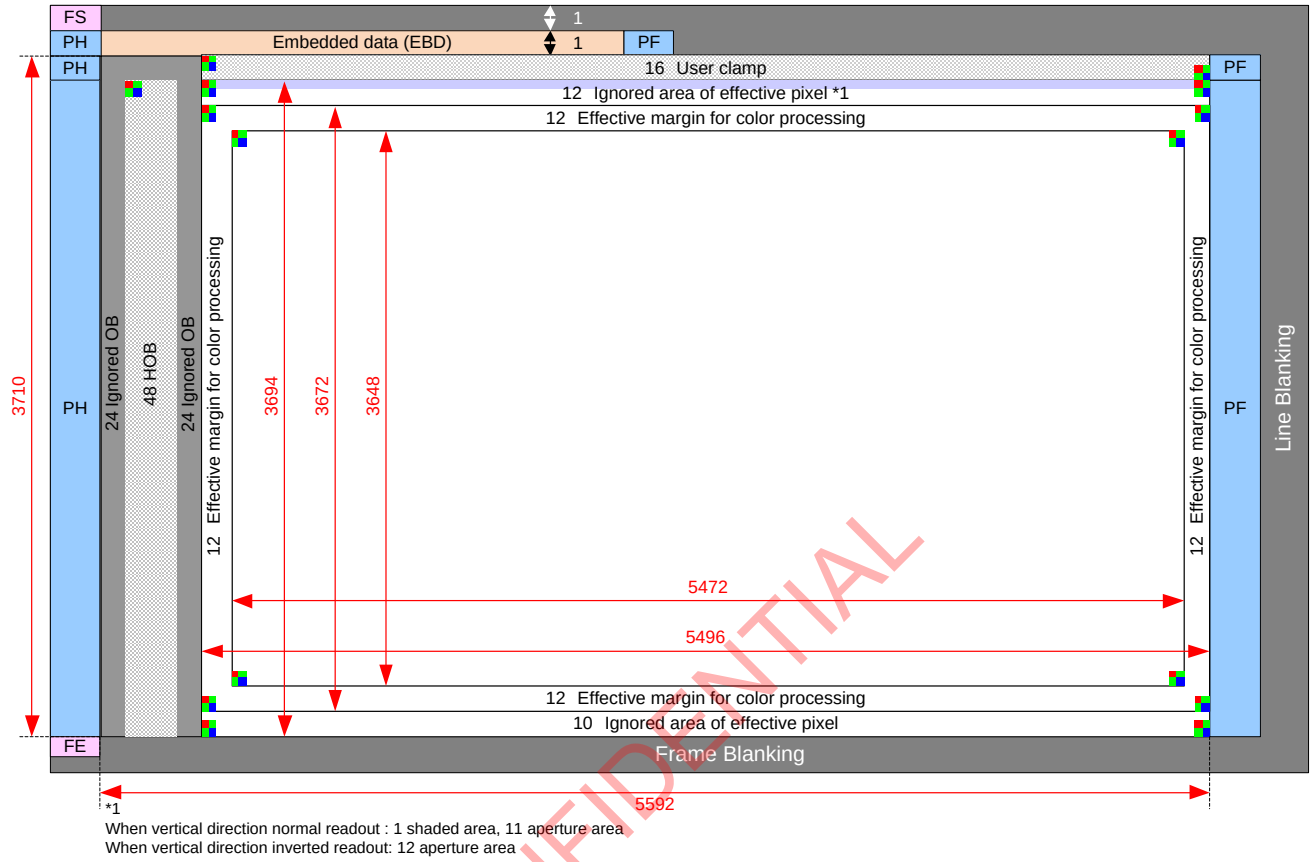
Examples of HMAX, VMAX and Frame Rate

Readout mode No.	HMAX[*1] min value	VMAX[*2] min value	Max frame frequency [frame/s]	NTSC compatible drive				PAL compatible drive			
				HMAX[*1] [dec]	VMAX[*2] [dec]	SVR	Frame frequency [frame/s]	HMAX[*1] [dec]	VMAX[*2] [dec]	SVR	Frame frequency [frame/s]
0	887	3793	21.40	900	4004	0	19.98	900	4000	0	20.00
1	745	3793	25.48	770	4680	0	19.98	750	3840	0	25.00
1A	745	3203	30.17	750	3203	0	29.97[*3]	750	3840	0	25.00
1S	544	3081	42.96	546	4400	0	29.97	576	5000	0	25.00
2	362	3840	51.80	364	3960	0	49.95	375	3840	0	50.00
2A	362	3300	60.27	364	3300	0	59.94	375	3840	0	50.00
3	284	4200	60.36	286	4200	0	59.94	288	5000	0	50.00
4	362	828	240.21	364	825	0	239.76	375	960	0	200.00
5	362	440	452.03	364	440	0	449.55	375	480	0	400.00
6	364	3296	60.01	364	3300	0	59.94	375	3840	0	50.00

[*1] The value set as HMAX (address 3036h, bit [7:0] and address 3037h, bit [7:0]).
[*2] The value set as VMAX (address 3038h, bit [7:0], address 3039h, bit [7:0] and address 303Ah, bit [3:0]).
[*3] This frame rate is not compatible for NTSC.

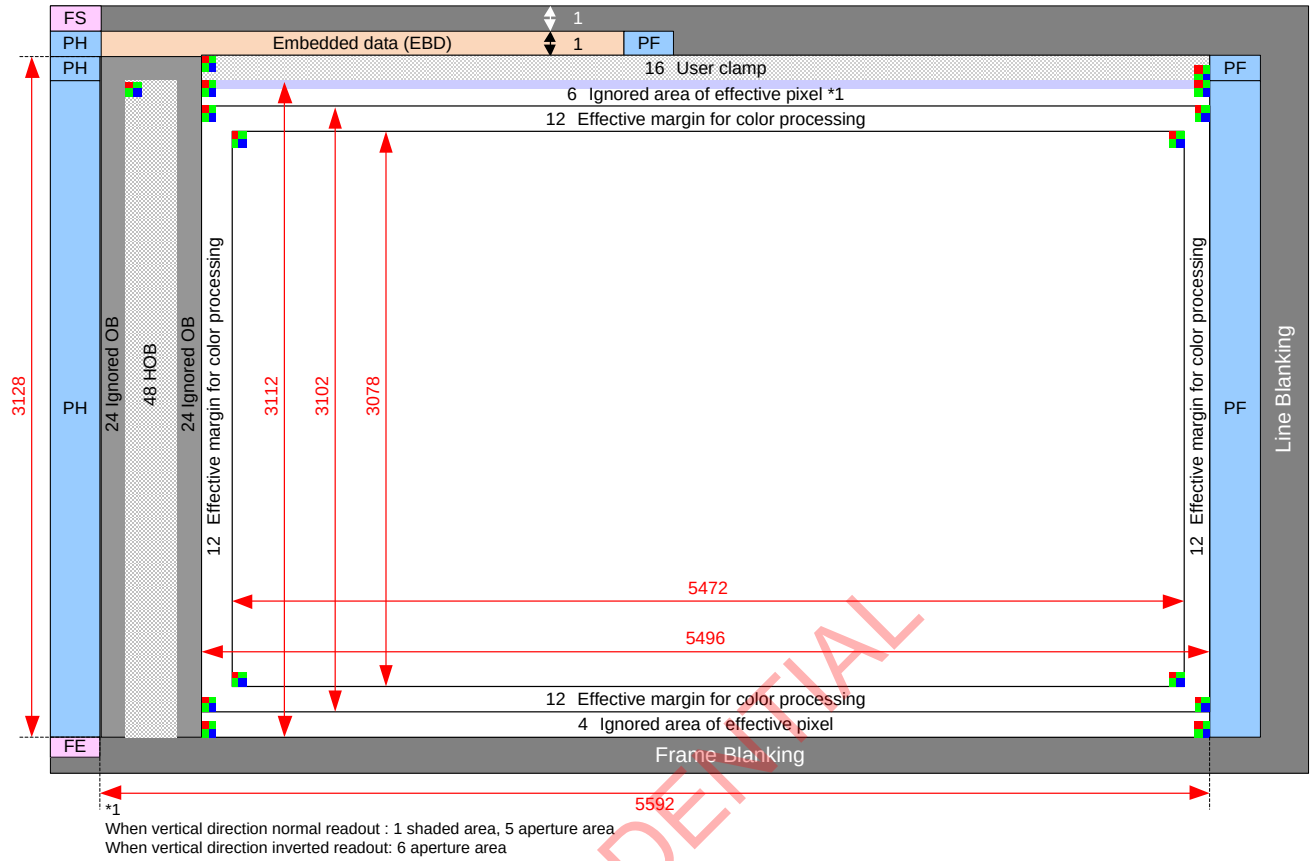
1-3. Image Data Output Format

MODE0: All-pixel scan mode (12-bit A/D conversion, 12-bit length output)
MODE1: All-pixel scan mode (10-bit A/D conversion, 10-bit length output)



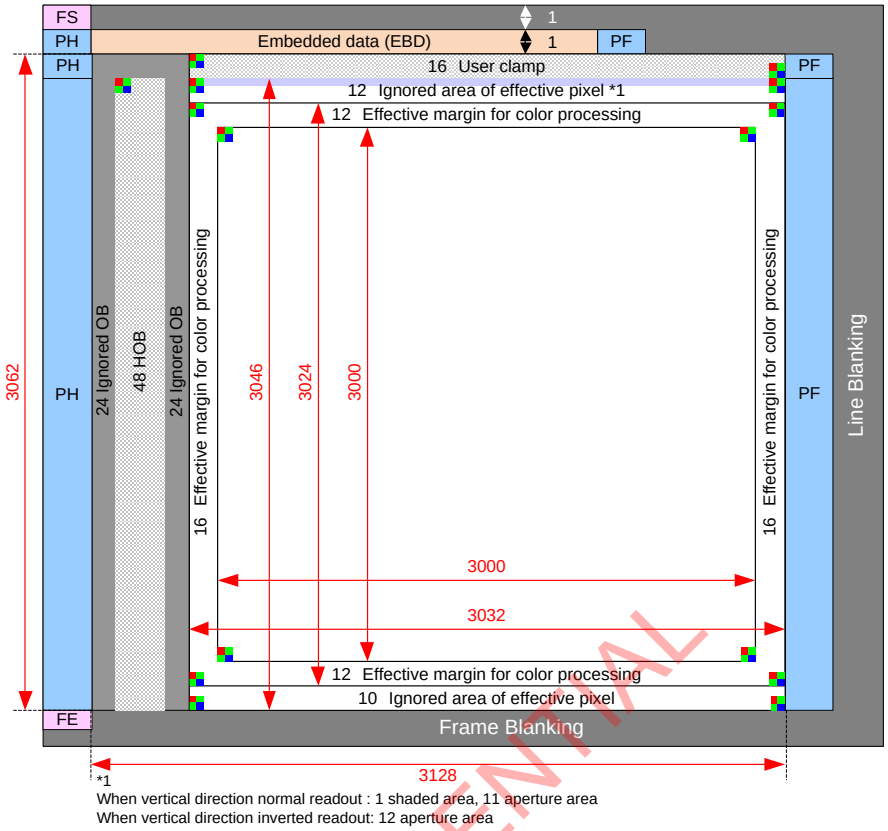
Readout Pixel Image Diagram (5472 × 3648)

MODE1A: All-pixel scan mode 16:9 cropping (10-bit A/D conversion, 10-bit length output)



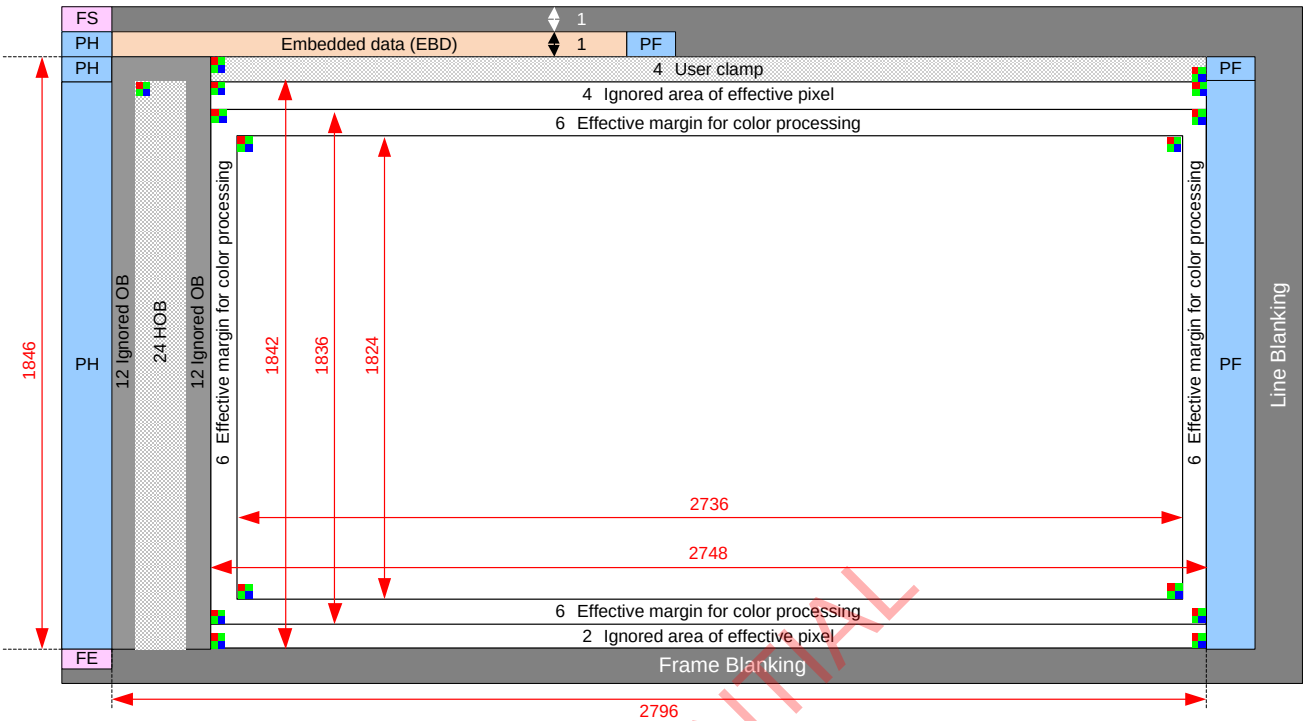
Readout Pixel Image Diagram (5472 × 3078)

MODE1S: All-pixel scan mode square cropping (10-bit A/D conversion, 10-bit length output)



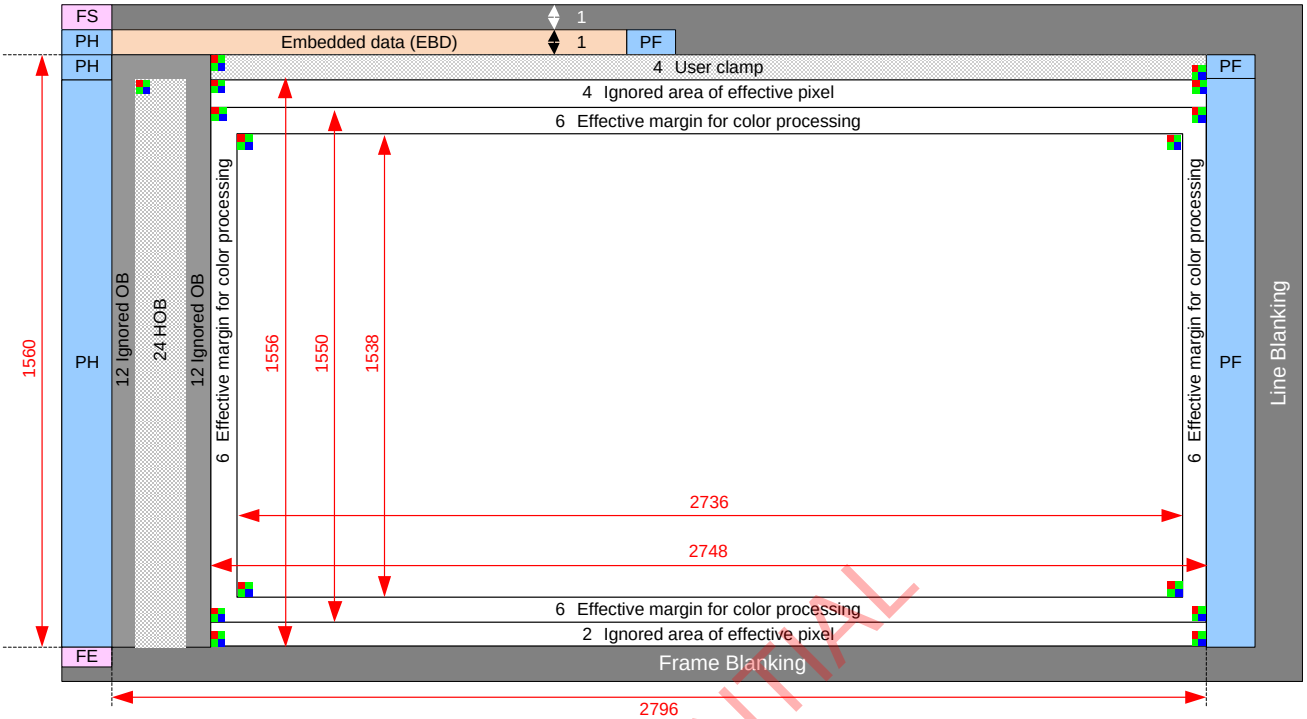
Readout Pixel Image Diagram (3000 × 3000)

MODE2: Horizontal/vertical 2/2-line binning (horizontal and vertical weighted binning)
(10-bit A/D conversion, 12-bit length output)



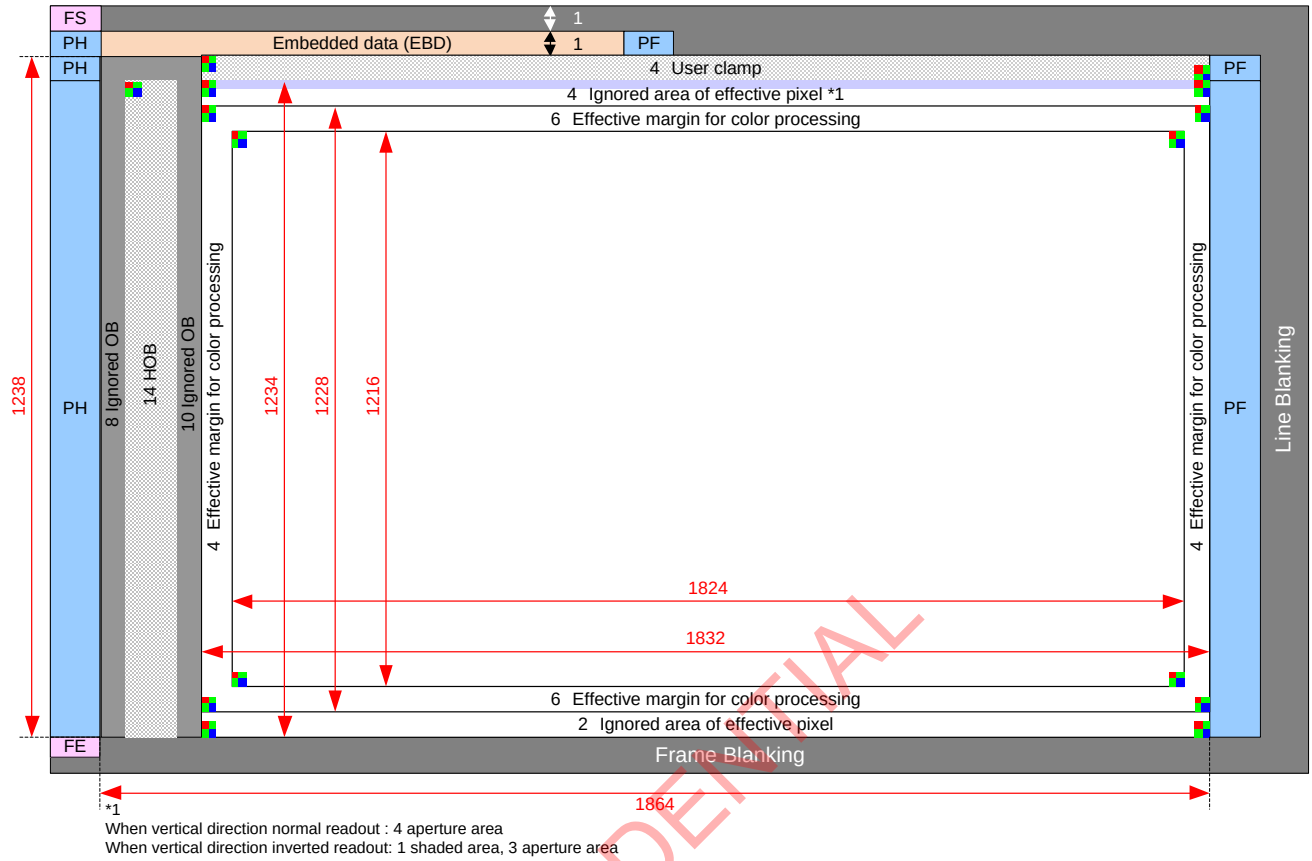
Readout Pixel Image Diagram (2736 × 1824)

MODE2A: Horizontal/vertical 2/2-line binning 16:9 cropping (horizontal and vertical weighted binning)
(10-bit A/D conversion, 12-bit length output)



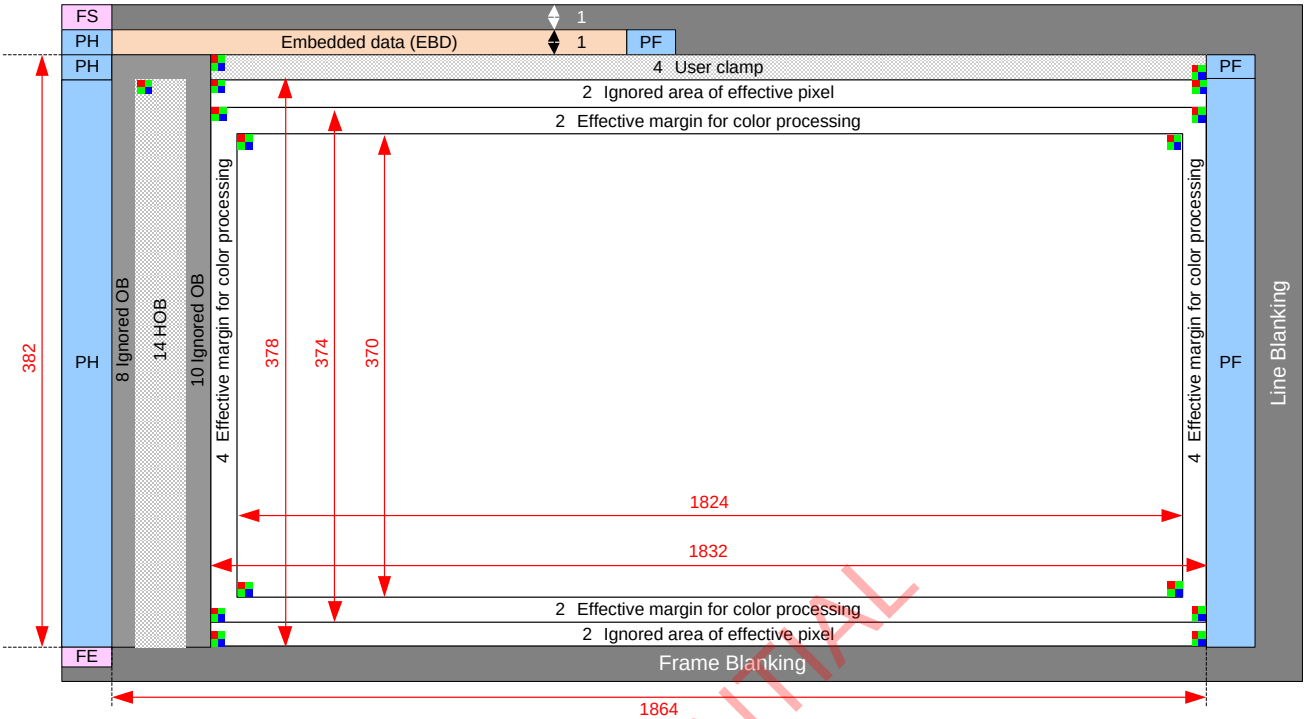
Readout Pixel Image Diagram (2736 × 1538)

MODE3: Horizontal/vertical 3/3-line binning (9-bit A/D conversion, 12-bit length output)



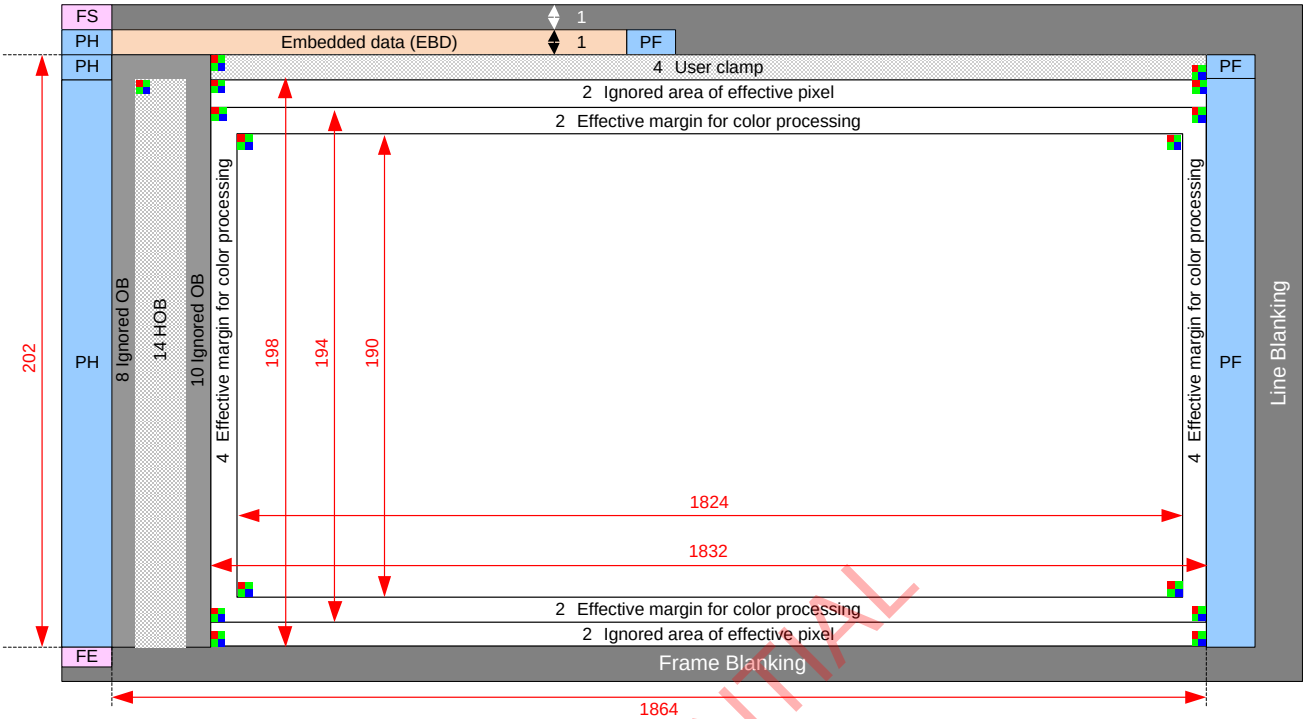
Readout Pixel Image Diagram (1824 × 1216)

MODE4: Vertical 2/9 subsampling binning horizontal 3 binning cropping
(9-bit A/D conversion, 12-bit length output)



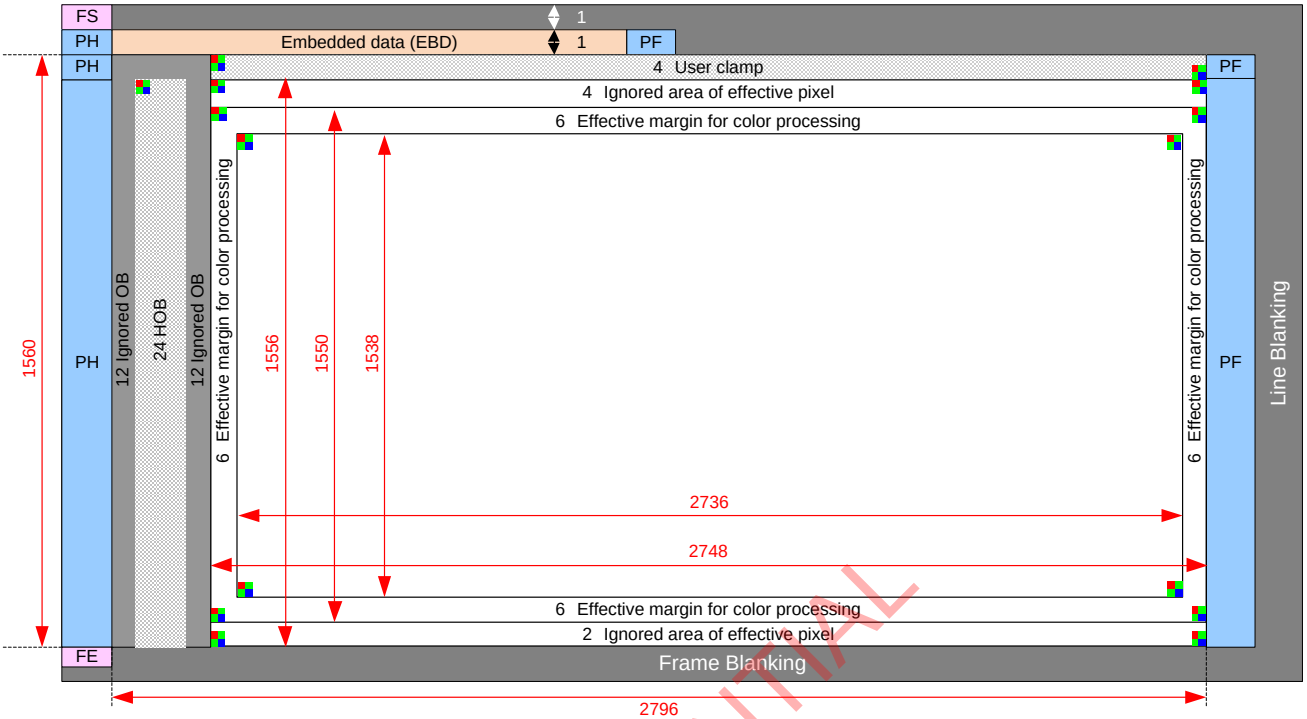
Readout Pixel Image Diagram (1824 × 370)

MODE5: Vertical 2/19 subsampling binning horizontal 3 binning cropping
(9-bit A/D conversion, 12-bit length output)



Readout Pixel Image Diagram (1824 × 190)

MODE6: Vertical 2 binning horizontal 2/4 subsampling 16:9 cropping (vertical weighted 2 binning)
(10-bit A/D conversion, 10-bit length output)



Readout Pixel Image Diagram (2736 × 1538)

2. When Using Type 1/1.4 Approx. 8.42 M Pixels (16:9)

2-1. Horizontal/Vertical Operation Period in Each Readout Drive Mode

Horizontal Operation Period in Each Readout Drive Mode

Readout mode No.	Horizontal operation period (Number of pixels conversion)						HMAX register minimum value
	Front OB area	Front ignored area of effective pixel	Front effective margin for color processing	Recommended recording pixels	Rear effective margin for color processing	Rear ignored area of effective pixel	
1	0	0	16	3840	16	0	544

Vertical Operation Period in Each Readout Drive Mode

Readout mode No.	Number of lines per vertical operation period (output data 1H conversion)						VMAX register minimum value
	Front OB area	Front ignore area of effective pixel	Front effective margin for color processing	Recommended recording pixels	Rear effective margin for color processing	Rear ignored area of effective pixel	
1	8	4	4	2160	4	2	2200

1-2. Frame Rate Adjustment

The formula for frame rate calculation is shown below.

Frame rate [frame/s] = (72×10^6) / {HMAX register value × VMAX register value × (SVR register value + 1) }

The frame rate can be changed by changing HMAX and VMAX register values as long as these are set to minimum value or larger. HMAX changes the line blanking period. VMAX changes the frame blanking period.
The examples of setting for each readout drive mode are shown in the table below. Set HMAX and VMAX considering ISP image processing time.
The vertical sync signal XVS can be subsampled inside the sensor according to the SVR register. When using SVR = 1h, the frame rate becomes half. See pages 70 to 74 “Electronic Shutter Timing” for details.

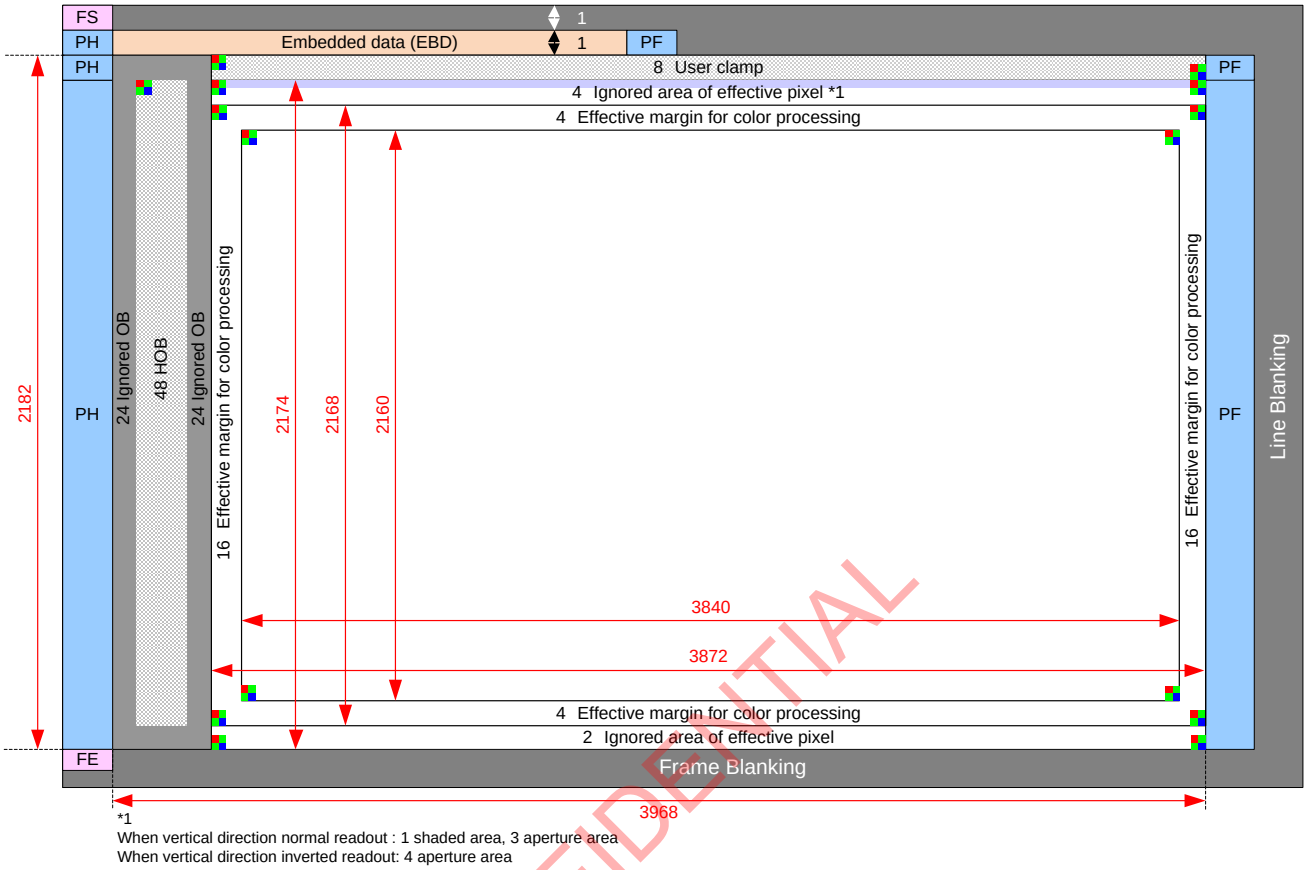
Examples of HMAX, VMAX and Frame Rate

Readout mode No.	HMAX[*1] min value	VMAX[*2] min value	Max frame frequency [frame/s]	NTSC compatible drive				PAL compatible drive			
				HMAX[*1] [dec]	VMAX[*2] [dec]	SVR	Frame frequency [frame/s]	HMAX[*1] [dec]	VMAX[*2] [dec]	SVR	Frame frequency [frame/s]
1	544	2200	60.16	546	2200	0	59.94	576	2500	0	50.00

[*1] The value set as HMAX (address 3036h, bit [7:0] and address 3037h, bit [7:0]).
[*2] The value set as VMAX (address 3038h, bit [7:0], address 3039h, bit [7:0] and address 303Ah, bit [3:0]).

2-3. Image Data Output Format

MODE1: All-pixel scan mode (10-bit A/D conversion, 10-bit length output)



Readout Pixel Image Diagram (3840 × 2160)

Vertical Arbitrary Cropping Function

Vertical cropping region of this sensor can be arbitrarily changed by registers.

(1) Register Setting

Enable vertical cropping with setting mode select register MDSEL3[7:0] and MDSEL4[7:0] to specified value every readout drive mode, and specify cropping width by the vertical cropping width register VWIDCUT, and cropping position by the vertical cropping start position register VWINPOS.
And set the number of total output lines (including VOB) after cropping to the register WRITE_VSIZE, and the number of effective pixel lines (not including VOB) after cropping to the register Y_OUT_SIZE.
Set VWINPOS negative value (two's complement) when the direction of vertical readout is inverted (MDVREV = 1h).
Veff indicates the number of effective lines output before cropping (including ignored area of effective pixel and effective margin for color processing) in following description.

MDSEL3 and MDSEL4 Setting

Name	Address	Bit	Readout mode No.									
			0	1*1	1A	1S	2	2A	3	4	5	6
MDSEL3	3006h	[7:0]	30h	20h	20h	20h	70h	70h	30h	30h	30h	20h
MDSEL4	3007h	[7:0]	50h	50h	50h	50h	50h	50h	50h	50h	50h	59h

*1 When using Type 1 Approx. 20.30 M Pixel (3:2) and Type 1/1.4 Approx. 8.42 M Pixel Readout mode No.1

VWINPOS Setting

Name	Address	Bit	Register value
VWINPOS [7:0]	300Fh	[7:0]	Vertical cropping start position (two's complement) Set cropping start line/2 + Vst
VWINPOS [11:8]	3010h	[3:0]	

VWIDCUT Setting

Name	Address	Bit	Register value
VWIDCUT [7:0]	3011h	[7:0]	Specify vertical cropping width Set (Veff – cropping width)/2+ Vct
VWIDCUT [10:8]	3012h	[2:0]	

Y_OUT_SIZE Setting

Name	Address	Bit	Register value
Y_OUT_SIZE [7:0]	302Fh	[7:0]	Set the number of effective pixel lines (not including VOB) after cropping
Y_OUT_SIZE [4:0]	3030h	[4:0]	

WRITE_VSIZE Setting

Name	Address	Bit	Register value
WRITE_VSIZE [7:0]	3031h	[7:0]	Set the number of total output lines (including VOB) after cropping
WRITE_VSIZE [4:0]	3032h	[4:0]	

Refer to the following table in the value of Vst, Vct and Veff.

Vst, Vct, Veff Value

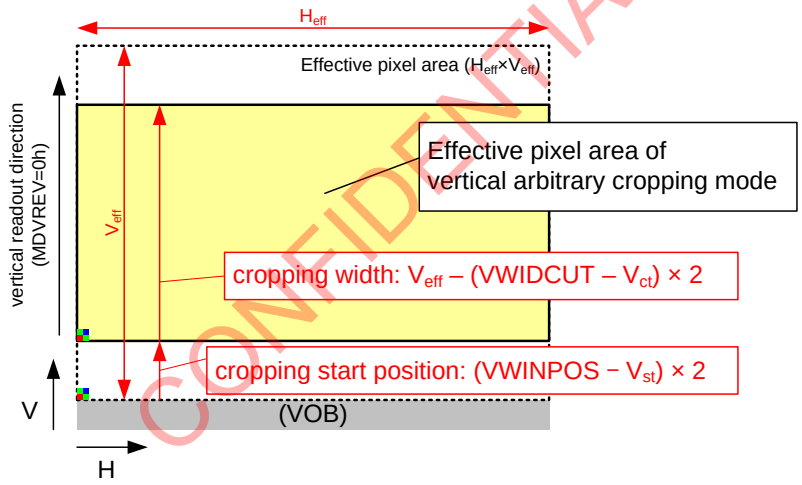
Readout mode No.	Type 1 approx. 20.30 M pixels										Type 1/1.4 approx. 8.42 M pixels
	0	1	1A	1S	2	2A	3	4	5	6	1
Vst	0	0	146	162	0	71	0	9	0	0	0
Vct	0	0	291	324	0	143	0	17	0	0	0
Veff	3694	3694	3112	3046	1824	1556	1234	378	198	1556	2172

When vertical readout direction is normal (MDVREV = 0h), relation between register setting values of VWINPOS / VWIDCUT and cropping region on physical pixel array is shown below.
Register setting values must satisfy following relations. (Setting ranges are within those values which satisfy following.)

(VWINPOS – Vst) × 2 ≥ 0 (Starting position of readout must be 0 or more)

Veff – (VWIDCUT – Vct) × 2 ≥ Veff / 2 (Number of readout lines must be half or more before cropping)

(VWINPOS – Vst) × 2 + Veff – (VWIDCUT– Vct) × 2 ≤ Veff (End position of readout must be within the area before cropping)



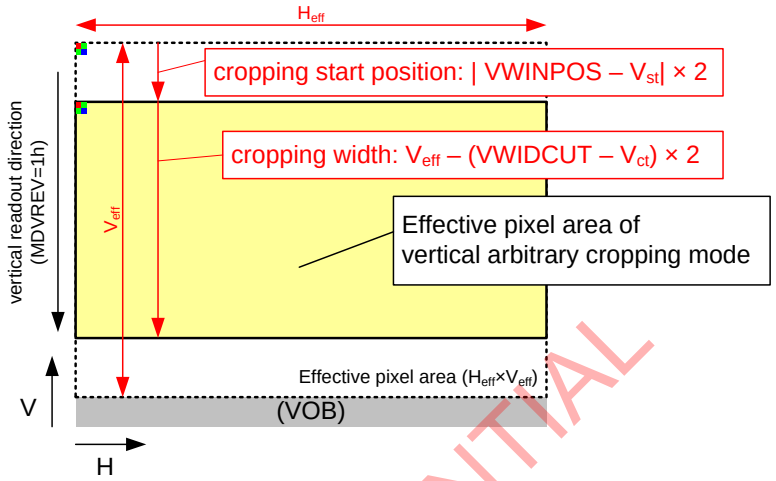
Relation between Register Settings of VWINPOS / VWIDCUT and Cropping Region on Physical Pixel Array (Vertical Readout Direction Normal)

For example, when the top 400 lines and bottom 400 lines (totally 800 lines) of Type 1 Approx. 20.30 M Pixel all-pixel scan mode (10-bit) 16:9 cropping is skipped and start cropping readout from the 401st line, setting values are as follows:

VWIDCUT 2B3h (691d) / VWINPOS 15Ah (346d) / Y_OUT_SIZE 908h (2312d) / WRITE_VSIZE 918h (2328d)

When vertical readout direction is inverted (MDVREV = 1h), relation between register setting value of VWINPOS / VWIDCUT and cropping region is shown below. Register setting values must satisfy following relations also. Note that VWINPOS must be negative.

|VWINPOS – Vst| × 2 ≥ 0 (Starting position of readout must be 0 or more)
Veff – (VWIDCUT – Vct) × 2 ≥ Veff / 2 (Number of readout lines must be 2 or more before cropping)
|VWINPOS – Vst| × 2 + Veff – (VWIDCUT – Vct) × 2 ≤ Veff (End position of readout must be within the area before cropping)



Relation between Register Settings of VWINPOS / VWIDCUT and Cropping Region on Physical Pixel Array (Vertical Readout Direction Inverted)

For example, when the top 400 lines and bottom 400 lines (total 800 lines) of Type 1 Approx. 20.30 M Pixel all-pixel scan mode (10-bit) 16:9 cropping (when vertical readout direction inverted) is skipped and start cropping readout from the 401st line, setting values are as follows:

VWIDCUT 2B3h (691d) / VWINPOS EA6h (-346d) / Y_OUT_SIZE 908h (2312d) / WRITE_VSIZE 918h (2328d)

(2) Vertical Minimum Period When Using Vertical Arbitrary Cropping Function

When using vertical arbitrary cropping function, VMAX minimum value gets smaller according to cropping width. The table below shows VMAX minimum value after cropping when VMAX minimum value before cropping is represented as V_{MAX0}.

VMAX Minimum Value When Using Vertical Arbitrary Cropping Function

Readout mode No.	VMAX minimum period
0, 1, 1A, 1S	V_{MAX0} – (VWIDCUT – Vct) × 2
2, 2A, 4, 5, 6	V_{MAX0} – (VWIDCUT – Vct) × 4
3	V_{MAX0} – (VWIDCUT – Vct) × 6

Horizontal Arbitrary Cropping Function

Horizontal cropping region of this sensor can be arbitrarily changed by registers.

(1) Register Settings

Set horizontal cropping enable register HTRIMMING_EN to 1h to enable horizontal arbitrary cropping function, and horizontal cropping area are determined by horizontal cropping position register HTRIMMING_START and HTRIMMING_END.

HTRIMMING_EN Setting

Name	Address	Bit	Register value	Function	Remarks
HTRIMMMING_EN	300Bh	[4]	0h	Horizontal arbitrary cropping OFF	Send with register setting for each readout drive mode.
			1h	Horizontal arbitrary cropping ON	

Horizontal Arbitrary Cropping Position Setting

Name	Address	Bit	Register value	Remarks
HTRIMMING_START [7:0]	3058h	[7:0]	horizontal cropping start position[*1] + HOST	Unit: pixel Send with register setting for each readout drive mode.
HTRIMMING_START [12:8]	3059h	[4:0]		
HTRIMMING_END [7:0]	305Ah	[7:0]	horizontal cropping end position[*1] + HOST + 1	
HTRIMMING_END [12:8]	305Bh	[4:0]		

[*1] In the readout mode with horizontal binning or subsampling, set the value of HTRIMMING_START and HTRIMMING_END according to the position before processing horizontal binning or subsampling.

HTRIMMING_START and HTRIMMING_END must satisfy following 3 restrictions.

HTRIMMING_START = HOST + N × step
HTRIMMING_END = HOST + HNUM – M × step
HTRIMMING_END – HTRIMMING_START ≥ MinH
(M and N are integers equal or more than 0)

Refer to the following tables in the value of step, HNUM, HOST and MinH every readout mode.

Readout mode No.	Type 1 approx. 20.30 M pixels										Type 1/1.4 approx. 8.42 M pixels
	0	1	1A	1S	2	2A	3	4	5	6	1
step	4						12			8	4
HNUM	5496			3036	5496						3872
HOST	120			656	120						236
MinH	240				480		720			480	240

(2) Horizontal Minimum Period When Using Horizontal Arbitrary Cropping Function

When using horizontal arbitrary cropping function, HMAX minimum period is as follows:

HMAX Minimum Period When Using Horizontal Arbitrary Cropping Function

Readout mode No.		HMAX minimum period
Type 1 approx. 20.30 M pixels	0	887
	1	745
	1A	745
	1S	544
	2	362
	2A	362
	3	284
	4	362
	5	362
	6	364
Type 1/1.4 approx. 8.42 M pixels	1	544

Electronic Shutter Timing

1. SHR, SVR SMD Setting

1-1. SHR, SVR Setting

The exposure start timing can be designated by setting the electronic shutter timing register SHR.
Note that this setting value unit is 1 [HMAX][*1] period regardless of the readout drive mode.
In addition, 1 frame period can be extended at VMAX period unit according to the SVR register.
(1 frame cycle is (SVR value + 1) times as long as VMAX period.)

*1 Setting value of register HMAX × 72MHz clock

Shutter Setting

Name	Address	Bit	Function
SHR [7:0]	303Bh	[7:0]	Specifies the integration start horizontal period
SHR [15:8]	303Ch	[7:0]	
SVR [7:0]	3009h	[7:0]	Specifies the integration shutdown vertical period
SVR [15:8]	300Ah	[7:0]	
HMAX [7:0]	3036h	[7:0]	Horizontal drive period length
HMAX [15:8]	3037h	[7:0]	
VMAX [7:0]	3038h	[7:0]	Vertical drive period length
VMAX [15:8]	3039h	[7:0]	
VMAX [19:16]	303Ah	[3:0]	

Register	Register Value		Function
SHR	11 to {(SVR value + 1) × VMAX value − 4}	Readout mode No.0 All-pixel scan mode (12 bits)	Specifies the integration start horizontal period
	10 to {(SVR value + 1) × VMAX value − 4}	Readout mode No.1, 1A, 1S All-pixel scan mode (10 bits)	
	12 to {(SVR value + 1) × VMAX value − 4 }	Readout mode No.2, 2A, 6 Horizontal/vertical 2/2-line binning (horizontal and vertical weighted binning) Vertical 2 binning horizontal 2/4 subsampling (vertical weighted 2 binning)	
	16 to {(SVR value + 1) × VMAX value − 4 }	Readout mode No.3 Horizontal/vertical 3/3-line binning	
	4 to {(SVR value + 1) × VMAX value − 4 }	Readout mode No.4, 5 Vertical 2/9 subsampling binning horizontal 3 binning cropping Vertical 2/19 subsampling binning horizontal 3 binning	
	0 to {(SVR value + 1) × VMAX value − 130}	Global reset shutter mode (SMD = 1) (12 bits)	
	0 to {(SVR value + 1) × VMAX value − 130}	Global reset shutter mode (SMD = 1) (10 bits)	
SVR	0h to FFFFh *Note 2.		Specifies the integration shutdown vertical period

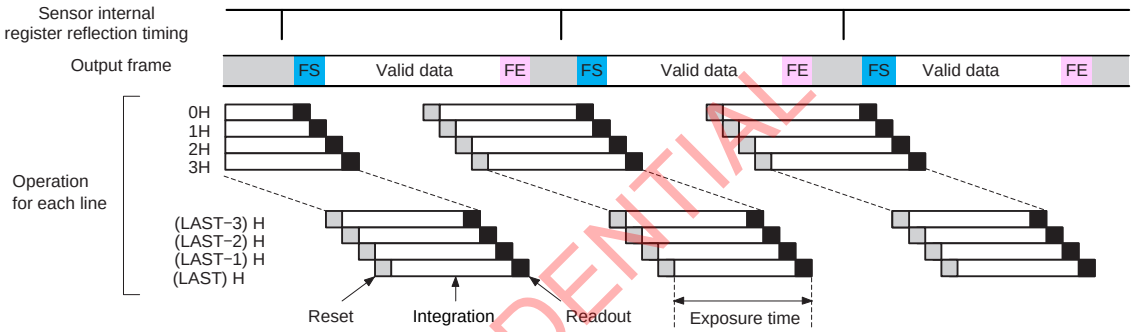
Note)
1. See ”Integration Time in Each Readout Drive Mode” on page 72 for the integration time calculation formula.
2. The SVR register definition areas are guaranteed as sensor functions, but the characteristics are not guaranteed.
3. SMD is the electronic shutter drive mode register (address 3008h, bit [0]).

1-2. Electronic Shutter Drive Mode

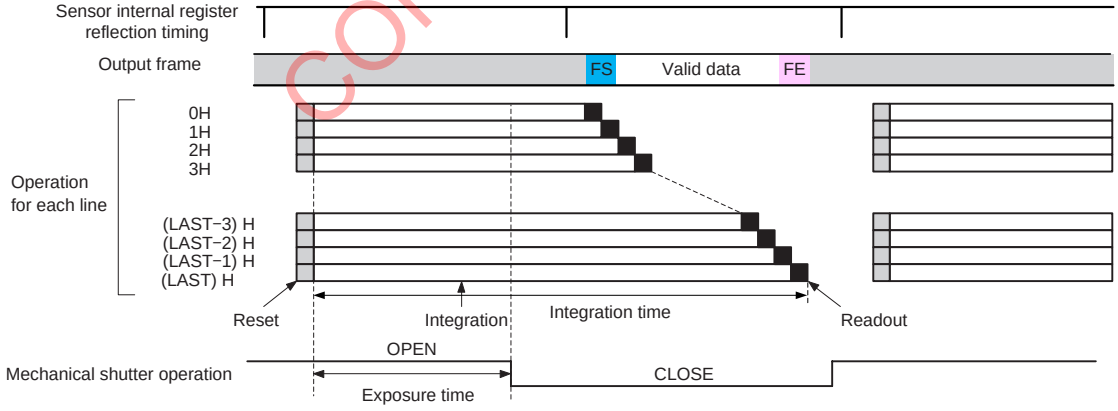
Global reset shutter operation can be performed by setting the electronic shutter drive mode register SMD. Rolling shutter operation performs pixel reset and integration sequentially in line units. Global reset shutter operation resets all pixels at once and then starts integration after that.
("Integration" is the state of a pixel between the reset and the readout. Pixels accumulate all the power of input light.)
The mechanical shutter must also be used during global reset shutter operation to make the exposure time the same for all pixels.
Using XVS output sync signal from sensor as trigger signal is recommended in the case of synchronizing global reset shutter timing of sensor and mechanical shutter timing outside of sensor is needed for fine adjustment of integration time.
Consult your Sony sales representative concerning to use XVS output signal.

SMD Setting

Name	Address	Bit	Register value	Function
SMD	3008h	[0]	0h	Rolling shutter (normal shutter mode)
			1h	Global reset shutter



Rolling Shutter Operation



Global Reset Shutter Operation

2. Integration Time in Each Readout Drive Mode and Mode Changes

2-1. Integration Time in Each Readout Drive Mode

The integration time for this sensor's output data is set using the electronic shutter timing setting registers SHR and SVR. The formulas and constants used to calculate the integration time are shown below.
In addition, the frame rate can be reduced by setting the SVR register to “1” or more.

◆ Integration time of normal readout drive mode

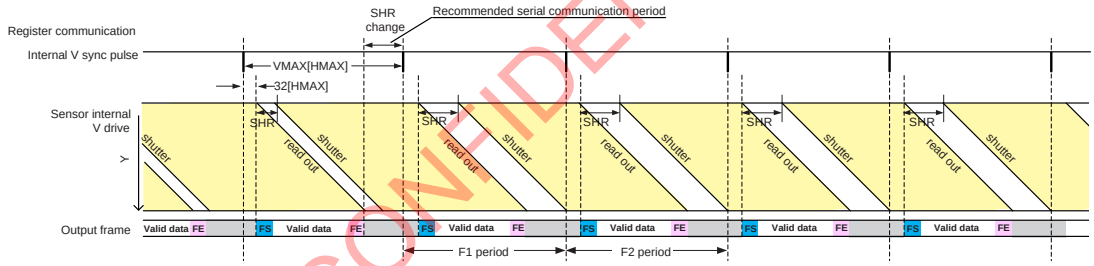
Integration Time [s] = [{VMAX value × (SVR value + 1) – (SHR value)}
× HMAX value + Number of clocks per internal offset period] / (72×10^6)

* See the following tables for the numbers of clocks per internal offset period.
* See “1-1. SHR, SVR Setting” on page 70 for the SHR register setting range.

Number of clocks per internal offset period

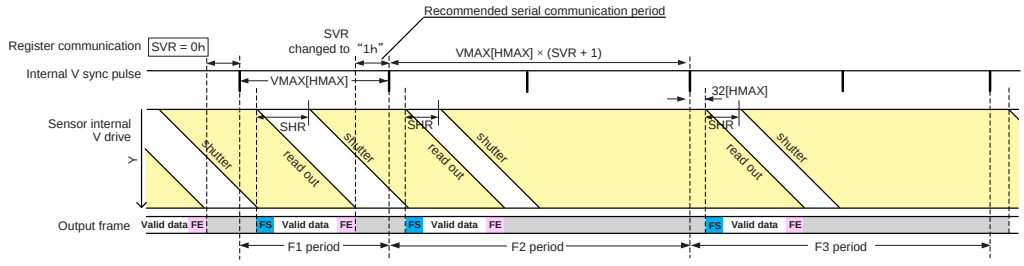
Readout mode No.	0	1	1A	1S	2	2A	3	4	5	6
Number of clocks per internal offset period	209	157	157	157	157	157	135	157	157	157

The figure below shows operation when SHR is being changed and REGHOLD is 0h. The F1 and F2 periods in the figure below are two continuous frames. The SHR value which is set in the recommended serial communication period[*1] just before F1 period is updated internally at the end of the communication period and then output data which reflect the new setting is output in the F2 period. Note that the SHR setting and output are offset by a frame.
[*1] Refer to "Register Communication Timing".



SHR Change Sequence

The internal vertical drive period which is set by the VMAX register can be subsampled by the SVR register. Its period is (SVR value + 1) times as long as VMAX period. Therefore the frame rate is multiplied by 1/ (SVR value + 1).
The figure below shows the operation when the SVR register is being changed from “0h” to “1h” and REGHOLD is 0h. The SVR value, which is set in the recommended serial communication period[*1] just before F2 period, is updated internally at the end of the communication period and then applied from the shutter operation in the F2 period. The output data which reflect the changing of SVR is output in the F3 period.
The image data of the F1 period before the SVR value is changed is output as valid data in the F2 period.
[*1] Refer to "Register Communication Timing".



SVR Change Sequence

2-2. Operation when Changing the Readout Drive Mode

When changing input INCK or CSI-2 output frequency, follow the below procedure.

1st step: Enter the sensor standby mode
2nd step: Change the frequency during standby mode.
3rd step: Follow the standby cancel sequence to resume the normal operation.

When changing input INCK frequency, don't input pulses whose width are shorter than the High / Low level width in front and behind of the INCK pulse at the frequency change. If the pulses above generate at the frequency change, change INCK frequency during system reset in the state of XCLR = Low. Then set the state of XCLR to High, following the item of "Power on sequence" in the section of "Power on / off sequence" in pages 75 to 76. Execute “Standby Cancel Sequence” again because the register settings become default state after system reset.

The following mode change cases are treated as a mode transition on this sensor and one frame of invalid data is generated.

1. Changing the readout mode setting
2. Changing the vertical direction readout setting
3. Changing the vertical arbitrary cropping setting

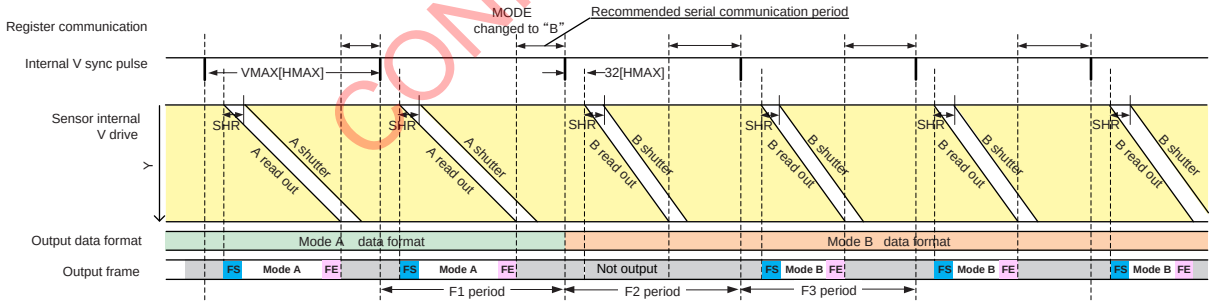
* Changing the horizontal arbitrary cropping setting is not treated as mode transition and no invalid data is generated.

The figure below shows the mode transition sequence, Mode A to Mode B, in case that the mode transition is performed in three continuous frames, F1 to F3, and REGHOLD is 0h.

(1) Set the register setting for Mode B in the recommended serial communication period[*1] just before F2 period. The F2 period data is not output.
(2) Valid data which reflect the new setting is output from the next frame (F3 period).

[*1] Refer to "Register Communication Timing"

In addition, note that when the output data length differs between Mode A and Mode B, the new data format is output from the start of F2 period in which the setting is changed to Mode B.

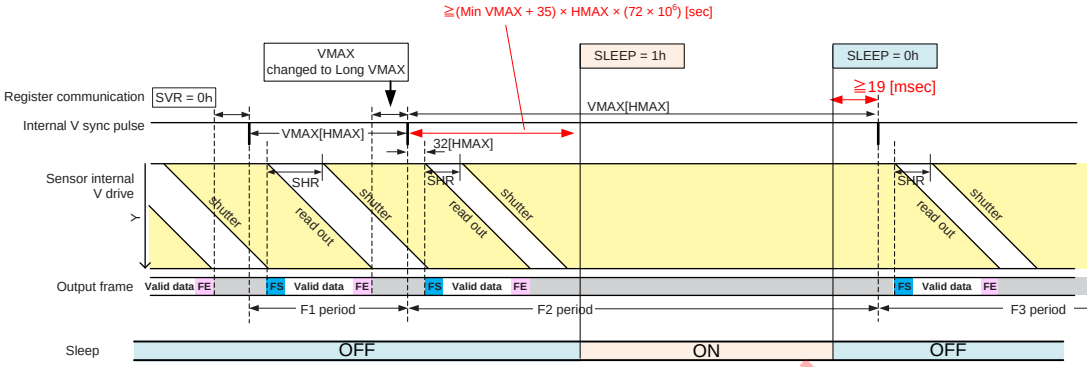


Mode Transition

2-3. Low Power Consumption Drive in Integration Time When Using Rolling Shutter Operation

To extend the integration time, VMAX register is available other than SVR register. VMAX register extends V period. SLEEP register can reduce power consumption during integration time when using large VMAX. To change to low power consumption drive, set SLEEP register to 1h after (VMAX value + 35) × HMAX value × (72 x 10^6) [sec] or more in the frame of changing the register SMD from 0h to 1h.
And for readout, set SLEEP to 0h before 19 ms of readout frame in order to cancel low power consumption mode.

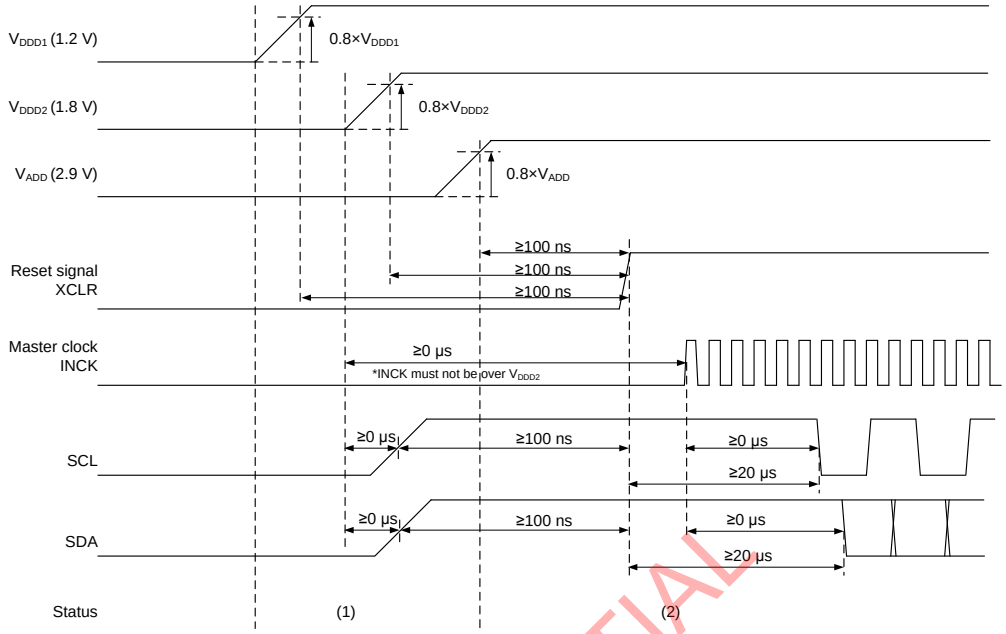
When using SVR ≥ 1h, this sequence is not necessary.



Low Power Consumption Drive in Integration Time When Using Rolling Shutter Operation

Power-on/off Sequence

1. Power-on Sequence

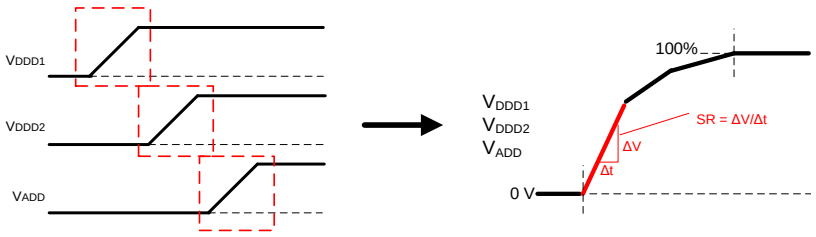


Power-on Sequence

Period name	Remarks
(1) Power stabilization period	All input signals are set to Low level. There are no constraints of the power-on sequence with V_{ADD}, V_{DDD1}, and V_{DDD2}.
(2) Register communication period for standby cancel	Wait 100 ns after the last power supply in V_{ADD}, V_{DDD1} and V_{DDD2}. Then set XCLR to “H” and start the standby cancel sequence.

2. Slew Rate Limitation of Power-on Sequence

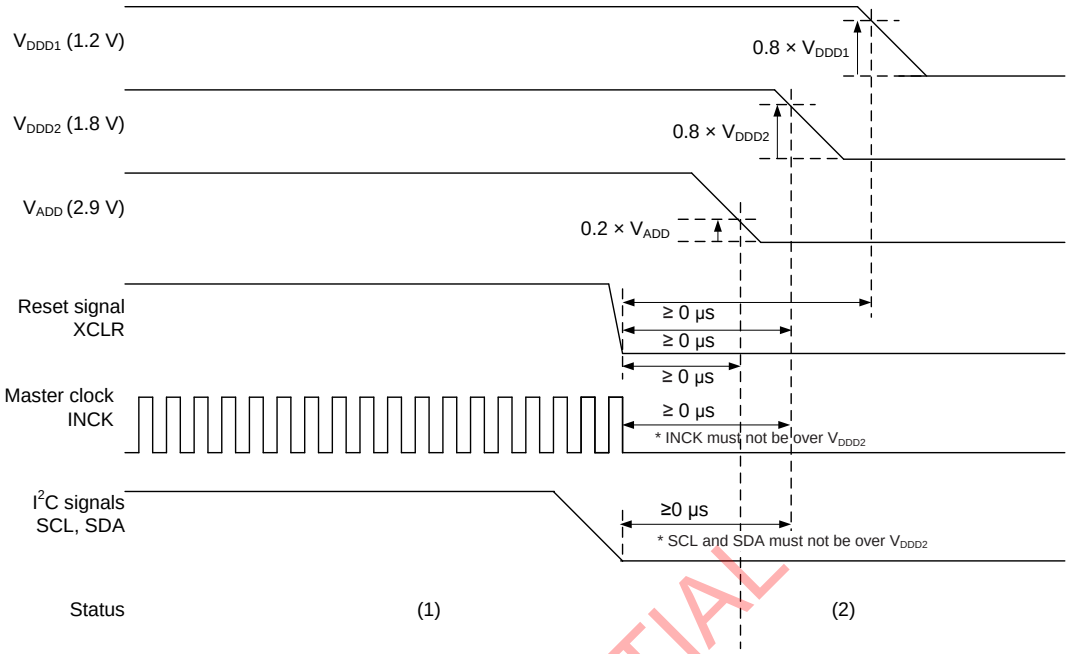
Conform to the slew rate limitation shown below when power supply change 0 V to each voltage (0 % to 100 %) in power-on sequence.



Item	Symbol	Power supply	Min.	Max.	Unit	Remarks
Slew rate	SR	V_{DDD1} (1.2 V)	—	25	mV/µs	
		V_{DDD2} (1.8 V)	—	25	mV/µs	
		V_{ADD} (2.9 V)	—	25	mV/µs	

3. Power-off Sequence

Make sure that all input signals are set to LOW level in the area of (2).



Power-off Sequence (CSI-2)

Period name	Remarks
(1) Pixel output period	Pixel signal output period
(2) Power-off period	Turn the power supplies off after all input signals are set to "Low" level except SCL and SDA. Set SCL and SDA to "Low" level at the same time with turning off the power supply of V_{DDD2}. There are no constraints of the power-off sequence with V_{ADD}, V_{DDD1}, and V_{DDD2}.

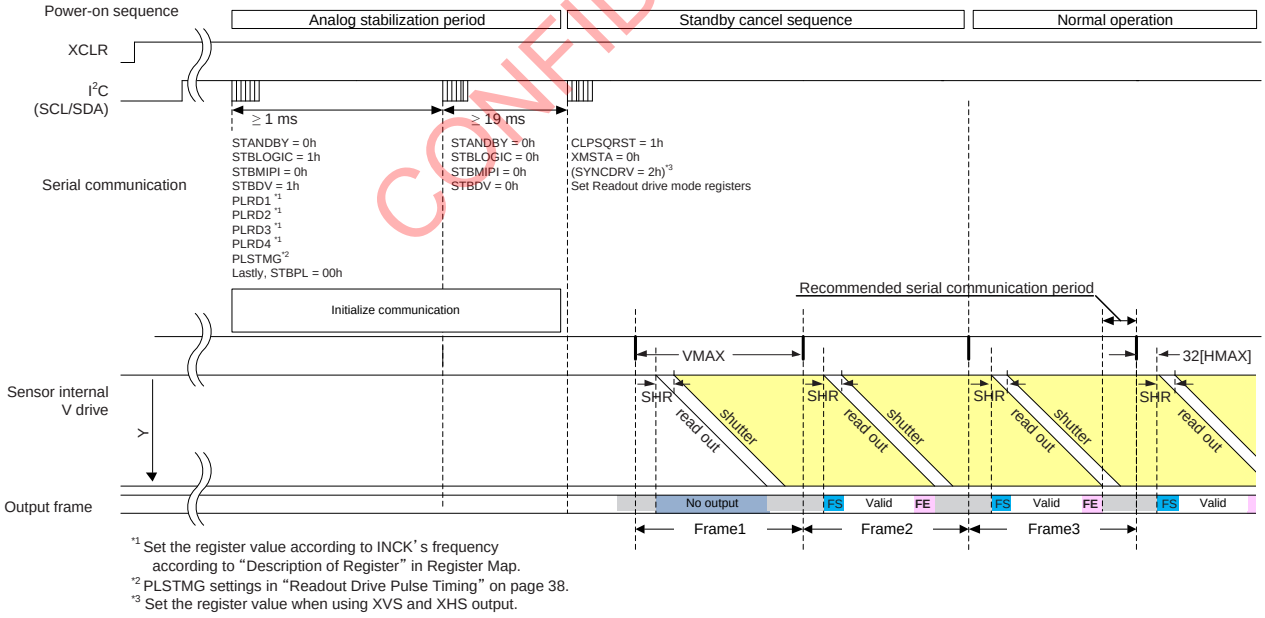
Standby Cancel Sequence

After the power-on start-up sequence is performed, this sensor is in standby mode. The standby cancel sequence is described below. Also perform this same sequence when canceling standby mode after shifting from normal operation to standby mode.

1. After performing the power-on start-up sequence, make the following register setting in listed order.
   - Set address 3000h, bit [3:0] to “Ah” (STANDBY register = 0h, STBLOGIC register = 1h, STBMIPI register = 0h, STBDV register = 1h).
   - Set the following registers to the appropriate value according to INCK’s frequency.
     Refer to “Input Frequency Setting” of “1. Description of Register” on page 34.
     Address 36C1h, bit [7:0] (PLRD1 register)
     Address 36C2h, bit [7:0], Address 36C3h, bit [7:0] (PLRD2 register)
     Address 36F7h, bit [7:0] (PLRD3 register)
     Address 36F8h, bit [7:0] (PLRD4 register)
   - Initialize communication
     Set all registers of PLSTMG settings in "Readout Drive Pulse Timing" on page 38.
   After Initial communication
   -Set address 320Bh, bit[7:0] to “00h” (STBPL register = 00h)

2. After the 1st stabilization period of 1 ms or more, make the following register setting.
   - Set address 3000h, bit [3:0] to “00h” (STANDBY register = 0h, STBLOGIC register = 0h, STBMIPI register = 0h, STBDV register = 0h).

3. After the 2nd stabilization period of 19ms or more,
   - Set address 3001h, bit[4] to “1h” (CLPSQRST = 1h)
   - Set address 3105h, bit [0] to “0h” (XMSTA =0h).
   - Set address 3107h, bit [1:0] to “2h” (SYNCDRV =2h) (when using XHS and XVS output)
   - Set the mode registers of the “Register Setting for Each Readout Drive Mode” on pages 39 to 42.
     Furthermore, set the required shutter and gain registers.



*1 Set the register value according to INCK’s frequency according to “Description of Register” in Register Map.
*2 PLSTMG settings in “Readout Drive Pulse Timing” on page 38.
*3 Set the register value when using XVS and XHS output.

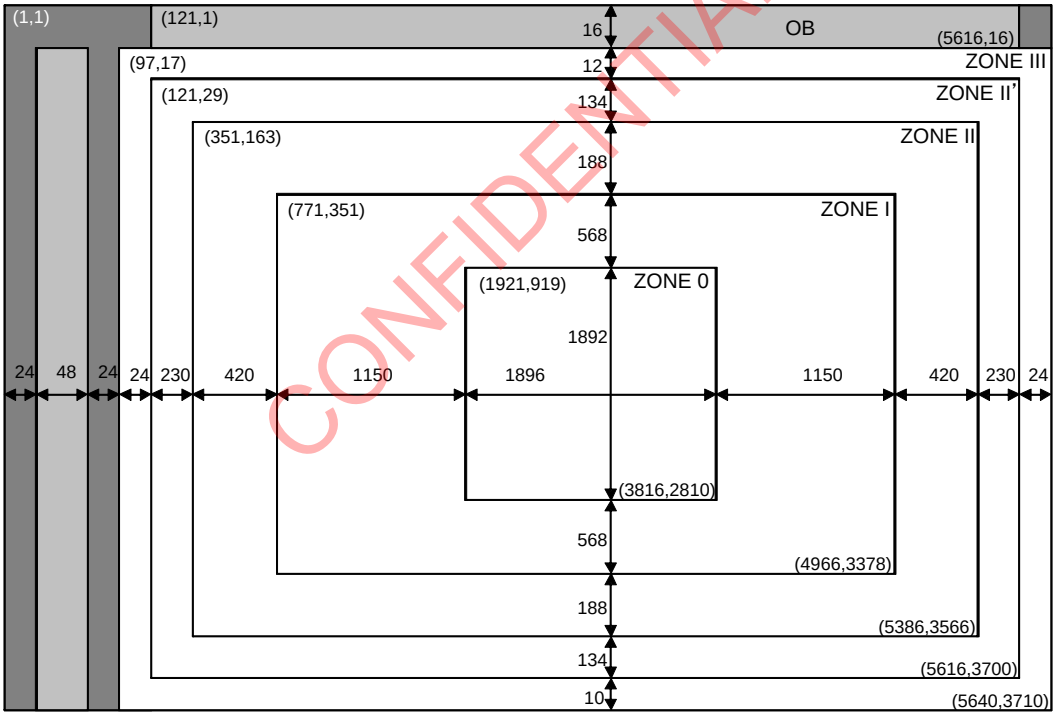
Spot Pixel Specifications

(V_{ADD} = 2.9 V, V_{DDD1} = 1.2 V, V_{DDD2} = 1.8 V, Tj = 60 ˚C, 19.98 frame/s, reference gain 0 dB)

Type of distortion	Level	Maximum distorted pixels in each zone						Measure-ment method	Remarks
		0	I	II	II'	OB	III		
Black pixels at high light	30 % ≤ D	A[*1]				No evaluation criteria applied		1	
White pixels at high light	30 % ≤ D					No evaluation criteria applied		1	
White pixels in the dark	32.7 digit ≤ D	B[*1]					No evaluation criteria applied	2	1/30 s integration
Black pixels at signal saturated	D ≤ 2676 digit	C[*1]				No evaluation criteria applied		3	

Note) 1. Spec of the sum of A, B and C is 4000 pixels.
2. D...Spot pixel level. Black pixels at signal saturated are prescribed at the signal output in spot pixel part.
3. Zone definition is illustrated in the figure below.
4. 1 digit ≈ 0.2465 mV when 12 bits output.

Spot Pixel Zone Definition



Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, particle radiation such as cosmic rays etc. may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".)
Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Semiconductor Solutions Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Semiconductor Solutions Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of storage time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
4.0 mV or higher	97.0 pcs
5.6 mV or higher	70.0 pcs
8.1 mV or higher	48.0 pcs
10.0 mV or higher	39.0 pcs
24.0 mV or higher	16.0 pcs
50.0 mV or higher	8.0 pcs
72.0 mV or higher	5.0 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

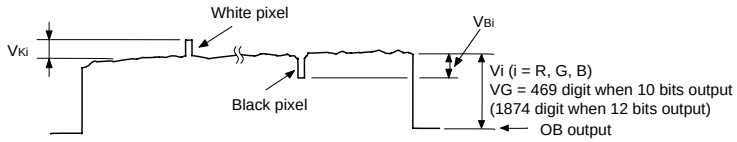
Material_No.03-0.0.10

Measurement Method for Spot Pixels

1. Black or white pixels at high light

After adjusting the luminous intensity so that the average value of the G channel signal output is 469 digit when 10 bits output (1874 digit when 12 bits output), measure the local dip point (black pixel at high light, V_{BR}, V_{BG} and V_{BB}) and peak point (white pixel at high light, V_{KR}, V_{KG} and V_{KB}) in each channel signal output. Substitute the values into the following formula.

Spot pixel level = (V_{Ki} (or) V_{Bi})/V_i × 100 [%] (i = R, G, B)



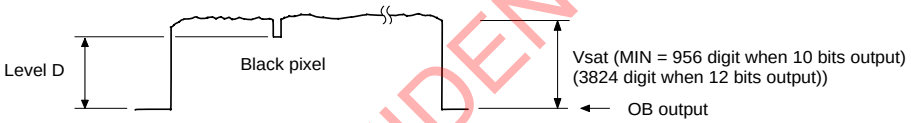
Signal output waveform of R/G/B channel (Black or White Pixels at High Light)

2. White pixels in the dark

Set the device to a dark setting and measure the local peak point of the signal output waveform using the average value of the dark signal output as a reference.

3. Black pixels at signal saturated

Set the device to operate in saturation and measure the local dip point in each of the R, G and B channels using the OB output with sensor as a reference.



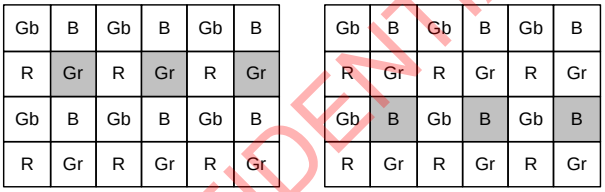
Signal output waveform of R/G/B channel (Black Pixels at Signal Saturated)

Spot Pixel Pattern Specifications

For patterns of white pixels in the dark (32.7 digit ≤ D), Black pixels at signal saturated (D ≤ 2676 digit), white pixels at high light (30 % ≤ D) and black pixels at high light (30 % ≤ D), the following table is applied.

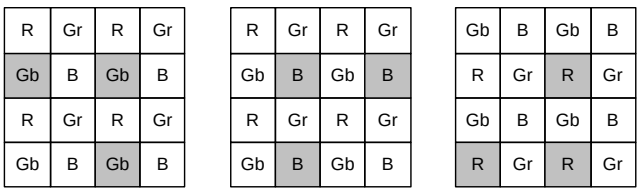
Type of distortion	Maximum distorted pixels in each zone						Remarks
	0	I	II	II'	OB	III	
(1) Three adjacent pixels in the horizontal direction with the same color	0 spot				No evaluation criteria applied		
(2) Three adjacent pixels in the vertical direction with the same color	0 spot				No evaluation criteria applied		
(3) Two adjacent pixels in the horizontal and two adjacent pixels in the vertical with the same color	0 spot				No evaluation criteria applied		

(1) Example of three adjacent pixels in the horizontal direction with the same color



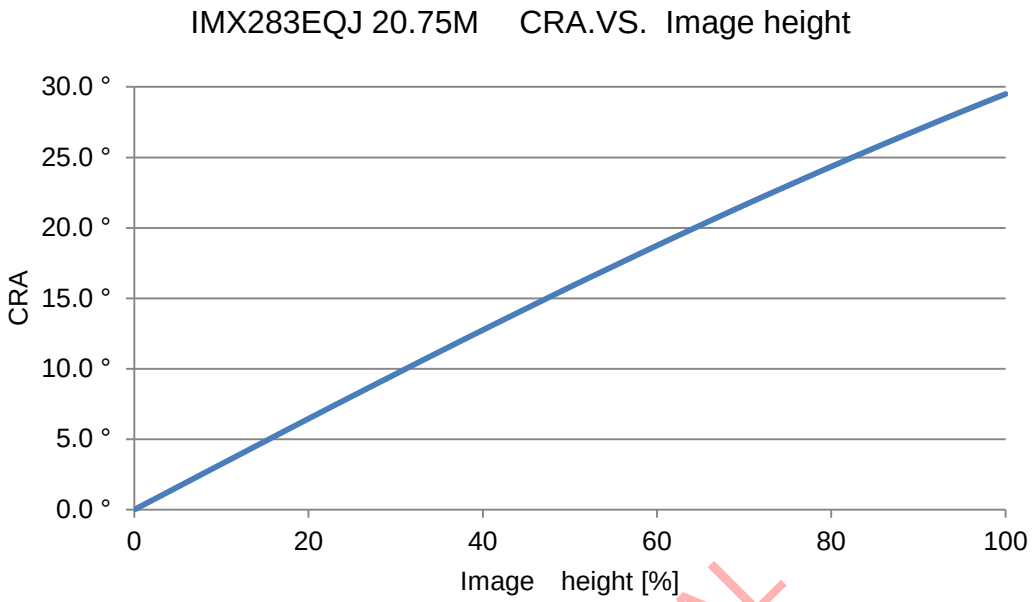
(2) Example of three adjacent pixels in the vertical direction with the same color

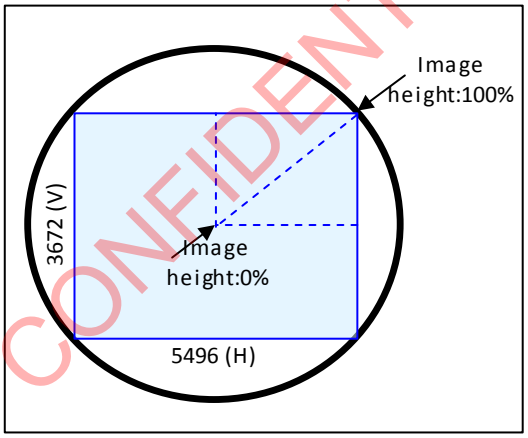
(3) Example of two adjacent pixels in the horizontal and two adjacent pixels in the vertical with the same color

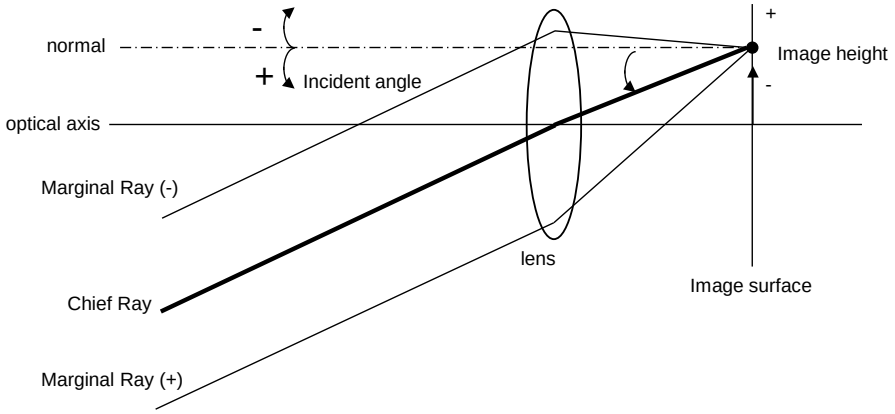


indicates spot pixels

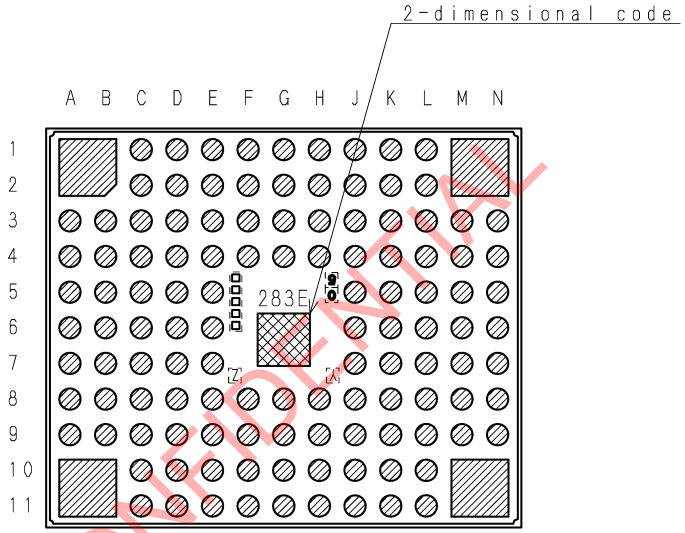
Relation between Image Height and target CRA







Marking



Note:Following characters enter into "Y", and "Z". (No Au coat)
Y:In English upper case character, One character
Z:Number, single number

DRAWING No. AM-Z283EQJ(2D)

Notes on Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

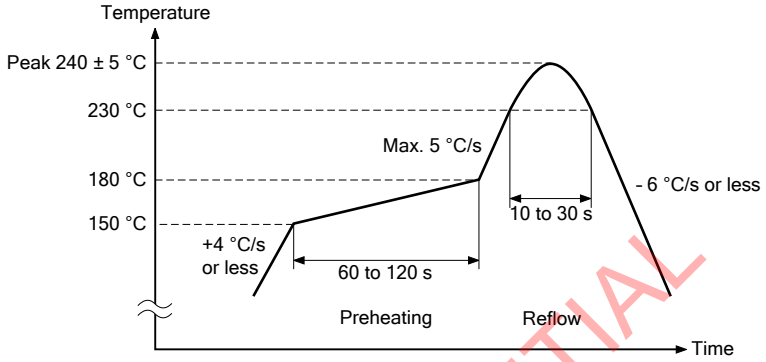
(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (- 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.

(b) Perform the reflow soldering only one time.

(c) Finish reflow soldering within 72 h after unsealing the degassed packing. Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.

(d) Perform re-baking only one time under the condition at 125 °C for 24 h.

(3) Others

(a) Carry out evaluation for the solder joint reliability in your company.

(b) After the reflow, the paste residue of protective tape may remain around the seal glass. (The paste residue of protective tape should be ignored except remarkable one.)

(c) Note that X-ray inspection may damage characteristics of the sensor.

5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.

(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.

(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.

(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.

(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

Material_No.14-0.0.6

Package Outline

(Unit: mm)