

## **TEB0707 TRM**

Revision v.45
Exported on 2020-11-25

Online version of this document:



# 1 Table of Contents

1	Table of Contents	2
2	Table of Figures	4
3	Table of Tables	5
4	Overview	6
4.1	Key Features	6
4.2	Block Diagram	6
4.3	Main Components	8
4.4	Initial Delivery State	9
4.5	Configuration Signals	9
5	Signals, Interfaces and Pins	11
5.1	Board to Board (B2B)	11
5.2	CRUVI B2B Connectors	12
5.3	JTAG Interface	13
5.4	SD Card socket	14
5.5	Micro USB2.0 Socket	15
5.6	USB A Socket	15
5.7	RJ45 LAN Socket	15
5.8	Jumpers	16
5.9	Pin Header	16
5.10	Test Points	16
6	On-board Peripherals	18
6.1	Intel Max10 CPLD	18
6.2	FTDI FT2232H	18
6.3	LEDs	19
6.4	EEPROM	20
6.5	DIP Switch	20
6.6	Push Buttons	20
6.7	Clock Sources	21
7	Power and Power-On Sequence	22
7.1	Power Supply	22
7.2	Power Consumption	22
7.3	Power Distribution Dependencies	23
7.4	Power-On Sequence	24
7.5	Power Rails	25
7.6	Bank Voltages	26





8	Board to Board Connectors	27
8.1	Connector Mating height	27
8.2	Connector Speed Ratings	28
8.3	Current Rating	28
8.4	Connector Mechanical Ratings	28
9	CRUVI Connectors	29
9.1	Connector Mating height	27
9.2	Current Rating	28
9.3	Speed Rating	29
9.4	Operating Temp Range	29
10	Technical Specifications	30
10.1	Absolute Maximum Ratings	30
10.2	Recommended Operating Conditions	30
10.3	Physical Dimensions	30
11	Currently Offered Variants	32
12	Revision History	33
12.1	Hardware Revision History	33
12.2	Document Change History	33
13	Disclaimer	34
13.1	Data Privacy	34
13.2	Document Warranty	34
13.3	Limitation of Liability	34
13.4	Copyright Notice	34
13.5	Technology Licenses	34
13.6	Environmental Protection	34
13.7	REACH, RoHS and WEEE	35





# 2 Table of Figures

Figure 1: TEB0707 block diagram	7
Figure 2: TEB0707 main components	
Figure 3: Power Distribution	23
Figure 4: Power Sequency	25
Figure 5: Physical Dimension	31
Figure 6: Board hardware revision number	33



# 3 Table of Tables

Table 1:	Initial delivery state of programmable devices on the module	<u>c</u>
Table 2:	Boot process	<u>c</u>
Table 3:	Reset process.	10
Table 4:	General PL I/O to B2B connectors information	11
Table 5:	CRUVI B2B connectors information	12
Table 6:	JTAG pins connection	14
Table 7:	JTAG pins connection	14
Table 8:	USB2.0 Socket information	14
Table 9:	Micro USB2.0 Socket information	15
Table 10:	USB A Socket information	15
Table 11:	RJ45 LAN Socket information	15
Table 12:	Jumpers information	16
Table 13:	Jumpers information	16
Table 14:	Test Points Information	17
Table 15:	On board peripherals	18
Table 16:	FTDI chip interfaces and pins	18
Table 17:	On-board LEDs	19
Table 18:	I2C EEPROM interface MIOs and pins	20
Table 19:	DIP Switch connections	20
Table 20:	Push Buttons informations	21
Table 21:	Osillators	21
Table 22:	Power Consumption	22
Table 23:	Module power rails	26
Table 24:	Zynq SoC bank voltages.	26
Table 25:	Connectors.	27
Table 26:	Speed rating.	28
Table 27:	Connector speed ratings	29
Table 28:	PS absolute maximum ratings	30
Table 29:	Recommended operating conditions.	30
Table 30:	Trenz Electronic Shop Overview	32
Table 31:	Hardware Revision History	33
Table 32:	Document change history.	33

#### 4 Overview

The Trenz Electronic TEB0707 is a carrier for 4 x 5 Trenz Electronic modules. It provides three high speed and one low speed CRUVI extension connectors. For more information, please refer to the CRUVI B2B Connectors<sup>1</sup>. The TEB0707 is integrated with an Intel MAX10 FPGA as system controller and is equipped with a Micro USB2.0 Socket with FTDI to JTAG/UART solution, RJ45 LAN Socket, USB A Socket, Micro SD Card Socket, User LEDs, Push Buttons and DIP Switches for controlling the SoM.

Refer to http://trenz.org/teb0707-info for the current online version of this manual and other available documentation.

### 4.1 Key Features

- Modules
  - · 4x5 Trenz Electronic modules
- RAM/Storage
  - EEPROM (FTDI Configuration)
- · On Board
  - Intel Max 10 FPGA
  - FTDI FT2223
  - 6x User LEDs (3x green, 3x red)
  - · 2x Status LED
  - · DIP Switch
  - · Push Buttons
- Interface
  - · Gigabit RJ45 LAN socket
  - SD Card socket
  - · Micro USB2.0 Socket
  - USB A Socket
  - 3x High Speed CRUVI B2B Connectors
  - 1x Low Speed CRUVI B2B Connector
  - 4x Jumpers
- Power
  - 5V Input Power Supply
- Dimension
  - 135 x 68 mm
- Notes

## 4.2 Block Diagram

<sup>1</sup> https://wiki.trenz-electronic.de/display/DRAFT/CRUVI+B2B+Connectors



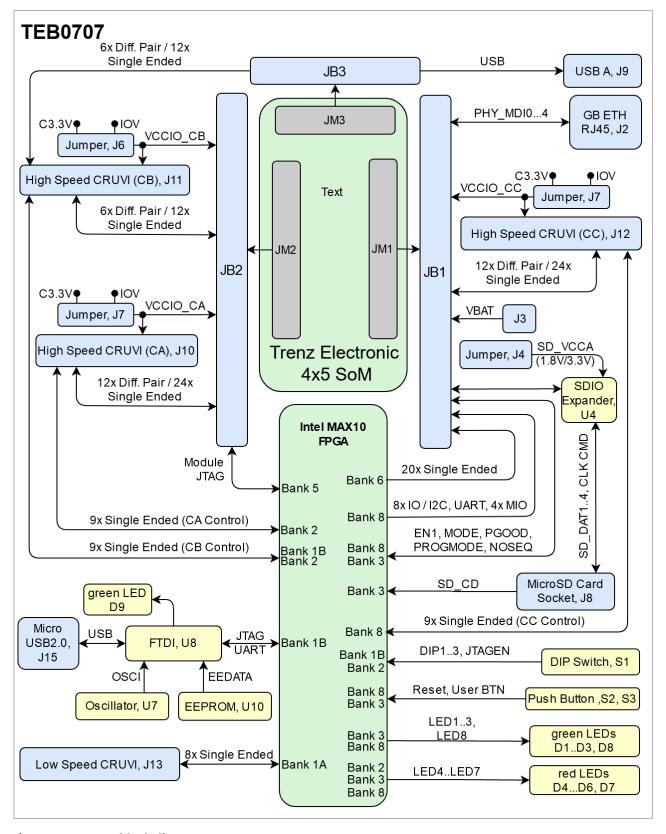


Figure 1: TEB0707 block diagram



## 4.3 Main Components

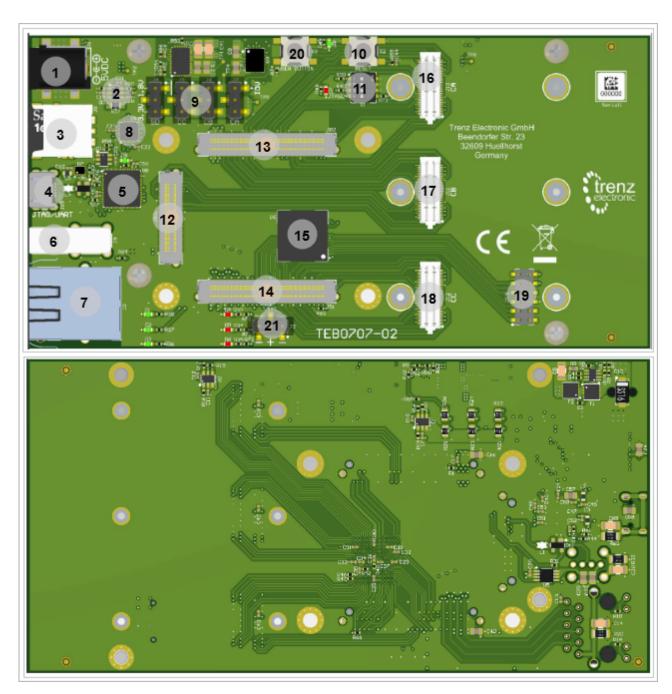


Figure 2: TEB0707 main components

- 1. Barrel Jack Power Supply, J1
- 2. Voltage Regulator, U1
- 3. Micro SD Card Socket, J8
- 4. Micro USB2.0 Socket, J15
- 5. FT2232H FTDI, U8
- 6. USB A Socket, J9
- 7. RJ45 LAN Socket, J2



- 8. SDIO Port Expander, U4
- 9. Jumpers, J4...7
- 10. Push Button (Reset), S2
- 11. DIP Switch, S1
- 12. B2B Connector, JB3
- 13. B2B Connector, JB2
- 14. B2B Connector, JB1
- 15. Intel MAX 10 FPGA, U6
- 16. High Speed CRUVI Connector, J10
- 17. High Speed CRUVI Connector, J11
- 18. High Speed CRUVI Connector, J12
- 19. Low Speed CRUVI Connector, J13
- 20. User Push Button, S3
- 21. Pin header, J3

## 4.4 Initial Delivery State

Storage device name	Content	Notes
EEPROM	Programmed	FTDI Configuration

Table 1: Initial delivery state of programmable devices on the module

## 4.5 Configuration Signals

MODE Signal State	Boot Mode
MODE	Boot Mode:  • SD Card (Low)  • QSPI (High)
PROGMODE	<ul> <li>Programming Mode:</li> <li>select between CPLD (low, closed, on)</li> <li>on SoM or FPGA/SoC (high, open, off)</li> </ul>

Table 2: Boot process.



Signal	Connected to	I/O	Note
Reset	Push Button, S2	Out	Module Reset signal

Table 3: Reset process.



# 5 Signals, Interfaces and Pins

## 5.1 Board to Board (B2B)

Interfaces and Number of I/O signals connected to the B2B connectors for Trenz 4x5 modules:

B2B Connec tor	Interface	I/O Signal Count	Connected to	Notes
JB1	Ethernet LAN	4x Diff pairs	RJ45 Socket, J2	
	SD Card	6 x Single Ended	IO Expander, U4	
	I/Os	20x Single Ended	MAX10 FPGA Bank 6, U6	
	CRUVI	12x Diff pairs/24x Single ended 4x Single Ended	High Speed CRUVI, J12	CRUVI C
	SoM Control Signals	5x Single Ended	MAX10 FPGA, U6	
	I/Os	8x Single ended	MAX10 FPGA Bank 8, U6	
JB2	CRUVI	12x Diff pairs/24x Single ended 4x Single Ended	High Speed CRUVI, J10	CRUVI A
	CRUVI	6x Diff pairs/12x Single ended	High Speed CRUVI, J11	CRUVI B
	JTAG	4x Single Ended	FPGA Bank 5, U6	
JB3	CRUVI	6x Diff pairs/12x Single ended 4x Single Ended	High Speed CRUVI, J11	CRUVI B



B2B Connec tor	Interface	I/O Signal Count	Connected to	Notes
	USB	1x Diff pair, 2x Single Ended	USB A, J9	

Table 4: General PL I/O to B2B connectors information

### 5.2 CRUVI B2B Connectors

The TEMB0707 is equipped with a Low Speed Connectors J 13 and three High Speed Connector J10...12. These connectors are provided for CRUVI extension cards. More information is provided in the B2B Connectors(see page 0) section.

Speed	Designators	Schematic	Connected to	Notes
High	CRUVI C, J12	A0A5 (N/ P)	B2B, JB1	
		B0B5 (N/ P)	B2B, JB1	
		MODE, REFCLK, SMB_ALERT , SMB_SDA, SMB_SCL, SEL, DO, DI, SCK	MAX10 FPGA Bank 8, U6	3.3V User IOs (Max10 Firmware dependent)
		HSIO, HI, HO, RESET	B2B, JB1	
High	CRUVI B, J11	A0A5 (N/ P)	B2B, JB1	
		B0B5 (N/ P)	B2B, JB1	



Speed	Designators	Schematic	Connected to	Notes
		MODE, REFCLK, SMB_ALERT, SMB_SDA, SMB_SCL, SEL, DO, DI, SCK	MAX10 FPGA Bank 2/3, U6	3.3V User IOs (Max10 Firmware dependent)
		HSIO, HSI, HSO, RESET	B2B, JB3	
High	CRUVI A, J13	A0A5 (N/ P)	B2B, JB2	
		B0B5 (N/ P)	B2B, JB2	
		MODE, REFCLK, SMB_ALERT, SMB_SDA, SMB_SCL, SEL, DO, DI, SCK	MAX10 FPGA Bank 2/3, U6	3.3V User IOs (Max10 Firmware dependent)
		HSIO, HSI, HSO, RESET	B2B, JB2	
Low	CRUVI	X0X7	MAX10 FPGA Bank 1A, U6	

Table 5: CRUVI B2B connectors information

### 5.3

### JTAG Interface

JTAG signals form FTDI U8 are routed to MAX10 CPLD. Via dip setting JTAG of MAX10 or JTAG of the connected Trenz 4x5 module can be selected. Forwarding signals to SoM is MAX10 Firmware dependent.



JTAG Signal	MAX10 Pin Bank 1B, U6	Connected to
TMS	G1	FTDI (U8) - ADBUS3
TDI	F5	FTDI (U8) - ADBUS1
TDO	F6	FTDI (U8) - ADBUS2
тск	G2	FTDI (U8) - ADBUS0
JTAGEN	E5	Dip S1-4

#### Table 6: JTAG pins connection

JTAG access to the Trenz 4x5 module is through B2B connector JB2.

JTAG Signal	MAX10 Pin Bank5, U6	B2B Connector
M_TMS	L12	JB2-94
M_TDI	L13	JB2-96
M_TDO	J10	JB2-100
M_TCK	Н8	JB2-98
VCCJTAG	J11, J12	JB2-92

Table 7: JTAG pins connection

### 5.4 SD Card socket

The TEB0707 is equipped with an Micro SD Card slot, J8. For levelshifting an IO Expander (U4) is used.

Pin	Schematic	Connected to	Notes
DAT03	ESD_DAT03	B2B, JB1	Through IO Expander, U4
CMD	ESD_CMD	B2B, JB1	Through IO Expander, U4
VDD	3.3V_SD	B2B, JB1	Through IO Expander, U4
CLK	ESD_CLK	B2B, JB1	Through IO Expander, U4



Revision: v.45 TEB0707 TRM

Pin	Schematic	Connected to	Notes
DLT	SD_CD	FPGA Bank 3, U6	Card detect.

**Table 8: USB2.0 Socket information** 

### 5.5 Micro USB2.0 Socket

There is a micro USB2.0 Socket, J15 provided in order to communicate with the FTDI, U8.

Pin	Schematic	Connected to	Notes
D+	O2-D_P	B2B, JB3	Through Line Filter, L4
D-	O2-D_N	B2B, JB3	Through Line Filter, L4
Vbus	VBUS	B2B, JB3	

**Table 9: Micro USB2.0 Socket information** 

### 5.6 USB A Socket

The SoM USB 2.0 signals are routed to a USB A socket (host).

Pin	Schematic	Connected to	Notes
Data+	O2-D_P	B2B, JB3	Through Line Filter, L1
Data-	02-D_N	B2B, JB3	Through Line Filter, L1
VCC	USB_VBUS	B2B, JB3	

#### **Table 10: USB A Socket information**

### 5.7 RJ45 LAN Socket

There is a RJ45 Ethernet LAN MagJack, J2 connected to B2B, JB1.

Pin	Schematic	Connected to	Notes
2	PHY_MDI0_P	B2B, JB1	
3	PHY_MDI0_N	B2B, JB1	
4	PHY_MDI1_P	B2B, JB1	



Pin	Schematic	Connected to	Notes
5	PHY_MDI1_N	B2B, JB1	
6	PHY_MDI2_P	B2B, JB1	
7	PHY_MDI2_N	B2B, JB1	
8	PHY_MDI3_P	B2B, JB1	
9	PHY_MDI3_N	B2B, JB1	
VCC	ETH-VCC	B2B, JB1	
Green LED	ETH1_LED0	Intel MAX 10, U6	MAX10 Firmware dependent
Yellow LED	ETH1_LED1	Intel MAX 10, U6	MAX10 Firmware dependent

Table 11: RJ45 LAN Socket information

## 5.8 Jumpers

There are three Jumpers provided to choose the CRUVI Extension power voltage.

Designator	Schematic	Connected to	Notes
J14	VCCIO_CC	B2B, JB2	CRUVI C
J16	VCCIO_CB	B2B, JB2	CRUVI B
J17	VCCIO_CA	B2B, JB2	CRUVI A

**Table 12: Jumpers information** 

## 5.9 Pin Header

Designator	Schematic	Connected to	Notes
J3	VBAT	B2B, JB1	

**Table 13: Jumpers information** 

### 5.10 Test Points



Test Point	Signal	Connected to	Notes
TP1	3.3V	Regulator, U1	
TP2	VIN	Voltage Protection, U2	
TP4	IOV	Regulator, U3	
TP5	3.3V	Power Switch, Q1	
TP6	C5VIN	Power Switch, Q2	

**Table 14: Test Points Information** 



## 6 On-board Peripherals

Chip/Interface	Designator	Notes
Intel MAX 10(see page 0)	U6	
FTDI(see page 18)	U8	
EEPROM(see page 20)	U10	FTDI, programmed with Xilinx licence
Oscillator(see page 21)	U7	
LEDS(see page 19)	D18	
DIP Switch(see page 20)	S1	
Push Buttons(see page 20)	S2, S3	

Table 15: On board peripherals

#### 6.1 Intel Max10 CPLD

The TEB0707 is quipped with an Intel Max10 as CPLD used for levelshifting of 3.3V signals on CRUVI connectors, JTAG/UART forward to modules, Module control pis, power sequencing and IO voltage selection along with providing User Push buttons, LEDs and switches. For complete information, please see the TEB0707 MAX10 CPLD<sup>2</sup>.

#### 6.2 FTDI FT2232H

The FTDI chip (U8) converts signals from USB2 to variety of standard serial and parallel interfaces. Refer to the FTDI data sheet<sup>3</sup> to get information about the capacity of the FT2232H chip which is used in Multi-Protocol Synchronous Serial Engine (MPPSE) mode for JTAG.

The configuration of FTDI FT2232H chip is pre-programmed on the EEPROM U10.

Pin	Schematic	Connected to	Notes
ADBUS0	TCK	FPGA Bank 1B, U6	JTAG interface
ADBUS1	TDI	FPGA Bank 1B, U6	
ADBUS2	TDO	FPGA Bank 1B, U6	
ADBUS3	TMS	FPGA Bank 1B, U6	

<sup>2</sup> https://wiki.trenz-electronic.de/display/PD/TEB0707+MAX10+CPLD

<sup>3</sup> http://www.ftdichip.com/Support/Documents/DataSheets/ICs/DS\_FT2232H.pdf



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Pin	Schematic	Connected to	Notes
BDBUS0	F_UART_TX	FPGA Bank 1B, U6	UART Transmitter output
BDBUS1	F_UART_RX	FPGA Bank 1B, U6	UART Receiver Input
OSCI	OSCI	Oscillator, U7	Clock 12 MHz
EECS	EECS	EEPROM, U10	EEPROM Contains FTDI configuration
EECLK	EECLK	EEPROM, U10	
EEDATA	EEDATA	EEPROM, U10	
DM/DP	FD_N/ FD_P	Micro USB, J15	USB to UART
nRESET	3.3V	3.3V	

Table 16: FTDI chip interfaces and pins

### 6.3 LEDs

The functions of the LEDs are MAX10 Firmware dependent. See TEB0707 MAX10 CPLD LEDs<sup>4</sup>.

Designator	Color	Schematic	Connected to	Active Level	Note
D1	green	LED3	FPGA Bank 8	Active High	
D2	green	LED5	FPGA Bank 8	Active High	
D3	green	LED7	FPGA Bank 8	Active High	
D4	red	LED4	FPGA Bank 3	Active High	
D5	red	LED6	FPGA Bank 2	Active High	
D6	red	LED8	FPGA Bank 8	Active High	
D7	red	LED2	FPGA Bank 3	Active High	
D8	green	LED1	FPGA Bank 3	Active High	

Table 17: On-board LEDs

 $<sup>{\</sup>tt 4\,https://wiki.trenz\text{-}electronic.de/display/PD/TEB0707+MAX10+CPLD\#TEB0707MAX10CPLD-LEDs}$ 



#### 6.4 EEPROM

The EEPROM IC, U8 contains the FTDI configuration and is prprogrammed with Xilinx JTAG licence.

Pin	Schematic	Connected to	Notes
CS	EECS	FTDI, U8	
CLK	EECLK	FTDI, U8	
DIN	EEDATA	FTDI, U8	

Table 18: I2C EEPROM interface MIOs and pins

#### 6.5 **DIP Switch**

There is a DIP Switch provided for user controlling of settings. Dip1..3 are connected to MAX10 CPLD and therefore function is Firmware dependent, see TEB0707 MAX10 Dips<sup>5</sup>.

Pin	Schemati c	Function (in standard Firmware)	Notes
DIP 1	DIP1	Forwarded to IO so SoM	MAX10 firmware dependent.
DIP 2	DIP2	IO Voltage selection	1.8V ('high', open, OFF), 2.5V ('low', closed, ON)
DIP 3	DIP3 (PROGMO DE)	Programming mode (JTAG selection on Trenz 4x5 module)	Select between FPGA/SoC (high, open, OFF) or CPLD (low, closed, ON), MAX10 firmware dependent.
DIP 4	JTAGEN	JTAG Selection	JTAG mode between CPLD (high, closed, ON) or SoM (low, open, OFF)

**Table 19: DIP Switch connections** 

#### 6.6 Push Buttons

Buttons are connected MAX10 CPLD and therefore function is Firmware dependent, see TEB0707 MAX10 CPLD Buttons<sup>6</sup>

<sup>5</sup> https://wiki.trenz-electronic.de/display/PD/TEB0707+MAX10+CPLD#TEB0707MAX10CPLD-UserDips: 6 https://wiki.trenz-electronic.de/display/PD/TEB0707+MAX10+CPLD#TEB0707MAX10CPLD-UserButton



Designator	Schematic	Function (in standard Firmware)	Notes
S2	RESET	SoM Reset	Hardware debounced.
S3	BUTTON1	User Button	debounced in Max10 FPGA

**Table 20: Push Buttons informations** 

## 6.7 Clock Sources

MEMS U7 Oscillator is nedded for FTDI. It is additionally connected to MAX 10 FPGA Bank 2 Pin H4 and can be used in custom Firmware.

Designator	Description	Frequency	Note
U7	MEMS Oscillator	12 MHz	

Table 21: Osillators

# 7 Power and Power-On Sequence

## 7.1 Power Supply

Power supply with minimum current capability of 3 A for system startup is recommended.

## 7.2 Power Consumption

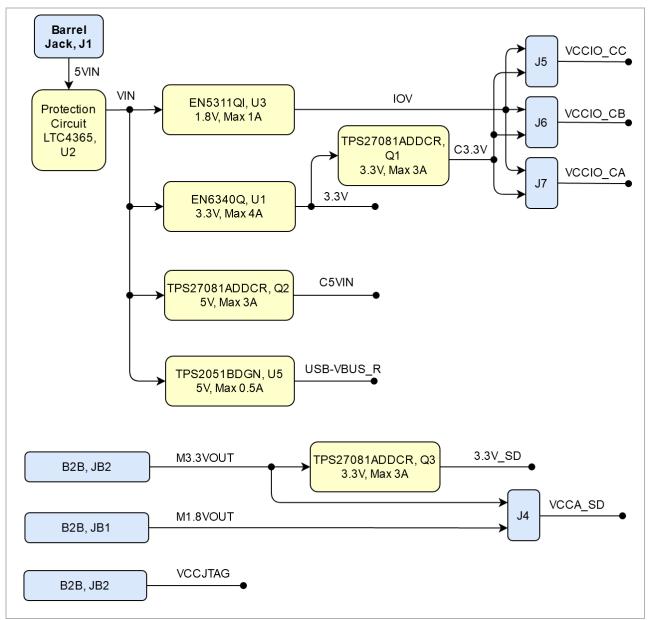
Power Input Pin	Typical Current
VIN	TBD*

**Table 22: Power Consumption** 

\* TBD - To Be Determined

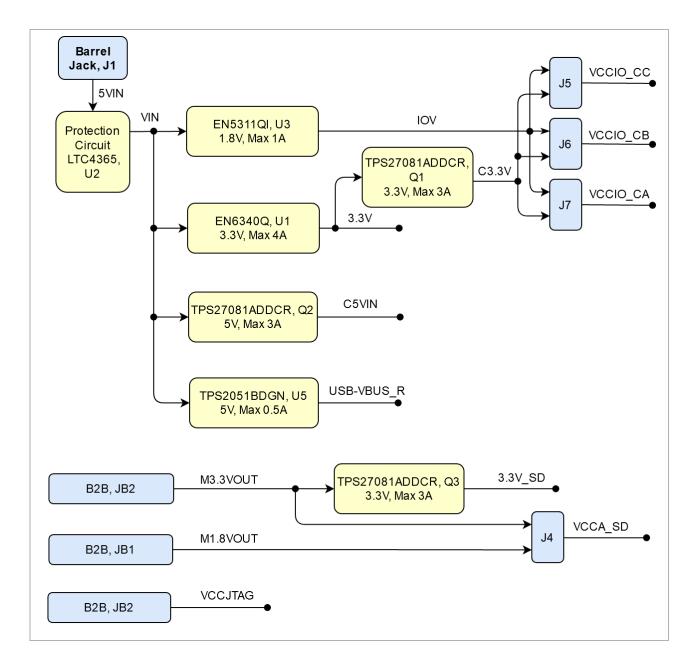


## 7.3 Power Distribution Dependencies



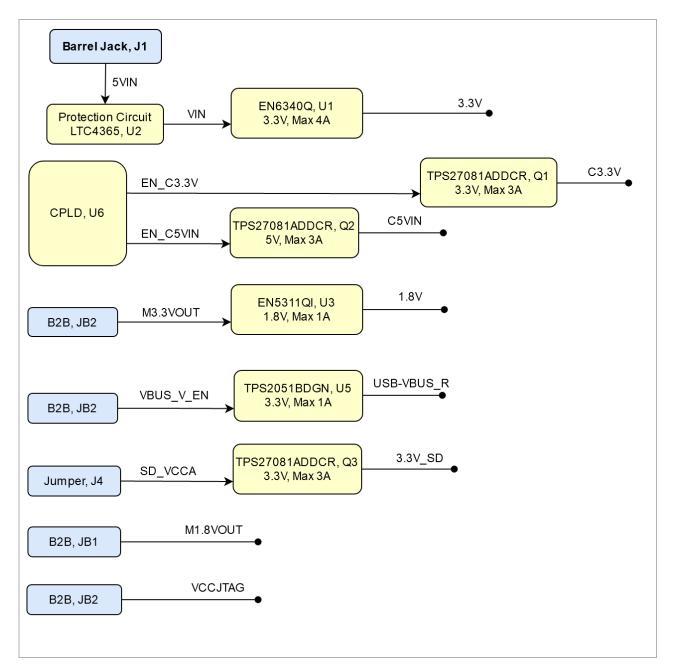
**Figure 3: Power Distribution** 





## 7.4 Power-On Sequence





**Figure 4: Power Sequency** 

## 7.5 Power Rails



Power Rail Name	B2B Connector JB1 Pin	B2B Connector JB2 Pin	B2B Connector JB3 Pin	Direction	Notes
VCCIO_CA	-	8, 10	-	Output	
VCCIO_CB	-	2, 4, 6	-	Output	
VCCIO_CC	10, 12	-	-	Output	
3.3V	14, 16	-	-	Output	
M1.8VOUT	40	-	-	Input	
M3.3VOUT	-	9, 11	-	Input	
ETH-VCC	13	-	-	Input	

Table 23: Module power rails.

# 7.6 Bank Voltages

Below MAX10 CPLD Bankvoltages are summarized.

Bank	Schematic Name	Voltage	Notes
Bank 1A	3.3V	3.3V	
Bank 1B	3.3V	3.3V	
Bank 2	3.3V	3.3V	
Bank 3	3.3V	3.3V	
Bank 5	VCCJTAG		from SoM
Bank 6	VCCIO_CC		Variable
Bank 8	3.3V	3.3V	

Table 24: Zynq SoC bank voltages.

Revision: v.45

8

### **Board to Board Connectors**



These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.

4 x 5 modules use two or three Samtec Razor Beam LSHM connectors<sup>7</sup> on the bottom side.

- 2 x REF-189016-02 (compatible to LSHM-150-04.0-L-DV-A-S-K-TR), (100 pins, "50" per row)
- 1 x REF-189017-02 (compatible to LSHM-130-04.0-L-DV-A-S-K-TR), (60 pins, "30" per row) (depending on module)

## 8.1 Connector Mating height

When using the same type on baseboard, the mating height is 8mm. Other mating heights are possible by using connectors with a different height

Order number	Connector on baseboard	compatible to	Mating height
23836	REF-189016-01	LSHM-150-02.5-L-DV-A- S-K-TR	6.5 mm
	LSHM-150-03.0-L-DV-A- S-K-TR	LSHM-150-03.0-L-DV-A- S-K-TR	7.0 mm
23838	REF-189016-02	LSHM-150-04.0-L-DV-A- S-K-TR	8.0 mm
	LSHM-150-06.0-L-DV-A- S-K-TR	LSHM-150-06.0-L-DV-A- S-K-TR	10.0mm
26125	REF-189017-01	LSHM-130-02.5-L-DV-A- S-K-TR	6.5 mm
	LSHM-130-03.0-L-DV-A- S-K-TR	LSHM-130-03.0-L-DV-A- S-K-TR	7.0 mm
24903	REF-189017-02	LSHM-130-04.0-L-DV-A- S-K-TR	8.0 mm
	LSHM-130-06.0-L-DV-A- S-K-TR	LSHM-130-06.0-L-DV-A- S-K-TR	10.0mm

Table 25: Connectors.

<sup>7</sup> https://www.samtec.com/technical-specifications/Default.aspx?SeriesMaster=LSHM

The module can be manufactured using other connectors upon request.

## 8.2 Connector Speed Ratings

The LSHM connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
12 mm, Single-Ended	7.5 GHz / 15 Gbps
12 mm, Differential	6.5 GHz / 13 Gbps
5 mm, Single-Ended	11.5 GHz / 23 Gbps
5 mm, Differential	7.0 GHz / 14 Gbps

Table 26: Speed rating.

### 8.3 Current Rating

Current rating of Samtec Razor Beam™ LSHM B2B connectors is 2.0A per pin (2 adjacent pins powered).

## 8.4 Connector Mechanical Ratings

- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 2 hours per axis, 3 axes total

Revision: v.45

### 9 CRUVI Connectors

CRUVI modules use on bottom side:

- TMMH-106-04-F-DV-A-M as Low Speed connectors, (12 pins, 6 per row)
- ST4-30-1.50-L-D as High Speed connectors, (60 pins, 30 per row)

CRUVI carrier use on top side:

- CLT-106-02-F-D-A-K as Low Speed connectors, (12 pins, 6 per row)
- SS4-30-3.50-L-D as High Speed connectors, (60 pins, 30 per row)

## 9.1 Connector Mating height

Mating heigh of the high speed connectors is 5mm. The low speed connectors mate correctly within a range from 4.78 mm to 5.29 mm.

## 9.2 Current Rating

Current rating of High Speed B2B connectors is 1.6A per pin (2 pins powered).

Current rating of Low Speed B2B connectors is 4.1A per pin (2 pins powered).

### 9.3 Speed Rating

There is no data available for the connectors actual used here. Data available for other stacking heights of same connectors is summarized in the following table:

Connector	Speed ratings
ST4/SS4 single ended (4mm stacking height!)	13.5GHz / 27 Gbps
ST4/SS4 differential (4mm stacking height!)	15.5 GHz / 31 Gbps
TMMH/CLT single ended (4.77mm stacking height!)	5.5GHz / 11 Gbps

**Table 27: Connector speed ratings** 

## 9.4 Operating Temp Range

All connectors are specified for a temp. range of -55 °C to 125 °C.



## 10 Technical Specifications

## 10.1 Absolute Maximum Ratings

Symbols	Description	Min	Max	Unit
5VIN	Input supply Voltage	-40	60	V
T_STG	Storage Temperature	-40	85	°C

Table 28: PS absolute maximum ratings

## 10.2 Recommended Operating Conditions

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

Parameter	Min	Max	Units	Reference Document
Input supply Voltage	4.06	5.58	V	See the OV/UV in the carrier datasheets.
T_OPT	0	70	°C	See Push Button datasheet.

Table 29: Recommended operating conditions.

## 10.3 Physical Dimensions

- Module size: 135 mm × 68 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 4 mm.

PCB thickness: 1.7 mm.



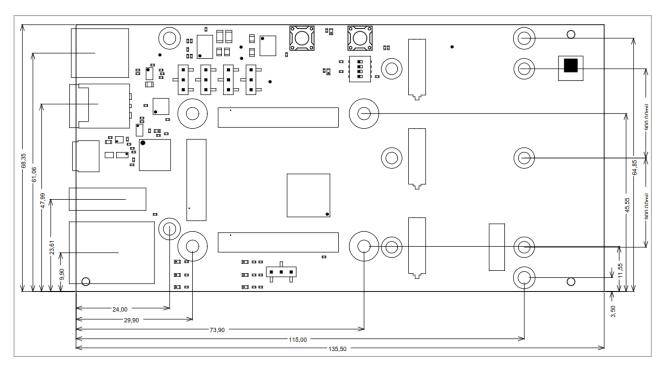


Figure 5: Physical Dimension





# 11 Currently Offered Variants

Trenz shop TEB0707 overview page		
English page <sup>8</sup>	German page <sup>9</sup>	

**Table 30: Trenz Electronic Shop Overview** 

<sup>8</sup> https://shop.trenz-electronic.de/en/Products/Trenz-Electronic/9 https://shop.trenz-electronic.de/de/Produkte/Trenz-Electronic/



Revision: v.45

## 12 Revision History

## 12.1 Hardware Revision History

Date	Revision	Changes	Documentation Link
2020-11-20	REV02	first production release	REV02
2020-04-01	REV01	Prototypes	-

**Table 31: Hardware Revision History** 

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.



Figure 6: Board hardware revision number.

## 12.2 Document Change History

Date	Revision	Contributor	Description
2020-11-25	v.45(see page 6)	Martin Rohrmüller <sup>10</sup>	• Initial Reslease
	all	Pedram Babakhani <sup>11</sup> , Martin Rohrmüller <sup>12</sup>	•

Table 32: Document change history.

<sup>10</sup> https://wiki.trenz-electronic.de/display/~m.rohrmueller

<sup>11</sup> https://wiki.trenz-electronic.de/display/~P.Babakhani

<sup>12</sup> https://wiki.trenz-electronic.de/display/~m.rohrmueller

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Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.



<sup>13</sup> http://guidance.echa.europa.eu/

<sup>14</sup> https://echa.europa.eu/candidate-list-table

<sup>15</sup> http://www.echa.europa.eu/