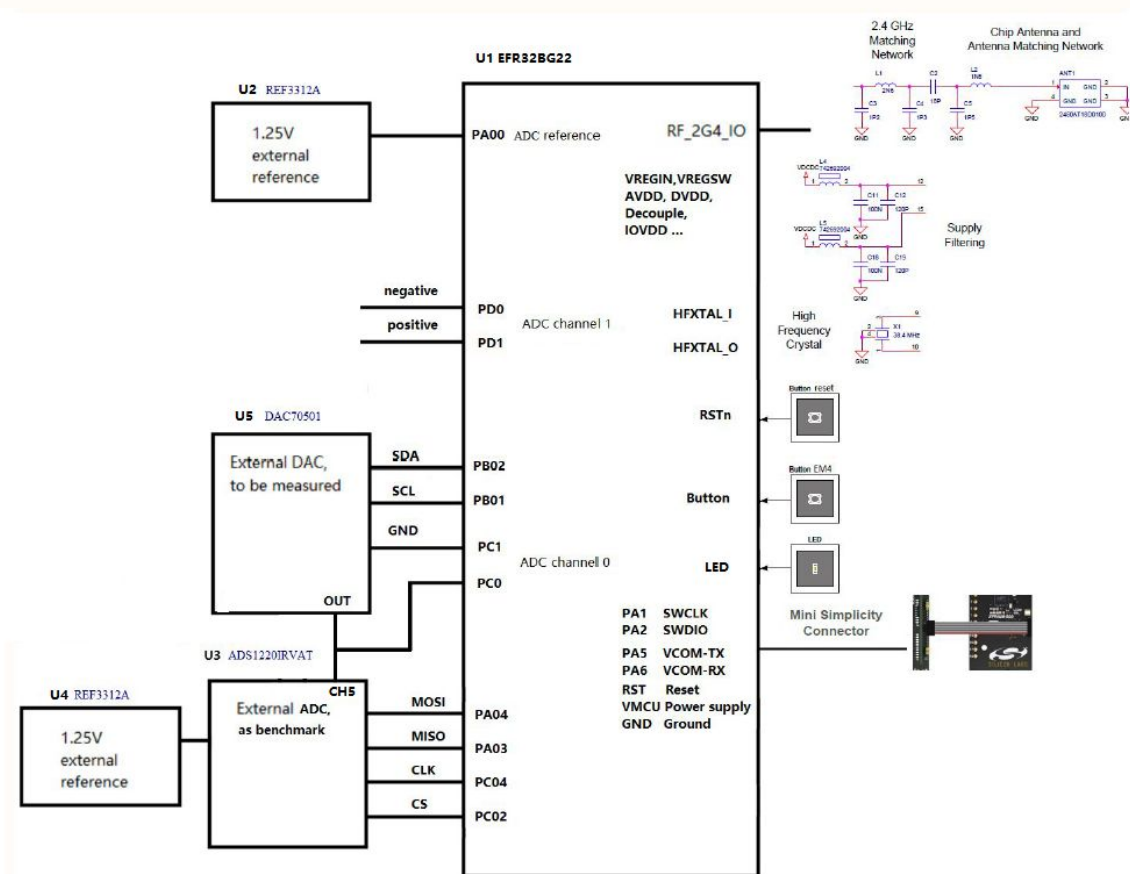



Function Block:



Version	Changes
V2.0	Initial Release
V2.1	Change Function Block Diagram

Board Function	Page
Title Page	1
RF Match, Antenna & Power	2
SoC GPIOs Connection	3
DAC & ADC	4



**SILICON LABS**

Schematic Title

**EFR32BG22 CGM Board**

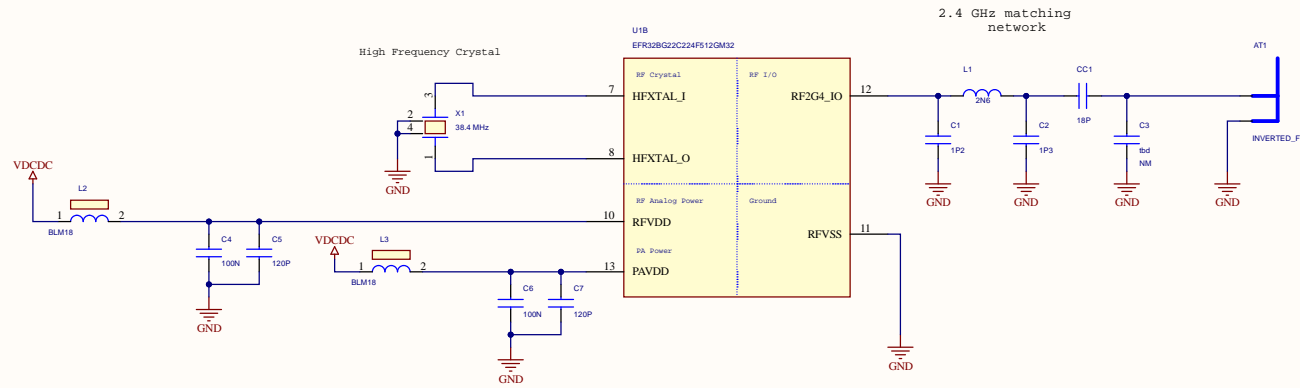
Page Title

**Title Page**

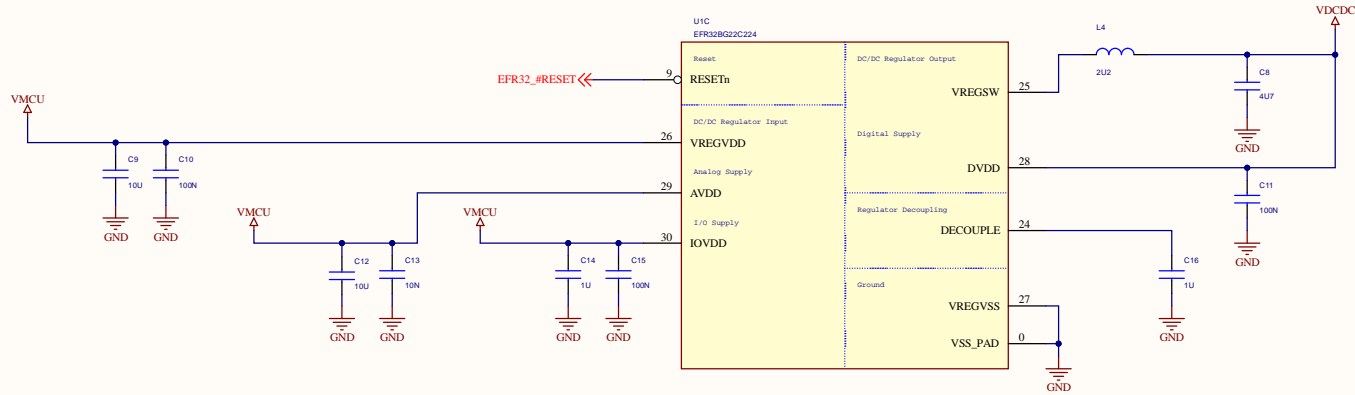
Designed: Jun Fan	Approved: Cheng Yuan
Size A3	BOM Doc No:
Design Created Date:	


Document number <b>BRD</b>	Revision <b>B01</b>
Sheet Created Date	Sheet Modified Date
1 of 4	

Antenna & Radio Interface

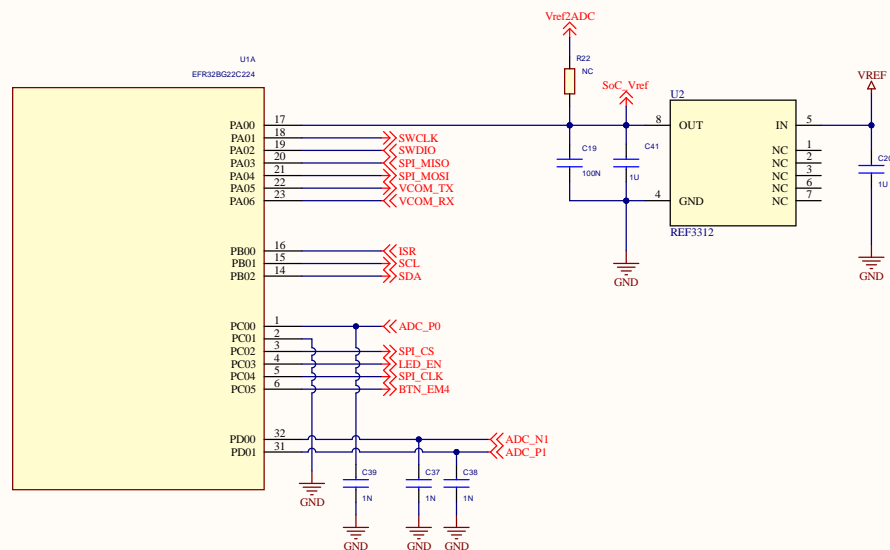


Power & Decoupling

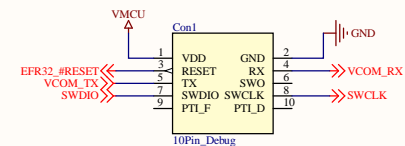
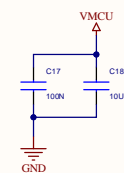


 <b>SILICON LABS</b>	Schematic Title	
	EFR32BG22 CGM Board	
Designed: Jun Fan	Approved: Cheng Yuan	Page Title RF Match, Antenna & Power
Size A3	BOM Doc No:	Document number BRD
Design Created Date:	Sheet Created Date	Sheet Modified Date
		Revision B01
		Sheet 2 of 4

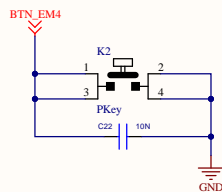
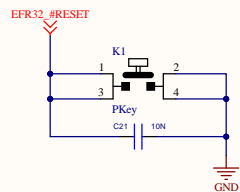
## EFR32 I/O Port Pins



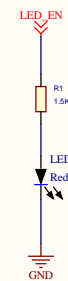
## Debug Connector




## Reset Button & Wakeup Button

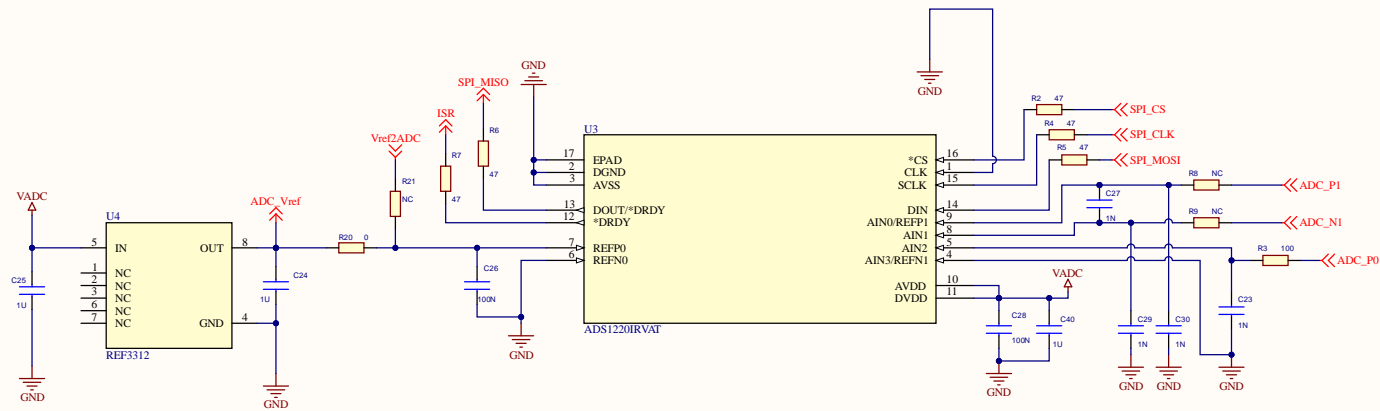


## LED

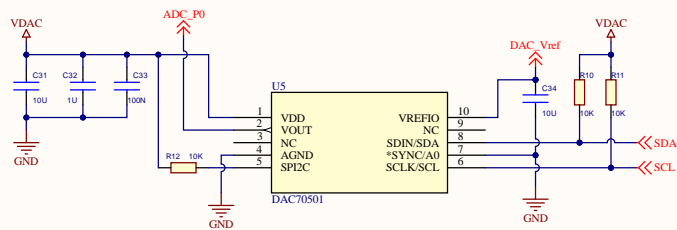


 <b>SILICON LABS</b>		Schematic Title	
		<b>EFR32BG22 CGM Board</b>	
Designed: Jun Fan		Page Title	
Approved: Cheng Yuan		<b>SoC GPIOs Connection</b>	
Size A3	BOM Doc No:	Document number <b>BRD</b>	Revision <b>B01</b>
Design Created Date:		Sheet Created Date	Sheet Modified Date
		Sheet	3 of 4

## ADC



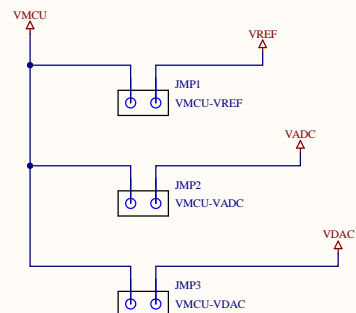
## DAC Source




## Test Points



## Divided Power Domains



		Schematic Title	
		EFR32BG22 CGM Board	
Designed: Jun Fan		Page Title	
Size A3		DAC & ADC	
BOM Doc No:		Document number	Revision
Design Created Date:		BRD	B01
		Sheet Created Date	Sheet Modified Date
		4	4