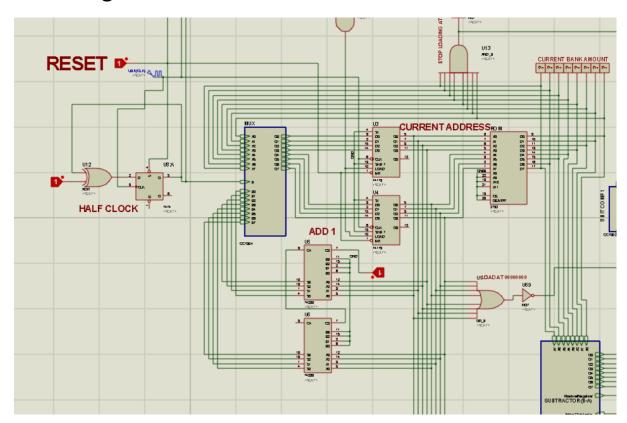
Digisim PS1



Traversing List



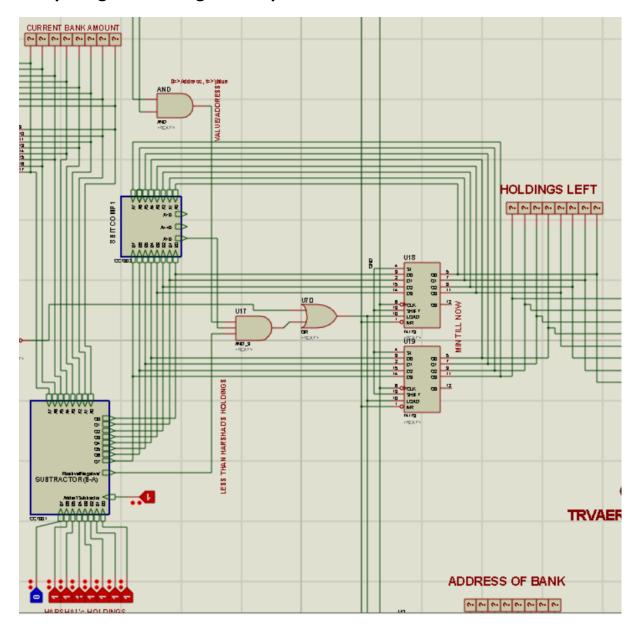
- 1. The clock is sent to T flip flop and the frequency of clock is halved.
- 2. When the reset is used to set the half clock to 1.
- 3. Using mux either B(Current address +1) is selected to get the address of the node or mux chooses the value at the current address to traverse to the next node.

4. Due to half clocked pulse(time period double), each output of mux gets a positive edge oof clock to update the register.

5.Overall:

Output of half clock	Output of Address	
0	Address of next node	
1	Value of current Node	

Comparing and storing the output



The output of rom is subtracted from harshad's holdings and compared with the current difference stored in the register.

One of the following things will make the register load the value:

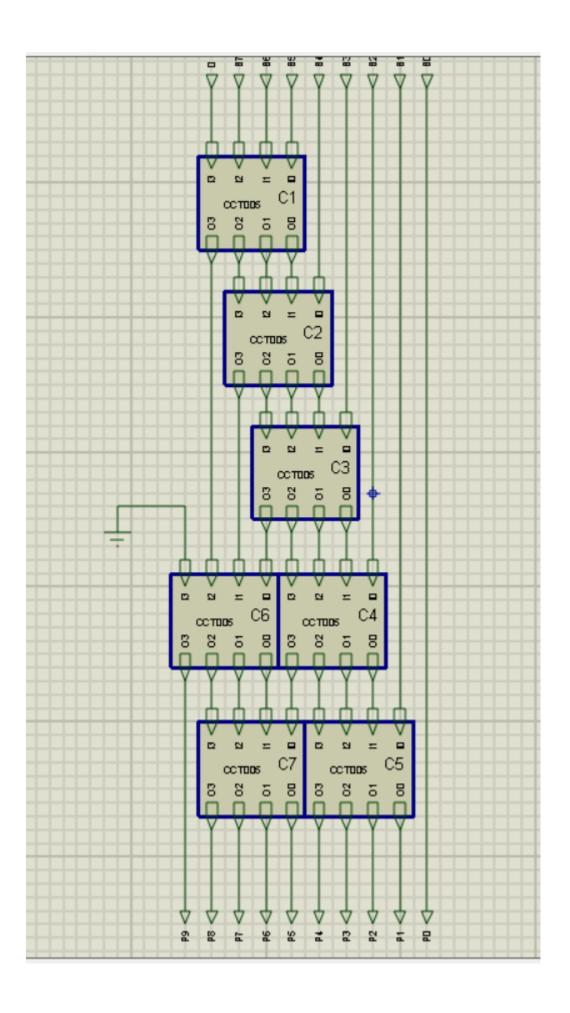
• Conditions:

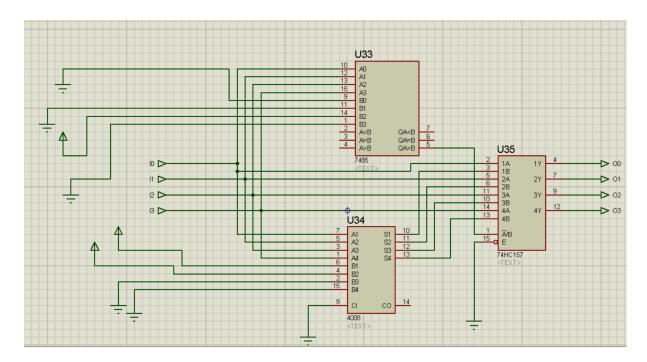
- a. The output of rom is not (111111111 and the half clock is at 1(means the rom is showing the value)).
- b. The number is less than holdings ,i.e. the carry of subtractor is 1.
- c. The difference calculated is less that the previous value.
- The output of rom is the value at first node, i.e. the address in 00000000.

Also using the same load line, clk and reset. The address of current node is also stored in registers.

8-bit Binary to 3 digit BCD display

Reference: https://www.youtube.com/watch?v=kusZDF3IfBA





In the child sheet 4 bits are taken as input and if the output is strictly greater than 4 then 3 is added to the current number and the output is sent back.

Using the series of this circuit we get the desired output.

The 10(P9 P8 P7 P6 P5 P4 P3 P2 P1 P0) bits obtained are sent to bcd to bcd disply decoder to display the output.

Hundredths Place	BCD decoder 1	0 0 P9 P8
Tenths Place	BCD decoder 2	P7 P6 P5 P4
Ones Place	BCD decoder 3	P3 P2 P1 P0

TEST CASE USED

