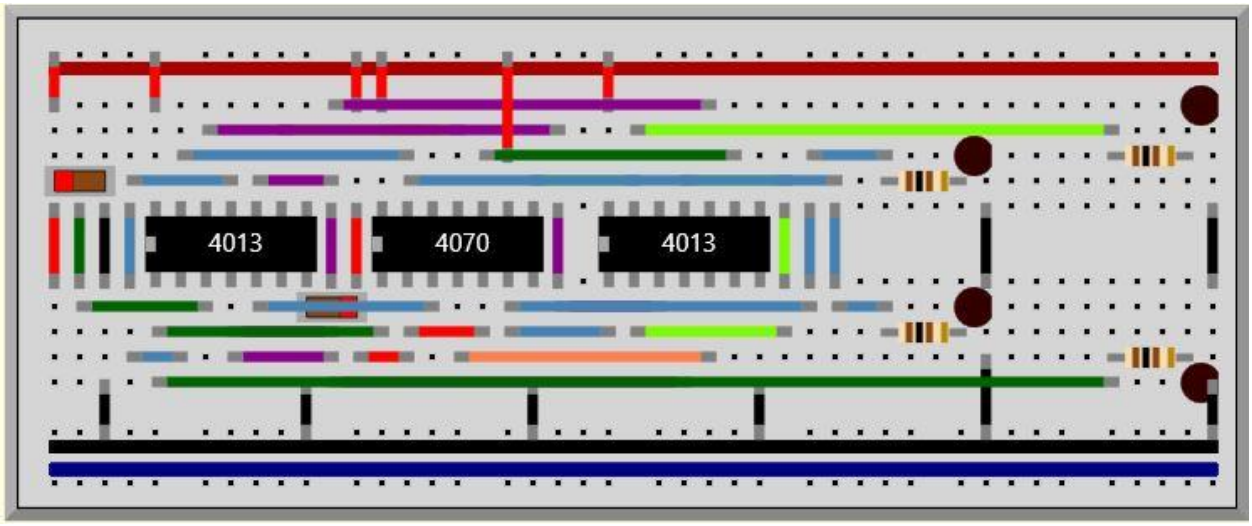
Design and verify the 4- Bit Synchronous/ Asynchronous Counter using JK flip flop

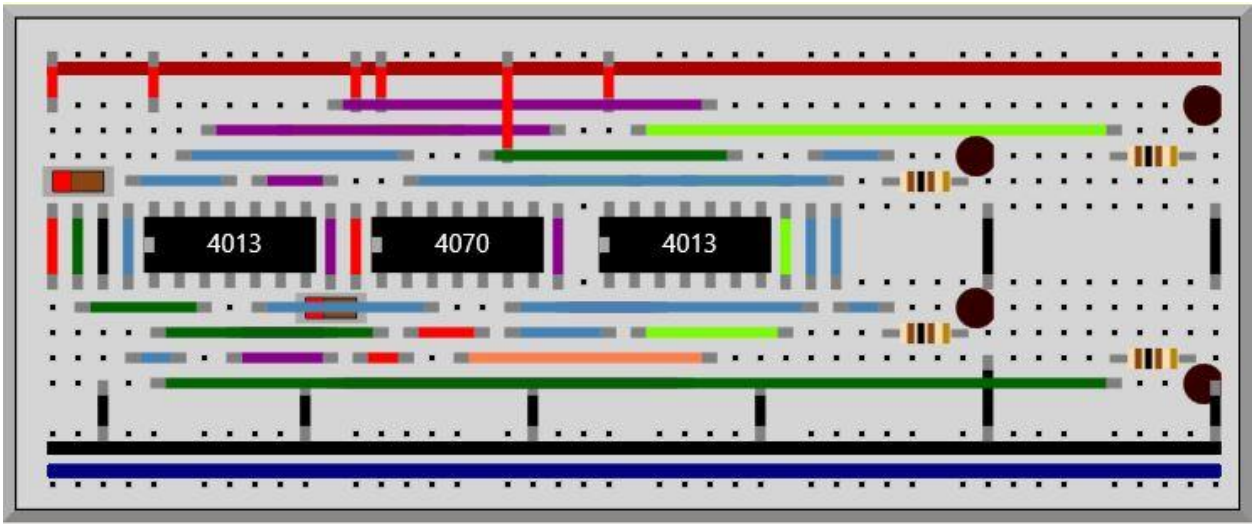
On every pos CLK edge, Output changes.

Asynchronous counter

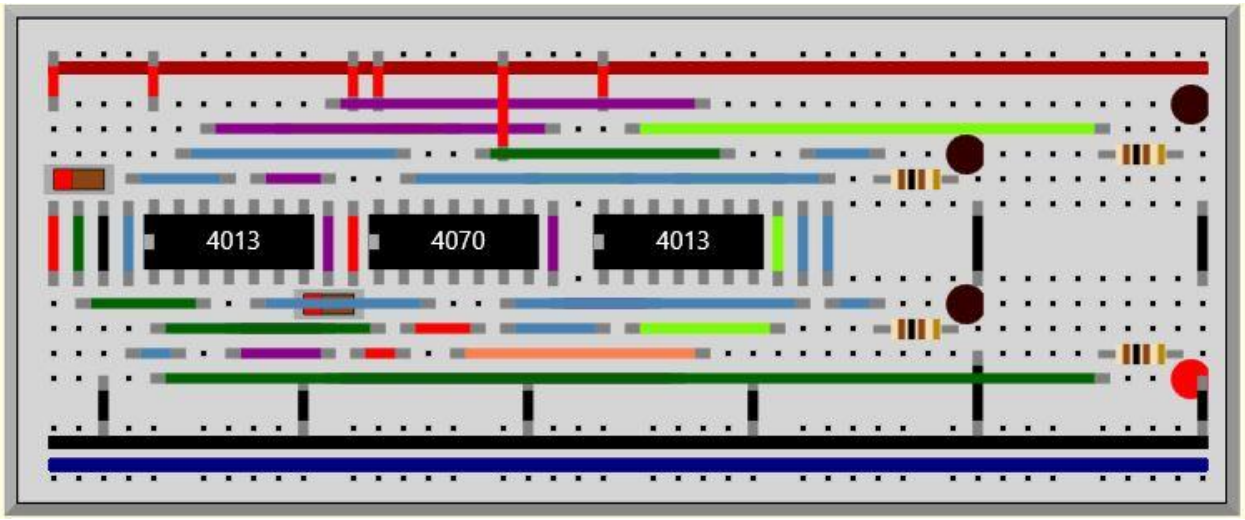
RESET 1



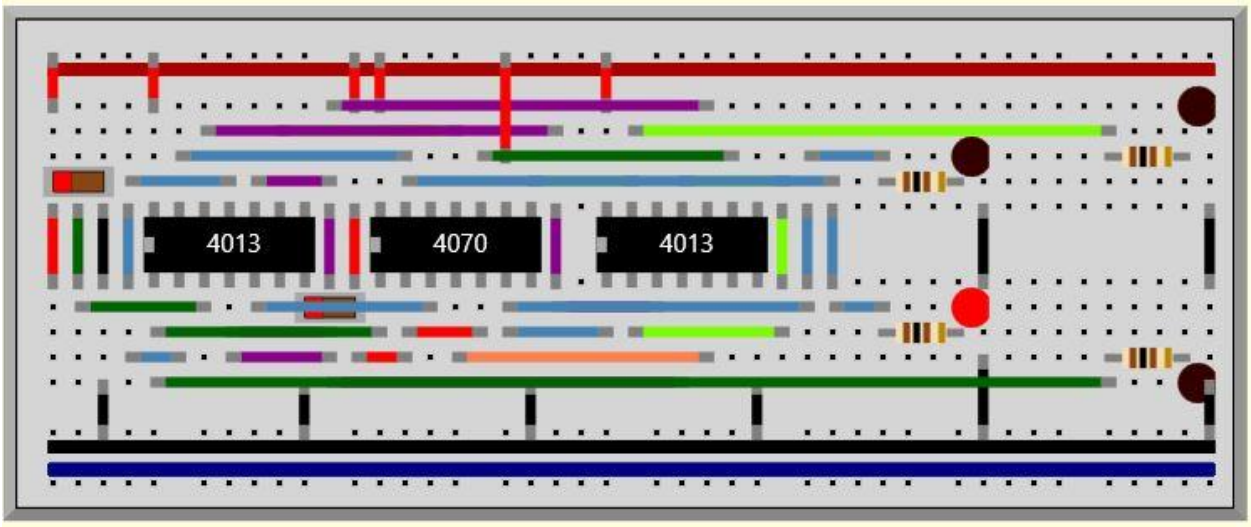
0000



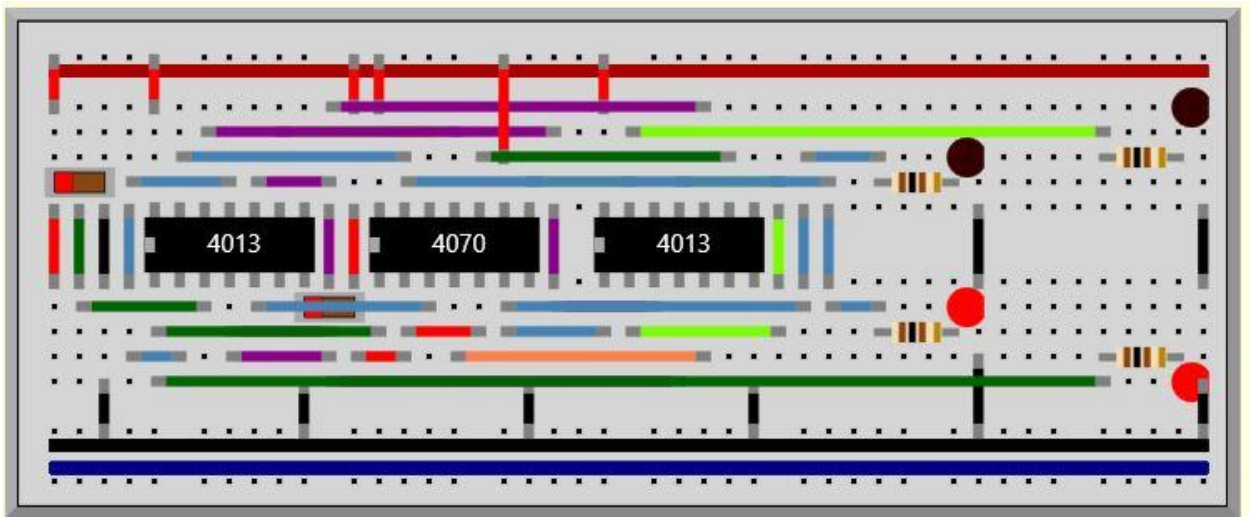
0001



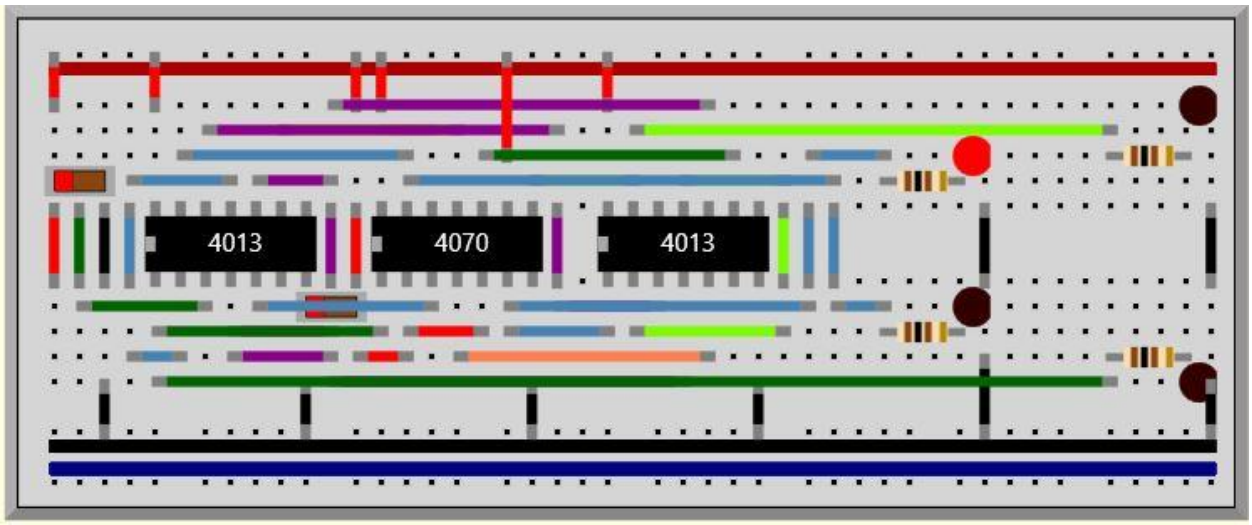
0010



0011



0100



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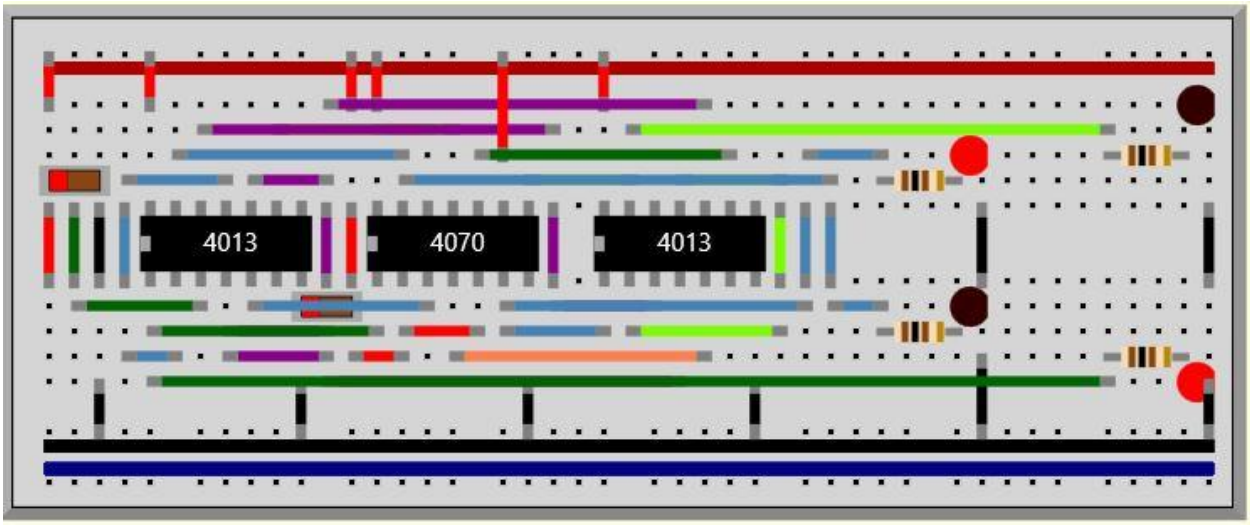

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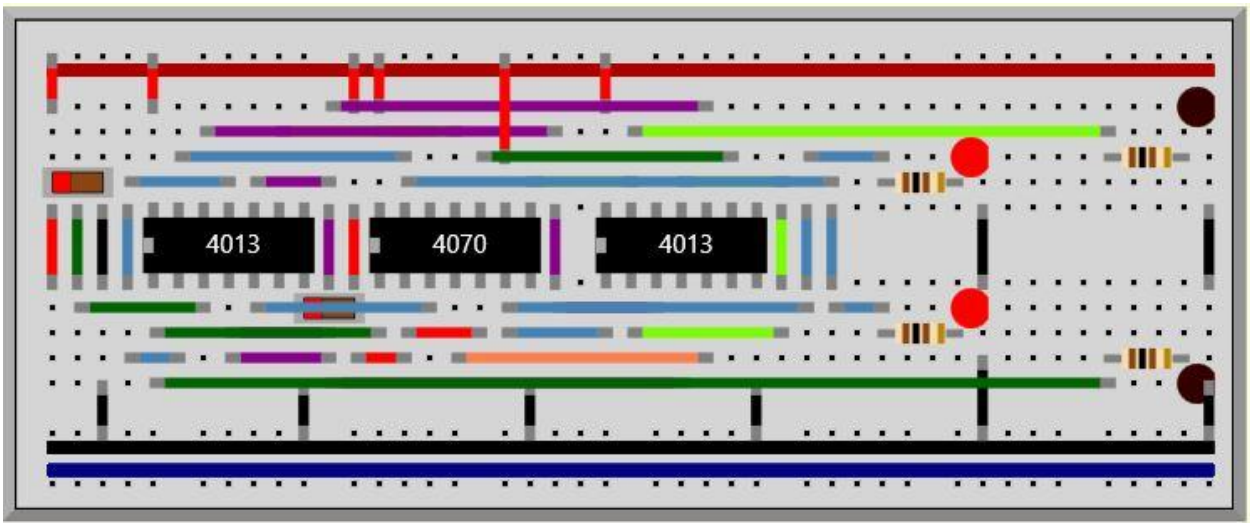
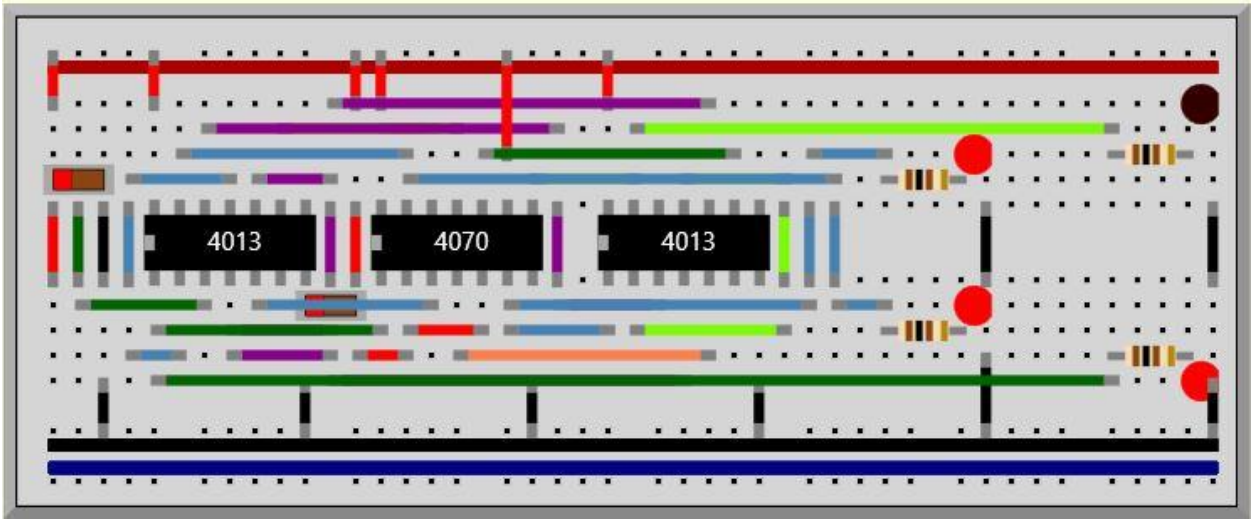


0111



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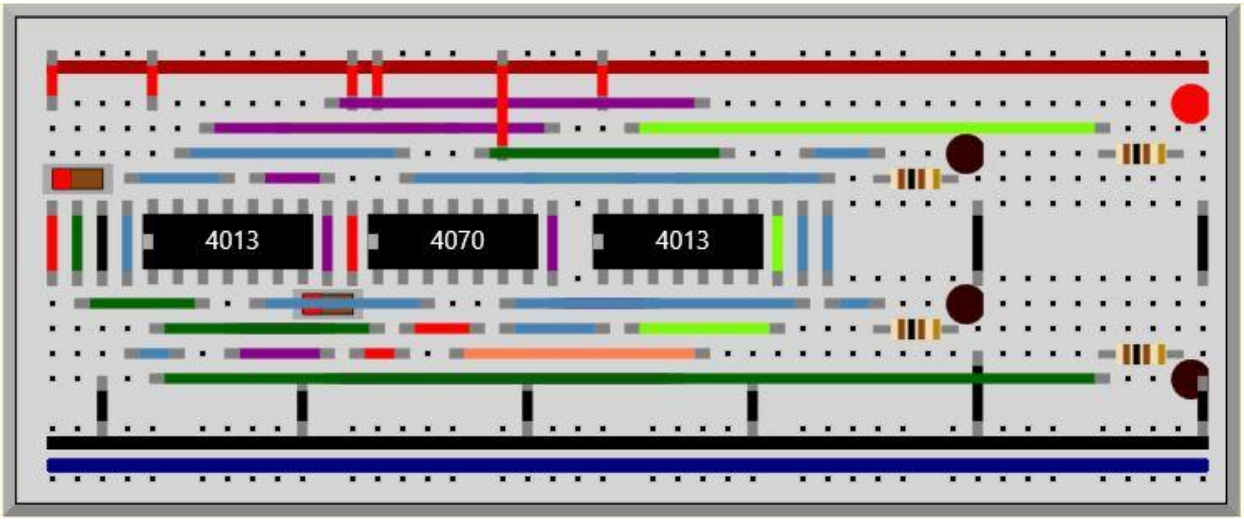

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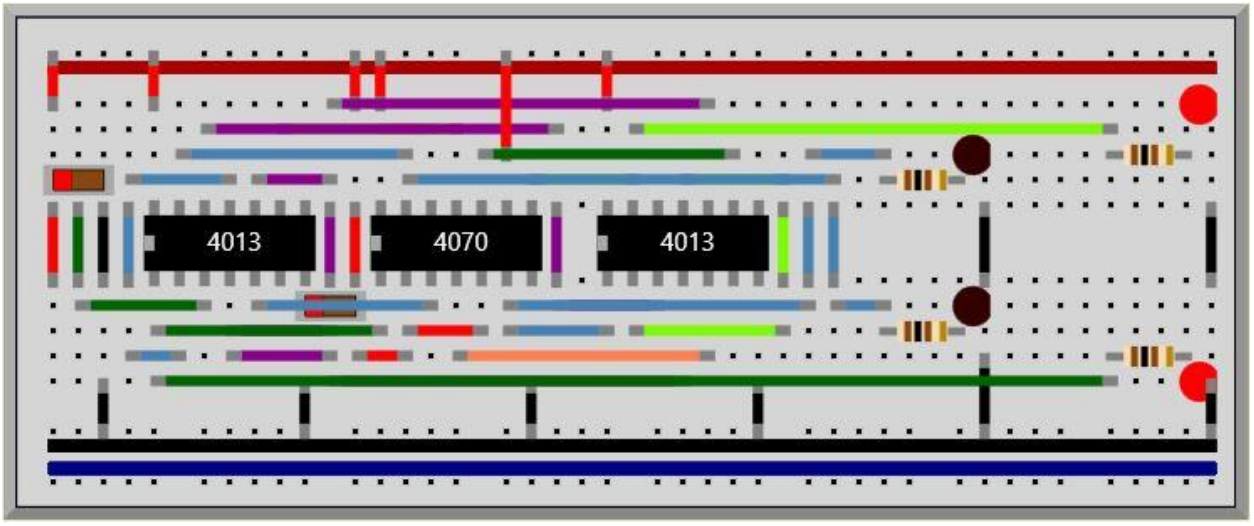

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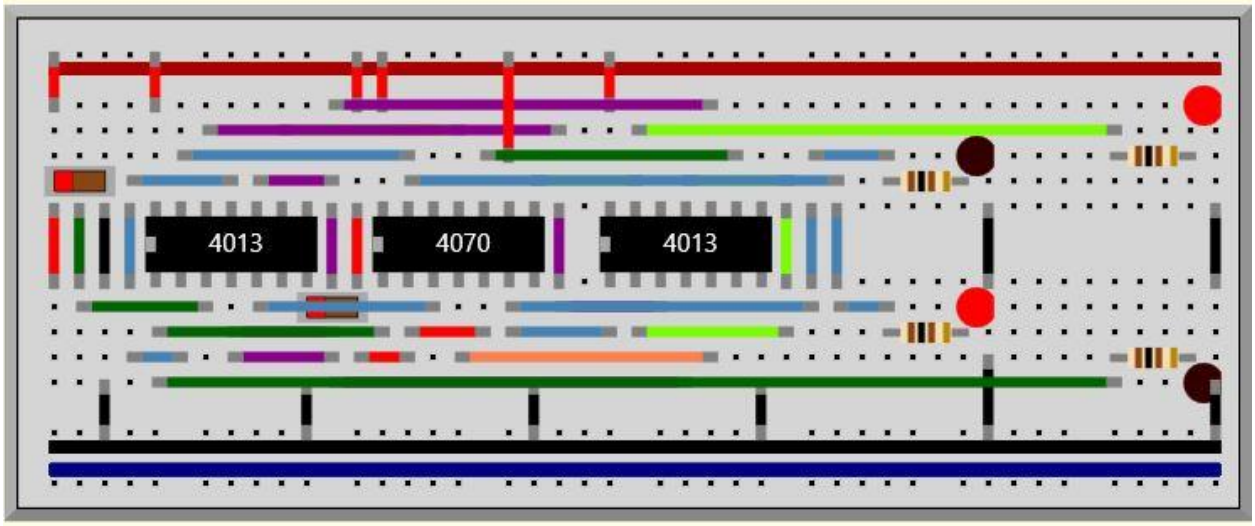

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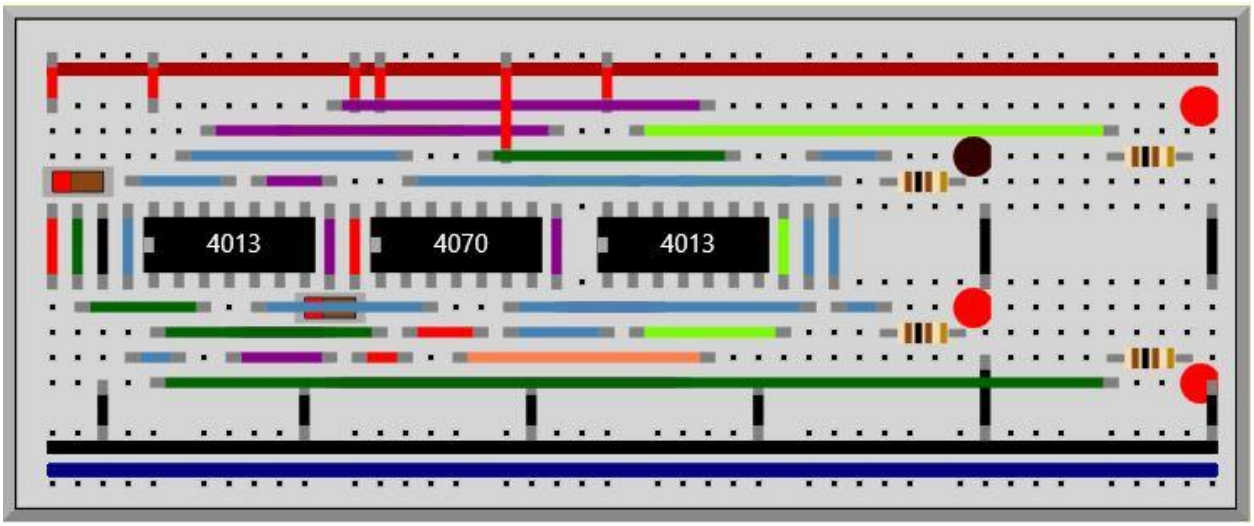

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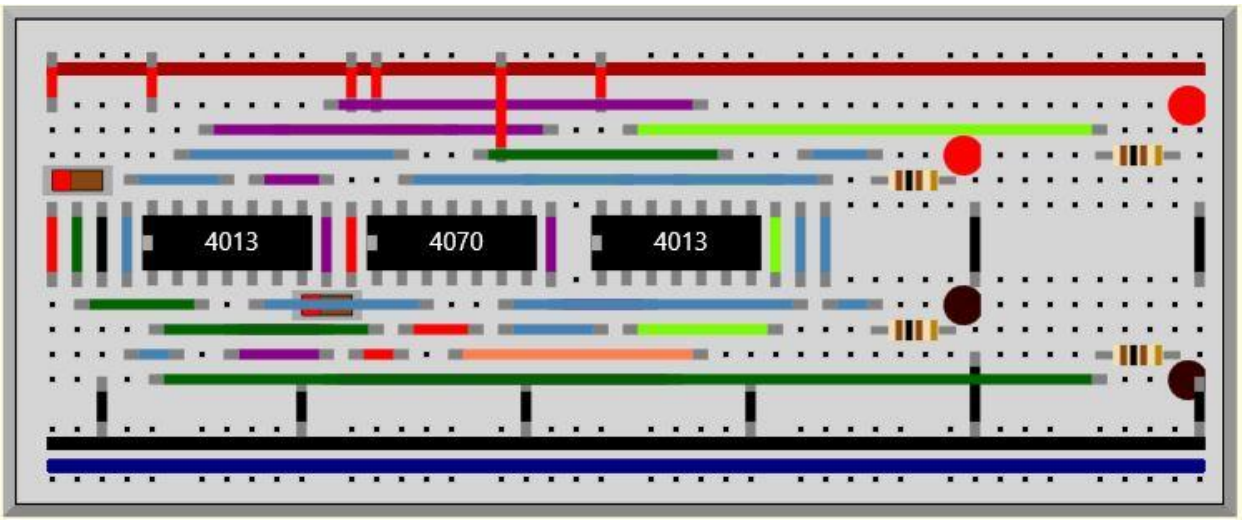

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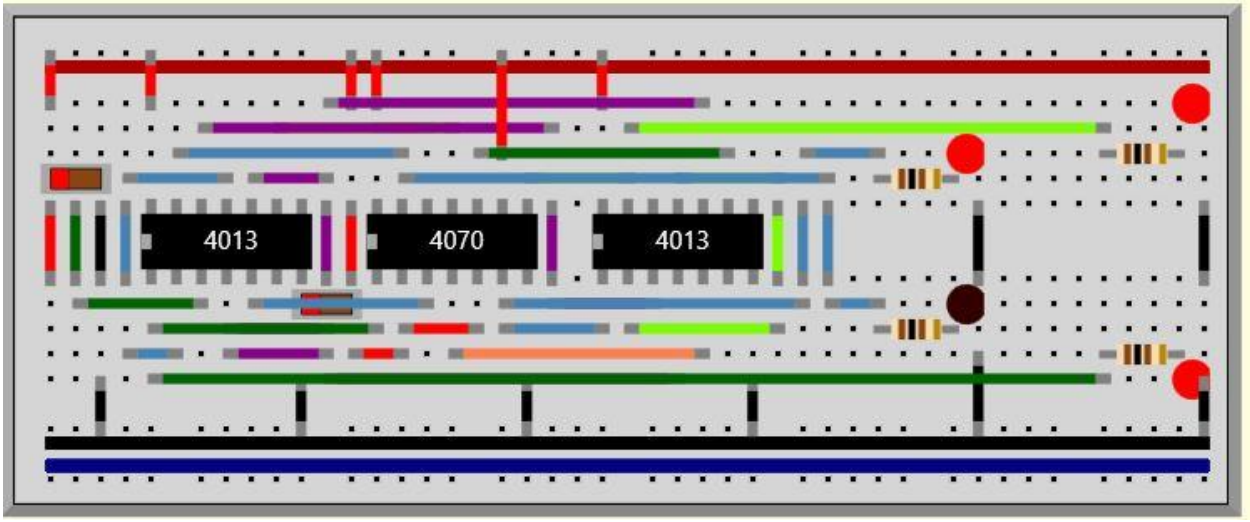

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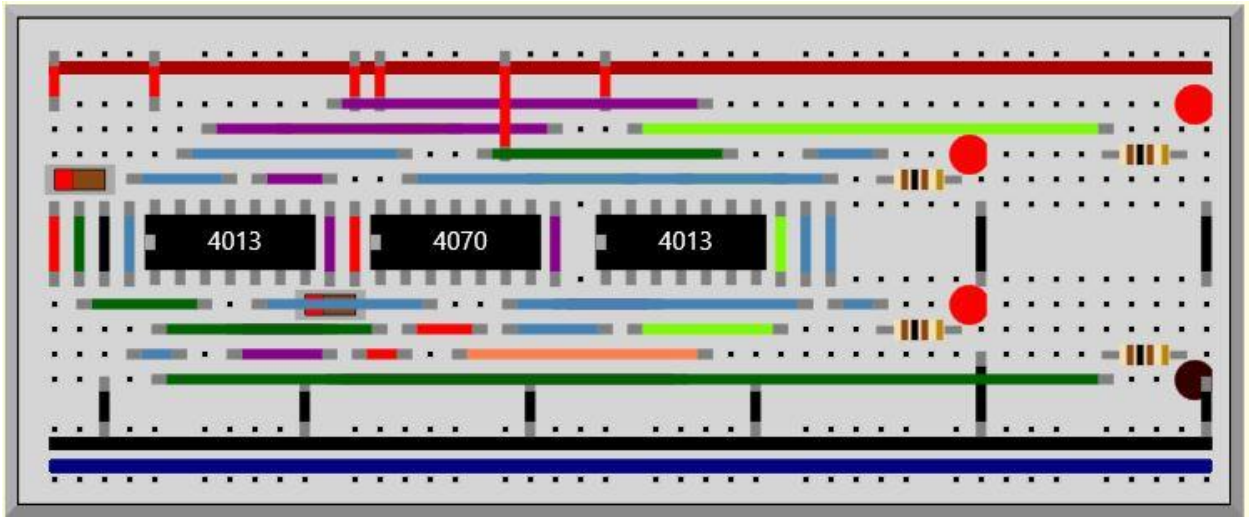
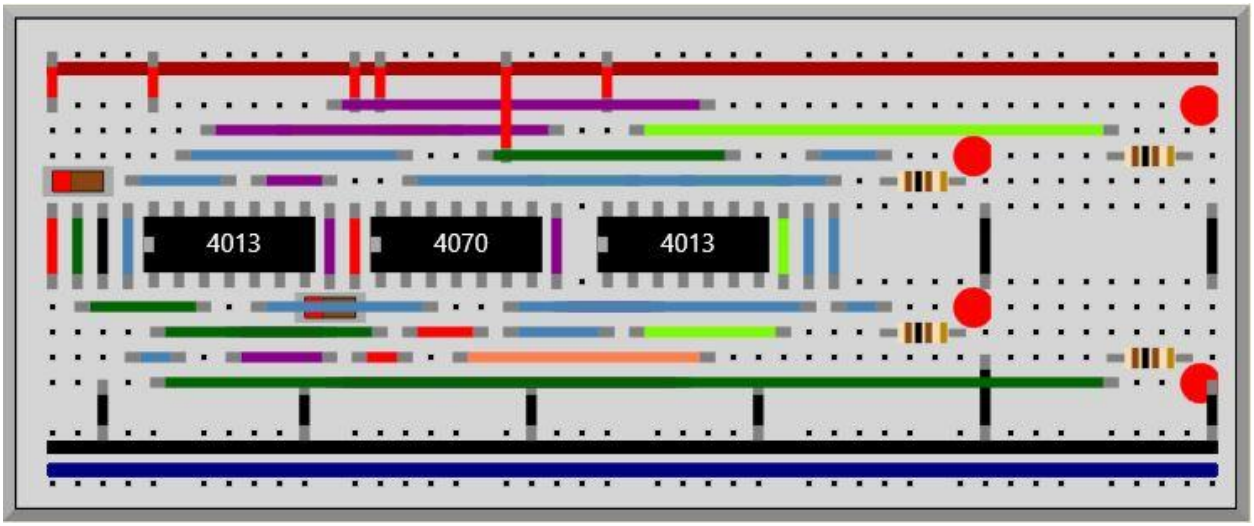
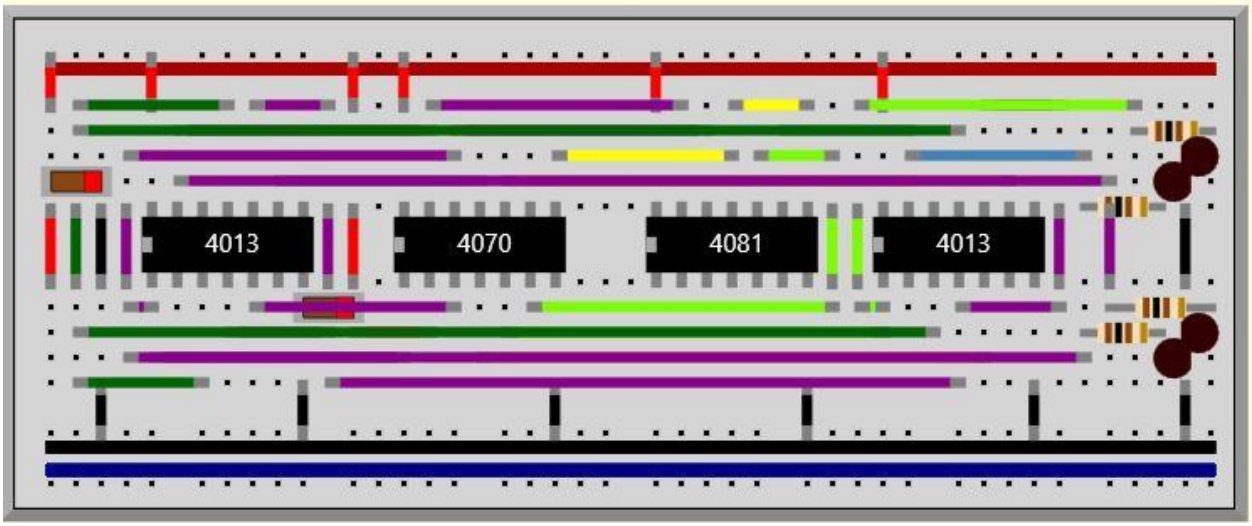


1111

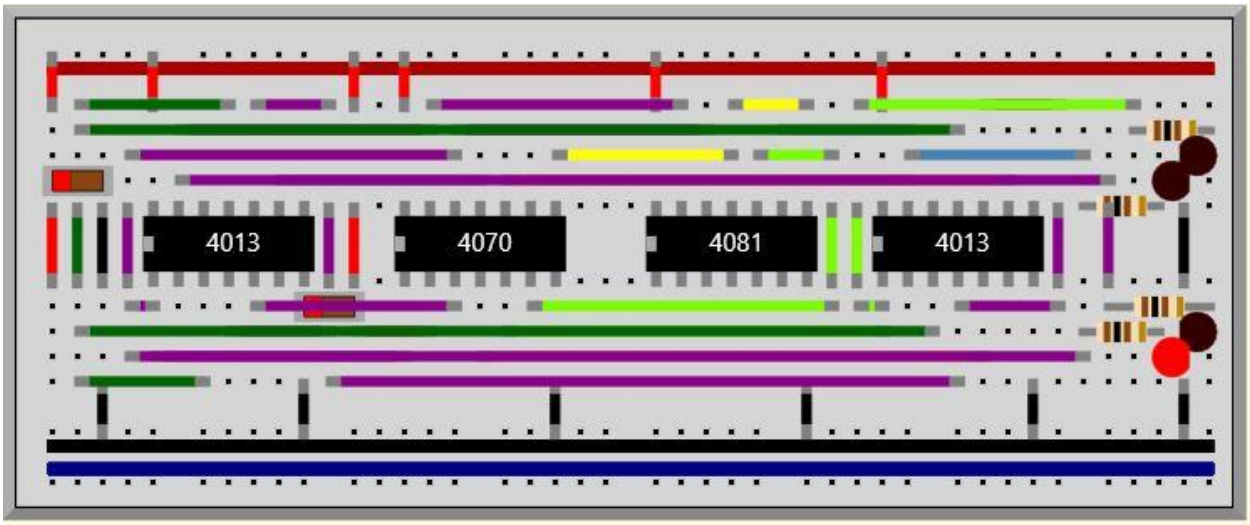


Synchronous

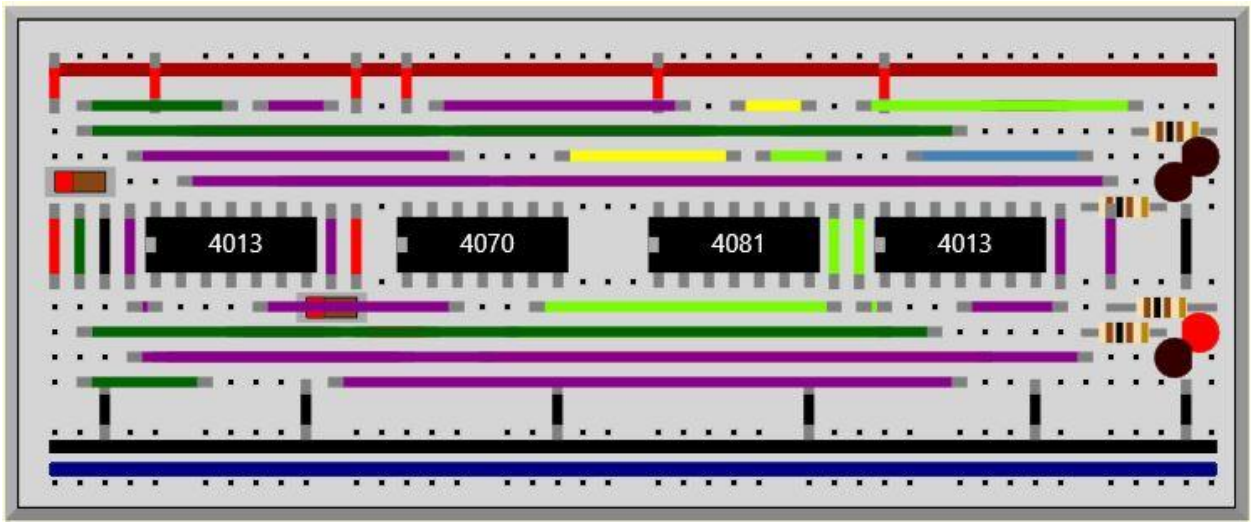
RESET1



0001



0010



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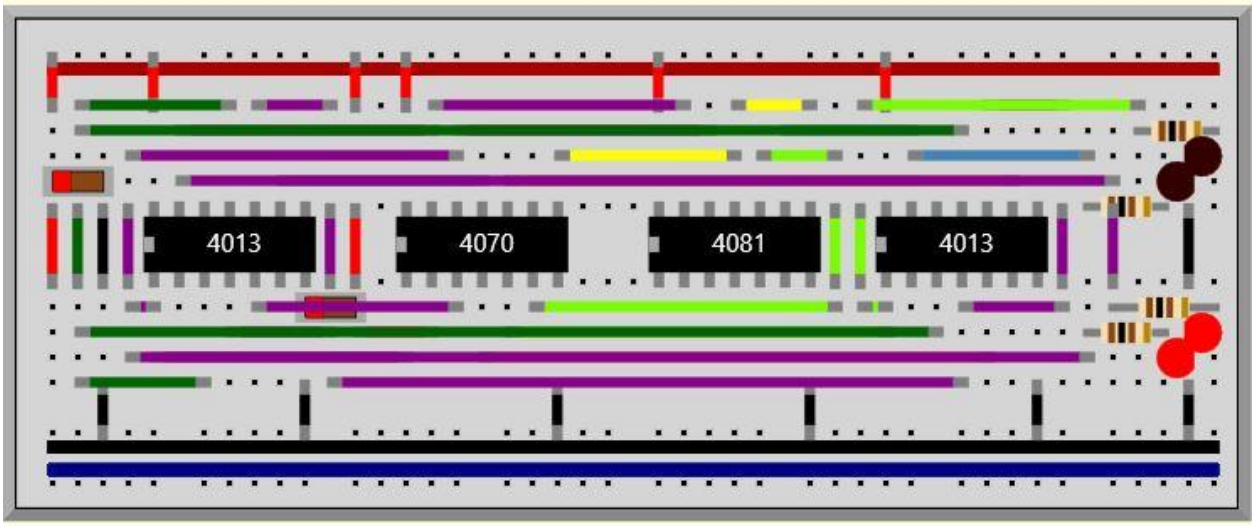

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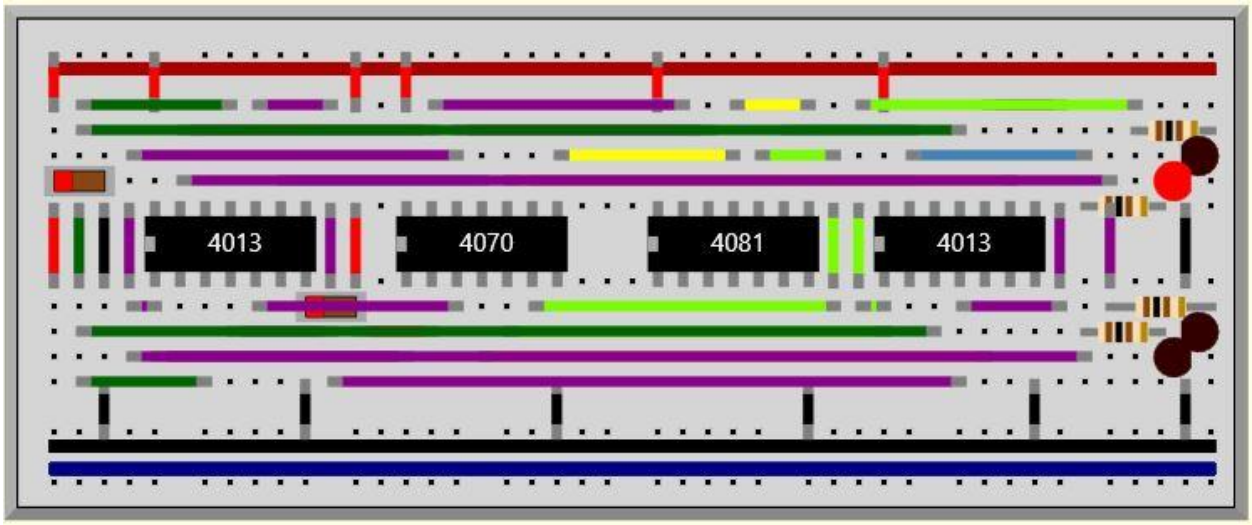

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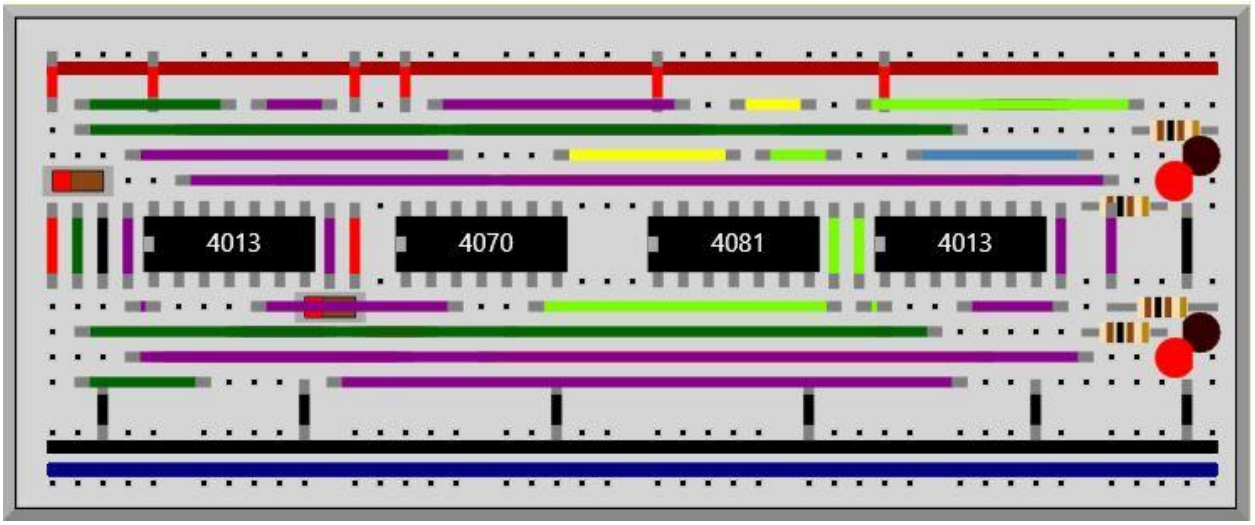

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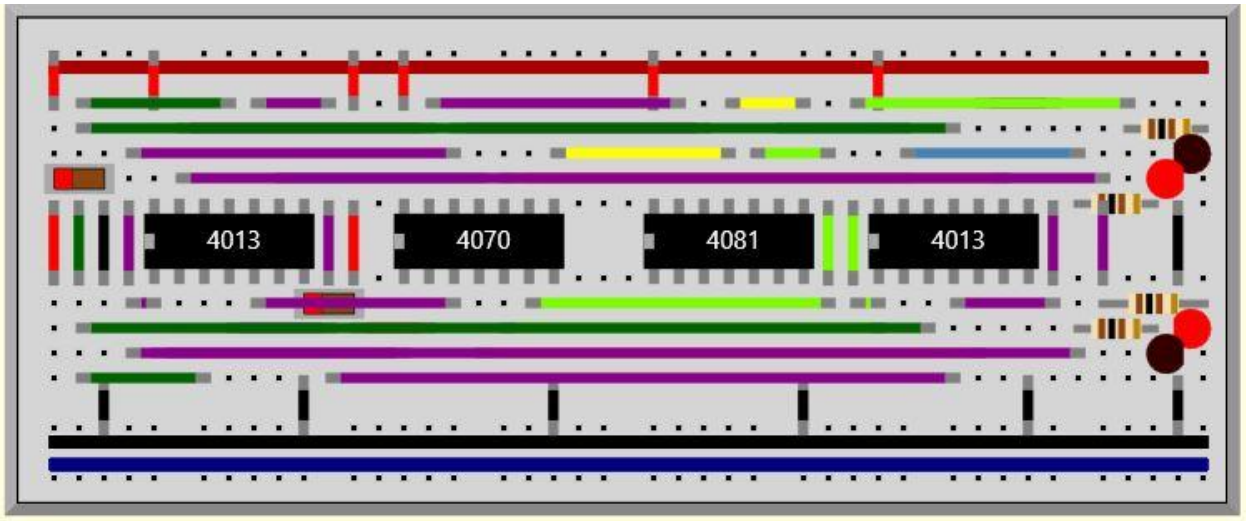

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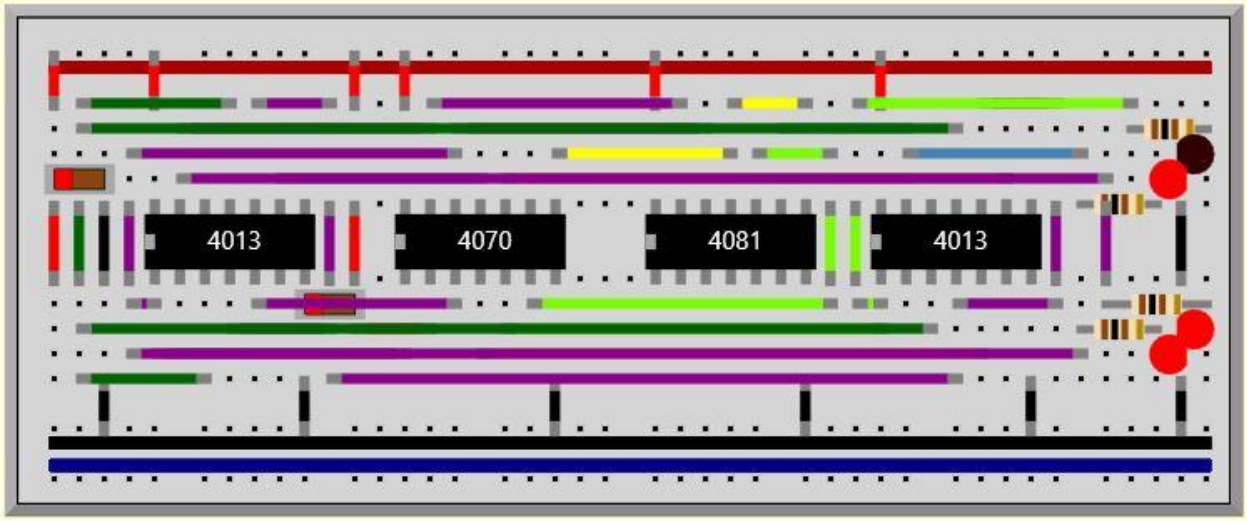

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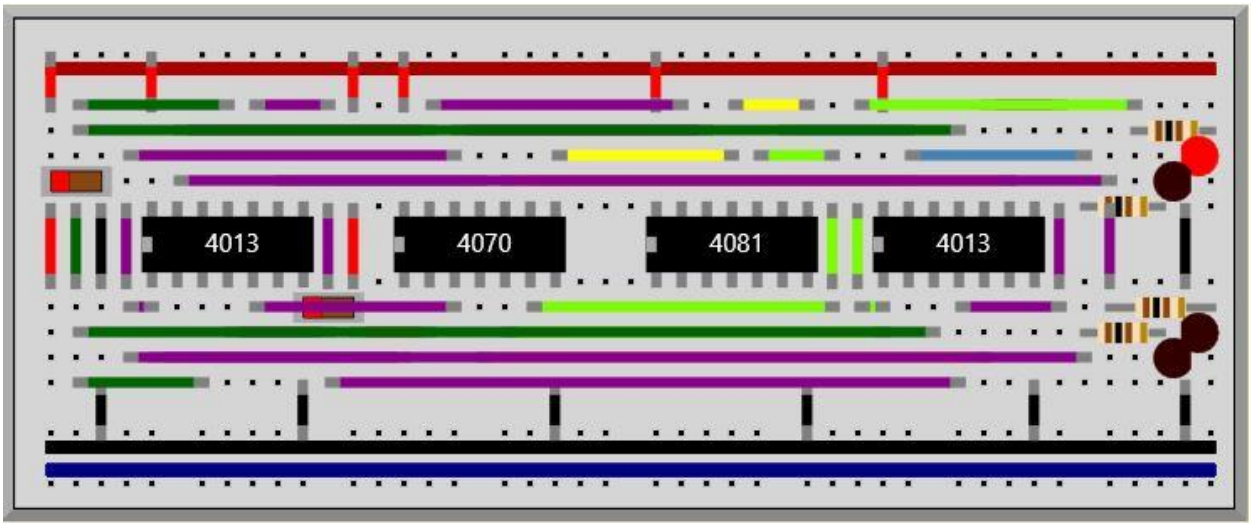

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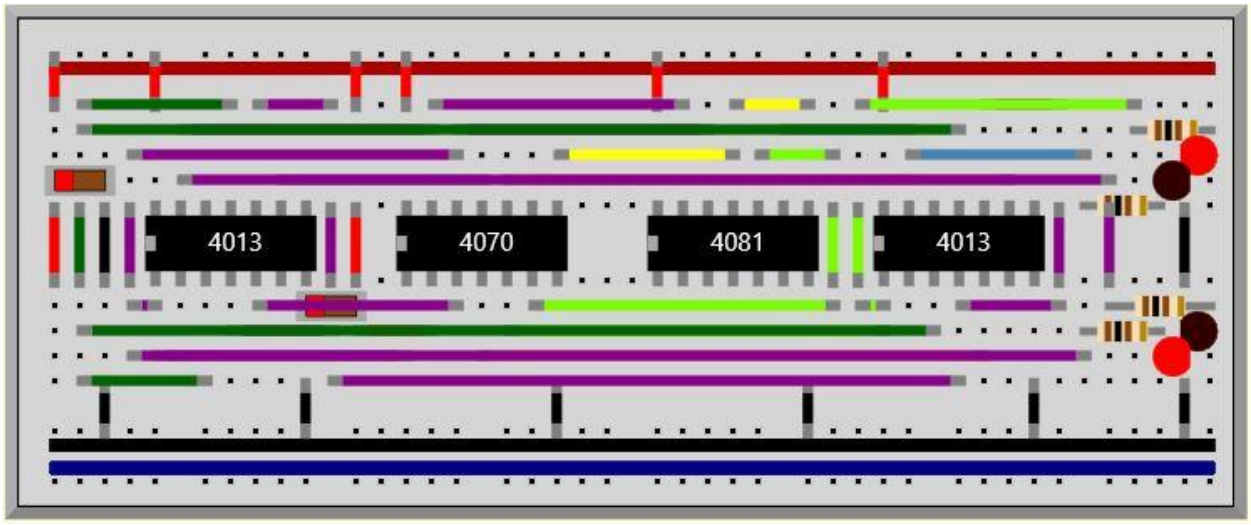

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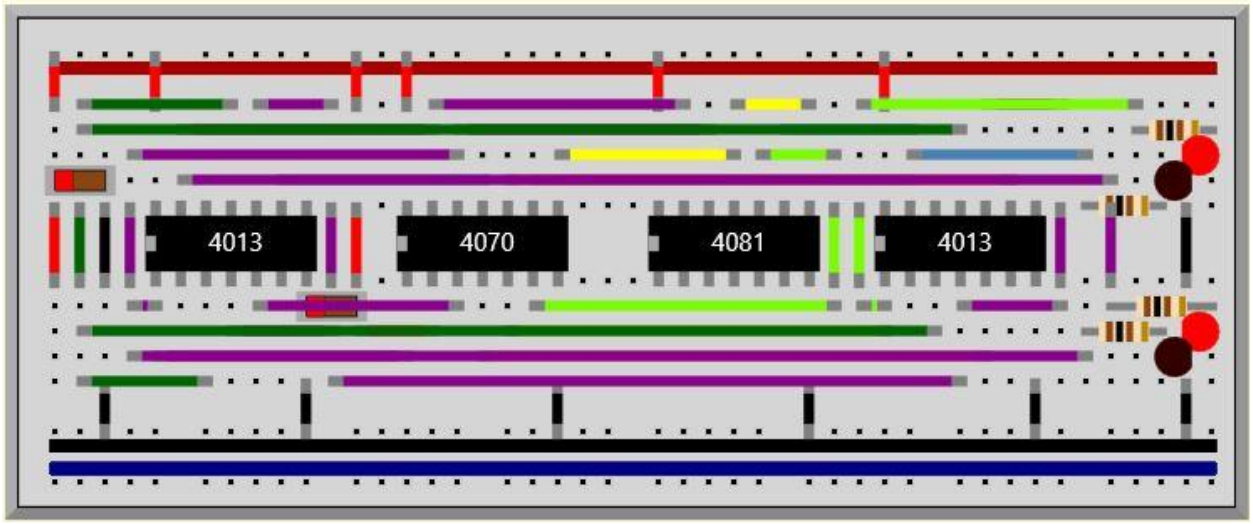

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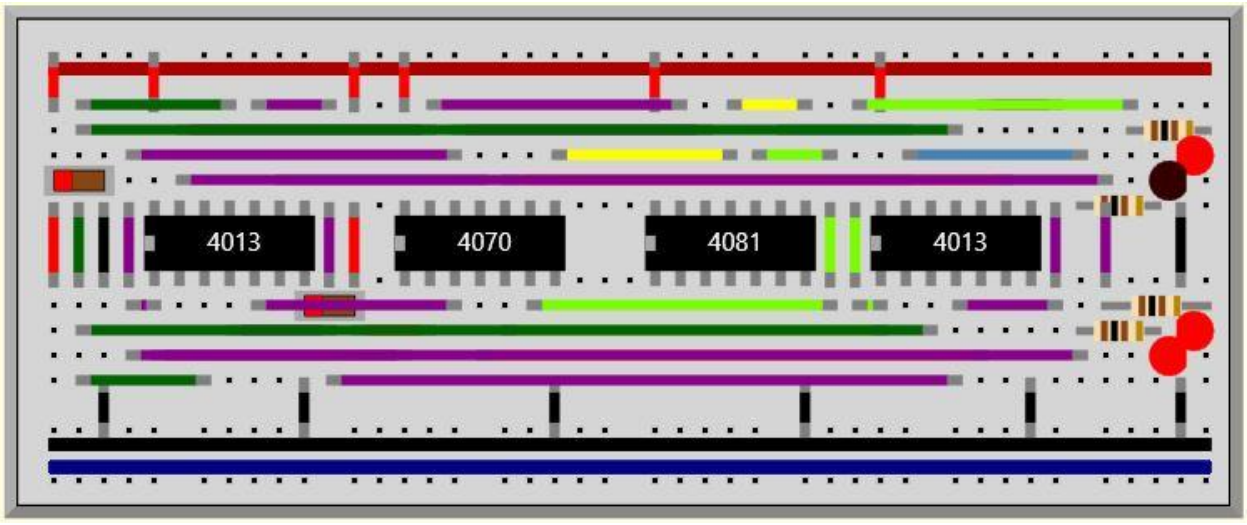

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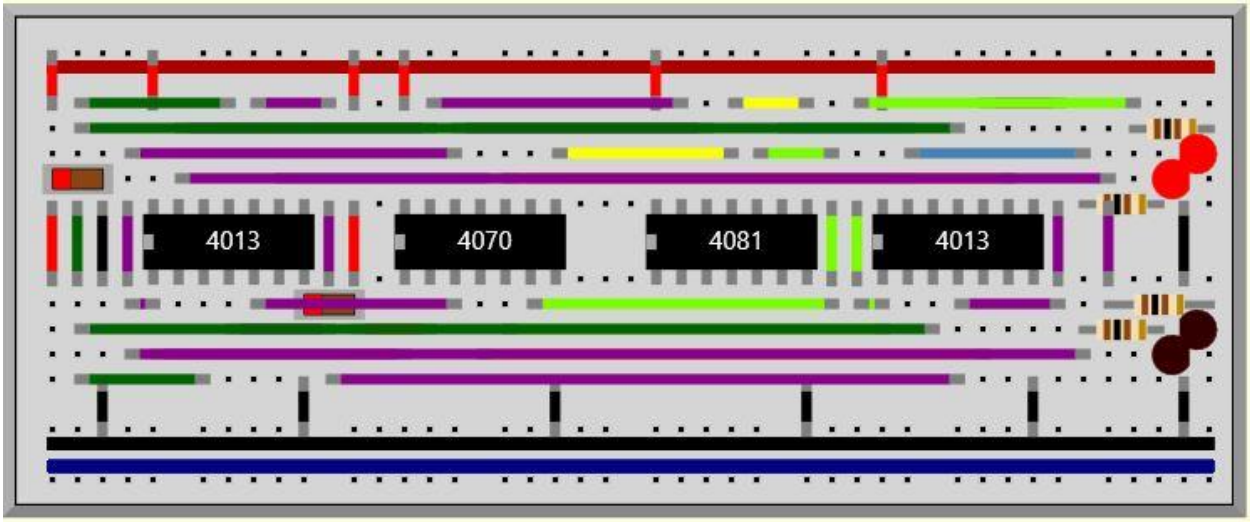

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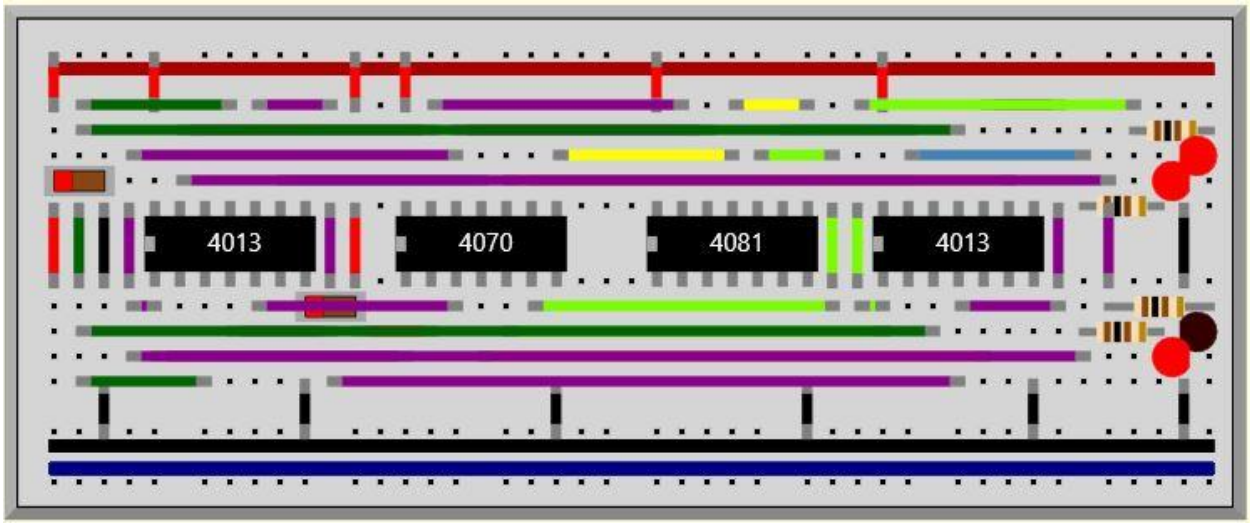

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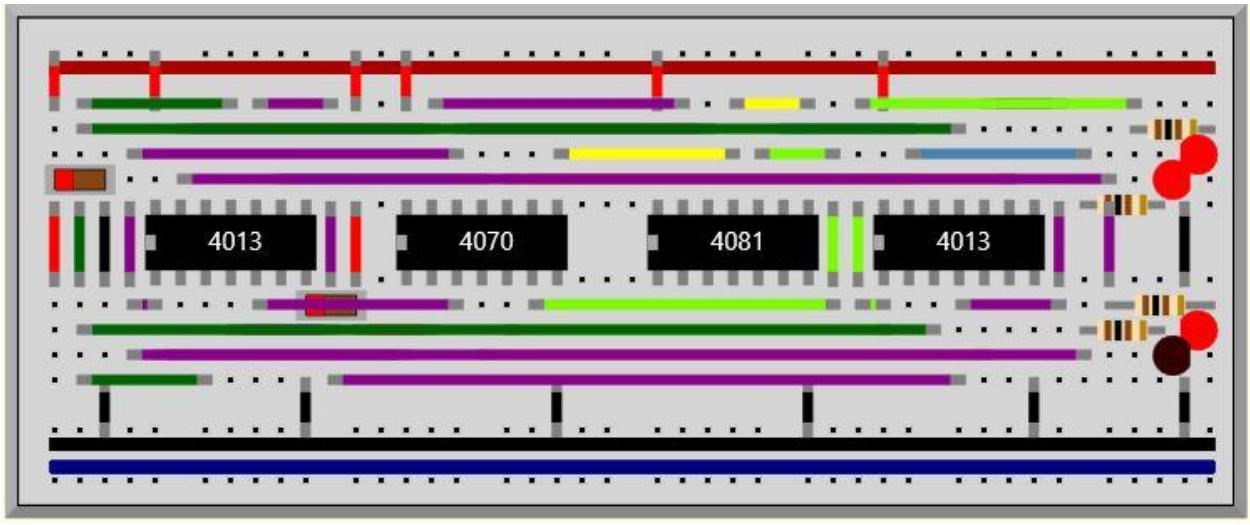

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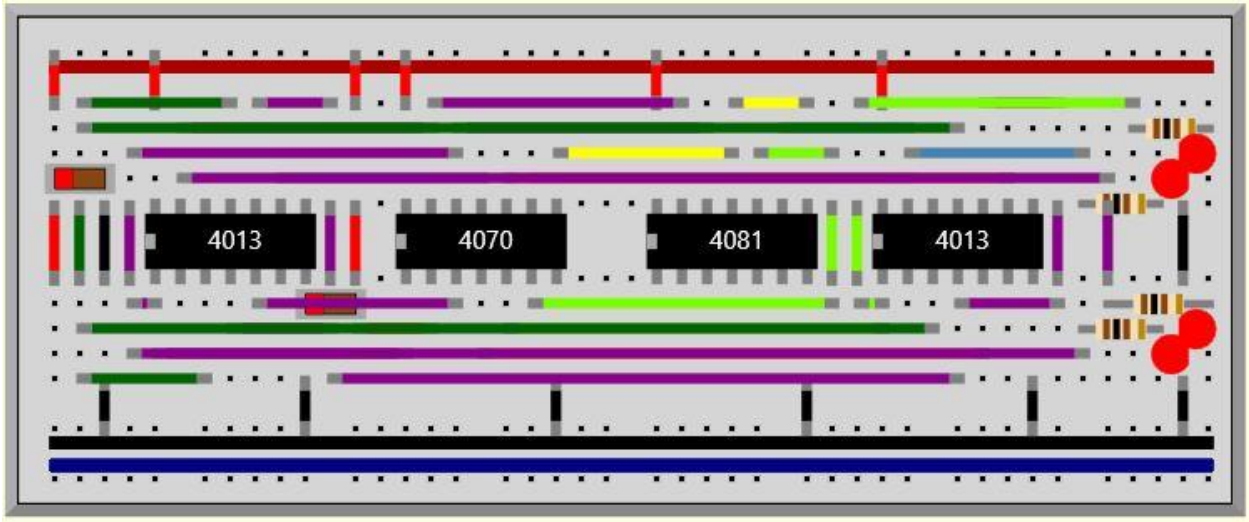
4013
4070
4081
4013