Construction of half/full adder using XOR and NAND gates and verification of its operation

Experiment 2

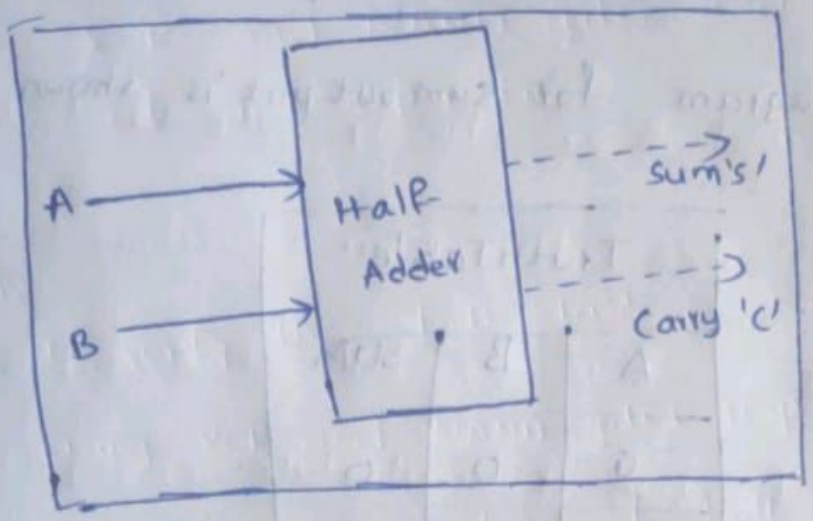
Aim:

To verify the truth table of half adder by using XOR and NAND gates respectively and analyse the working of half adder and full adder circuit with the help of LEDs in stimulator 1 and verify the truthtable only of half adder and full adder in simulator 2.

Theorey:

Introduction

Adders are digital circuits that carry out addition of numbers. Adders are a key component of arithmetic logic unit. Adders can be constructed for the most of the numerical representations like Binary Coded Decimal (BCD) Excess-3, Gray code, Binary etc. out of these binary addition is the mostly frequently performed task by most common adders. A part from addition, adders are also used



Truth Table

Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Block diagram and truth table of half adder

The sum output of the binary addition carried out above is similar to that of Ex-OR operation while the carry output is similar to that of and AND operation. The same can be verified with help of Karnaugh Map.

digital
in certain applications like table index calculation, address decoding etc

Binary addition is similar to that of decimal addition, some basic binary additions are shown below

0	0	1	1
+0	+1	+0	+1
0	1	1	carry 1 0

Schematic representation of half adder

1) Half Adder:

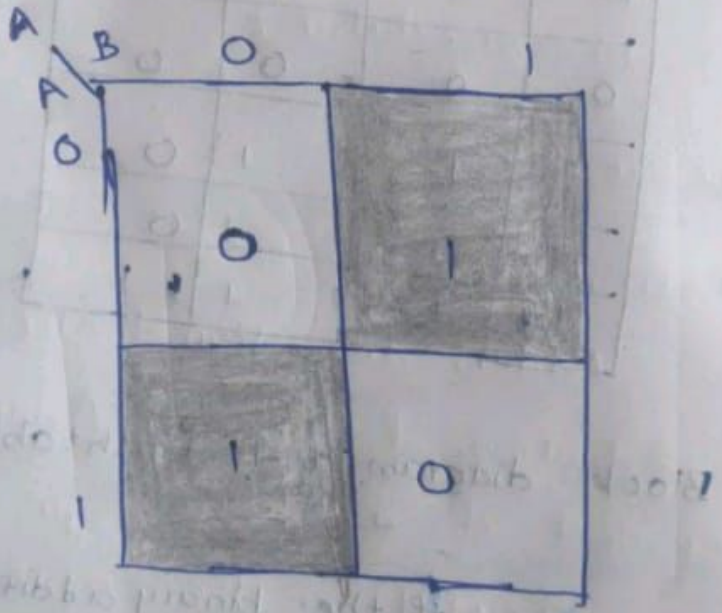
Half adder is a combinational circuit that performs simple addition of two ~~not~~ binary numbers

If we assume A and B as the two bits whose addition is to be performed the block diagram and a truth table for half adder with A, B as inputs and Sum, Carry as outputs can be tabulated as follows

The truth table and K Map simplification and logic diagram for sum output is shown below

Truth Table

A	B	SUM
0	0	0
0	1	1
1	0	1
1	1	0

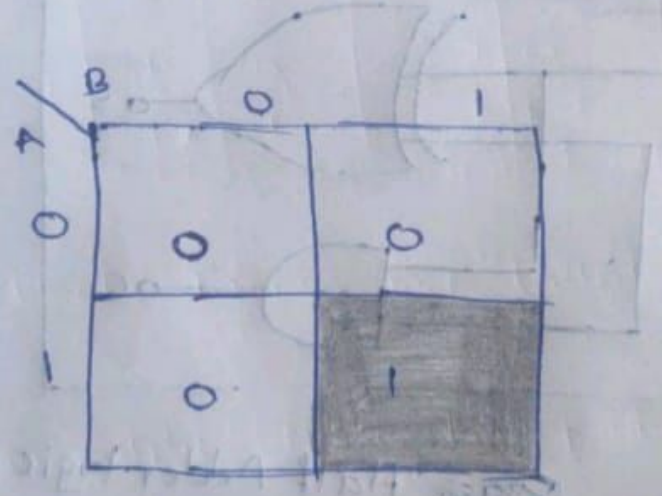


Truth Table, k Map simplification and Logic diagram for sum output of half adder

$$Sum = AB' + A'B$$

The truth table and k Map simplification and logic diagram for carry is shown below.

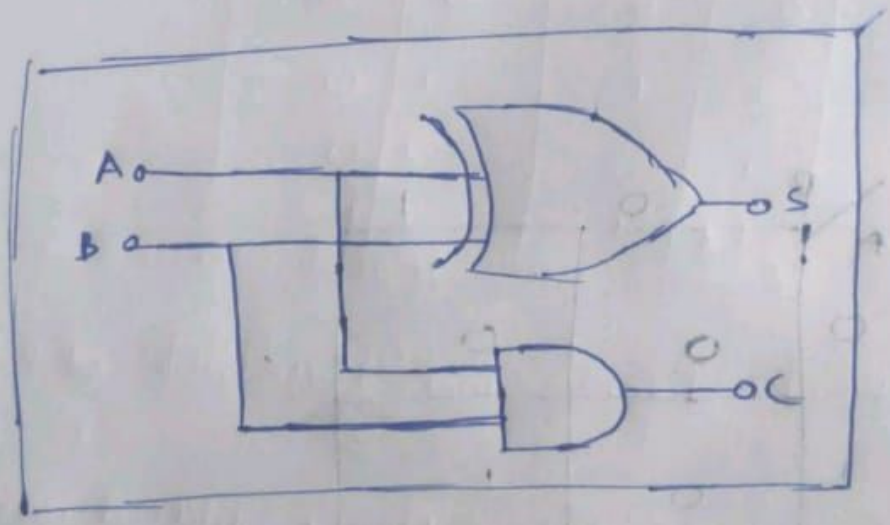
Truth Table		
A	B	Carry
0	0	0
0	1	0
1	0	0
1	1	1



Truth Table, k Map simplification & logic diagram for sum output of half adder.

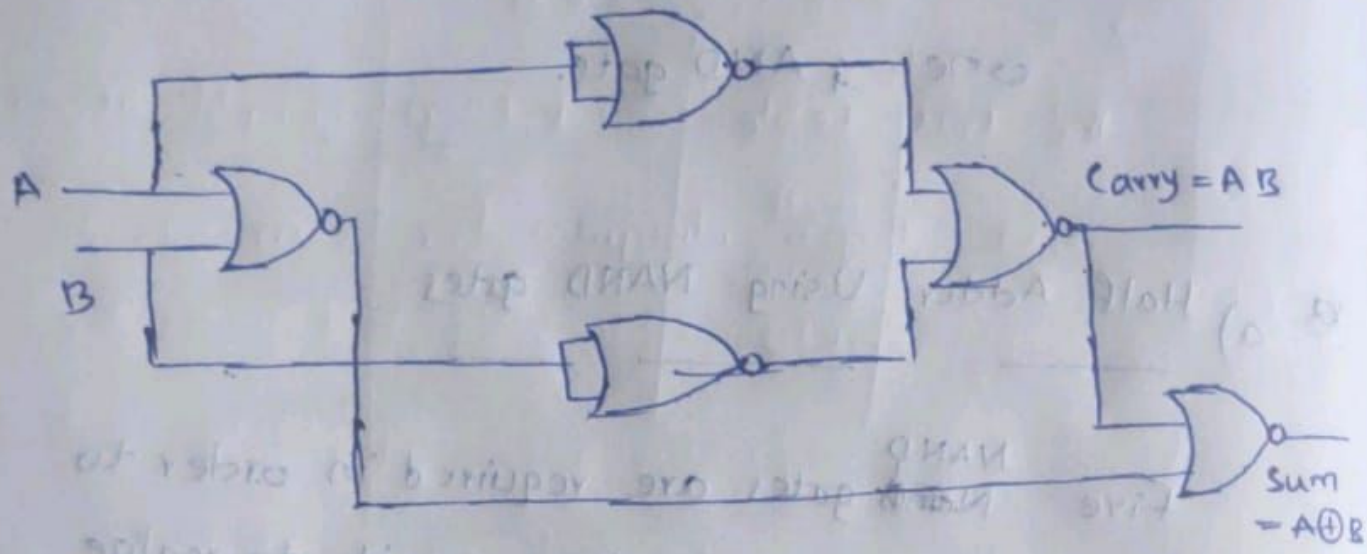
Carry = AB

If A and B are binary outputs, to the half adder, then the logic function to calculate ~~carry~~ sum S is Ex-OR of A and B and logic function to calculate carry C is AND of A and B. Combining these two, the logical circuit to implement the combinational circuit of half adder is shown below.



Half Adder logic diagram.

As we know that NAND and NOR are called universal gates as any logic system can be implemented using these two, the half adder circuit can also be implemented using them. We know that a half

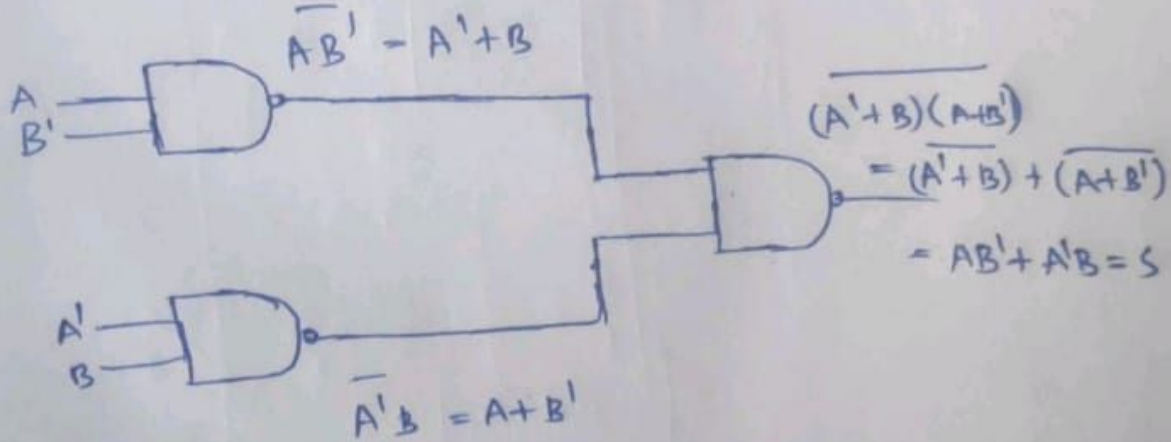


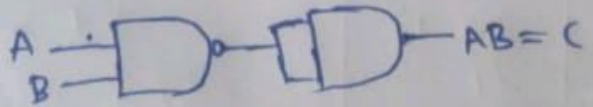
Realization of half adder
using NAND gates

adder Circuit has one Ex-OR gate and one AND gate.

a) Half Adder Using NAND gates

Five NAND gates are required in order to design a half adder. The circuit to realize half adder using NAND gates is shown below.





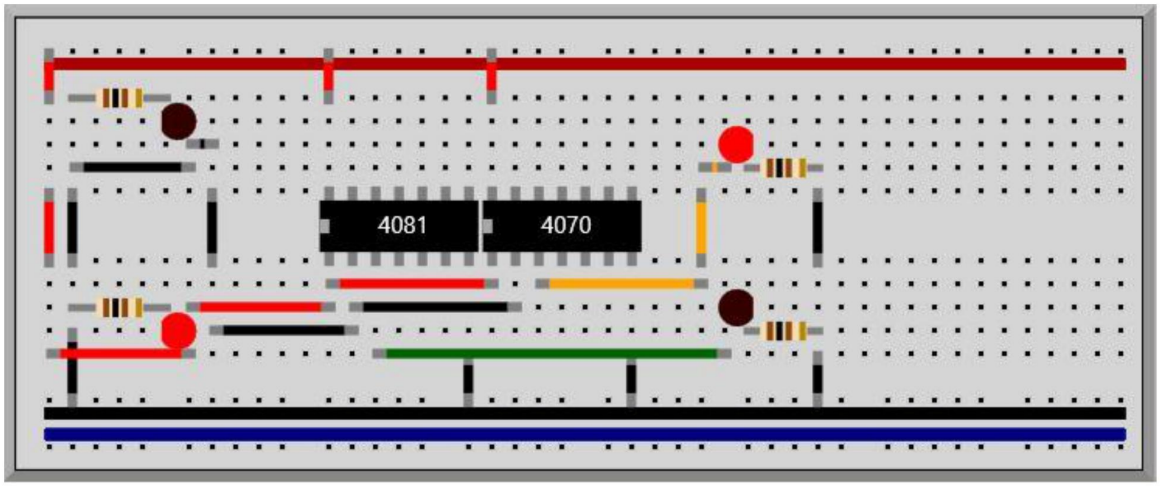
Realization of half adder using NAND gates.

b) Half Adder Using NOR gates

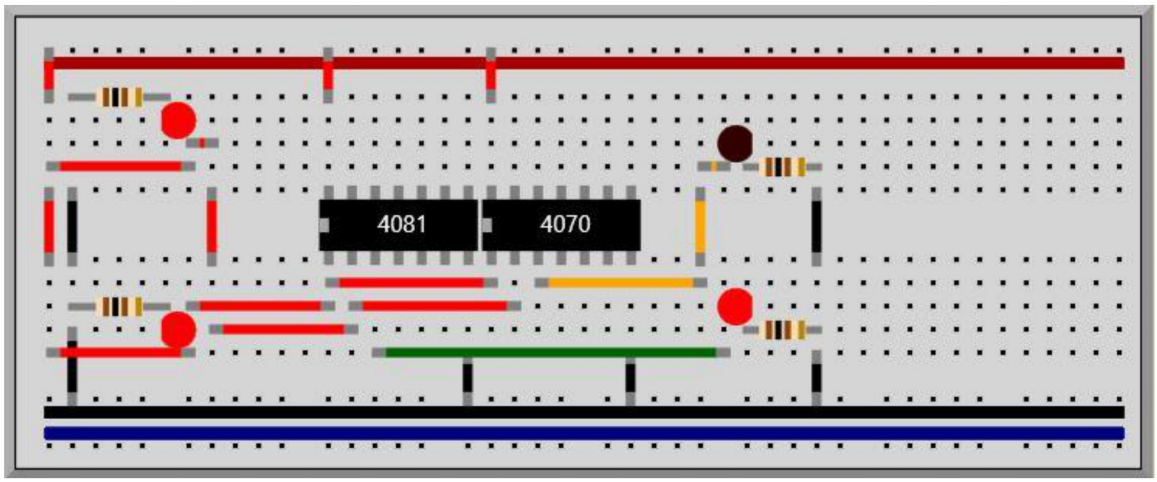
Five NOR gates are required in order to design a half adder. The circuit to realize half adder using NOR gates is shown below.

Half Adder

Input:0 1, Output:Sum:1, Carry:0



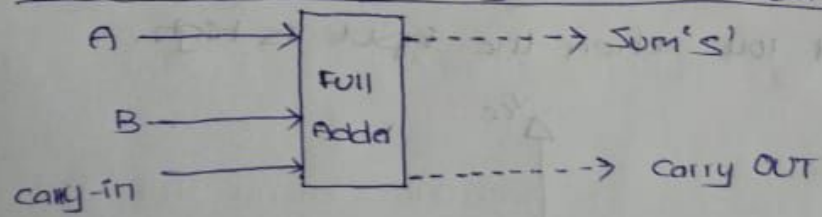
Input:1 1, Output:Sum:0, Carry:1



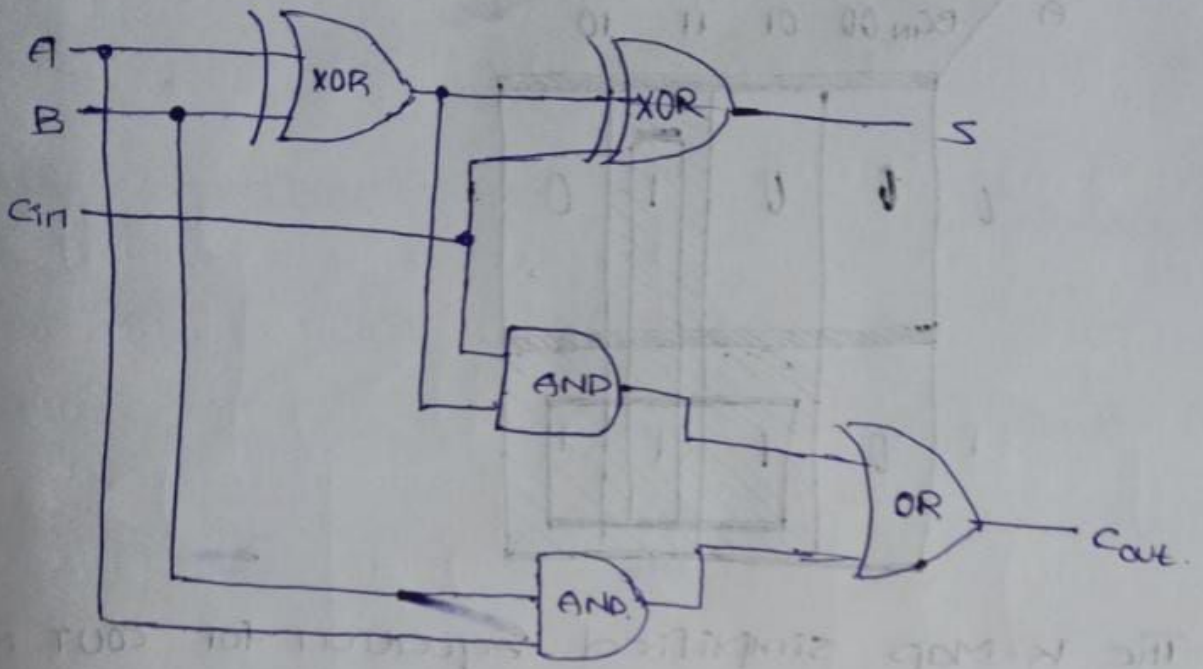
2) full Adder

→ It is a digital circuit used to calculate the sum of three Binary bits. full adders are complex and difficult to implement when compared to half adders. Two of the three bits are same as before which are A. The augend bit and B, the addend bit. The additional third bit is carry bit from the previous stage and is called 'carry' - in generally represented by & CIN. It calculates the sum of three bits along with the carry. The output carry is called carry-out and is respresented by carry OUT.

⟺ FULL Adder BLOCK Diagram and Truth Table :-

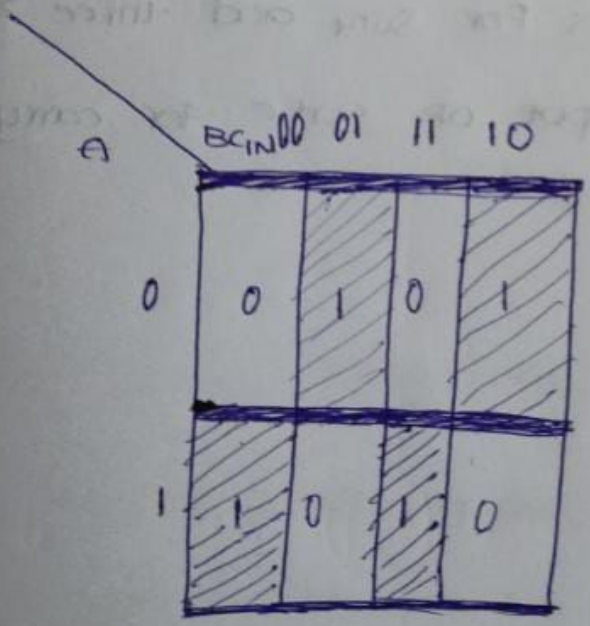


Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	0	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



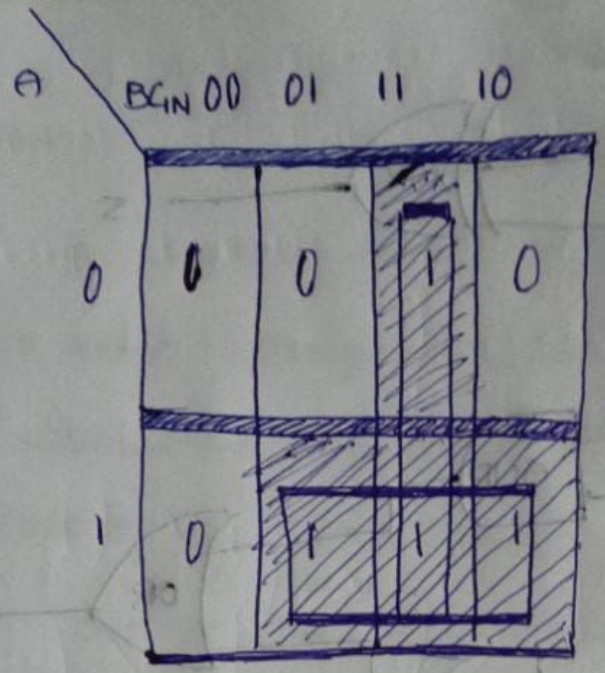
: Full Adder Logic Diagram

Based on the truth table, the Boolean function for sum (S) and carry-out (COUT) derived using K-Map



→ The K-Map simplified equation for sum is

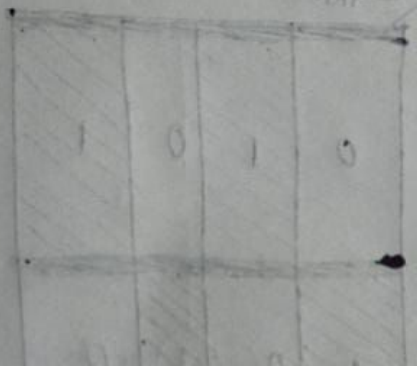
$S = A'B'C_{in} + A'BC_{in}' + ABC_{in}$



:-The K-Map simplified equation for COUT is

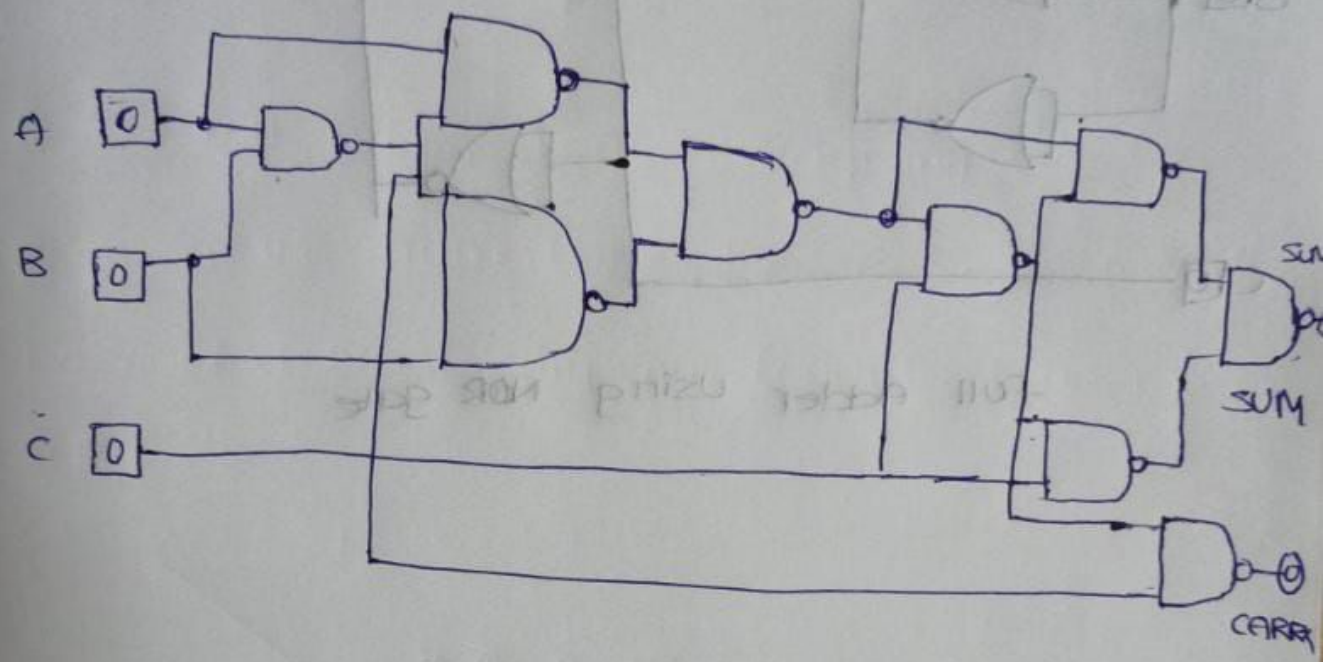
$$COUT = AB + ACIN + BCIN$$

In order to implement a combinational circuit for full adder, it is clear from the equations derived above, that we need four 3-input AND gates and one 4-input OR gates for Sum and three 2-input AND gates and one 3-input OR gate for carry-out.



(2.1) Full Adder using NAND gates

→ As mentioned earlier, a NAND gate is one of the universal gates and can be used to implement any logic design. The circuit of full adder using only NAND gates is:

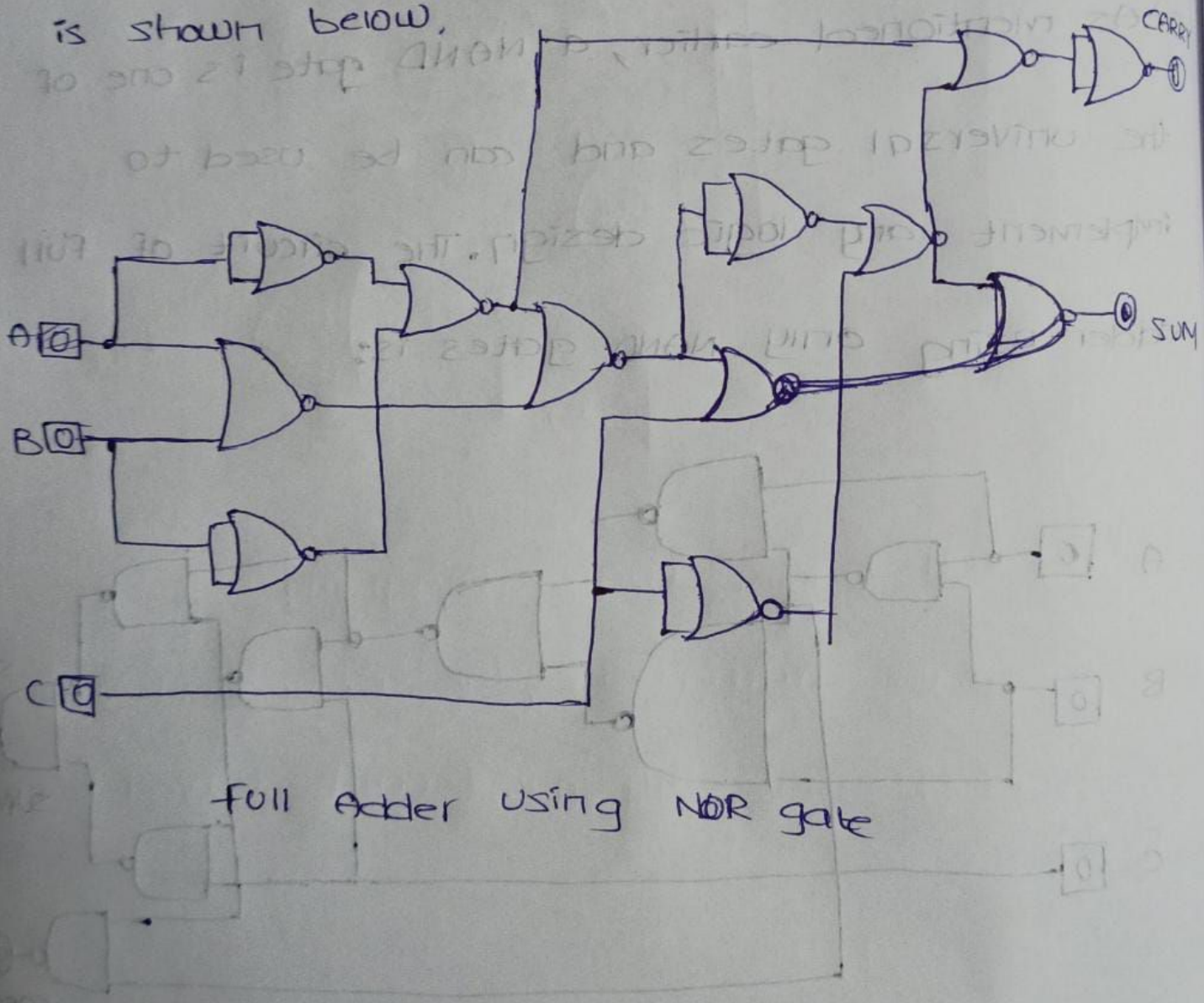


% Full Adder using NAND Gates

(2.2) Full Adder using NOR gates

→ As mentioned earlier, a NOR gate is one of the universal gates and can be used to implement any logic design.

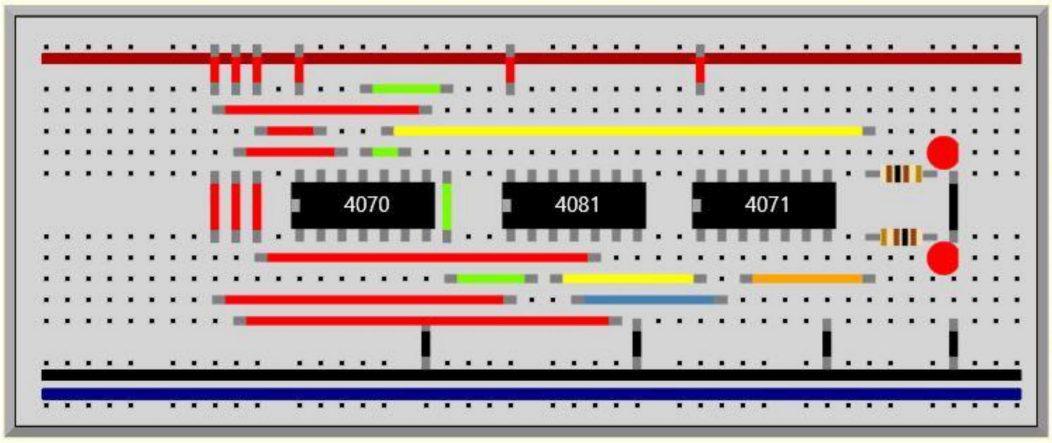
The circuit of full adder using only NOR gate is shown below,



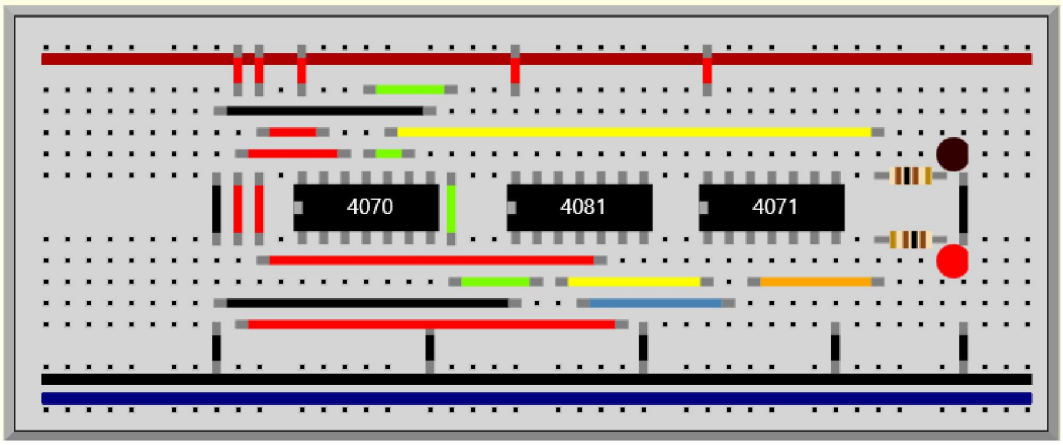
Full Adder using NOR gate

Full Adder

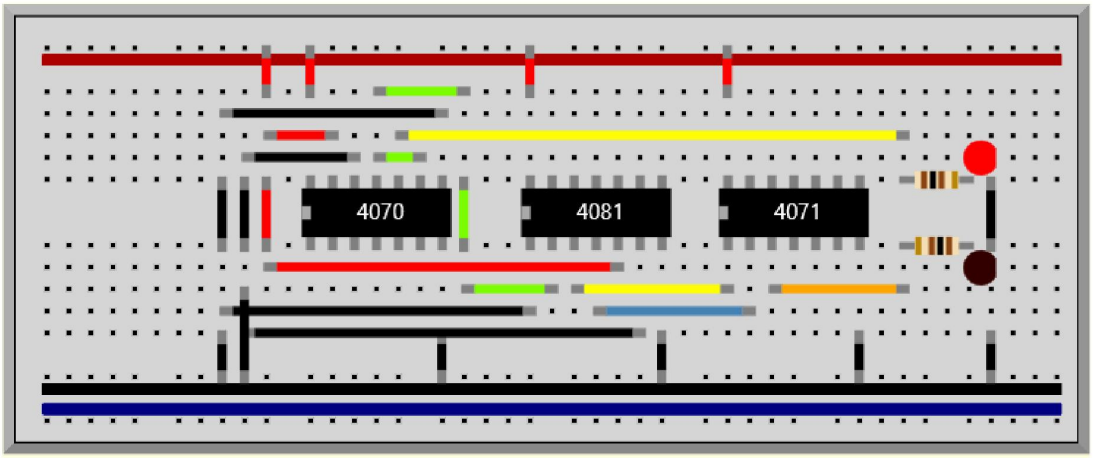
Input:1 1 1,Output:Sum:1,Carry:1



Input:1 1 0,Output:Sum:0,Carry:1



Input:1 0 0,Output:Sum:1,Carry:0



Input:0 0 0,Output:Sum:0,Carry:0