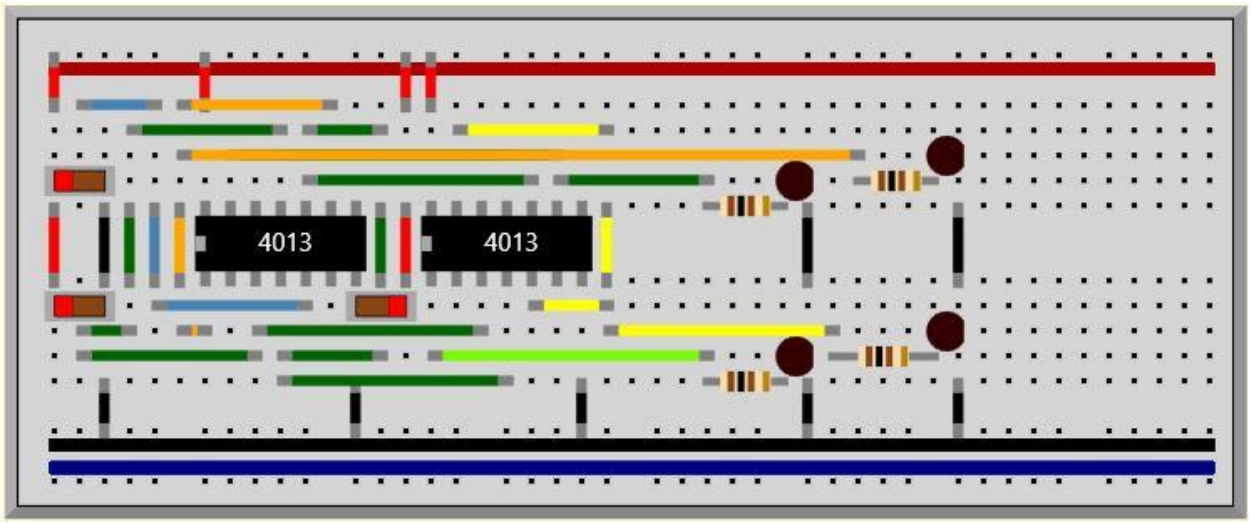
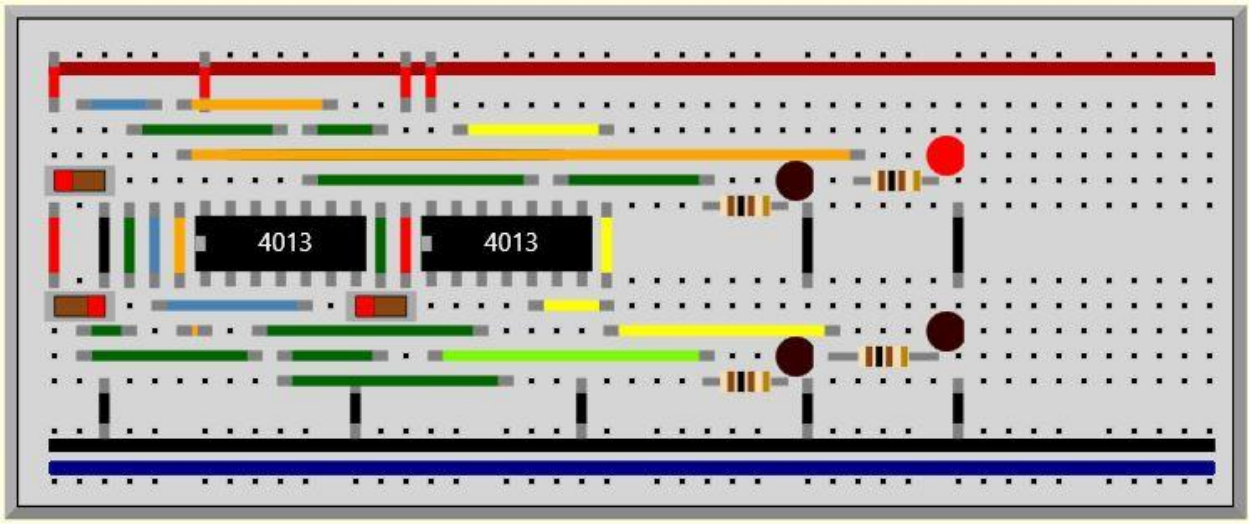
Design and Verify the 4-Bit Serial In - Parallel Out Shift Registers.

On every posedge of CLK output changes

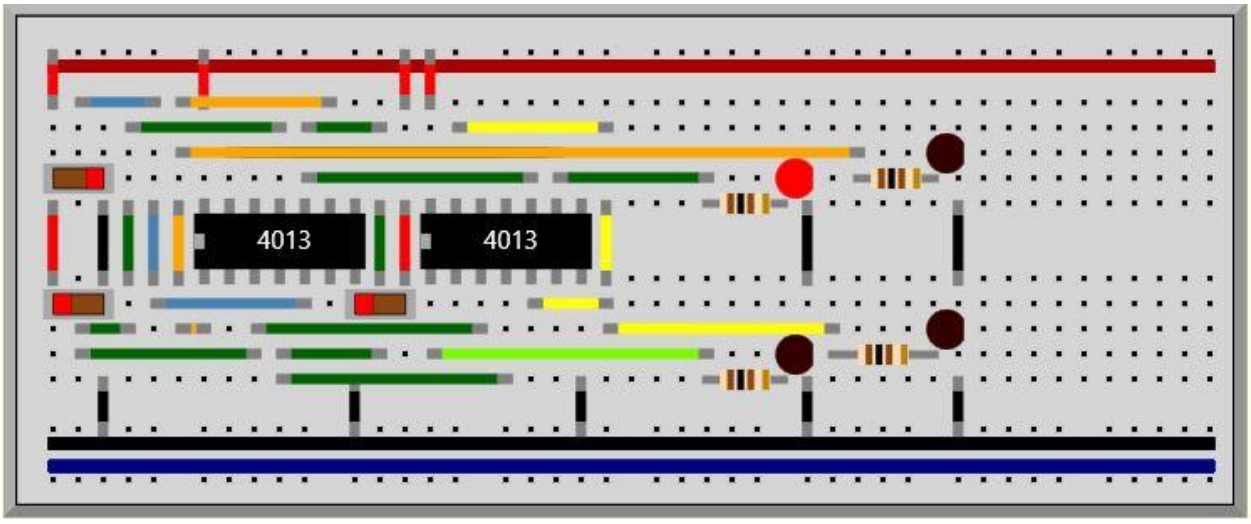
Step 1 . Reset:1 Output:0000



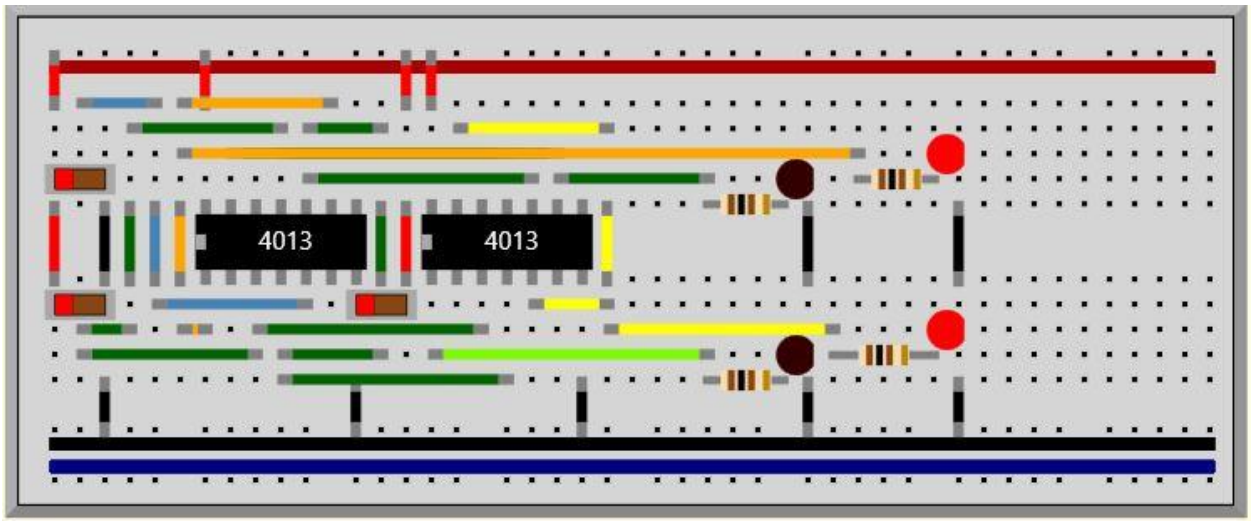
Step 2 . D:1 Output:0001(after posedge of CLK)



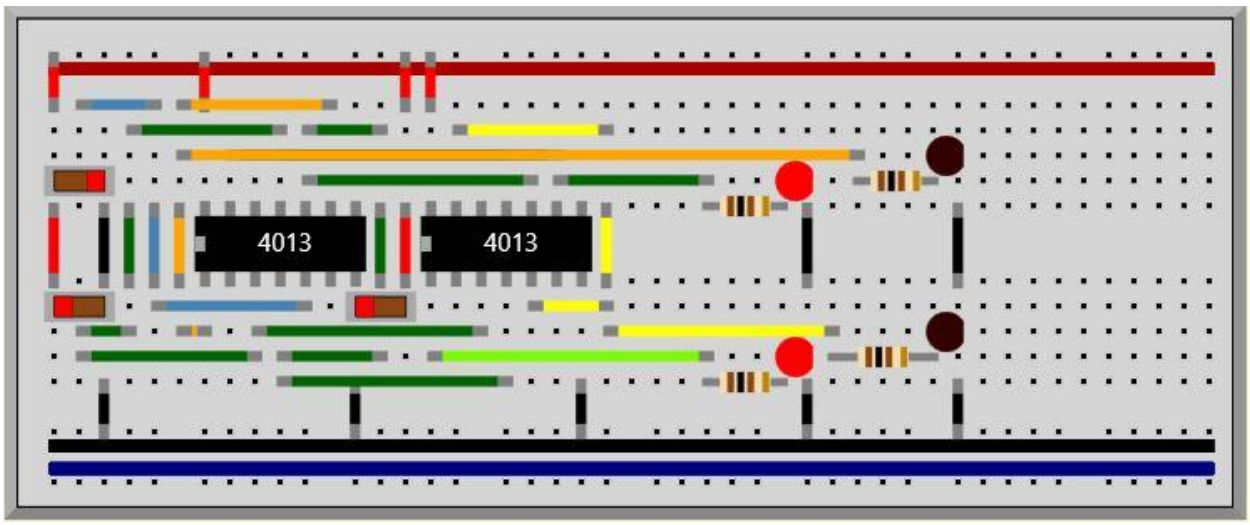
Step 3 . D:0 Output:0010(after posedge of CLK)



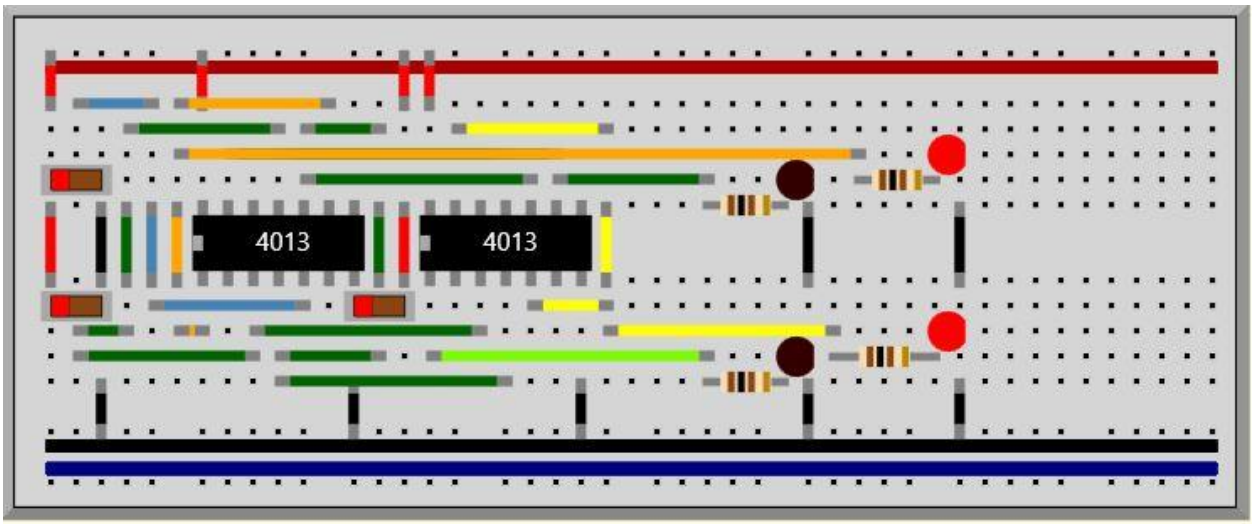
Step 4 . D:1 Output:0101(after posedge of CLK)



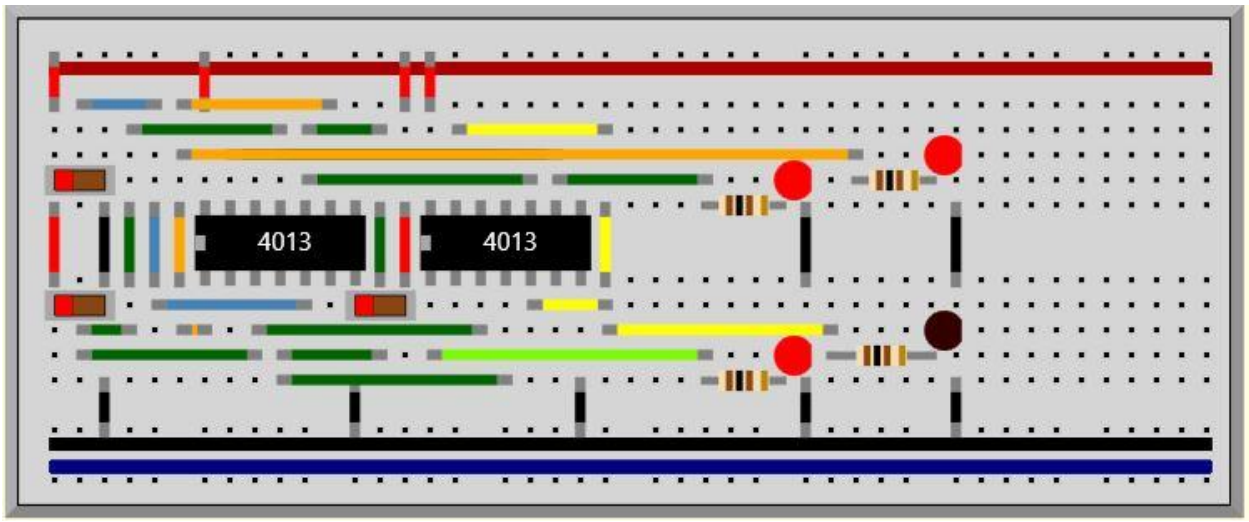
Step 5 . D:0 Output:1010(after posedge of CLK)



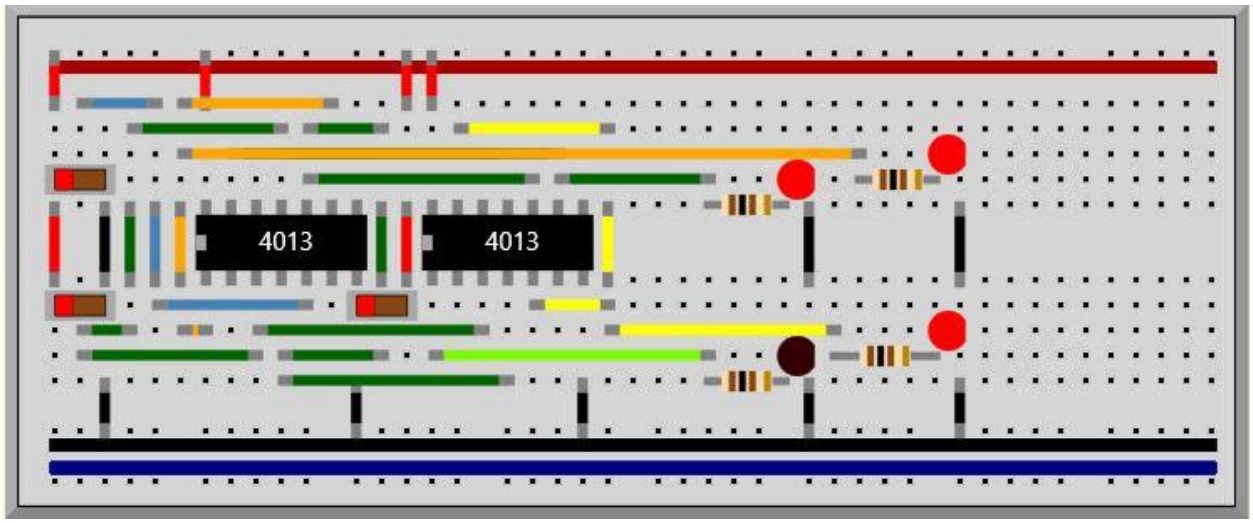
Step 6 . D:1 Output:0101(after posedge of CLK)



Step 7 . D:1 Output:1011(after posedge of CLK)



Step 8 . D:1 Output:0111(after posedge of CLK)



Step 9 . D:1 Output:1111(after posedge of CLK)