EC-273

Digital Circuit And Systems Lab
Experiment 5–6

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Experiment 5

Aim:

To analyse the truthtable of 4*2 decoder/de-multiplexer using NOT (7404 and AND(7408) logic gate ICs and 2*4 encoder using OR (7403) logic gate IC and to understand the working of 4*2 decoder and 2*4 encoder circuit with the help of LEDs display.

Theory:-

Binary code of N digits can be used to store 2^N distinct elements of coded information. This is what encoders are decoders are used for ENcoders convert 2^N lines of input into a code of N bits and Decoders decode the N bits into 2^N lines.

(1) 2x4 Decoder/De-multiplexer

The name "Decoder" means to translate or decode coded information from oneformat into another.

A decoder is a combirational circuit that converts binary information from n input lines to a maximum of $m=2^n$ unique output lines.

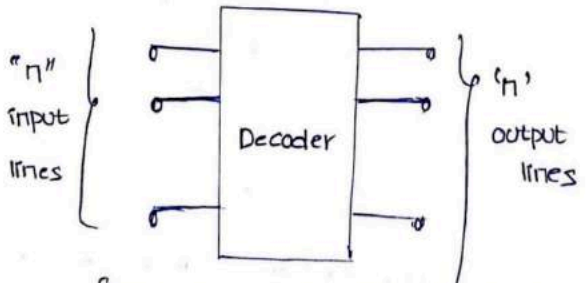


figure 1. Logic Diagram of Decoder.

(1.1) 2-to-4 Binary Decoder

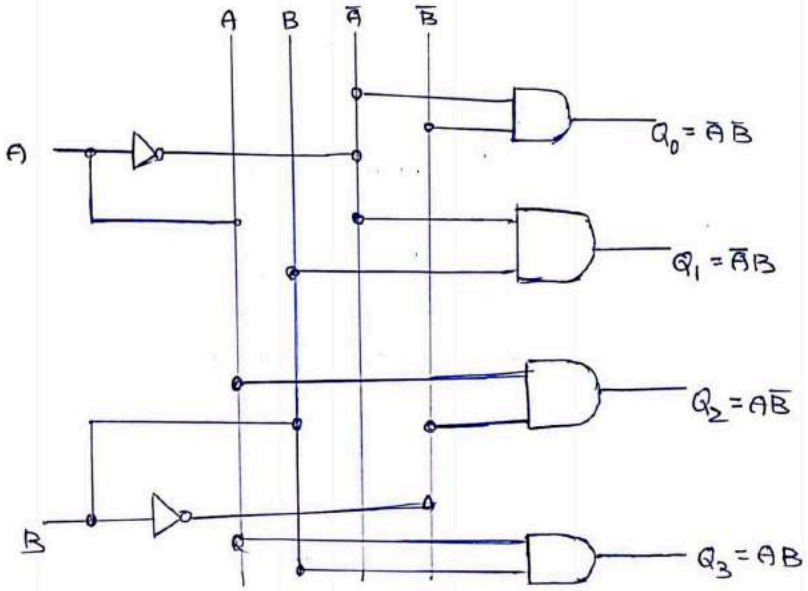
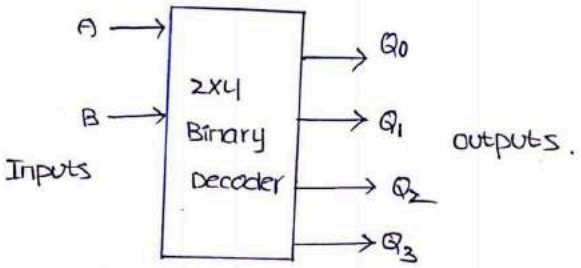


figure 2. Circuit Diagram of 2-to-4 Decoder.

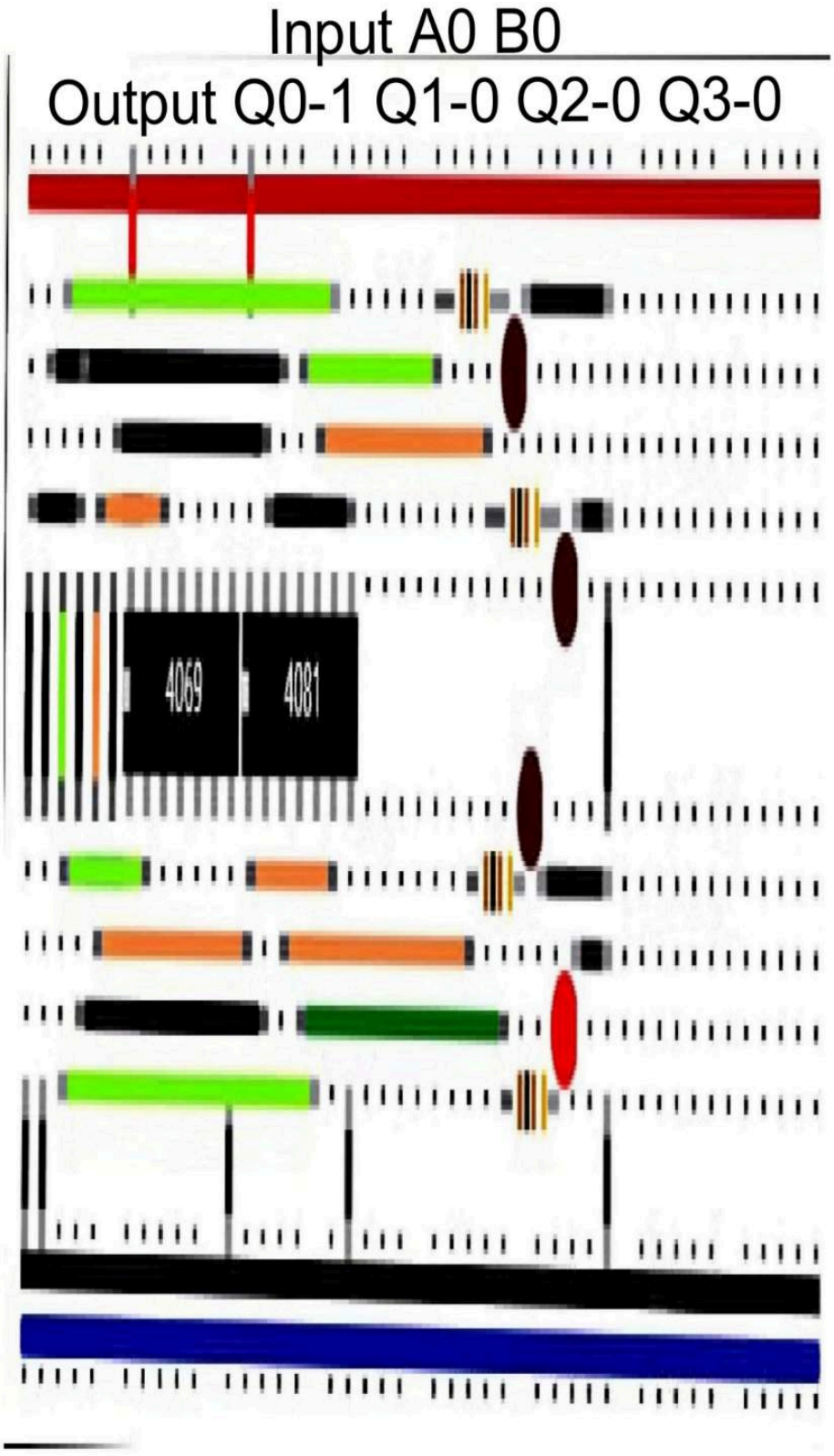
The 2-to-4 line binary decoder depicted above consists of an array of four AND gates. The 2 binary inputs labelled A and B are decoded into one of 4 outputs. (each output = a minterm).



A	B	Q_0	Q_1	Q_2	Q_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

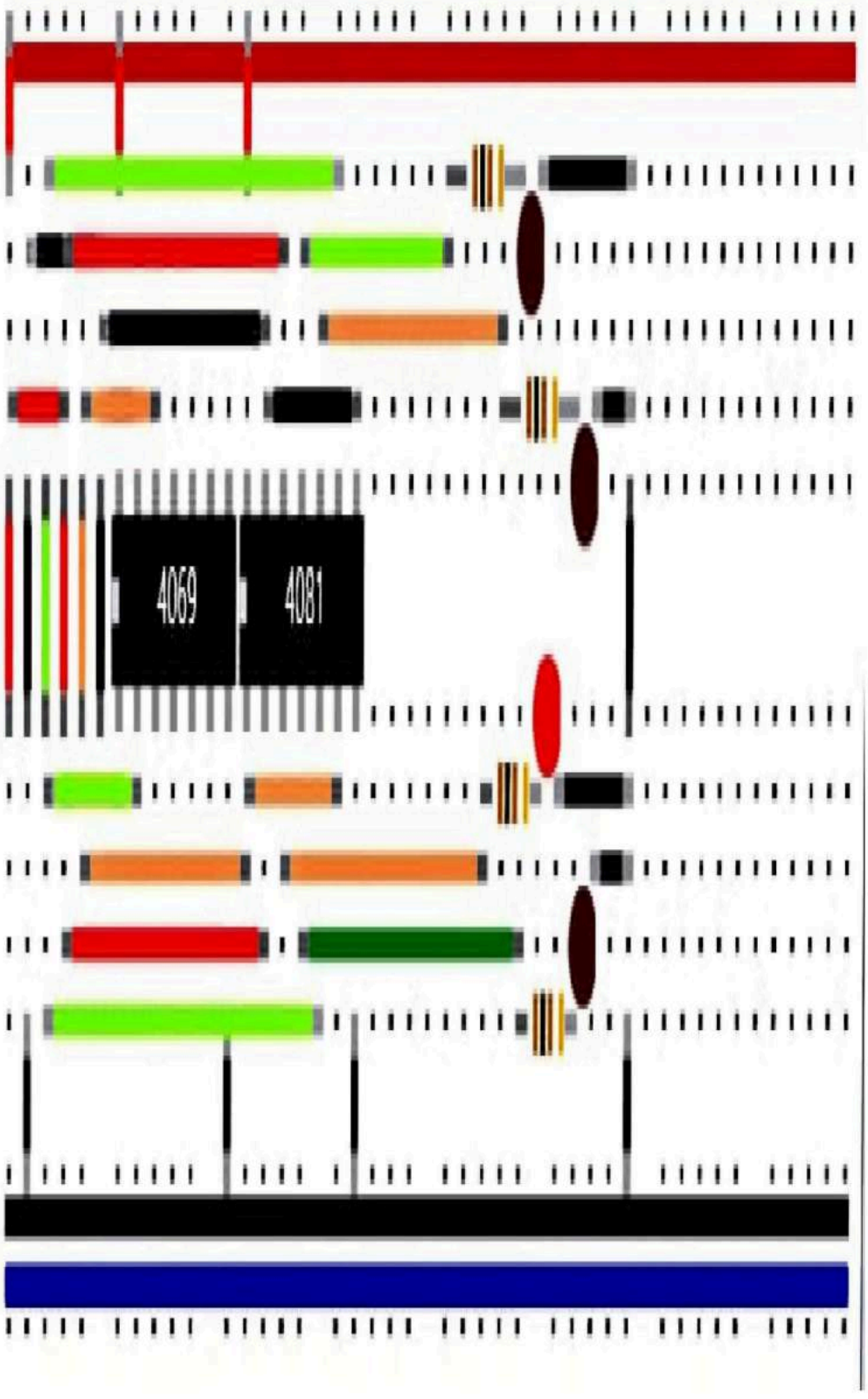
figure 3: Logic Diagram and Truth table of 2-to-4 Decoder

DECODER



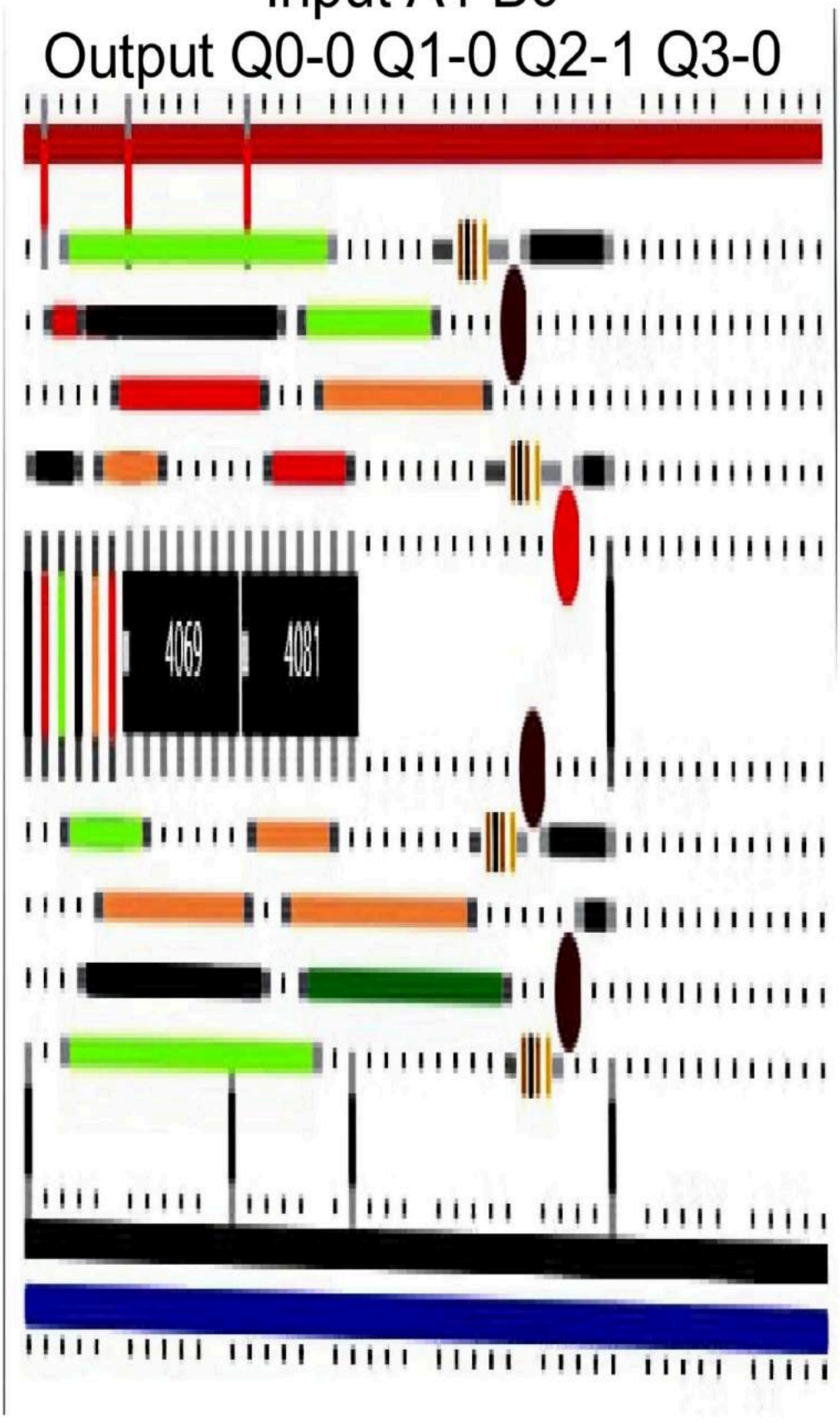
Input A0 B1

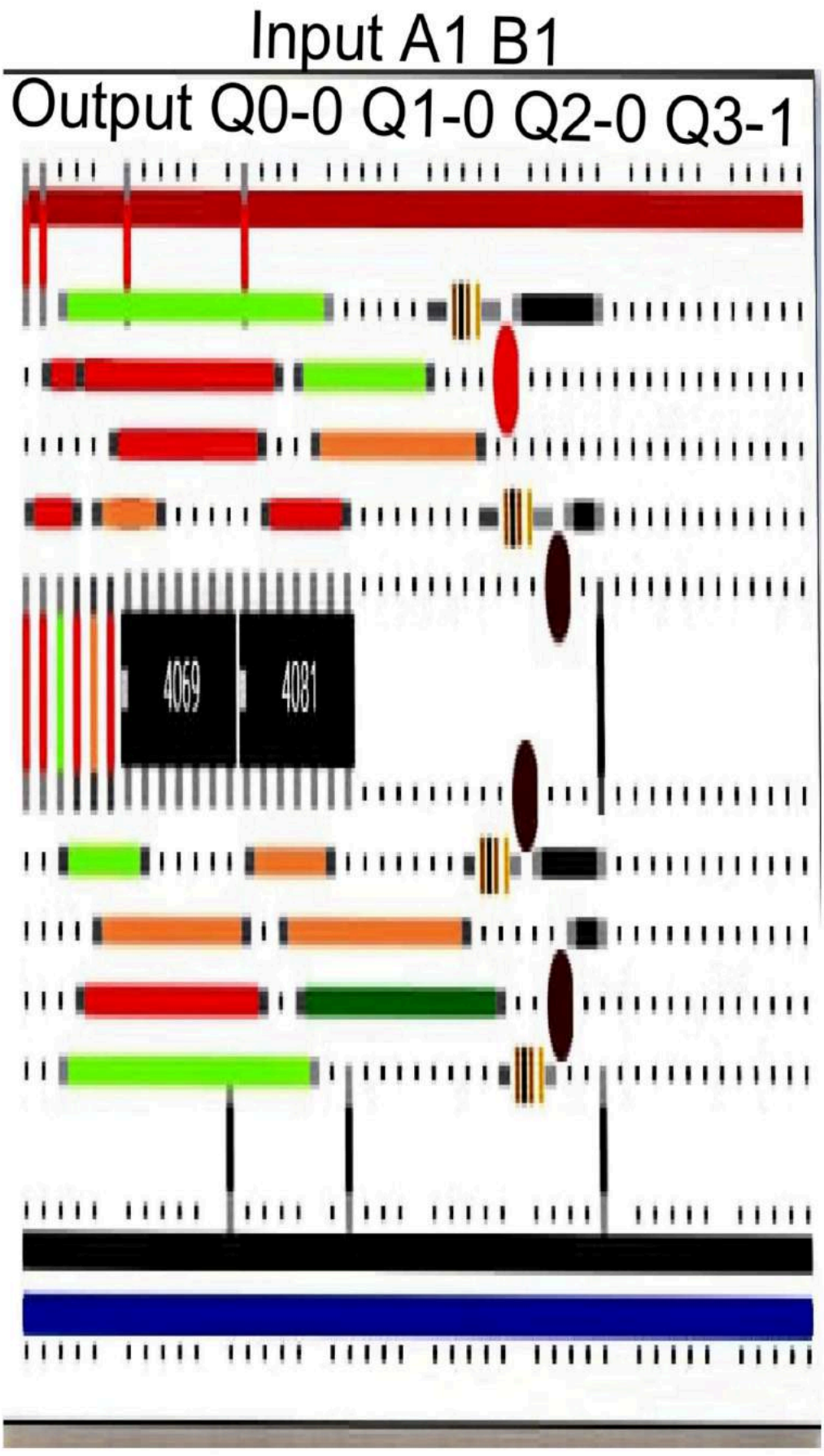
Output Q0-0 Q1-1 Q2-0 Q3-0



Input A1 B0

Output Q0-0 Q1-0 Q2-1 Q3-0




Input A1 B1
Output Q0-0 Q1-0 Q2-0 Q3-1
4069
4081

→ The binary inputs A and B determine which output line from Q_0 to Q_3 is "HIGH" at logic level "1" while the remaining outputs are held "LOW" at logic "0" so only one output can be active (HIGH) at any one time.

→ Some binary coders have an additional input pin labelled "ENABLE" that controls the outputs from the device. This extra input allows the decoders outputs to be turned "ON" or "OFF" as required.

Hence, If Enable is 0, All AND gates are supplied with one of the inputs as 0 and hence no output is produced. when Enable is 1, the AND gates get one of the inputs as 1.

→ output of the decoder is dependent on whether the Enable is High or low.

(2) Encoder:

An Encoder is a combinational circuit that performs the reverse operation of Decoder. It has maximum of 2^n input lines and 'n' output lines. It will produce a binary code equivalent to the input, which is active high. Therefore, the encoder encodes 2^n input lines with 'n' bits

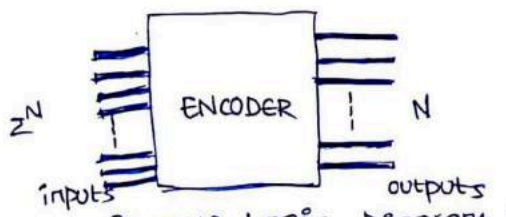
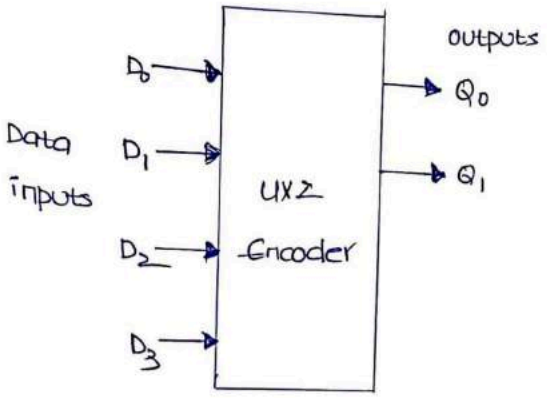


figure 4:- Logic Diagram of ENCODER

2.1) 4:2 Encoder:-

The 4 to 2 Encoder consists of four inputs Y_3, Y_2, Y_1 & Y_0 and two outputs A_1 & A_0. At any time, only one of these 4 inputs can be '1' in order to get the respective binary code at the output.



Inputs				Outputs	
D_3	D_2	D_1	D_0	Q_1	Q_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1
0	0	0	0	x	x

figure 5: Logic symbol and truth table of 4to2 encoder.

$$Q_1 = \overline{D_3} D_2 \overline{D_1} \overline{D_0} + D_3 \overline{D_2} \overline{D_1} \overline{D_0}$$

$$Q_0 = \overline{D_3} \overline{D_2} D_1 \overline{D_0} + D_3 \overline{D_2} \overline{D_1} \overline{D_0}$$

$$= \overline{D_2} \overline{D_0} \left[\overline{D_3} D_1 + D_3 \overline{D_1} \right]$$

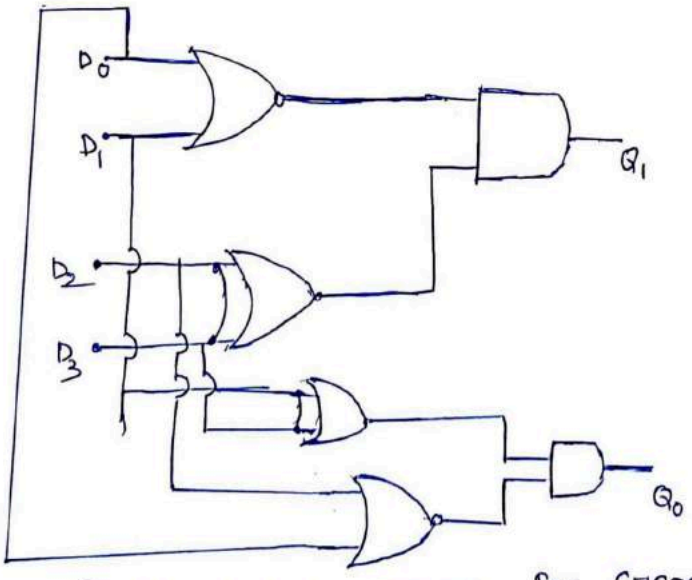
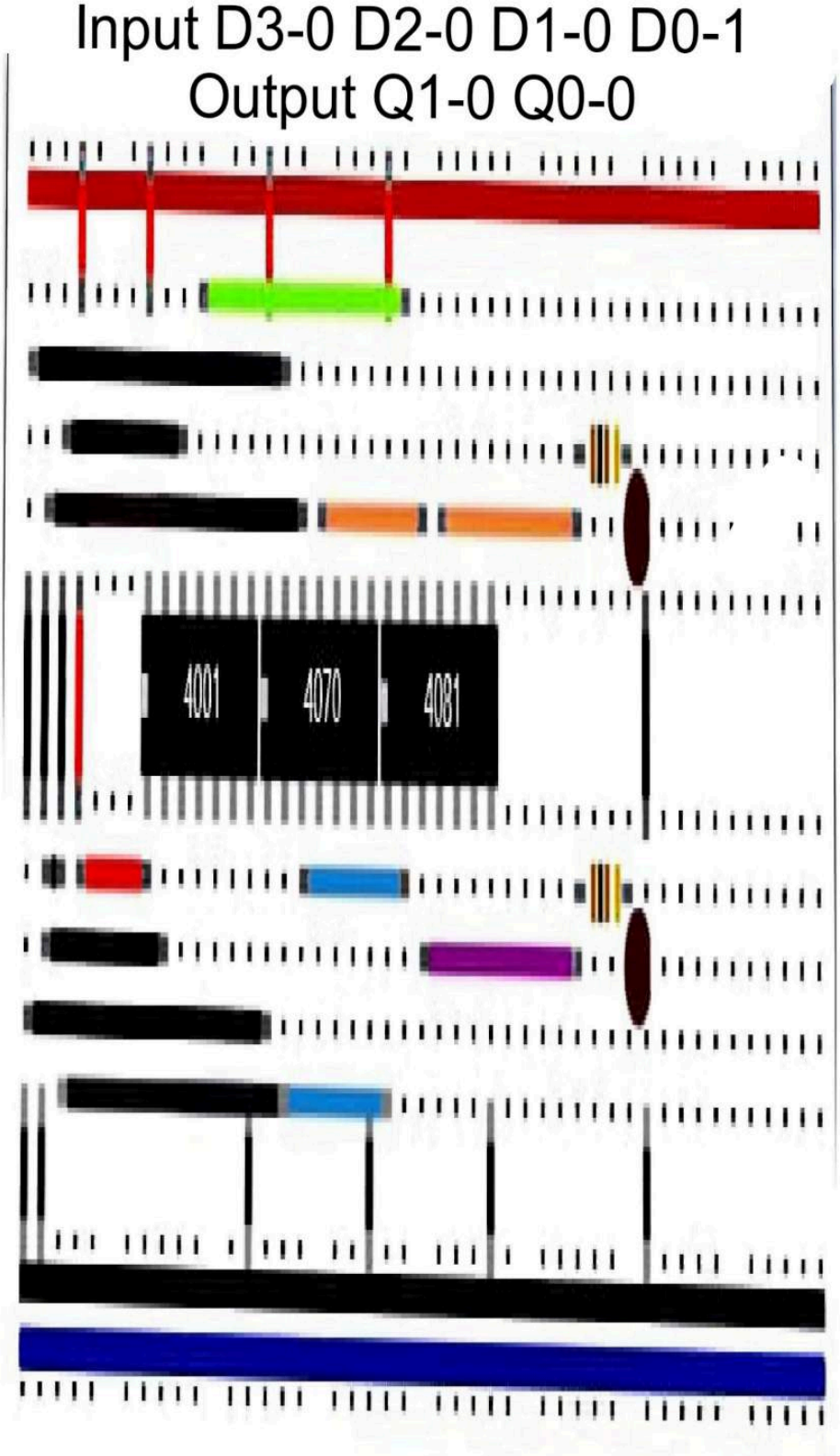
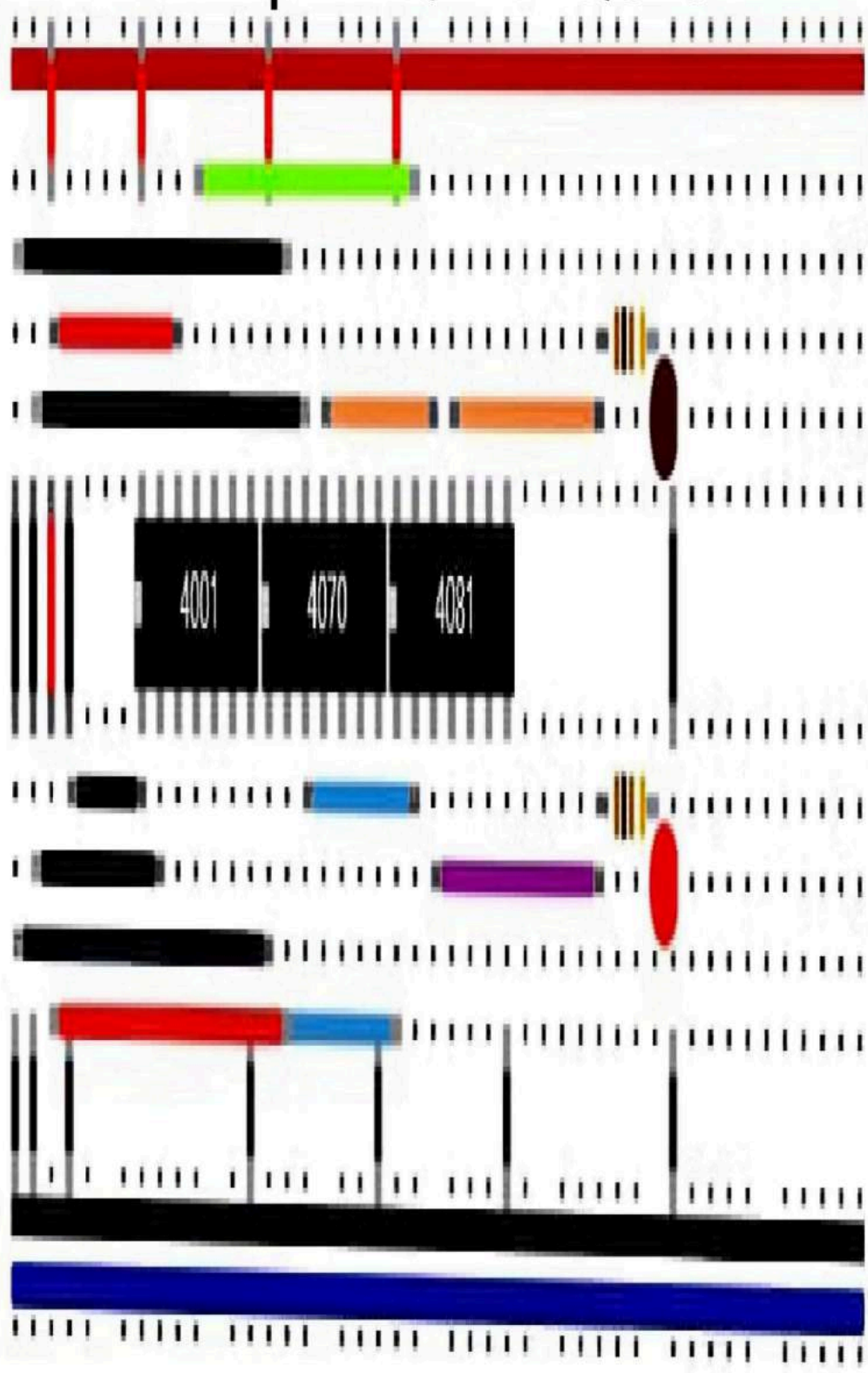


figure 6: circuit diagram for Encoder.

ENCODER

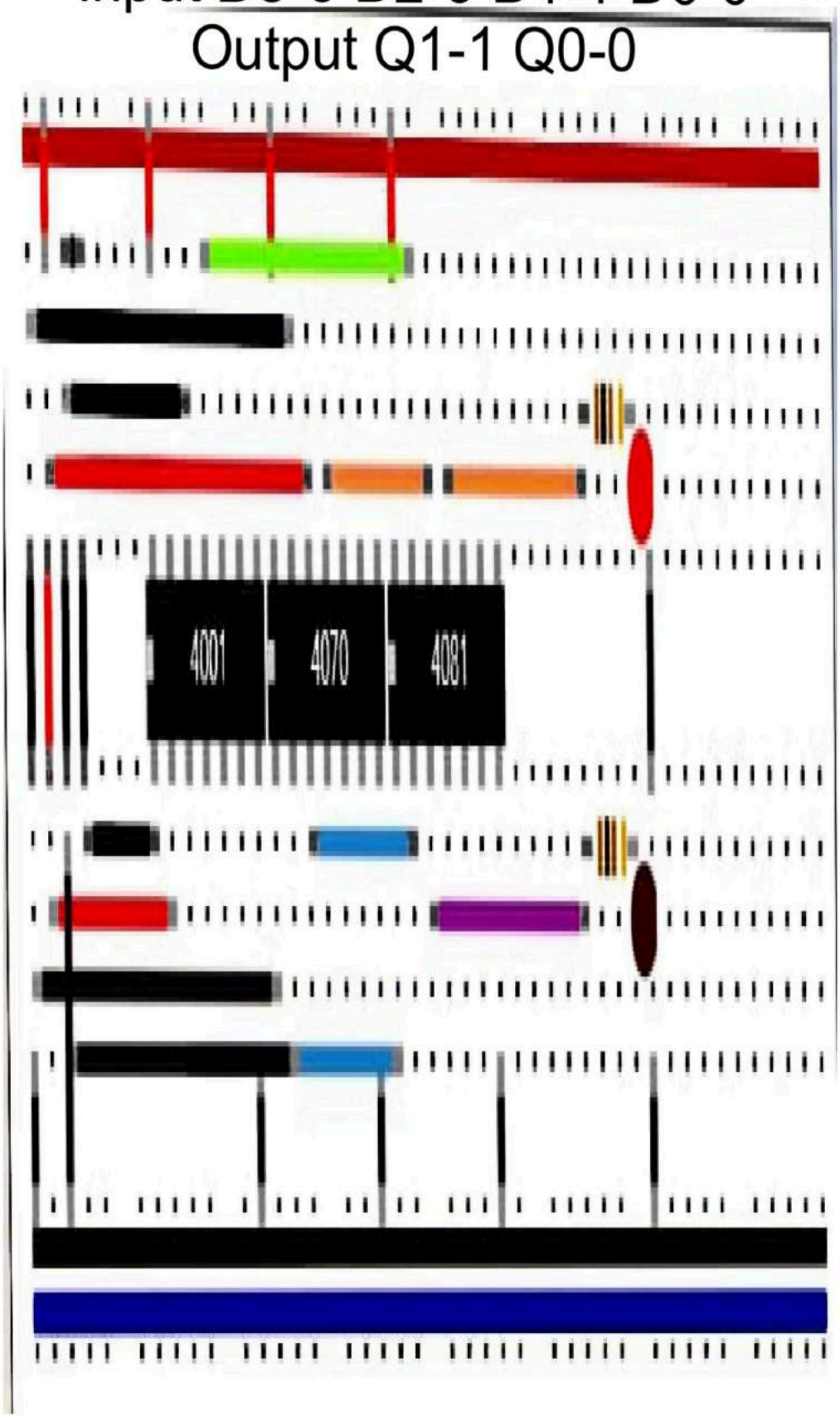


Input D3-0 D2-1 D1-0 D0-0
Output Q1-1 Q0-0



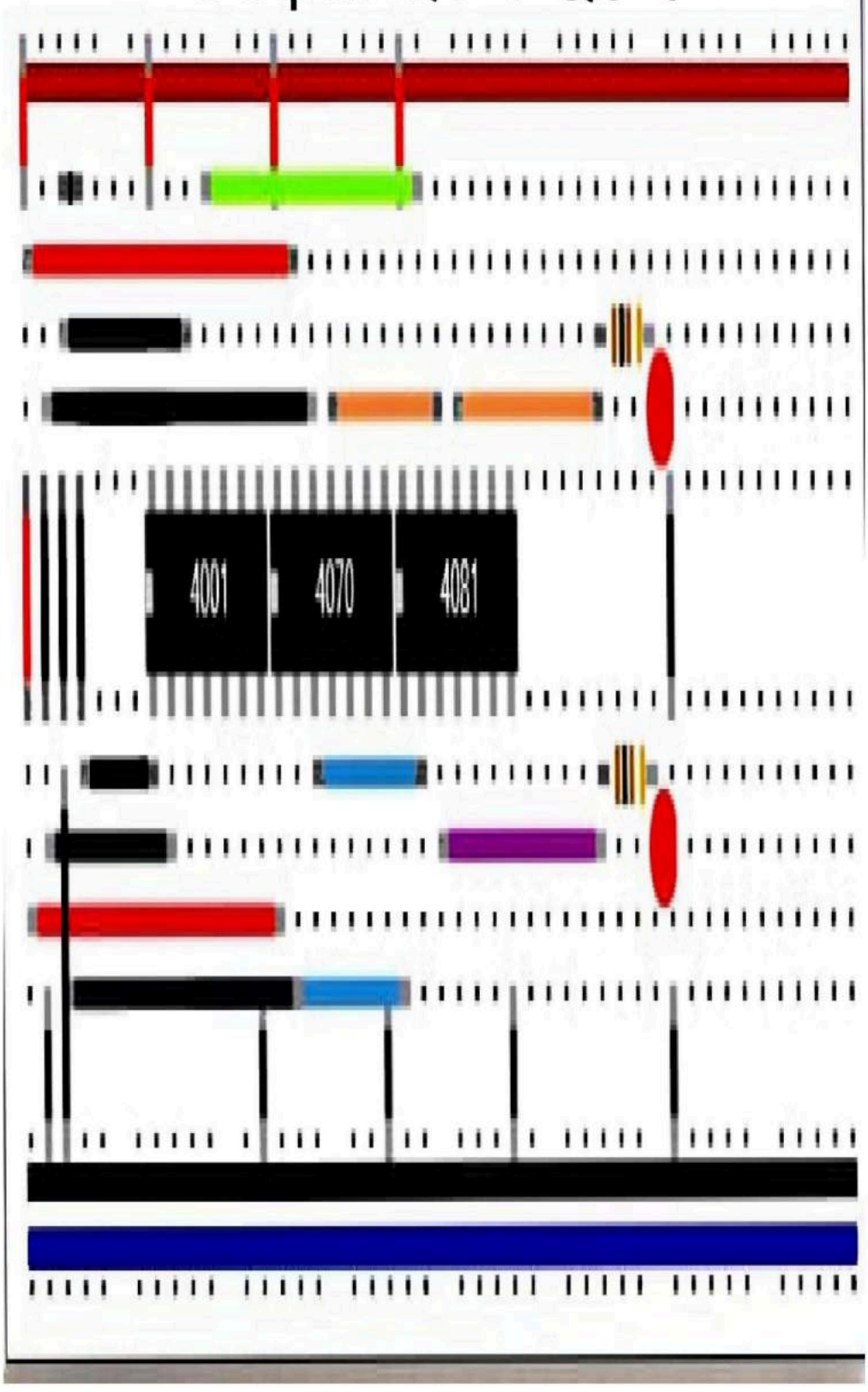
Input D3-0 D2-0 D1-1 D0-0

Output Q1-1 Q0-0



Input D3-1 D2-0 D1-0 D0-0

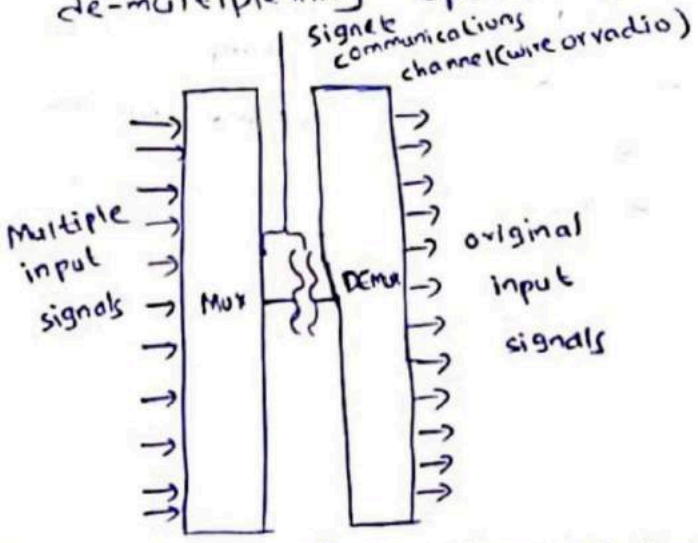
Output Q1-1 Q0-1



Experiment 6

Aim To analyse the truth table and working of 1x4 De-multiplexer by using 3-input NAND and 1-input NOT logic gate ICs and 4x1 Multiplexer by using 3-input AND 3-input OR, and 1-input NOT logic gate ICs

Theory: The function of a multiplexer is to select the input of any 'n' input lines and feed that to one output line. The function of de-multiplexer is to inverse the functio of the multiplexer and the shortcut forms of the multiplexer The de-multiplexers are mux and demux. Some multiplexers perform both multiplexing and de-multiplexing operations



Block diagram of Multiplexer and De-multiplexer

Multiplexer : Multiplexer is a device that has multiple inputs and a single line output. The select lines determine which input is connected to the output, and also to increase the amount of data that can be sent over a network within certain time. It is also called a data selector

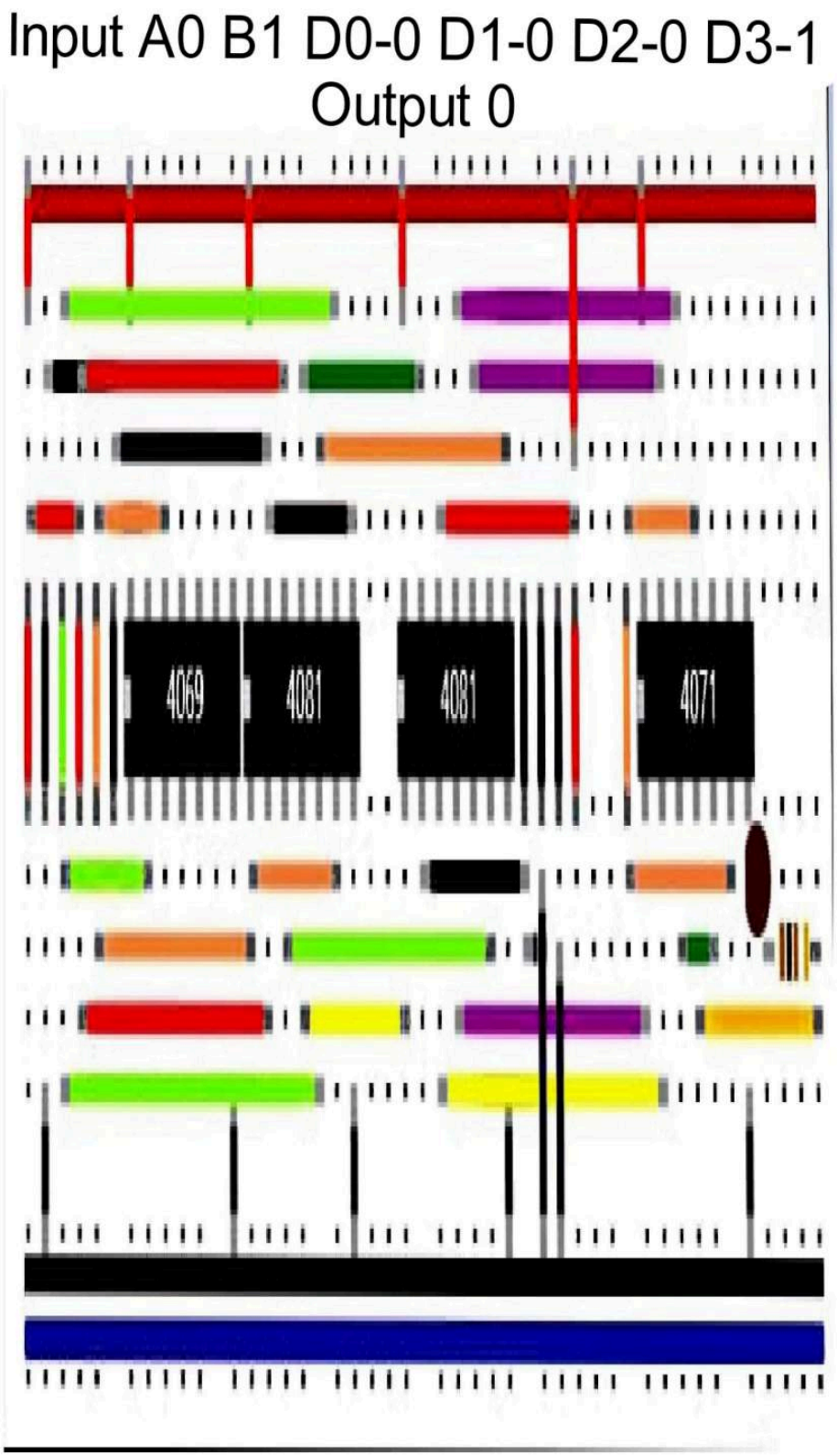
Multiplexers are classified in 4 types

a) 2-1 multiplexer (1 select line)
b) 4-1 multiplexer (2 select lines)
c) 8-1 multiplexer (3 select lines)
d) 16-1 multiplexer (4 select lines)

11.) 4x1 Multiplexer

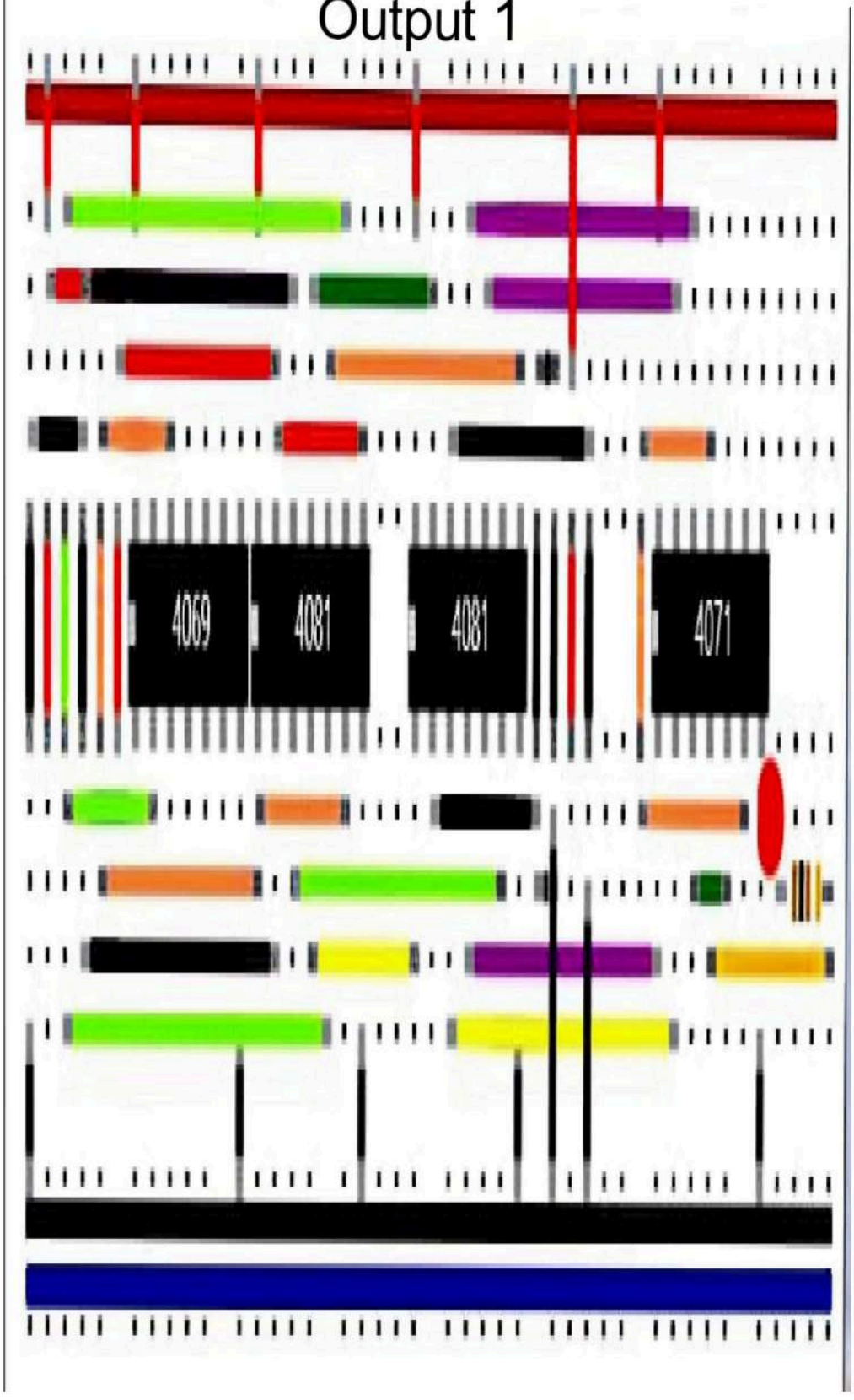
4x1 Multiplexer has four data inputs D_0, D_1, D_2 & D_3, two selection lines S_0 & S_1 and one output Y. The block diagram of 4x1 Multiplexer is shown in the following figure. one of these 4 inputs will be connected to the output based on the combination of inputs present at these two selection lines. Truth table of 4x1 Multiplexer is shown below

MULTIPLEXER



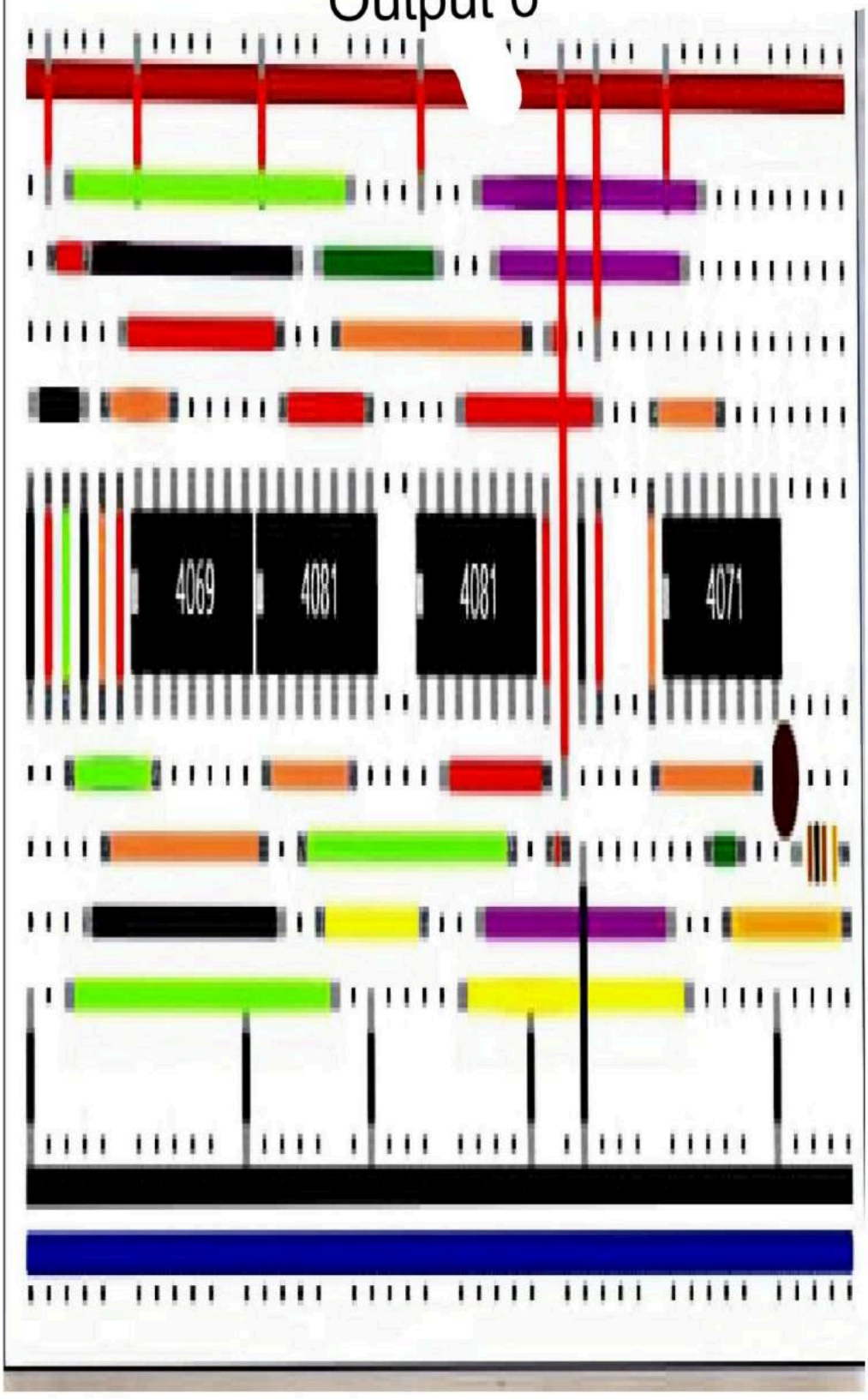
Input A1 B0 D0-0 D1-0 D2-1 D3-0

Output 1

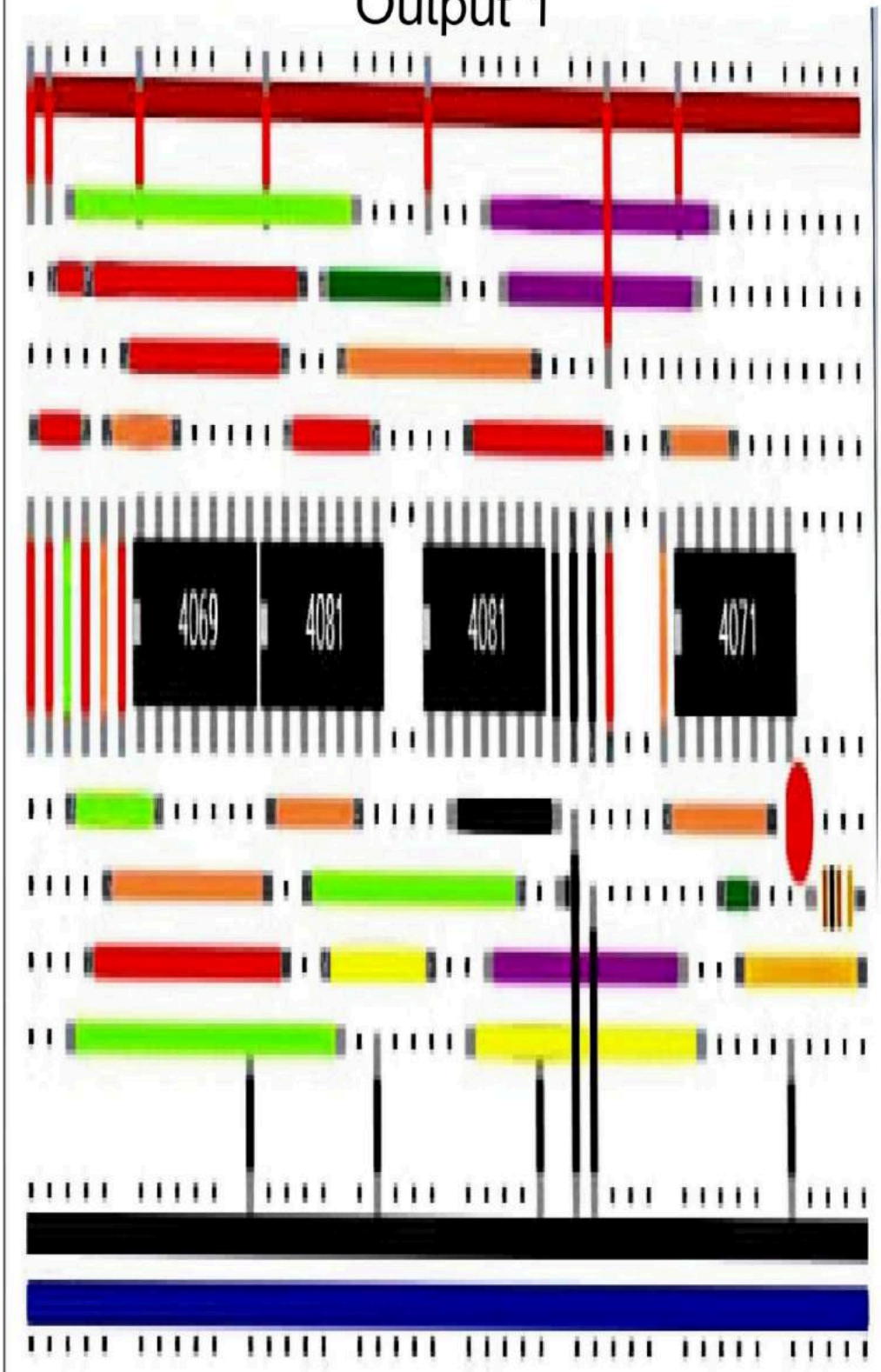


Input A1 B0 D0-1 D1-1 D2-0 D3-1

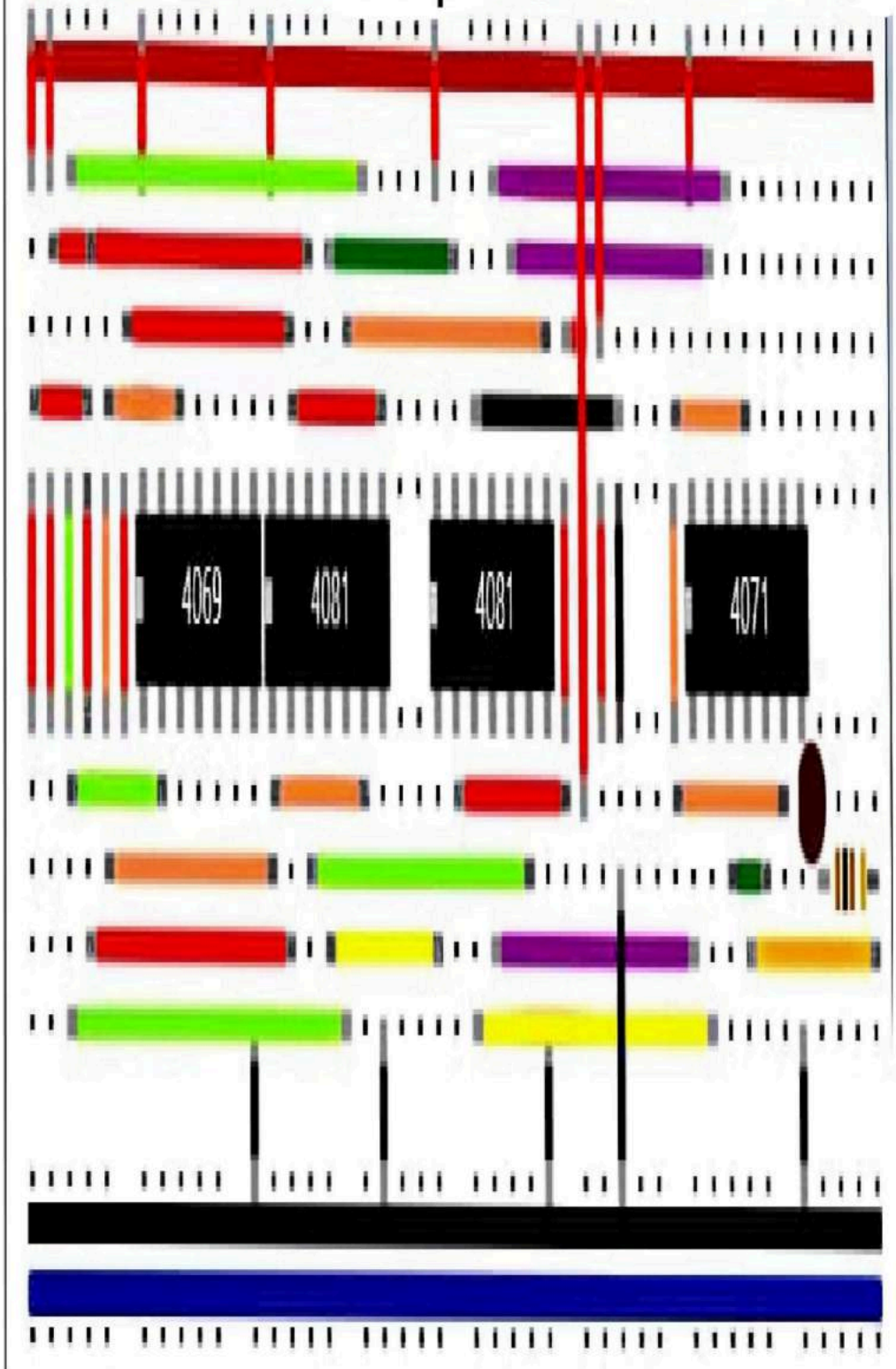
Output 0



Input A1 B1 D0-0 D1-0 D2-0 D3-1
Output 1



Input A1 B1 D0-1 D1-1 D2-1 D3-0
Output 0



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a) 1-2 demultiplexer (1 select line)

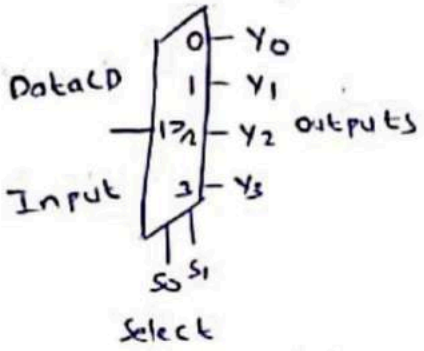
b) 1-4 demultiplexer (2 select line)

c) 1-8 demultiplexer (3 select lines)

d) 1-16 demultiplexer (4 select lines)

2.2) 1x4 De-multiplexer

1x4 De-multiplexer has one input data, two selection lines S_0 & S_1 and four outputs Y_0, Y_1, Y_2 & Y_3. The block diagram of 1x4 De-multiplexer is shown in the following figure.

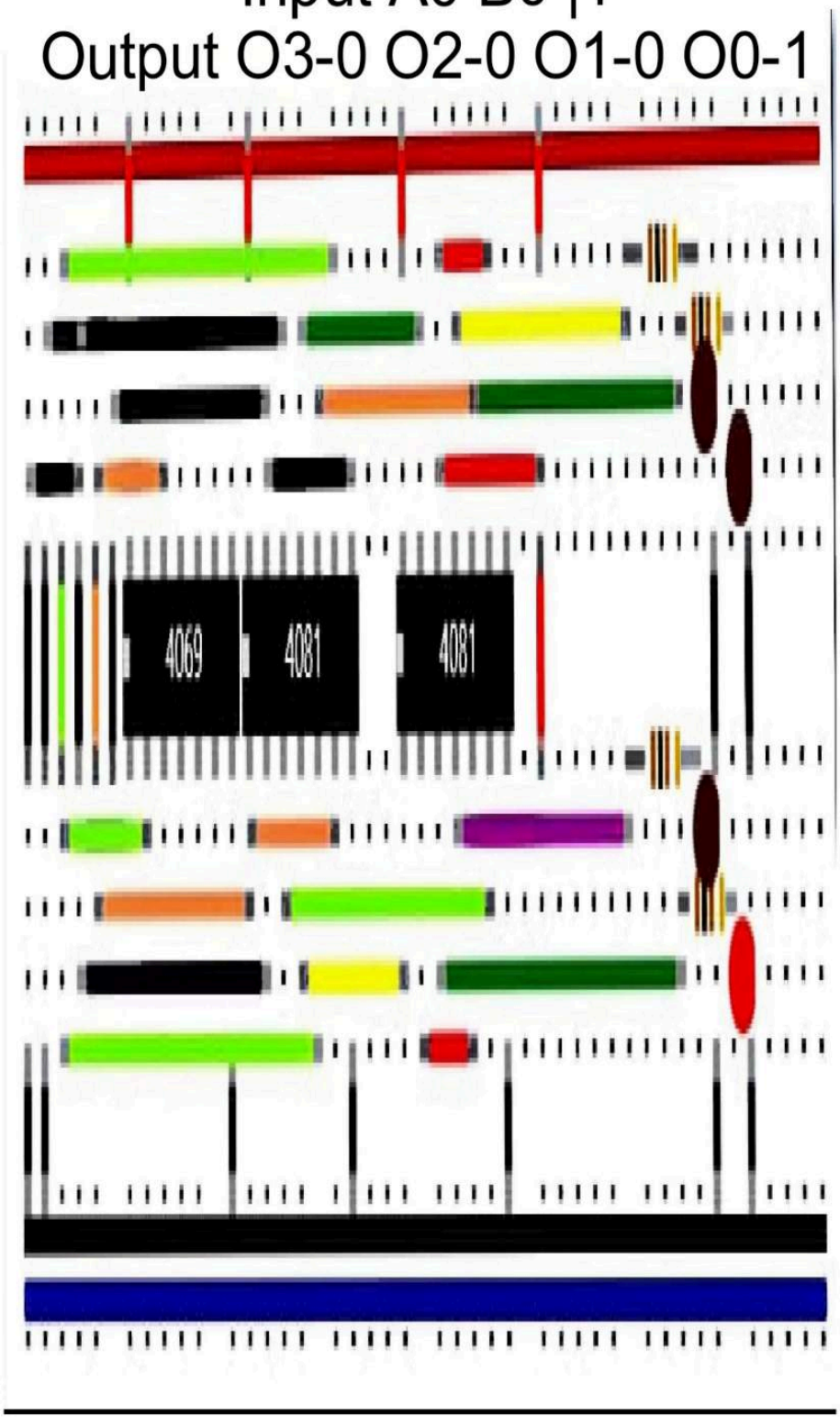


Block diagram of 1x4 De-multiplexer

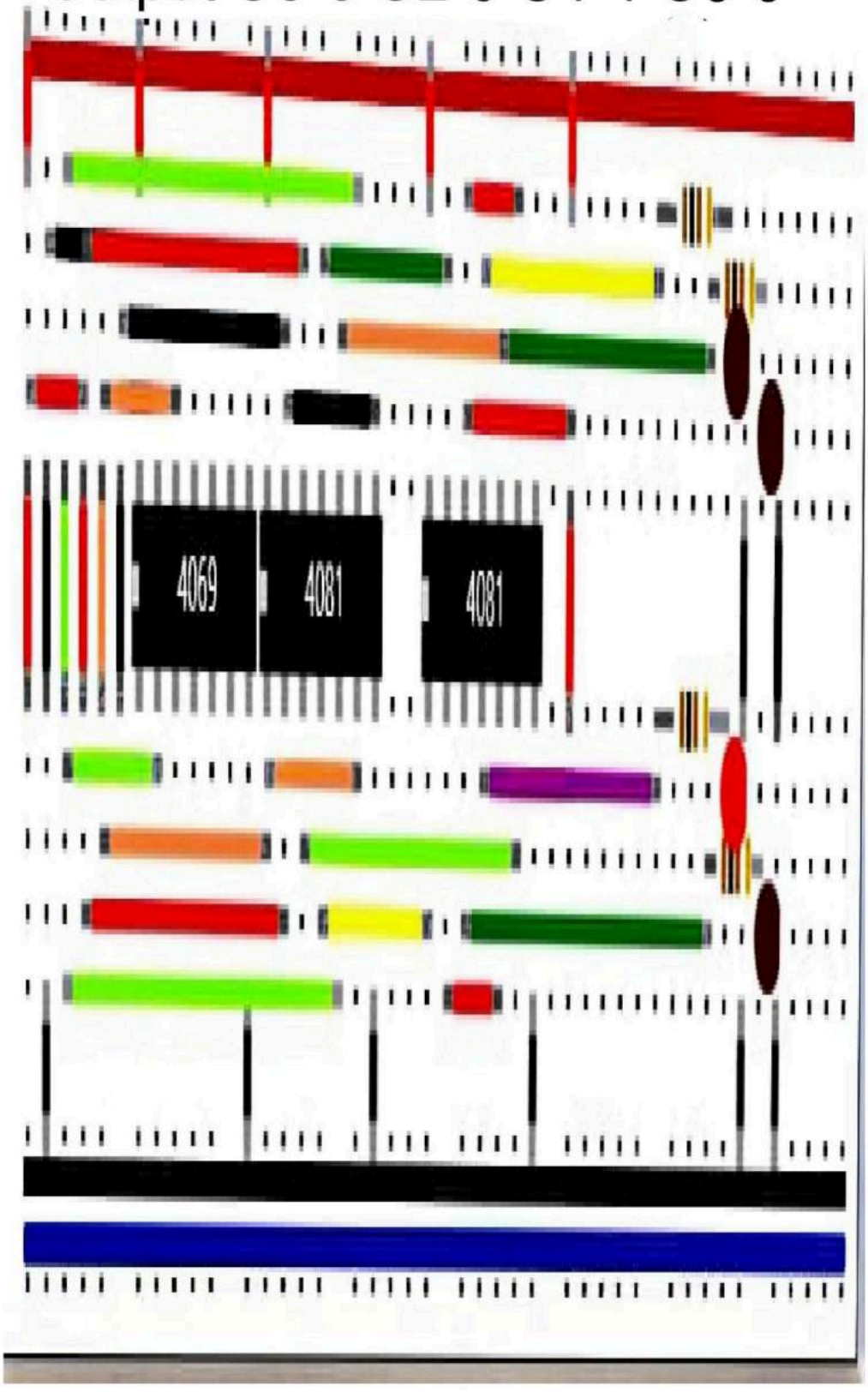
Selection Inputs		Outputs			
S_0	S_1	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0
0	1	0	0	0	0
1	0	0	0	0	0
1	1	0	0	0	0

Truth table of 1x4 De-multiplexer

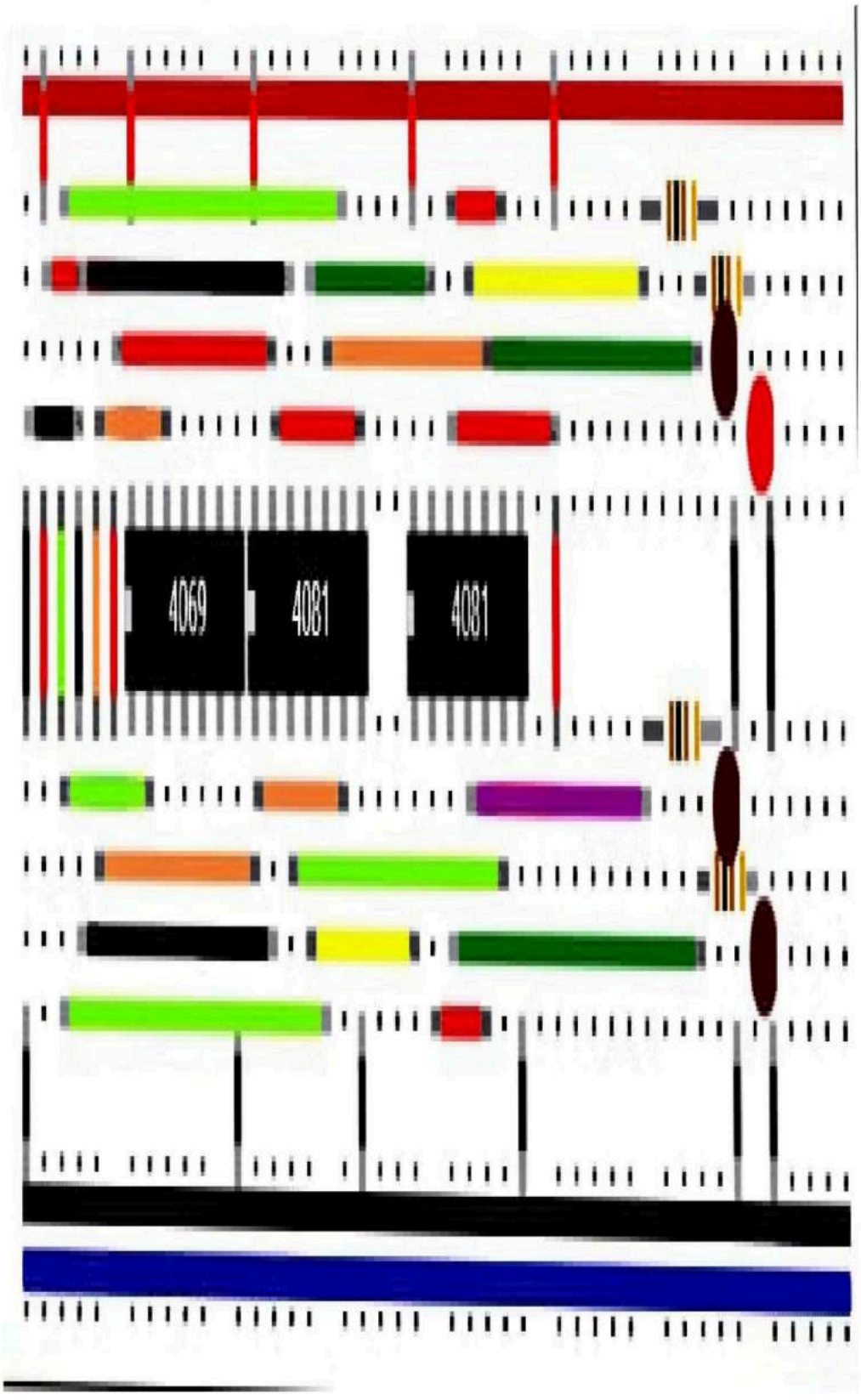
DE MULTIPLEXER



Input A0 B1 |1
Output O3-0 O2-0 O1-1 O0-0



Input A1 B0 |1
Output O3-0 O2-1 O1-0 O0-0



Input A1 B1 |1

Output O3-1 O2-0 O1-0 O0-0