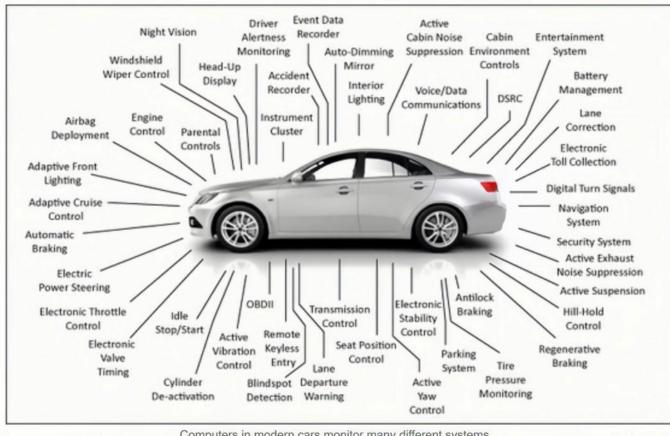


# What is a chip?

Also called Integrated Circuit (IC) or microchip Packaged Chip Wafer Chip Printed circuit board (PCB)

# Where are they used?

#### >1000 in a modern car



Computers in modern cars monitor many different systems

### >50 in a modern smartphone

### Key chip suppliers for Apple's iPhone 15

This infographic was created by Quartr based on TechInsights' teardown of iPhone 15 Pro.

**□** Ouartr → www.quartr.com









### **Medical Devices**

Continuous glucose monitor 2-3

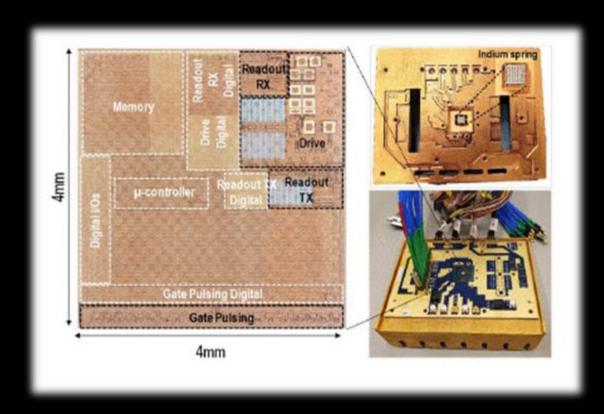




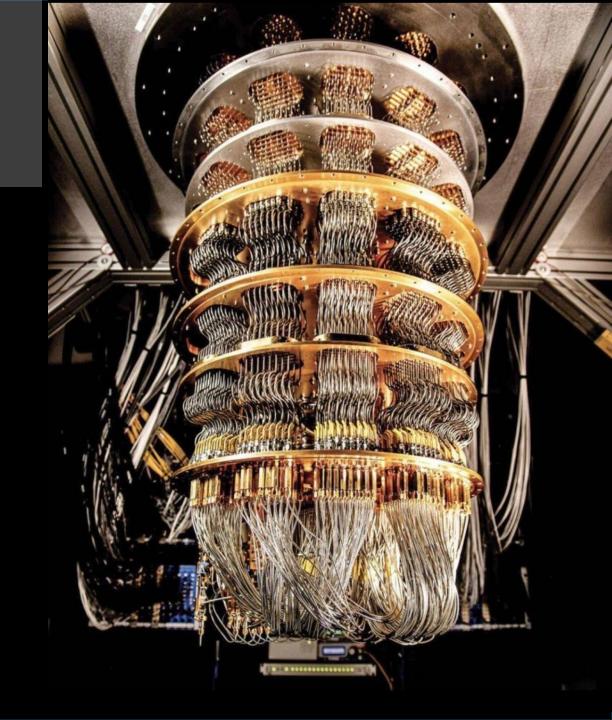
https://www.ifixit.com/Teardown/FreeStyle+Libre+2+Sensor+Teardown/137719

### Quantum

Qubit control and readout

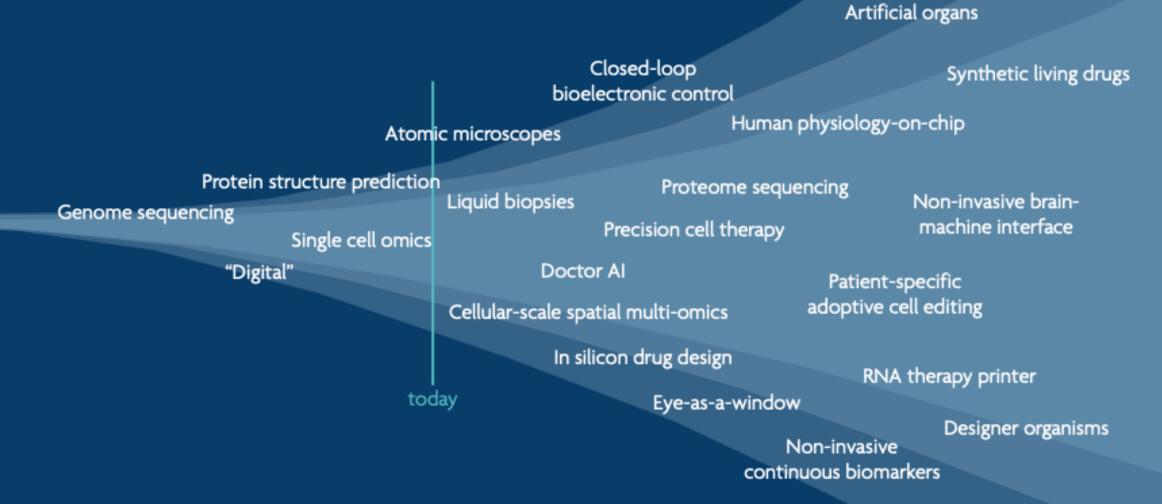


https://quantumai.google/quantumcomputer https://www.nature.com/articles/d41586-024-03288-3



# The explosion in bioconvergence has just started

### **Biotechnology**



### **Critical technologies**

The critical technology priority fields are:

- advanced manufacturing and materials technologies
- artificial intelligence (AI) technologies
- advanced information and communication technologies
- quantum technologies
- autonomous systems, robotics, positioning, timing and sensing
- biotechnologies
- clean energy generation and storage technologies.

Critical technologies are built on integrated circuits!

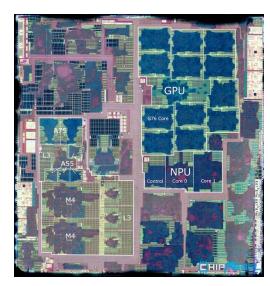
### **Integrated Circuit Types**

By technology

#### **Silicon** (single element)

~100K-1B transistors / chip 90% of the global market

- CMOS
- BiPolar



90% of the market

#### Compound

~10-20 transistors / chip 10% of the global market

#### III-V

#### IV-IV

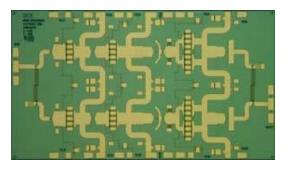
GaAs

• SiC

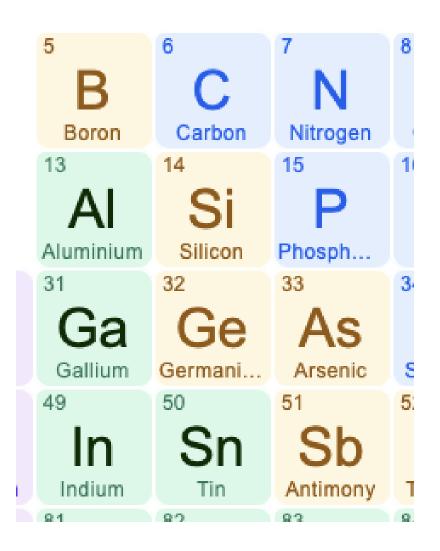
• GaN

SiGe

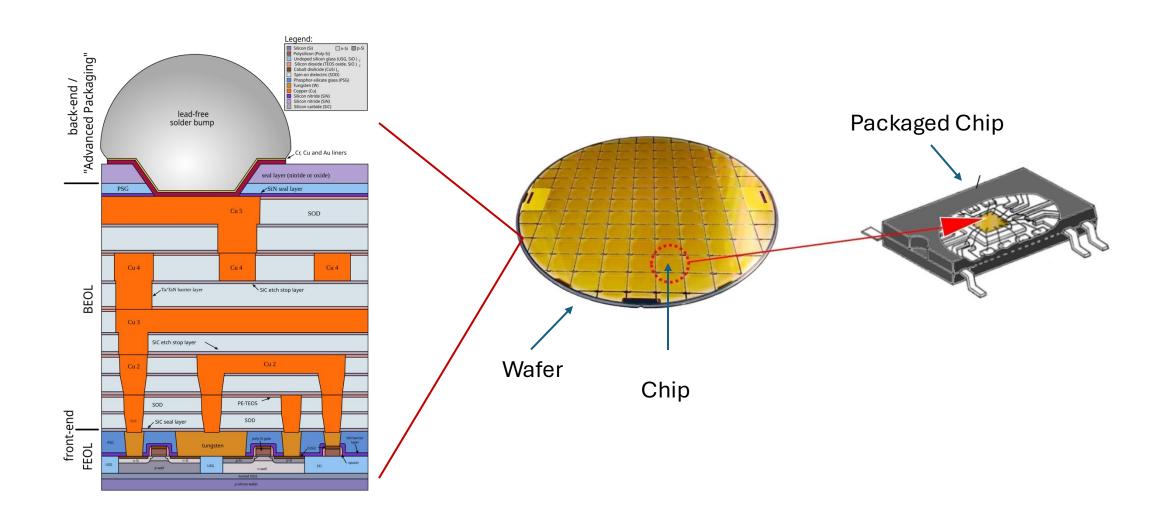
• InP



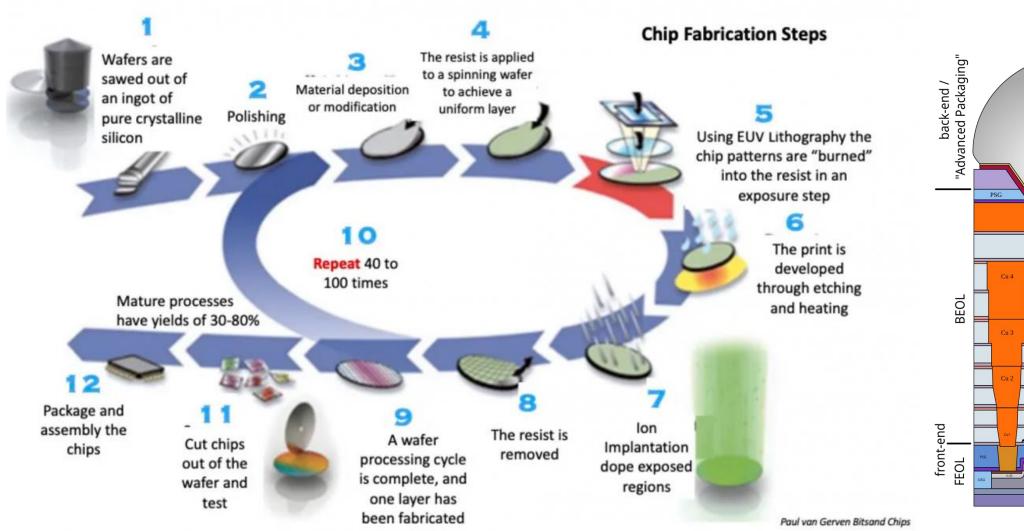
10% of the market

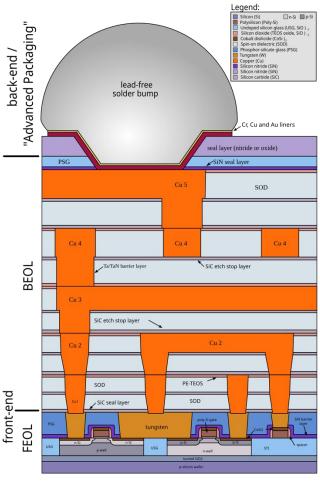


# How are they made? (CMOS)



# How are they made? (CMOS)







https://www.youtube.com/watch?v=h\_zgURwr6nA

### Semiconductor Value Chain

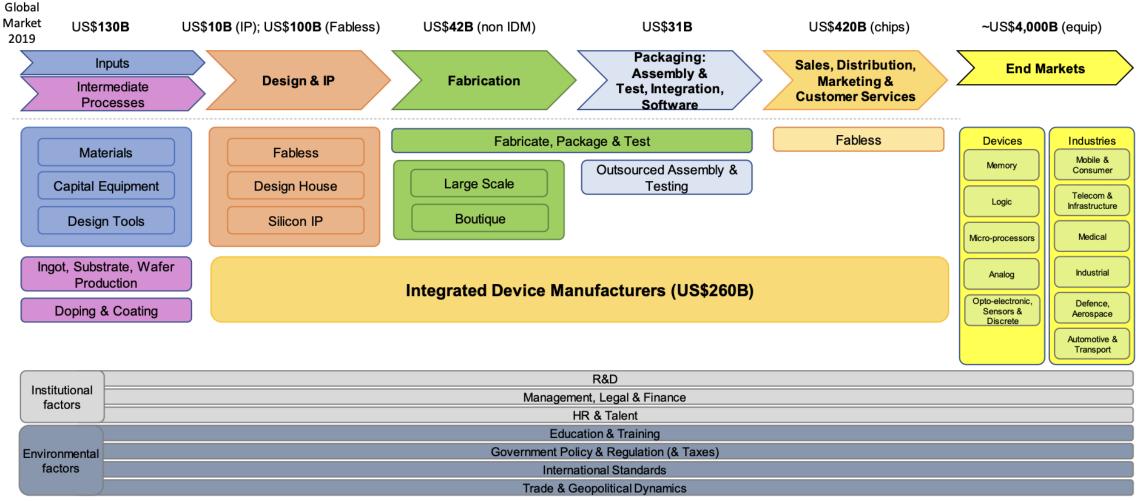
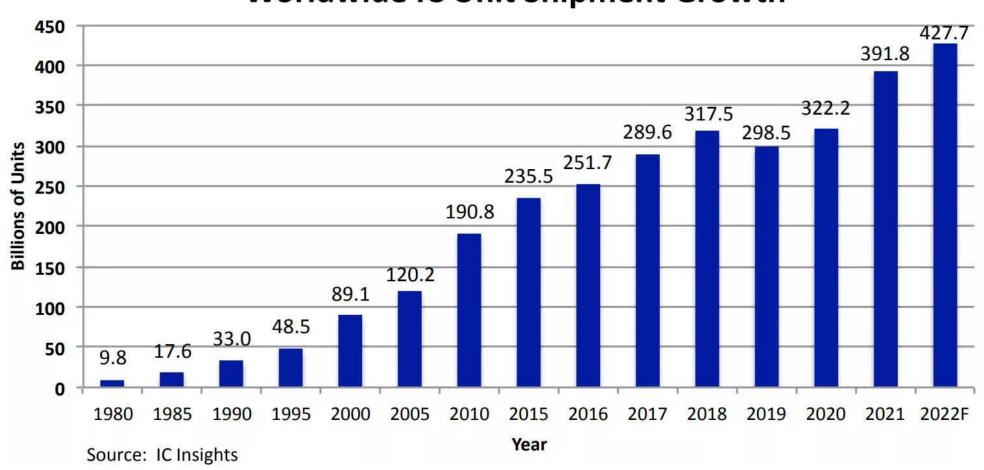


Figure 1: Semiconductor value chain

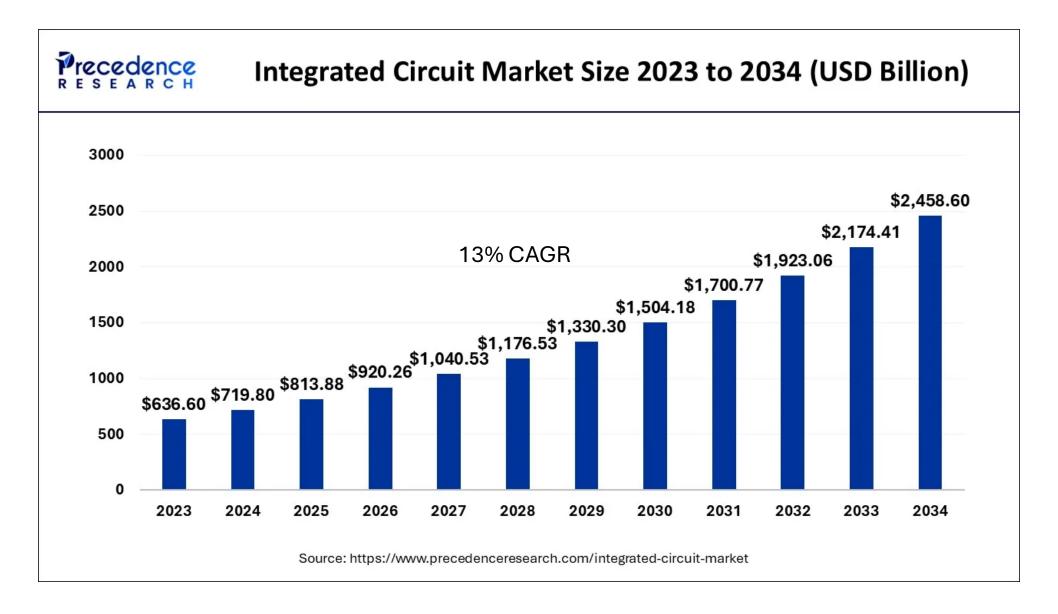
Note: Global market size estimates in US\$ billion. Refer to Appendix 2 for references supporting estimates of market size in 2019.

### **Market Size - Annual Shipments**

### **Worldwide IC Unit Shipment Growth**



### Market Size - Sales to 2034



# **Tech Companies**

>\$10B USD market cap, total is \$33T

Microsoft	Amazon	Tesla	Oracle	Intel	Siemens Ge	eneral Ele Appl	ied M Uber	Hor	eywel Intu	itive S P	rosus R	Raytheon Airbi	ıs Deutsche	AT&T Booki
				Alibaba	-									
			AMD		Sony	CATL Tol	kyo E Merc	ado Bosto	n S Fiserv	Infosys	Arista N	Synopsy KLA	Cadence AB	B Safran Equ
		Broadcom	_	* - 5		]								
		Dionacom		Intuit	Medtronic	Workday	PayPal LC	Ene Nor	hrc Atlassi	SoftBar	Nintene No	etEas Siemen A	 Amphe Marve I	Dell Roper Co
			Adobe		Lam Research									
				Verizon			Midea		nira DexC	Foxed B	AE Mindi	Nu H Digita T	E C Hoya Do	orl Spoti Datae B
	NVIDIA	Visa	Salesforce		Schneider Elec	ct Atlas Copco	Saudi Tele							
Apple		Visa	Salestores	Pinduoduo		Arm Holding		STM: Hil	cvi Xiaor L	3Ha IQV	I Adye Co	ogn Agile Mura	Johns Ame Fi	del Foxc Baid E
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# **Tech Companies – That Design Chips**

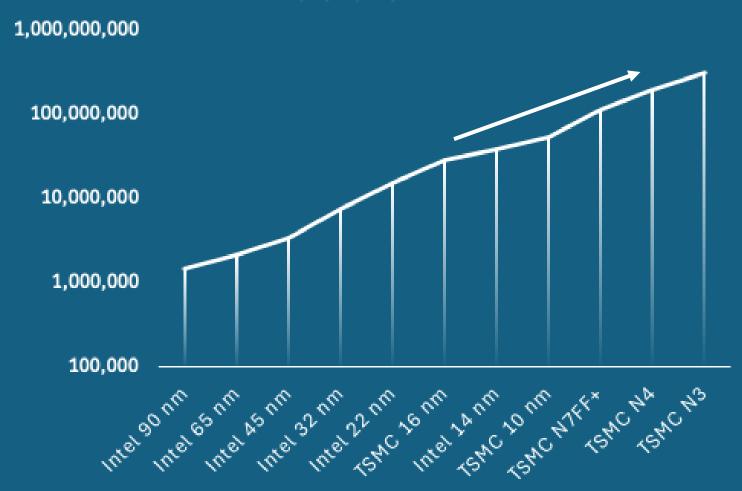
>\$10B USD market cap, total is \$33T

Microsoft	Amazon	Tesla	Oracle	Intel	Siemens	General Ele Applied M	Uber I	Honeywel 1	Intuitive S	Prosus	Raytheon Airbus	Deutsche A	T&T Booking
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				Verizon		Mide		Emira De	C Foxed	BAE Mind	Nu H Digita TE	C Hoya Doorl	Spoti Datad Bloc
	NVIDIA		Salesforce		Schneider E	lect Atlas Copco Saud	Tele						
Apple		Visa	Salesforce	Pinduoduo	1		STM	Hikvi Xiac	т L3На ІС	QVI Adye C	ogn Agile Mura J	ohns Ame Fide	Foxe Baid Elec
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						General Dyn Moto	Capgei	m Coinbas	Wipi Chui	Hex: Rene	Mon HP Mon A	ns Adv Resi E	ast Haie ASN Del
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	TSMC	Tencent			Airbnb	Thomson Re	Veeva	S FICO	Schindl G	ONG Axon	Sams Wise Nex	Affii Zooi Alle	Ne Ce As Ce M
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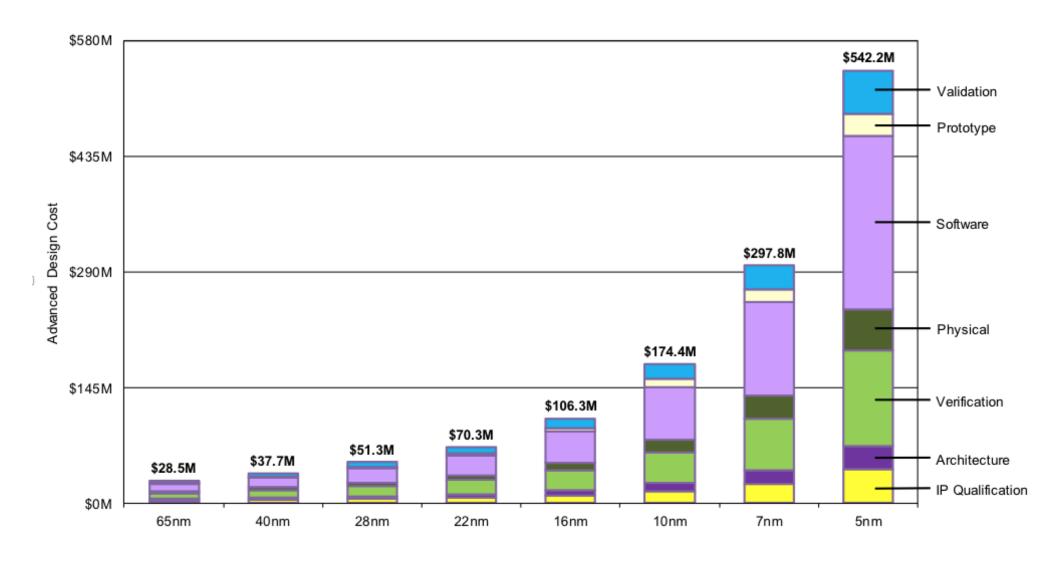
# Trends

### **Trends – Transistor Density**

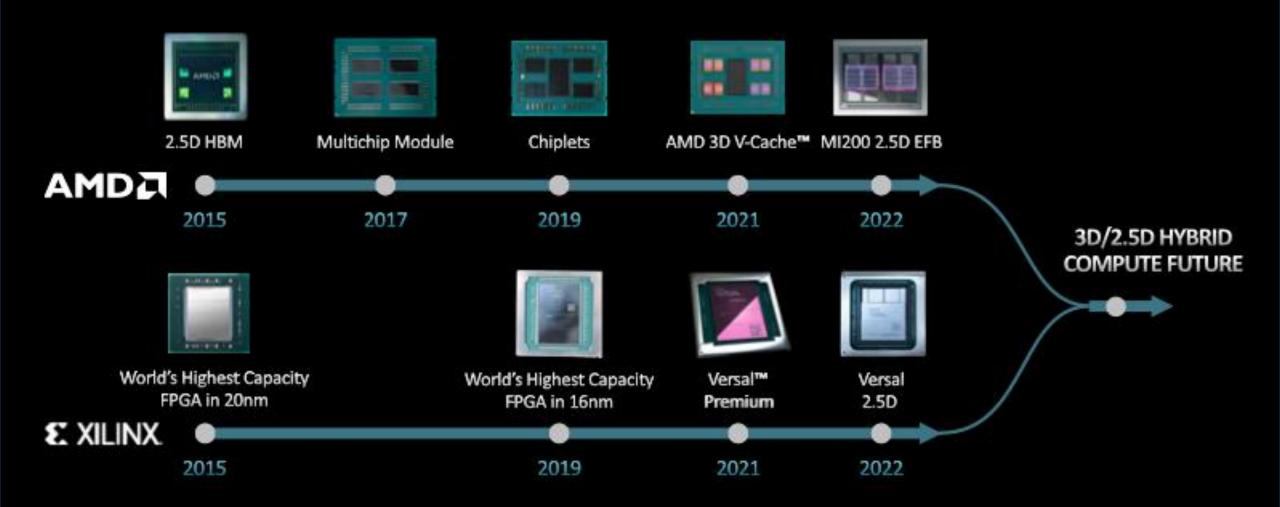




# Trends - Increasing costs

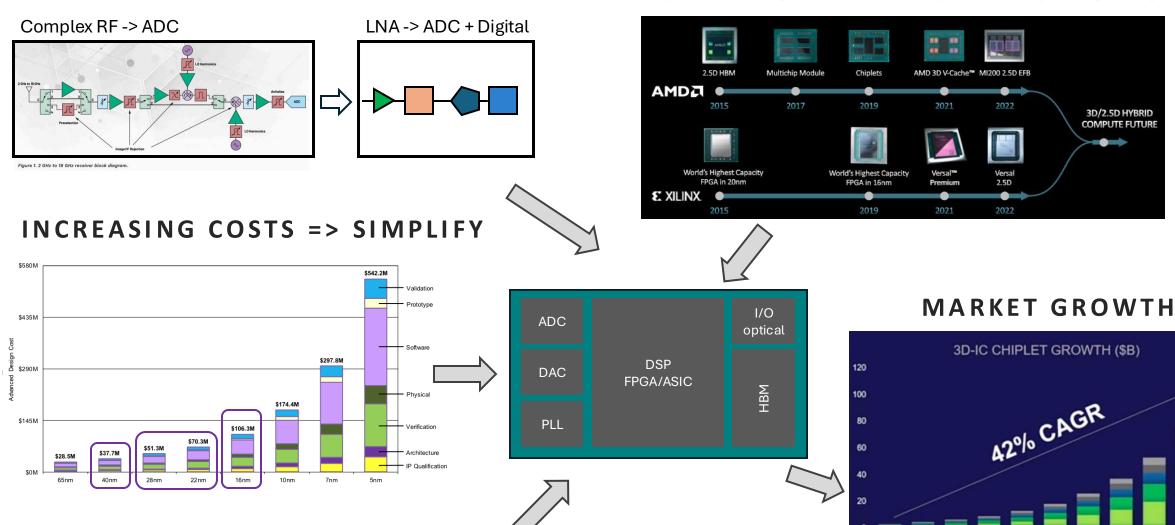


# Trends - Advanced Packaging



#### TRANSISTOR DENSITY => MORE DIGITAL

#### CHIPLETS + ADVANCED PACKAGING



SW (AI/ML) DRIVEN DESIGN AND VERIFICATION => REDUCE DEV COSTS

Memory Chiplets

GPU Chiplets

■ Sensor Chiplets

■ Networking Chiplets

# Chips In Oz

# Chip Design in Australia

#### Headquartered in Australia













#### **Design Centre in Australia**













#### Also make chips



Listed in Australia

brainchip

# **Increasing Participation**

#### Inputs

Critical minerals, mining and processing

Rare earth minerals, mining and processing

New design tools/ techniques/methodologies

#### Fabless Design and IP

Design centres and startups

Quantum

Biotechnology

**Photonics** 

Communications and sensing

Defence and critical technologies

#### Manufacturing

Advanced packaging

Mature CMOS fab (12-28nm)?

Compound (GaAs/GaN/Other..)?



**SILICON PLATFORMS LAB** 

# **Macquarie University**



SILICON PLATFORMS LAB

1990-2000

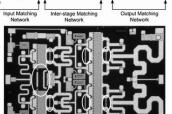
WiFi (Radiata) (CMOS) 2006-2010

60GHz GLIMMR (SiGe)

2020-

MADLab (GaAs, GaN)

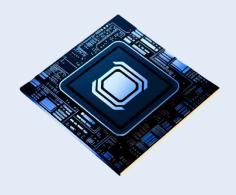
RFIN Vel Vel Vel RFOU





2024-

SiP Lab (CMOS, SOI advanced packaging)



11a/b/g Modem



4.75mm by 4.75mm 8 million transistors TSMC 0.13um 7 level metal 31mW sleep 206mW Tx 362mW Rx 2.4GHz/5GHz transceiver



5mm by 5mm TSMC 0.13um 7 level metal 31mW sleep 405mW Tx 360mW Rx

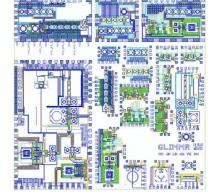


Figure C.3: GLIMMR test-chip 3 (GTC3).

Neil Weste David Skellern **Neil Weste** 

### Silicon Platforms Lab

**PEOPLE** 



SILICON PLATFORMS LAB



Industry Professor Mike Boers



Senior Lecturer Jafar Shojaii



Admin Officer Shannah Gray Williams



RF / mmWave WiFi Cellular Satellite







ASIC CMOS Rad Hard





### Silicon Platforms Lab

**PEOPLE** 



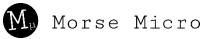
**SILICON PLATFORMS LAB** 



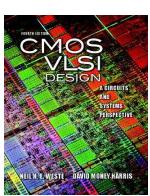
### Adjunct Professor Neil Weste













# Adjunct Professor David Skellern (AO)







ASIC CMOS GaN/GaAs Satellite

### Silicon Platforms Lab

**PEOPLE** 



**SILICON PLATFORMS LAB** 



Senior Principal
Engineer
Lead Systems





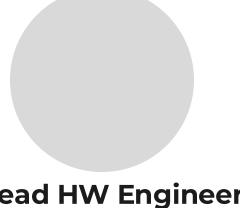




RF / mmWave Cellular DSP, DPD



Lead Digital Engineer Hiring



Lead HW Engineer Hiring

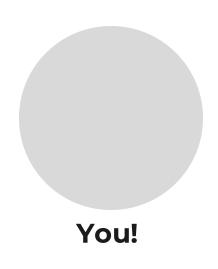


Hiring

### We are hiring

**PEOPLE** 





### 7 Open Positions + HDR Roles

- <u>Digital Backend Engineer</u>
- Layout Engineer
- <u>Lead Analogue/Mixed Signal Engineer</u>
- <u>Lead Digital Engineer</u>
- <u>Lead Hardware Engineer</u>
- Research Fellow in High Performance Mixed Signal CMOS Design
- Senior Software Engineer
- Masters + PhD scholarships

### Learn More

https://www.mq.edu.au/faculty-of-science-and-engineering/our-research/silicon-platforms-lab

### Focus areas

- Communications and sensing systems using chiplets and advanced packaging –
   with a focus on SW driven efficient design
- Training the next generation of integrated circuit design engineers
- Supporting research teams and startups that require integrated circuits
  - Biotechnology
  - Quantum sensing and compute
  - Photonics

# Why now?

- Integrated circuits power all advanced technology
- Critical technologies and Defence rely on them
- New era of scaling using heterogenous integration provides a good entry point
- Opportunity for new highly efficient SW driven design flows
- Huge market opportunity

### How to work with us

- Research collaboration
- Support for early-stage start-ups and University spin-outs
- Research and design services for industry
- Custom ASIC design
- Student internships

# Thank You!

Contact
Mike Boers
m.boers@mq.edu.au

