

# Chips



What is a chip?

Where are they used

How are they made

The semiconductor value chain

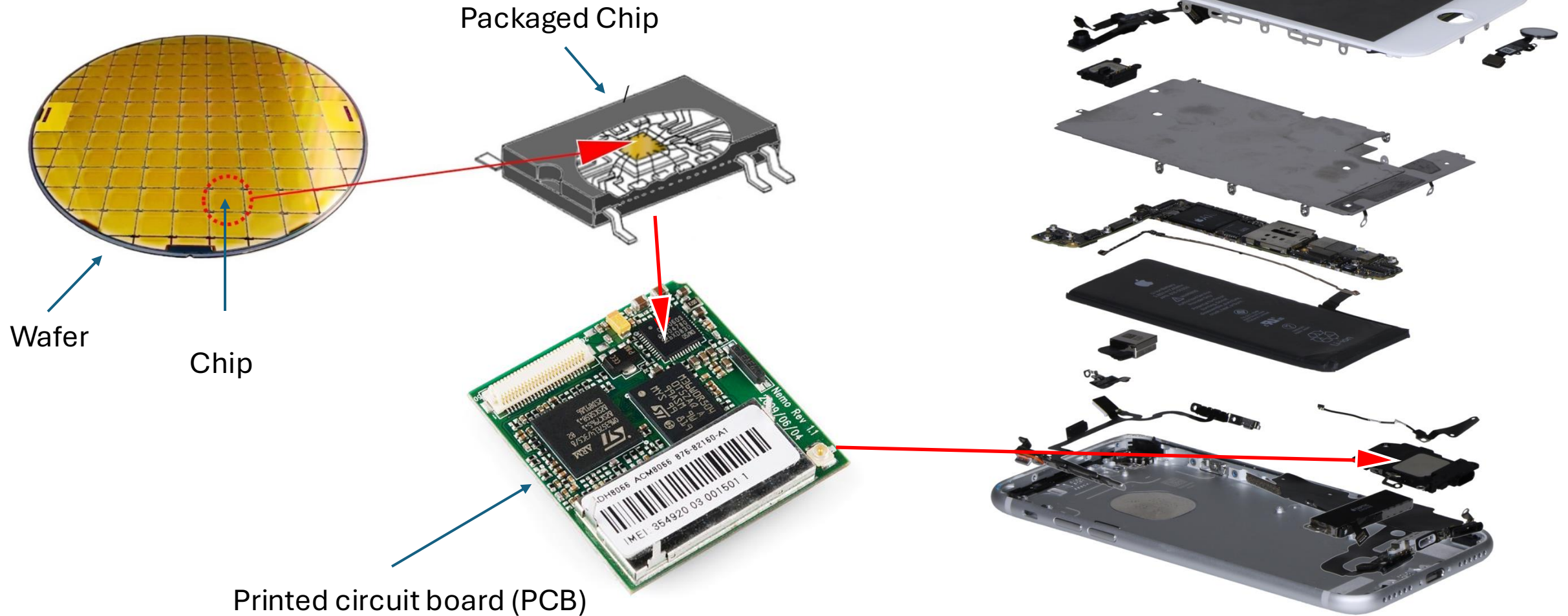
Australia's place – where do we participate, can we do more?

Macquarie University - Silicon Platforms Lab



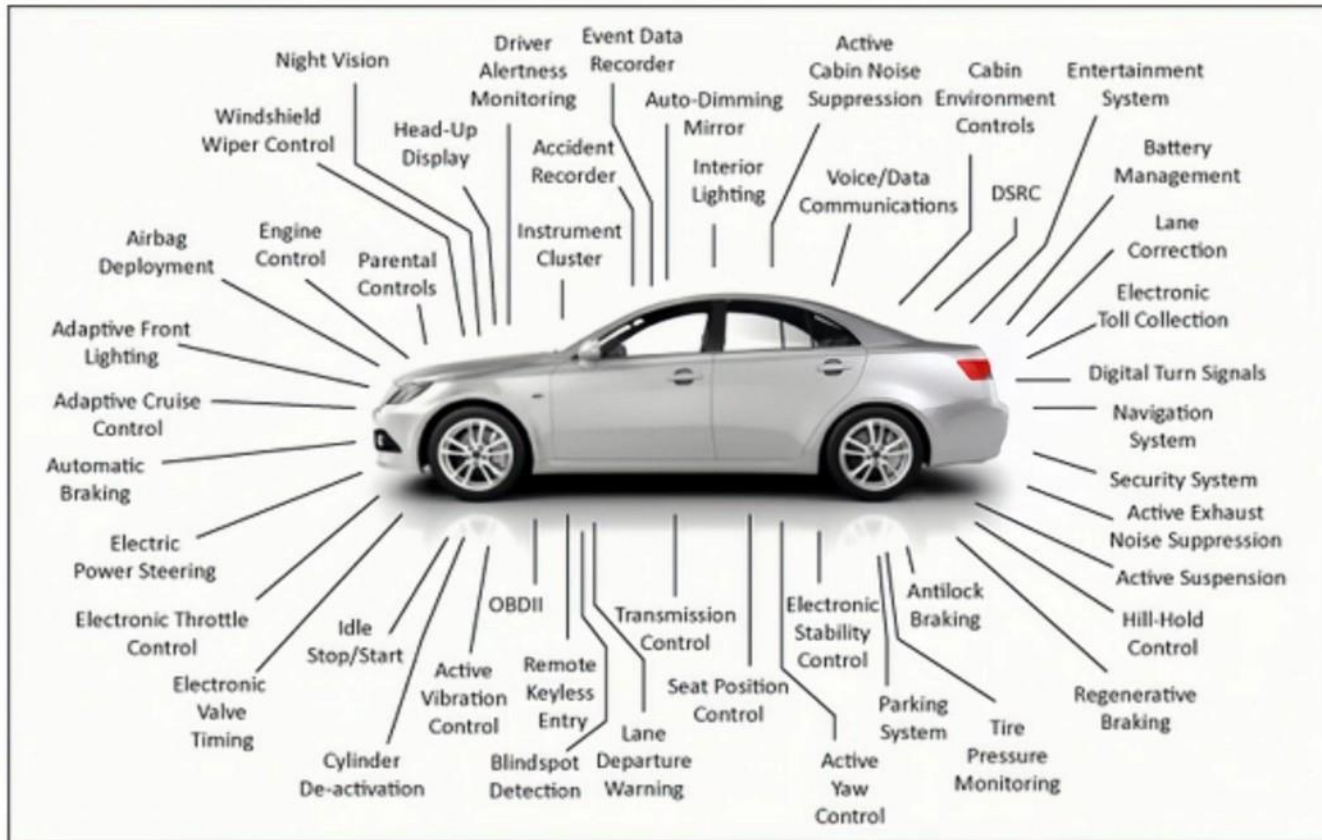
# What is a chip?

Also called Integrated Circuit (IC) or microchip



# Where are they used?

>1000 in a modern car



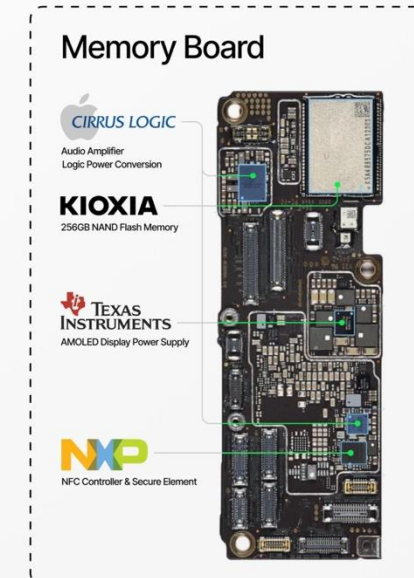
Computers in modern cars monitor many different systems

>50 in a modern smartphone

## Key chip suppliers for Apple's iPhone 15

This infographic was created by Quartr based on TechInsights' teardown of iPhone 15 Pro.

Quartr → [www.quartr.com](http://www.quartr.com)





# Communications

Starlink satellite terminal >400

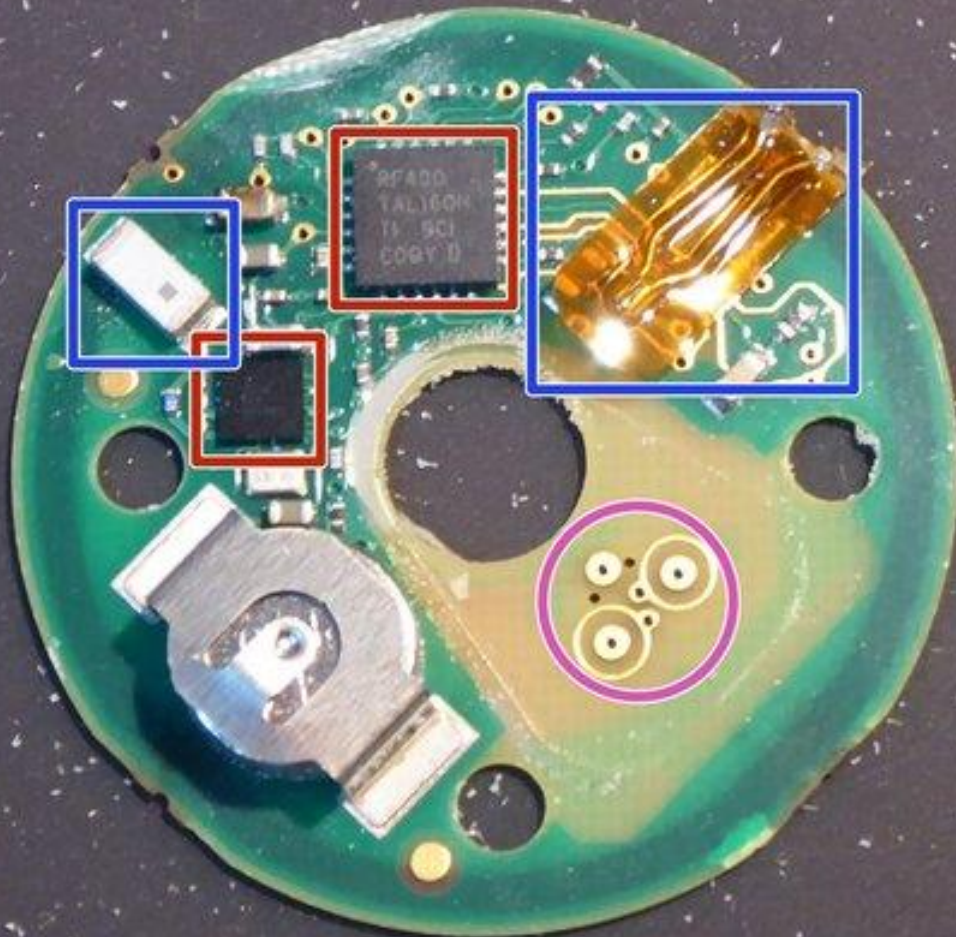


MADE ON EARTH BY HUMANS



# Medical Devices

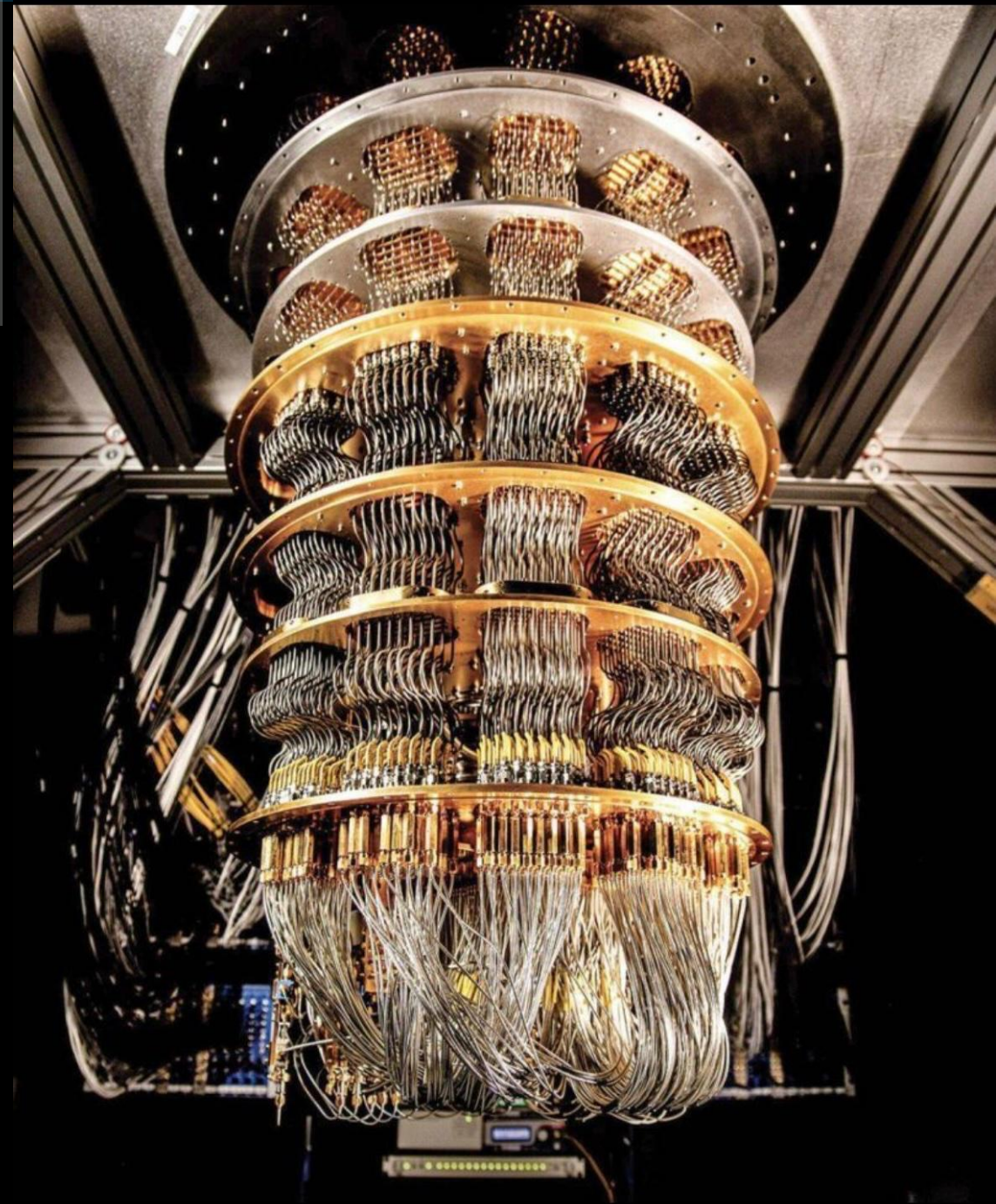
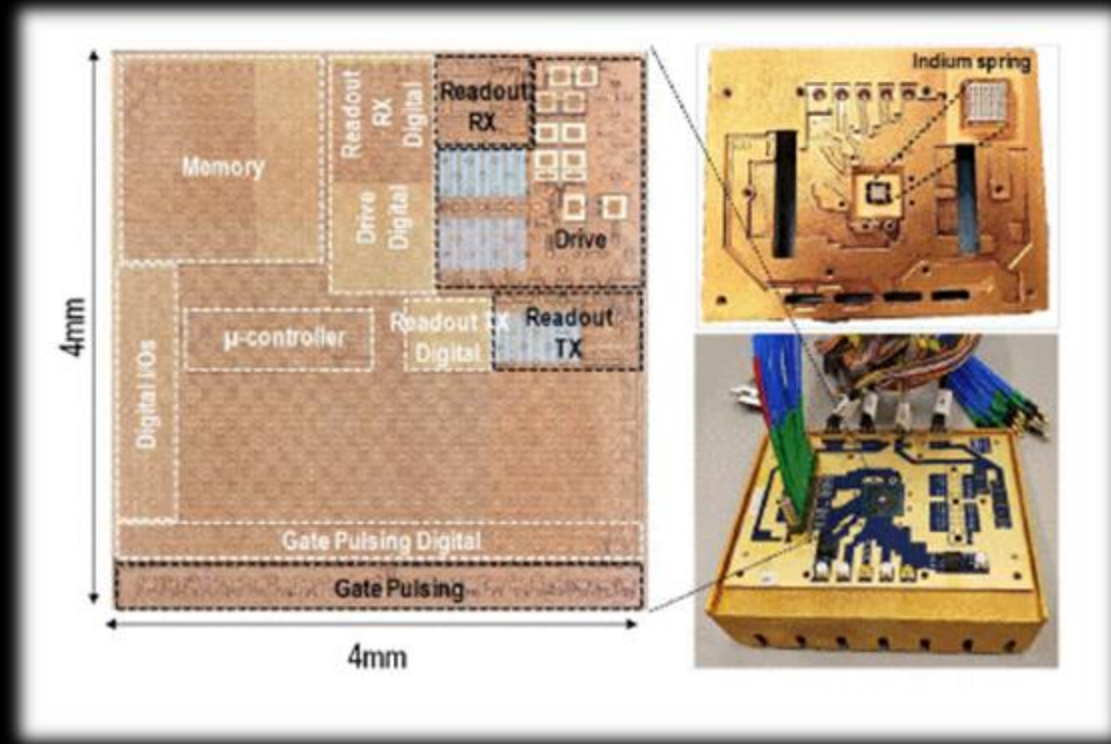
## Continuous glucose monitor 2-3





# Quantum

## Qubit control and readout

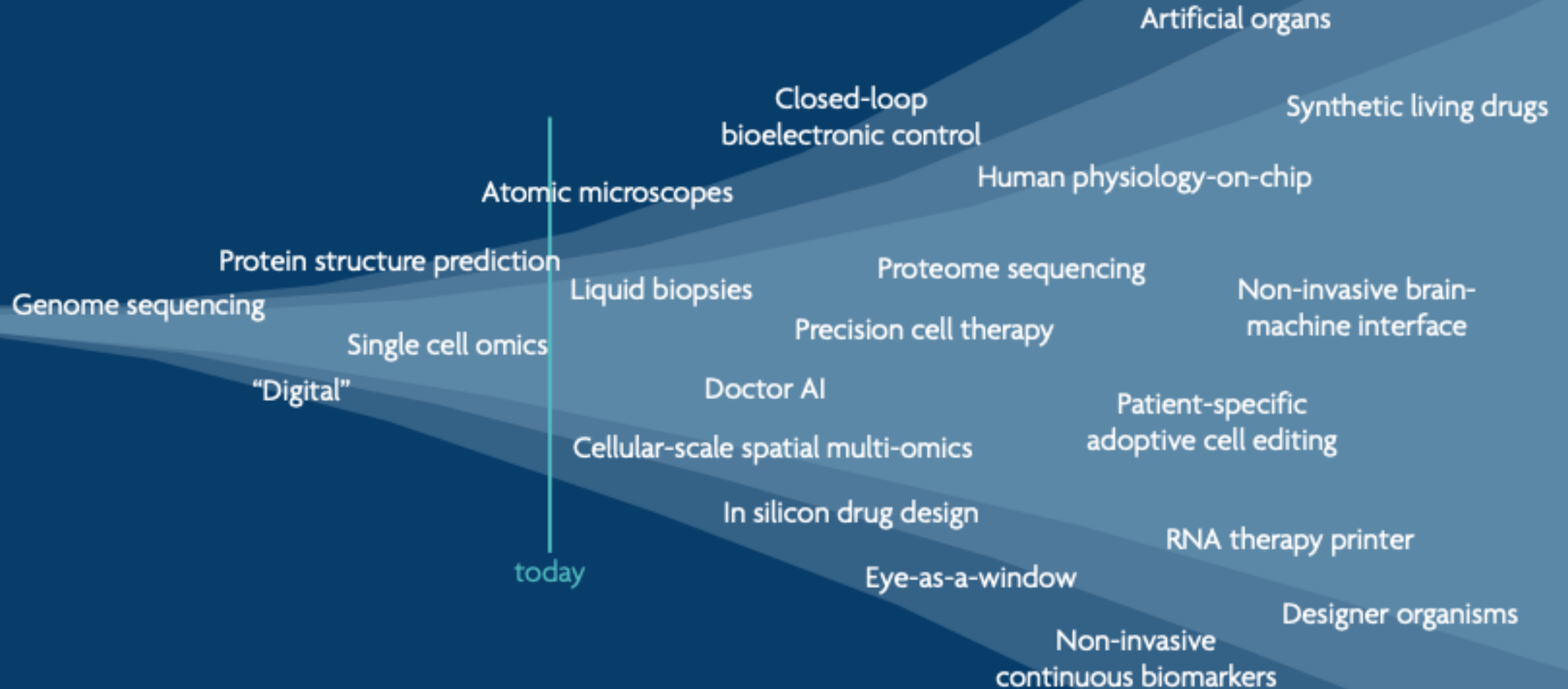


<https://quantumai.google/quantumcomputer>

<https://www.nature.com/articles/d41586-024-03288-3>

# The explosion in bioconvergence has just started

## Biotechnology



# Critical technologies

The critical technology priority fields are:

- advanced manufacturing and materials technologies
- artificial intelligence (AI) technologies
- advanced information and communication technologies
- quantum technologies
- autonomous systems, robotics, positioning, timing and sensing
- biotechnologies
- clean energy generation and storage technologies.

**Critical technologies are built on integrated circuits!**



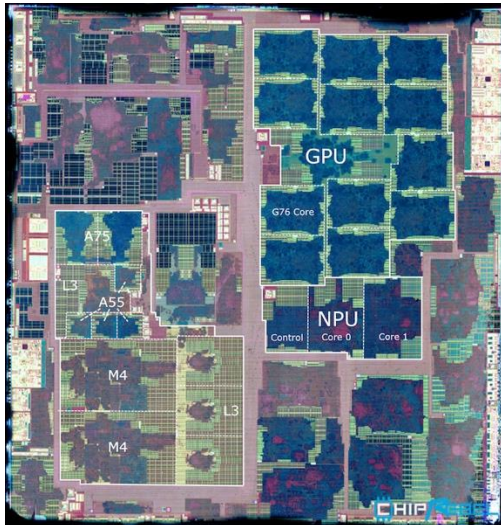
# Integrated Circuit Types

By technology

## Silicon (single element)

~100K-1B transistors / chip  
90% of the global market

- CMOS
- BiPolar



90% of the market

## Compound

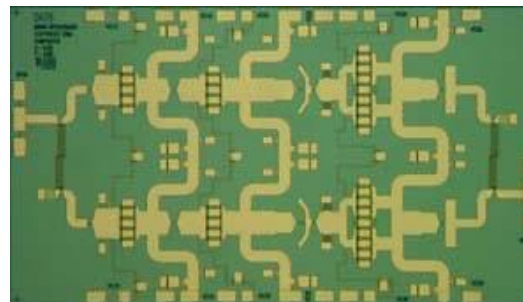
~10-20 transistors / chip  
10% of the global market

### III-V

- GaAs
- GaN
- InP

### IV-IV

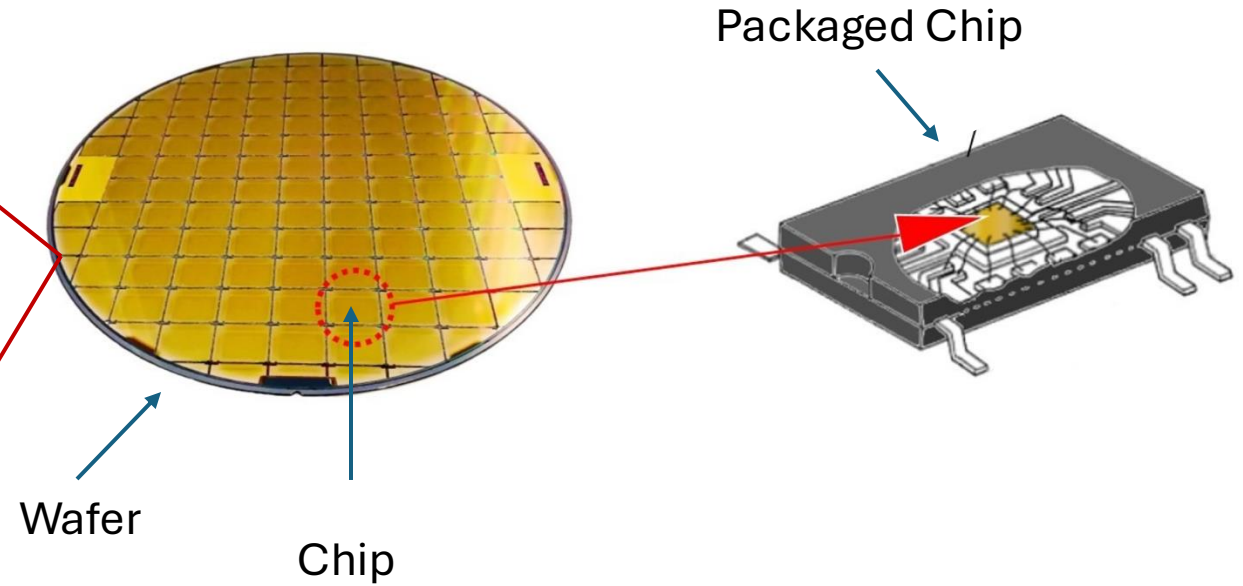
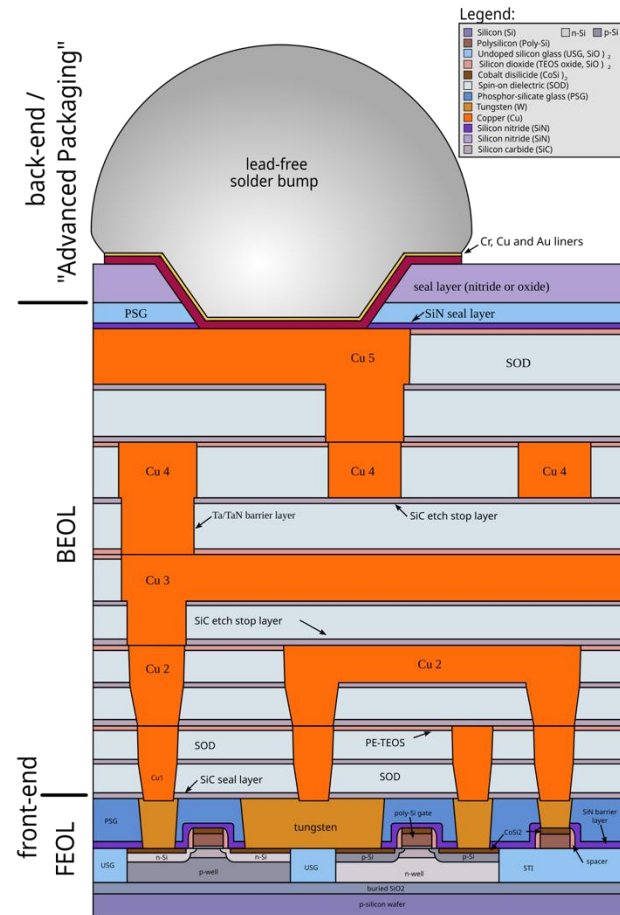
- SiC
- SiGe



10% of the market

5 B Boron	6 C Carbon	7 N Nitrogen	8 O Oxygen
13 Al Aluminium	14 Si Silicon	15 P Phosphorus	16 S Sulfur
31 Ga Gallium	32 Ge Germanium	33 As Arsenic	34 Se Selenium
49 In Indium	50 Sn Tin	51 Sb Antimony	52 Te Tellurium
81 Tl Thallium	82 Pb Lead	83 Bi Bismuth	84 Po Polonium

# How are they made? (CMOS)





### Chip Fabrication Steps

**1** Wafers are sawed out of an ingot of pure crystalline silicon

**2** Polishing

**3** Material deposition or modification

**4** The resist is applied to a spinning wafer to achieve a uniform layer

**5** Using EUV Lithography the chip patterns are "burned" into the resist in an exposure step

**6** The print is developed through etching and heating

**7** Ion Implantation dope exposed regions

**8** The resist is removed

**9** A wafer processing cycle is complete, and one layer has been fabricated

**10** Repeat 40 to 100 times

**11** Cut chips out of the wafer and test

**12** Package and assembly the chips

Mature processes have yields of 30-80%

*Paul van Gerven Bitsand Chips*

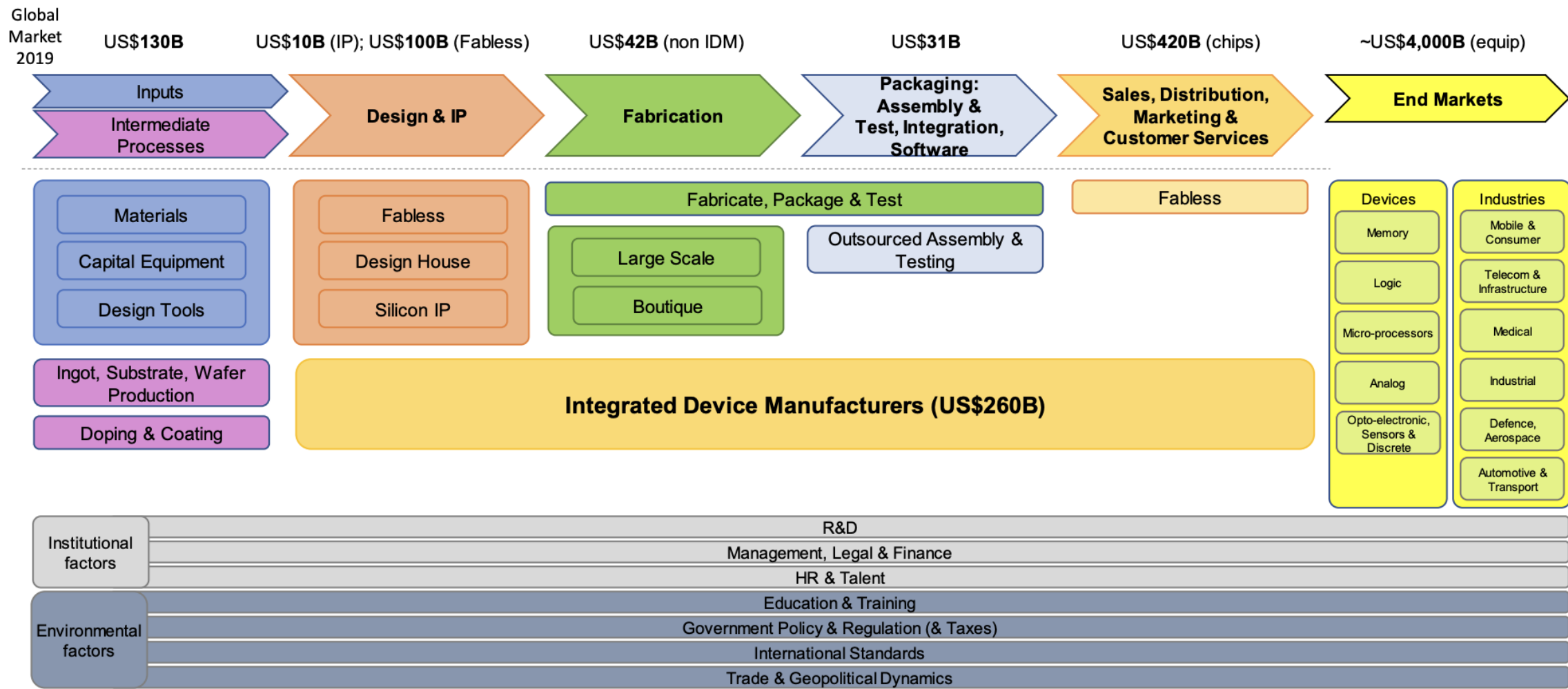




[https://www.youtube.com/watch?v=h\\_zgURwr6nA](https://www.youtube.com/watch?v=h_zgURwr6nA)



# Semiconductor Value Chain

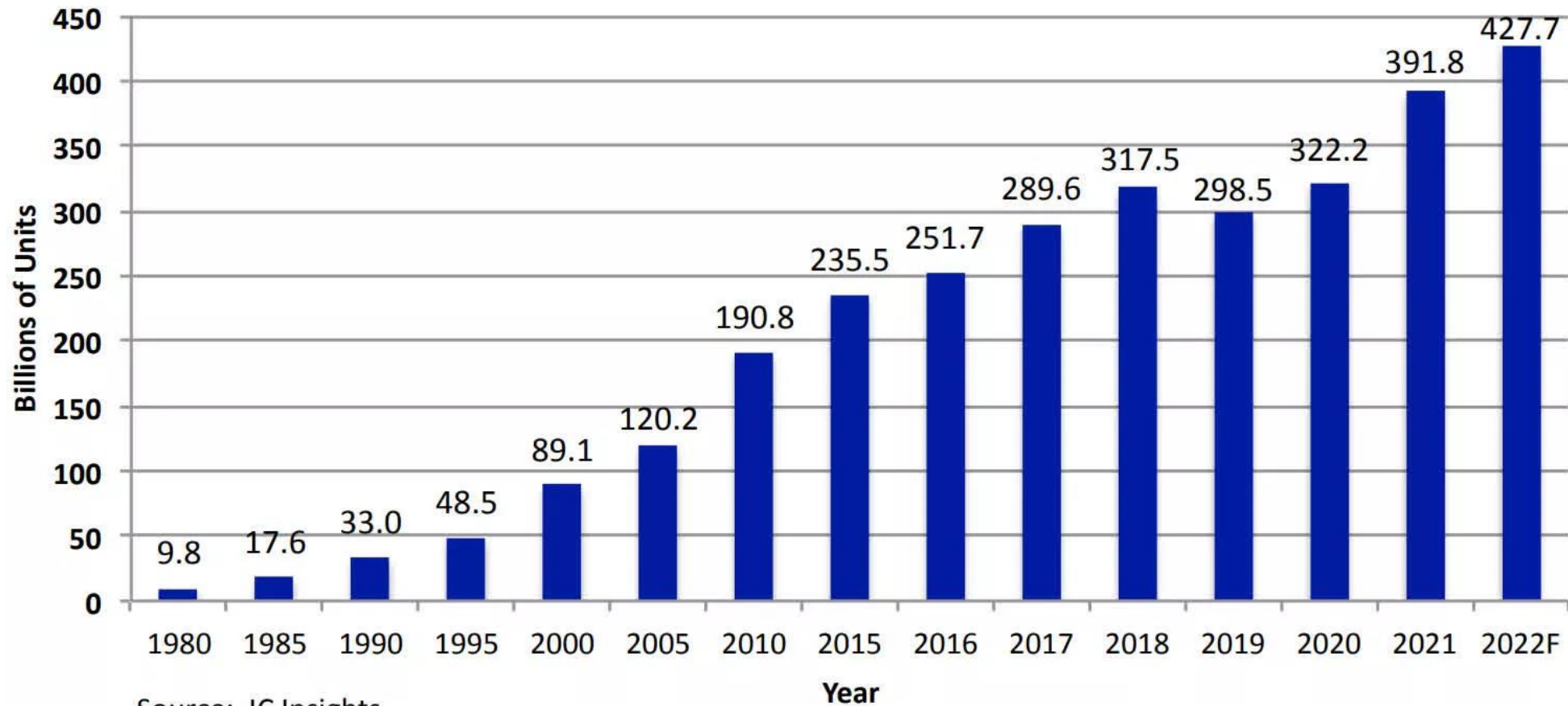


**Figure 1: Semiconductor value chain**

Note: Global market size estimates in US\$ billion. Refer to Appendix 2 for references supporting estimates of market size in 2019.

# Market Size - Annual Shipments

## Worldwide IC Unit Shipment Growth



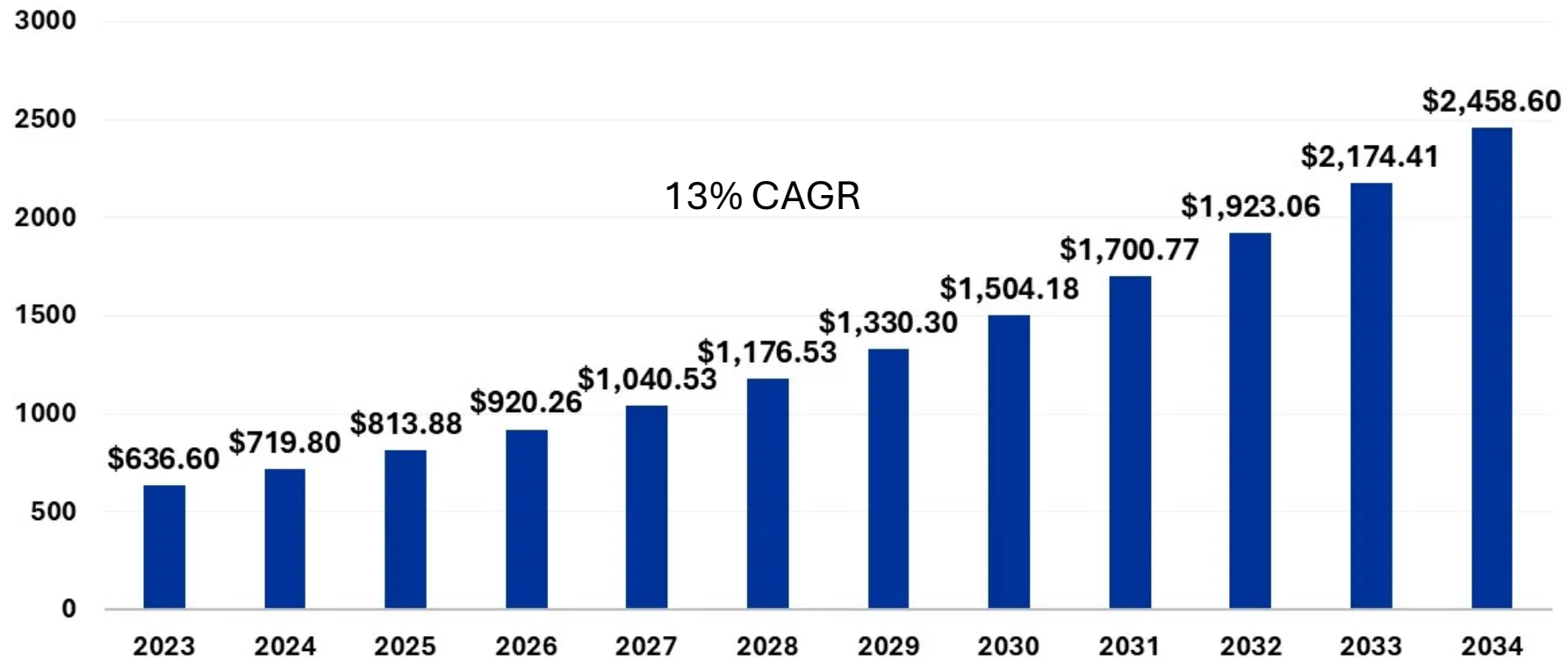
Source: IC Insights



# Market Size – Sales to 2034



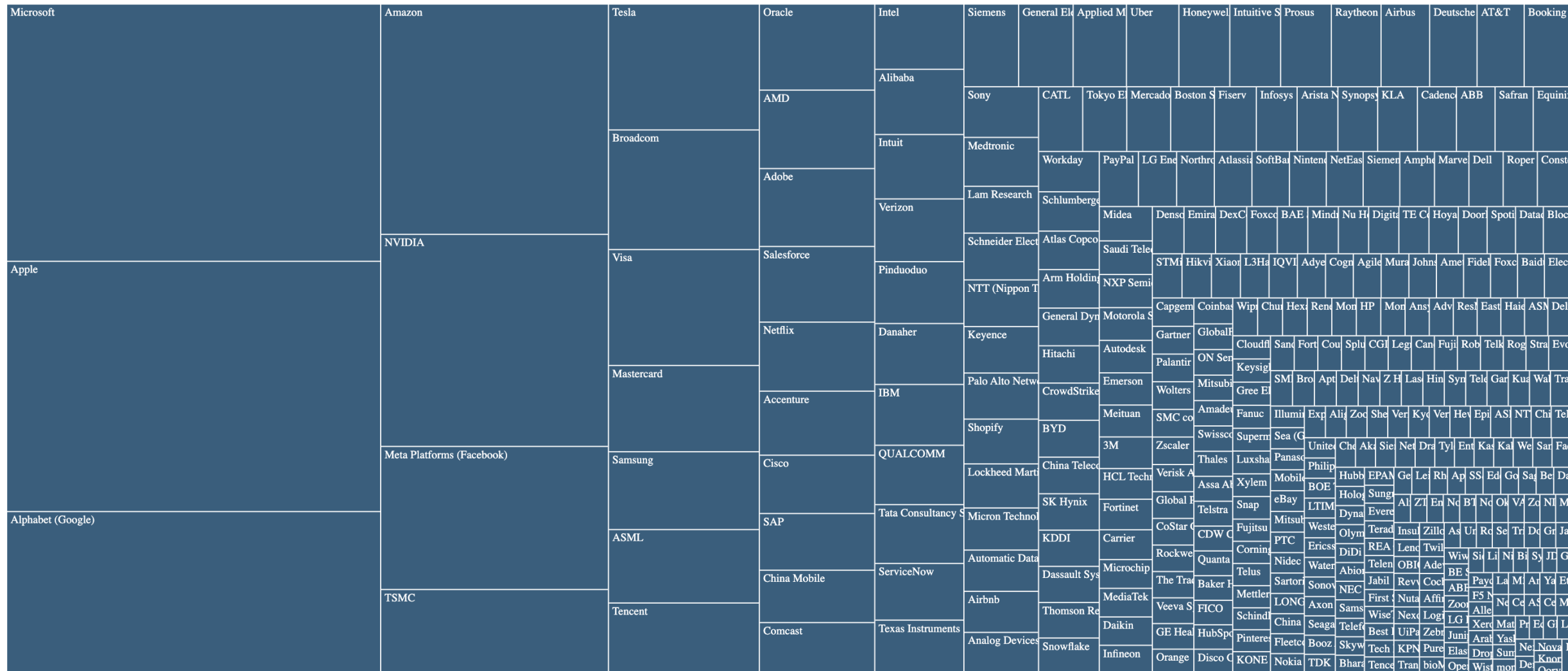
## Integrated Circuit Market Size 2023 to 2034 (USD Billion)



Source: <https://www.precedenceresearch.com/integrated-circuit-market>

# Tech Companies

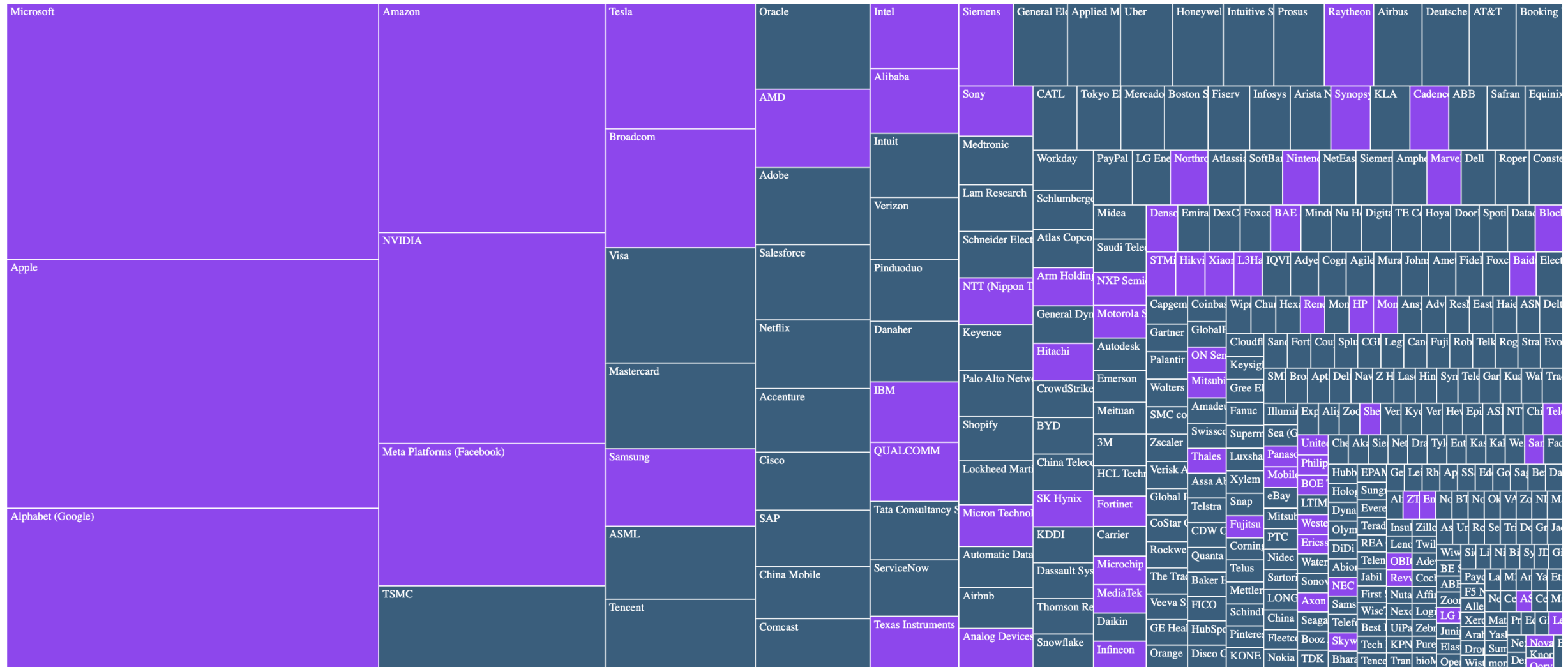
>\$10B USD market cap, total is \$33T





# Tech Companies – That Design Chips

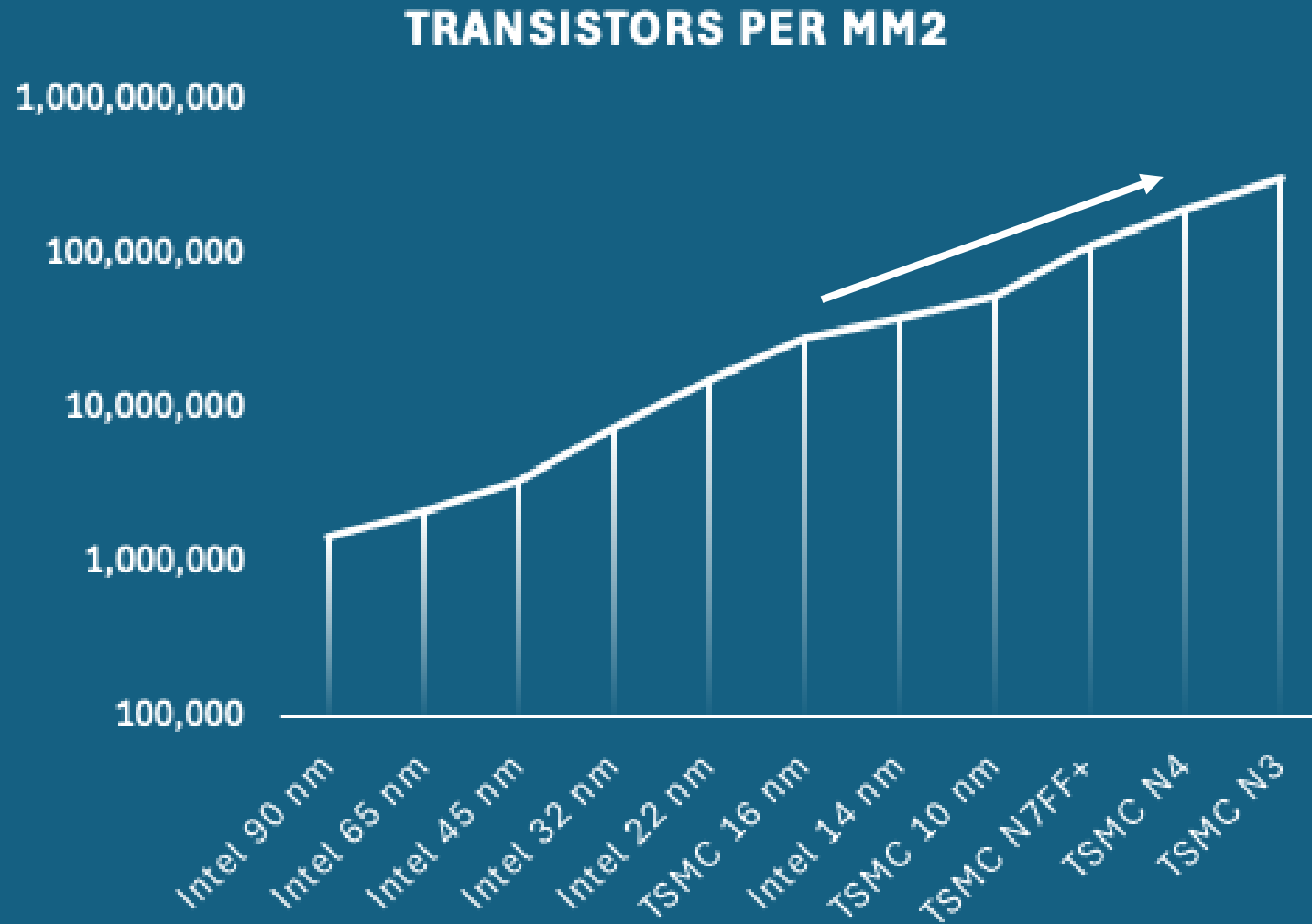
>\$10B USD market cap, total is \$33T



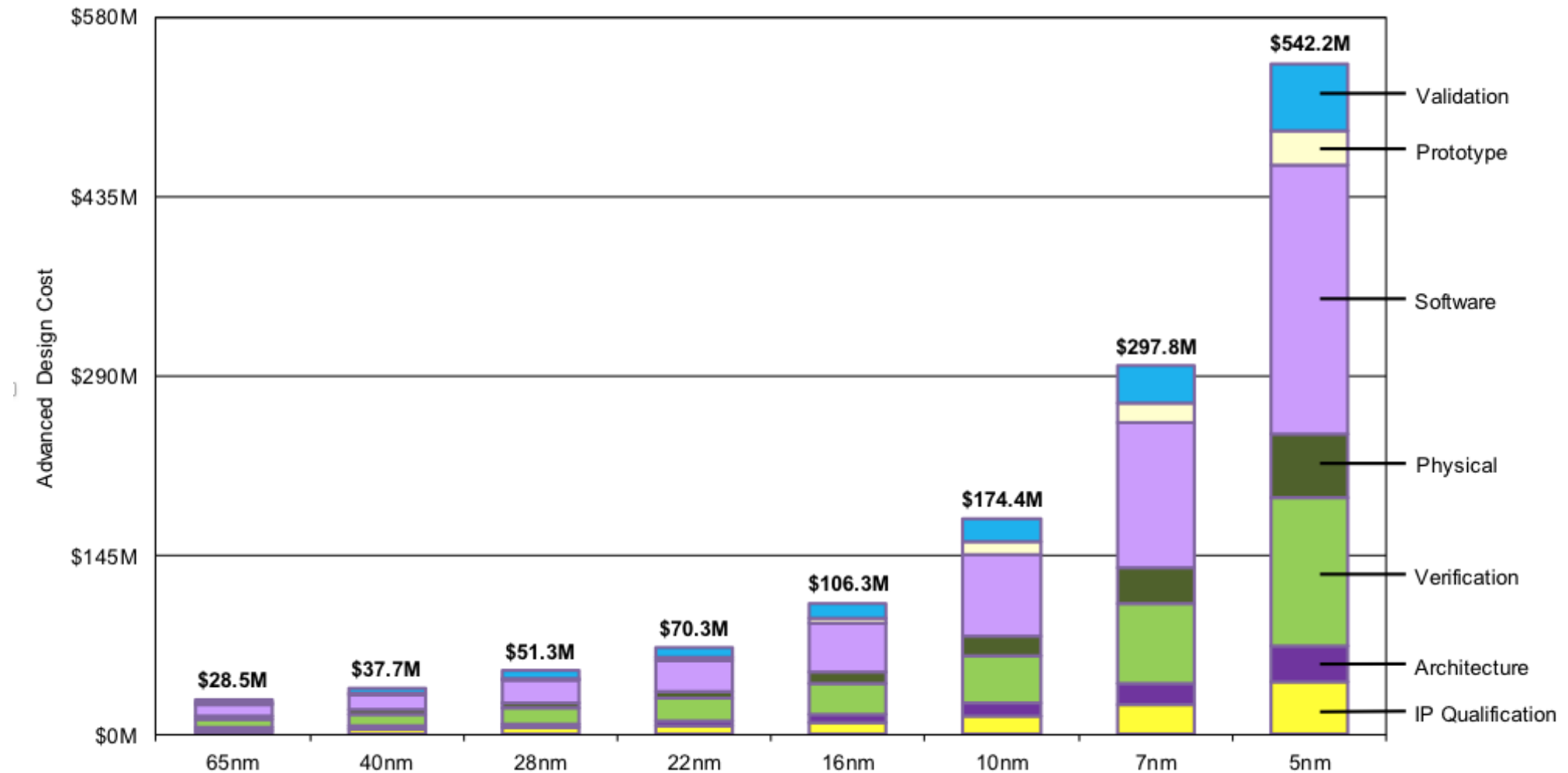
# Trends



# Trends – Transistor Density



# Trends – Increasing costs



# Trends - Advanced Packaging





## TRANSISTOR DENSITY => MORE DIGITAL

Complex RF -> ADC

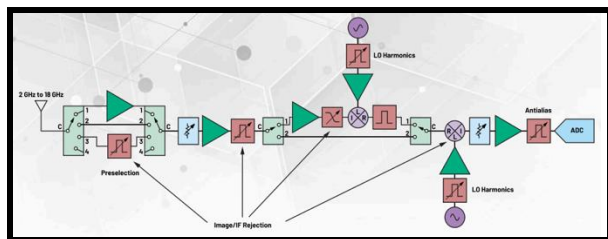
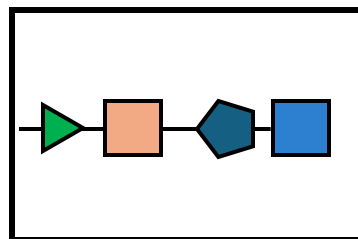
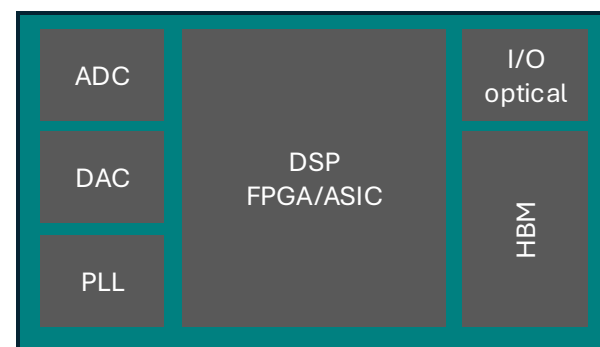
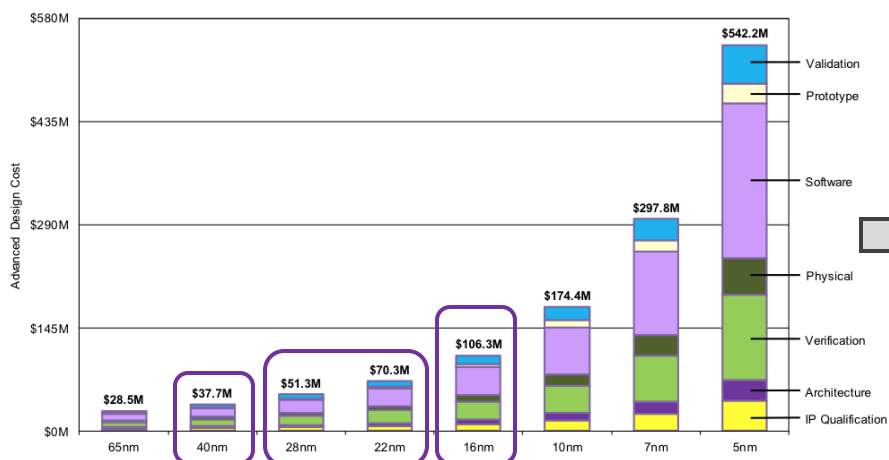


Figure 1. 2 GHz to 18 GHz receiver block diagram.

LNA -> ADC + Digital

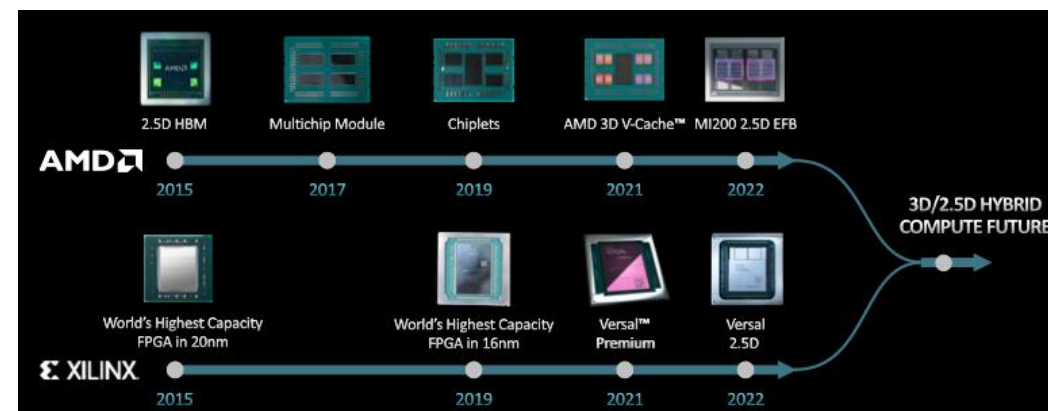


## INCREASING COSTS => SIMPLIFY

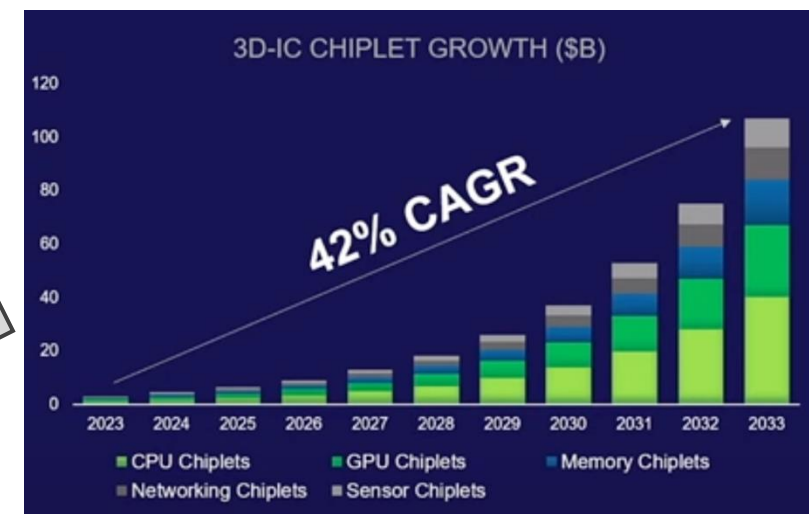


SW (AI/ML) DRIVEN DESIGN AND VERIFICATION  
=> REDUCE DEV COSTS

## CHIPLETS + ADVANCED PACKAGING



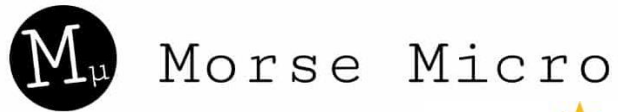
## MARKET GROWTH



Chips In Oz

# Chip Design in Australia

## Headquartered in Australia



## Design Centre in Australia



## Also make chips



## Listed in Australia





# Increasing Participation

## Inputs

Critical minerals, mining and processing

Rare earth minerals, mining and processing

New design tools/  
techniques/methodologies

## Fabless Design and IP

Design centres and startups

Quantum

Biotechnology

Photonics

Communications and sensing

Defence and critical technologies

## Manufacturing

Advanced packaging

*Mature CMOS fab  
(12-28nm)?*

*Compound  
(GaAs/GaN/Other..)?*



**MACQUARIE**  
University

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**SILICON PLATFORMS LAB**

# Macquarie University



MACQUARIE  
University

SILICON PLATFORMS LAB

1990-2000

WiFi (Radiata)  
(CMOS)

11a/b/g Modem



4.75mm by 4.75mm  
8 million transistors  
TSMC 0.13um 7 level metal  
31mW sleep  
206mW Tx  
362mW Rx

2.4GHz/5GHz transceiver



5mm by 5mm  
TSMC 0.13um 7 level metal  
31mW sleep  
405mW Tx  
360mW Rx

2006-2010

60GHz GLIMMR  
(SiGe)

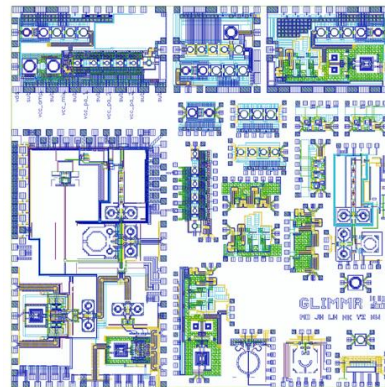
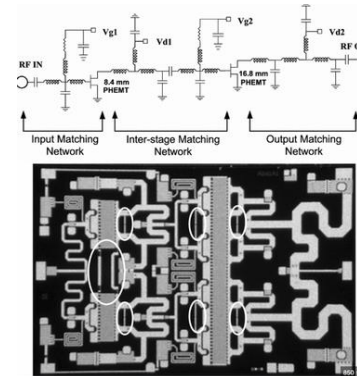


Figure C.3: GLIMMR test-chip 3 (GTC3).

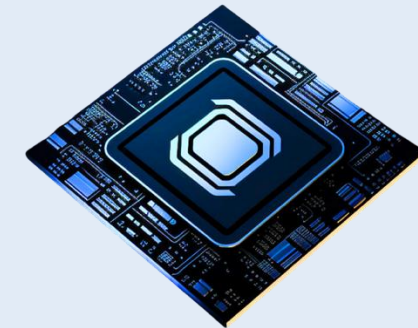
2020-

MADLab  
(GaAs, GaN)



2024-

SiP Lab  
(CMOS, SOI  
advanced packaging)



Neil Weste  
David Skellern

Neil Weste



# Silicon Platforms Lab

## PEOPLE



SILICON PLATFORMS LAB



**Industry Professor  
Mike Boers**



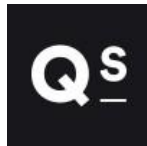
**Senior Lecturer  
Jafar Shojaii**



**Admin Officer  
Shannah Gray  
Williams**



RF / mmWave  
WiFi  
Cellular  
Satellite



ASIC  
CMOS  
Rad Hard

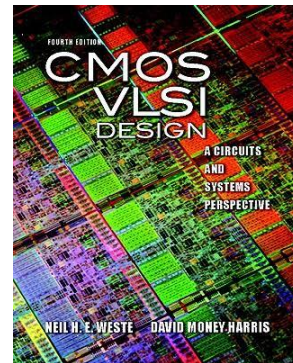
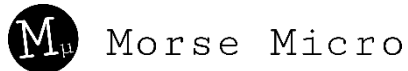


# Silicon Platforms Lab

PEOPLE



**Adjunct Professor  
Neil Weste**



ASIC  
CMOS  
Digital Design  
RF / mmWave



**Adjunct Professor  
David Skellern (AO)**



ASIC  
CMOS  
GaN/GaAs  
Satellite

# Silicon Platforms Lab

PEOPLE



SILICON PLATFORMS LAB

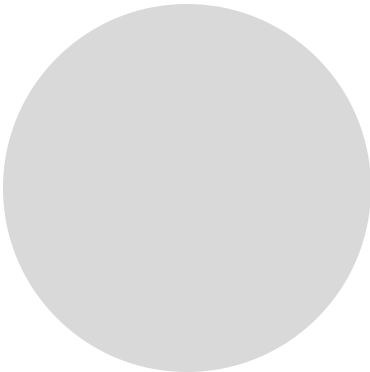


Senior Principal  
Engineer  
Lead Systems  
Architect

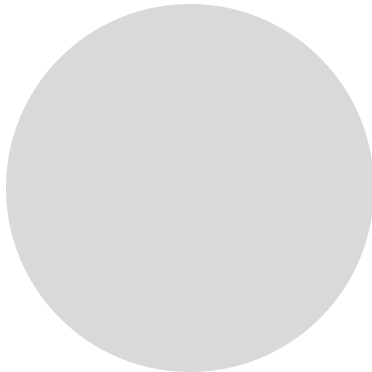
Rick M. P. Berg



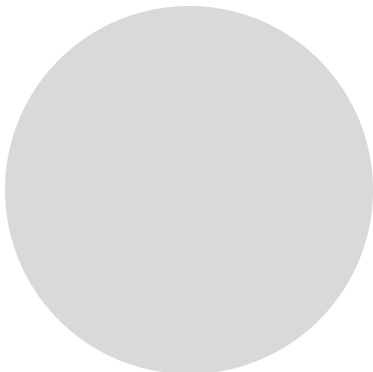
RF / mmWave  
Cellular  
DSP, DPD



Lead Digital  
Engineer  
Hiring



Lead HW Engineer  
Hiring



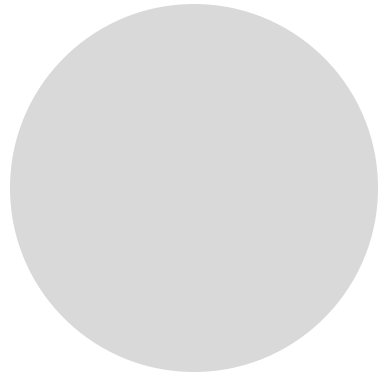
Lead ASIC/AMS  
Engineer  
Hiring



# We are hiring

PEOPLE

## 7 Open Positions + HDR Roles



**You!**

- Digital Backend Engineer
- Layout Engineer
- Lead Analogue/Mixed Signal Engineer
- Lead Digital Engineer
- Lead Hardware Engineer
- Research Fellow in High Performance Mixed Signal CMOS Design
- Senior Software Engineer
- Masters + PhD scholarships

## Learn More

<https://www.mq.edu.au/faculty-of-science-and-engineering/our-research/silicon-platforms-lab>

# Focus areas

- Communications and sensing systems using chiplets and advanced packaging – with a focus on SW driven efficient design
- Training the next generation of integrated circuit design engineers
- Supporting research teams and startups that require integrated circuits
  - Biotechnology
  - Quantum sensing and compute
  - Photonics

# Why now?

- Integrated circuits power all advanced technology
- Critical technologies and Defence rely on them
- New era of scaling using heterogenous integration provides a good entry point
- Opportunity for new highly efficient SW driven design flows
- Huge market opportunity

# How to work with us

- Research collaboration
- Support for early-stage start-ups and University spin-outs
- Research and design services for industry
- Custom ASIC design
- Student internships



# Thank You!

Contact  
Mike Boers  
[m.boers@mq.edu.au](mailto:m.boers@mq.edu.au)



**MACQUARIE**  
University  
SYDNEY • AUSTRALIA