In this assignment, you will be building a streaming FM Stereo Radio. Here is the radio software

Using the attached C software model, you will need to implement each of the function blocks in SystemVerilog. Compile the software and run the FM Radio to see how it works. It will take it raw binary (digital) data as input, which may be found in the "test" directory. Refer to the readme page for compilation instructions.

Note: If you're on a Mac or Linux, you may need to adjust the header files and/or the soundcard interface. I recommend using Cygwin on Windows and gcc or g++ to compile. Otherwise, I recommend using MS Visual Studio, which is a good platform for debugging.

Throughout your design I recommend that you create input/output vectors (from the software program) to test each module. Don't wait until the end to debug the entire design, as that will likely result in many complications.

In your design, you should employ the following strategies:

* C macros should be implemented as inlined SystemVerilog functions
* Use the same quantization bit width as in the software (10-bits).
* Create a package with the array of filter coefficients and use parameters to configure the filter taps and coefficients for each module.
* High-level for-loops can be eliminated and replaced with streaming FIFOs
* Unroll internal function loops completely where applicable, such as shift registers
* Apply one or more optimizations, such as loop unrolling or pipelining where applicable
* Implement the division algorithm discussed in class for the qarctan function. Do not use the division operation (e.g. a/b for variables).
* Optimize FIFO buffer sizes
* For synthesis, your design should target 100MHZ (10ns), which means you will need to optimize the long data paths to achieve or get very close to the target frequency.
* Implement UVM model to validate the design. I should be able to run the run\_simulation script to run the program and simulation.

For simulation/verification, I recommend modifying the C program to run only a small subset of the entire input and output data (maybe a few K). This way you can design and test much more rapidly. Otherwise the entire file may take hours to complete simulation.

What you will turn in:

* The SystemVerilog files (design, FIFOs, UVM, etc) - 15 pts
* Working simulation that includes:  - 5 pts
  + Modelsim sim.do and wave.do files
  + UVM model
  + Input & Output simulation data files (a small subset of a few KB)
  + The simulation should run to completion when I type "run\_simulation" with the following operations:
    1. create the work directory
    2. compile the SystemVerilog files
    3. compile the UVM files
    4. run vsim on the UVM module with QuestaSim
    5. load signals in to the wave as hexadecimal values, separating components by dividers
    6. Run the simulation to completion
    7. Compare outputs and report total cycles and any errors
    8. The simulation must be able to run start to finish upon execution of the simulation file.
* A project report (no more than 10 pages) with the following sections:  - 10pts
  + Basic FM Radio background / theory
  + The system architecture
  + Design process
  + Optimizations and impact on design
  + Simulation and performance results, including throughput analysis (e.g. how many Mb/s for each function) and bottlenecks.
  + Synthesis results, including memory and resource utilization, the resulting frequency, and the longest data path. You should also discuss how you achieved said results.

Before submitting:

1. Clean your simulation work directory
2. Clean your synthesis work directory
3. Remove all unnecessary files
4. Zip your entire directory structure and name it using the format: **team\_[number]\_final\_project.zip**
5. Your zip file should be no more than 20MB.
6. Upload your zip file and pdf report separately using the format: **team\_[number]\_final\_report.pdf**