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SWEET16: The 6502 Dream Machine

While writing Apple BASIC for a 6502 microprocessor I repeatedly encountered a variant of Murphy's Law. Briefly stated, any routine operating on 16 bit data will require at least twice the code that it should. Programs making extensive use of 16 bit pointers (such as compilers, editors and assemblers) are included in this category. In my case, even the addition of a few double byte instructions to the 6502 would have only slightly alleviated the problem. What I really needed was a hybrid of the MOS Technology 6502 and RCA 1800 architectures, a powerful 8 bit data handler complemented by an easy to use processor with an abundance of 16 bit registers and excellent pointer capability. My solution was to implement a nonexistent 16 bit "metaprocessor" in software, interpreter style, which I call SWEET16. This metaprocessor was sketched at the end of my article in May 1977 BYTE, and the purpose of this article is to fill in the details of SWEET16.

SWEET16 is based around sixteen 16 bit

registers called R0 to R15, actually implemented as 32 memory locations. R0 doubles as the SWEET16 accumulator (ACC), R15 as the program counter (PC), and R14 as the status register. R13 holds compare instruction results and R12 is the subroutine return stack pointer if SWEET16 subroutines are used. All other SWEET16 registers are at the user's unrestricted disposal.

SWEET16 instructions fall into register and nonregister categories. The register operations specify one of the 16 registers to be used as either a data element or a pointer to data in memory depending on the specific instruction. For example, the instruction INR R5 uses R5 as data and ST @R7 uses R7 as a pointer to data in memory. Except for the SET instruction, register operations only require one byte. The nonregister operations are primarily 6502 style branches with the second byte specifying a ± 127 byte displacement relative to the address of the following instruction. If a prior register operation result meets a specified branch condition, the displacement is added to SWEET16's program counter, effecting a branch.

SWEET16 is intended as a 6502 enhancement package, not a stand alone processor. A 6502 program switches to SWEET16 mode with a subroutine call, and subsequent code is interpreted as SWEET16 instructions. The nonregister operation RTN returns the user program to the 6502's direct execution mode after restoring the internal register contents (A, X, Y, P and S). The example of listing 1 illustrates how to use SWEET16 in some program segment.

Instruction Descriptions

The SWEET16 op code list is short and uncomplicated. Excepting relative branch displacements, hand assembly is trivial. All register op codes are formed by combining two hexadecimal digits, one for the op code and one to specify a register. For example,

op codes 15 and 45 both specify register R5 while codes 23, 27 and 29 are all ST (store) operations. Most register operations of SWEET16 are assigned to numerically adjacent pairs to facilitate remembering them. Thus LD and ST are op codes 2n and 3n respectively, while LD @ and ST @ are codes 4n and 5n.

Operation codes 00 to 0C (hexadecimal) are assigned to the 13 nonregister operations. Except for RTN (op code 0), BK (0A), and RS (B), the nonregister operations are 6502 style relative branches. The second byte of a branch instruction contains a ± 127 byte displacement value (in two's complement form) relative to the address of the instruction immediately following the branch. If a specified branch condition is met by the prior register operation result, the displacement is added to the program counter effecting a branch. Except for BR (Branch always) and BS (Branch to Subroutine), the branch operation codes are assigned in complementary pairs, rendering them easily remembered for hand coding. For example, Branch if Plus and Branch if Minus are op codes 04 and 05, while Branch if Zero and Branch if NonZero are op codes 06 and 07.

Theory of Operation

SWEET16 execution mode begins with a subroutine call to SW16 (see listing 2, an assembly of SWEET16). The user must insure that the 6502 is in hexadecimal mode upon entry. [For those unfamiliar with the 6502, arithmetic is either decimal or hexadecimal (binary) depending on a programmable flag. .CH] All 6502 registers are saved at this time, to be restored when a SWEET16 RTN instruction returns control to the 6502. If you can tolerate indefinite 6502 register contents upon exit, approximately 30 μ s may be saved by entering SWEET16 at location SW16 + 3. Because this might cause an inadvertent switch from hexadecimal to decimal mode, it is advisable to enter at SW16 the first time through.

After saving the 6502 registers, SWEET16 initializes its program counter (R15) with the subroutine return address off the 6502 stack. SWEET16's program counter points to the location preceding the next instruction to be executed. Following the subroutine call are 1 byte, 2 byte, or 3 byte long SWEET16 instructions, stored in ascending

Listing 2: SWEET16 assembly. The SWEET16 program, assembled to reside at location 800 hexadecimal, is presented by this listing. The primary entry point is at the beginning, location SW16. An alternate entry point if there is no need to save processor registers is at location 803 in this assembly, SW16+3.

```
11:16 A-M-+ THU, MAY 12, 1977
SWEET16 INTERPRETER
00001 *****
00002 * APPLE-II PSEUDO *
00003 * MACHINE INTERPRETER *
00004 * S. WOZNIAK *
00005 * APPLE COMPUTER INC *
00006 *
00007 *****
00008 *TITLE "SWEET16 INTERPRETER"
00009 *****
00010 LD R0, #0          ; R0 = 0
00011 LD R1, #0          ; R1 = 0
00012 LD R2, #0          ; R2 = 0
00013 LD R3, #0          ; R3 = 0
00014 LD R4, #0          ; R4 = 0
00015 LD R5, #0          ; R5 = 0
00016 LD R6, #0          ; R6 = 0
00017 LD R7, #0          ; R7 = 0
00018 LD R8, #0          ; R8 = 0
00019 LD R9, #0          ; R9 = 0
00020 LD R10, #0         ; R10 = 0
00021 LD R11, #0         ; R11 = 0
00022 LD R12, #0        ; R12 = 0
00023 LD R13, #0        ; R13 = 0
00024 LD R14, #0        ; R14 = 0
00025 LD R15, #0        ; R15 = 0
00026 LD R16, #0        ; R16 = 0
00027 LD R17, #0        ; R17 = 0
00028 LD R18, #0        ; R18 = 0
00029 LD R19, #0        ; R19 = 0
00030 LD R20, #0        ; R20 = 0
00031 LD R21, #0        ; R21 = 0
00032 LD R22, #0        ; R22 = 0
00033 LD R23, #0        ; R23 = 0
00034 LD R24, #0        ; R24 = 0
00035 LD R25, #0        ; R25 = 0
00036 LD R26, #0        ; R26 = 0
00037 LD R27, #0        ; R27 = 0
00038 LD R28, #0        ; R28 = 0
00039 LD R29, #0        ; R29 = 0
00040 LD R30, #0        ; R30 = 0
00041 LD R31, #0        ; R31 = 0
00042 LD R32, #0        ; R32 = 0
00043 LD R33, #0        ; R33 = 0
00044 LD R34, #0        ; R34 = 0
00045 LD R35, #0        ; R35 = 0
00046 LD R36, #0        ; R36 = 0
00047 LD R37, #0        ; R37 = 0
00048 LD R38, #0        ; R38 = 0
00049 LD R39, #0        ; R39 = 0
00050 LD R40, #0        ; R40 = 0
00051 LD R41, #0        ; R41 = 0
00052 LD R42, #0        ; R42 = 0
00053 LD R43, #0        ; R43 = 0
00054 LD R44, #0        ; R44 = 0
00055 LD R45, #0        ; R45 = 0
00056 LD R46, #0        ; R46 = 0
00057 LD R47, #0        ; R47 = 0
00058 LD R48, #0        ; R48 = 0
00059 LD R49, #0        ; R49 = 0
00060 LD R50, #0        ; R50 = 0
00061 LD R51, #0        ; R51 = 0
00062 LD R52, #0        ; R52 = 0
00063 LD R53, #0        ; R53 = 0
00064 LD R54, #0        ; R54 = 0
00065 LD R55, #0        ; R55 = 0
00066 LD R56, #0        ; R56 = 0
00067 LD R57, #0        ; R57 = 0
00068 LD R58, #0        ; R58 = 0
00069 LD R59, #0        ; R59 = 0
00070 LD R60, #0        ; R60 = 0
00071 LD R61, #0        ; R61 = 0
00072 LD R62, #0        ; R62 = 0
00073 LD R63, #0        ; R63 = 0
00074 LD R64, #0        ; R64 = 0
00075 LD R65, #0        ; R65 = 0
00076 LD R66, #0        ; R66 = 0
00077 LD R67, #0        ; R67 = 0
00078 LD R68, #0        ; R68 = 0
00079 LD R69, #0        ; R69 = 0
00080 LD R70, #0        ; R70 = 0
00081 LD R71, #0        ; R71 = 0
00082 LD R72, #0        ; R72 = 0
00083 LD R73, #0        ; R73 = 0
00084 LD R74, #0        ; R74 = 0
00085 LD R75, #0        ; R75 = 0
00086 LD R76, #0        ; R76 = 0
00087 LD R77, #0        ; R77 = 0
00088 LD R78, #0        ; R78 = 0
00089 LD R79, #0        ; R79 = 0
00090 LD R80, #0        ; R80 = 0
00091 LD R81, #0        ; R81 = 0
00092 LD R82, #0        ; R82 = 0
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00094 LD R84, #0        ; R84 = 0
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00096 LD R86, #0        ; R86 = 0
00097 LD R87, #0        ; R87 = 0
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00099 LD R89, #0        ; R89 = 0
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00102 LD R92, #0        ; R92 = 0
00103 LD R93, #0        ; R93 = 0
00104 LD R94, #0        ; R94 = 0
00105 LD R95, #0        ; R95 = 0
00106 LD R96, #0        ; R96 = 0
00107 LD R97, #0        ; R97 = 0
00108 LD R98, #0        ; R98 = 0
00109 LD R99, #0        ; R99 = 0
00110 LD R100, #0       ; R100 = 0
00111 LD R101, #0       ; R101 = 0
00112 LD R102, #0       ; R102 = 0
00113 LD R103, #0       ; R103 = 0
00114 LD R104, #0       ; R104 = 0
00115 LD R105, #0       ; R105 = 0
00116 LD R106, #0       ; R106 = 0
00117 LD R107, #0       ; R107 = 0
00118 LD R108, #0       ; R108 = 0
00119 LD R109, #0       ; R109 = 0
00120 LD R110, #0       ; R110 = 0
00121 LD R111, #0       ; R111 = 0
00122 LD R112, #0       ; R112 = 0
00123 LD R113, #0       ; R113 = 0
00124 LD R114, #0       ; R114 = 0
00125 LD R115, #0       ; R115 = 0
00126 LD R116, #0       ; R116 = 0
00127 LD R117, #0       ; R117 = 0
00128 LD R118, #0       ; R118 = 0
00129 LD R119, #0       ; R119 = 0
00130 LD R120, #0       ; R120 = 0
00131 LD R121, #0       ; R121 = 0
00132 LD R122, #0       ; R122 = 0
00133 LD R123, #0       ; R123 = 0
00134 LD R124, #0       ; R124 = 0
00135 LD R125, #0       ; R125 = 0
00136 LD R126, #0       ; R126 = 0
00137 LD R127, #0       ; R127 = 0
00138 LD R128, #0       ; R128 = 0
00139 LD R129, #0       ; R129 = 0
00140 LD R130, #0       ; R130 = 0
00141 LD R131, #0       ; R131 = 0
00142 LD R132, #0       ; R132 = 0
00143 LD R133, #0       ; R133 = 0
00144 LD R134, #0       ; R134 = 0
00145 LD R135, #0       ; R135 = 0
00146 LD R136, #0       ; R136 = 0
00147 LD R137, #0       ; R137 = 0
00148 LD R138, #0       ; R138 = 0
00149 LD R139, #0       ; R139 = 0
00150 LD R140, #0       ; R140 = 0
00151 LD R141, #0       ; R141 = 0
00152 LD R142, #0       ; R142 = 0
00153 LD R143, #0       ; R143 = 0
00154 LD R144, #0       ; R144 = 0
00155 LD R145, #0       ; R145 = 0
00156 LD R146, #0       ; R146 = 0
00157 LD R147, #0       ; R147 = 0
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00179 LD R169, #0       ; R169 = 0
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00281 LD R271, #0       ; R271 = 0
00282 LD R272, #0       ; R272 = 0
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00302 LD R292, #0       ; R292 = 0
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00317 LD R307, #0       ; R307 = 0
00318 LD R308, #0       ; R308 = 0
00319 LD R309, #0       ; R309 = 0
00320 LD R310, #0       ; R310 = 0
00321 LD R311, #0       ; R311 = 0
00322 LD R312, #0       ; R312 = 0
00323 LD R313, #0       ; R313 = 0
00324 LD R314, #0       ; R314 = 0
00325 LD R315, #0       ; R315 = 0
00326 LD R316, #0       ; R316 = 0
00327 LD R317, #0       ; R317 = 0
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00360 LD R350, #0       ; R350 = 0
00361 LD R351, #0       ; R351 = 0
00362 LD R352, #0       ; R352 = 0
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00386 LD R376, #0       ; R376 = 0
00387 LD R377, #0       ; R377 = 0
00388 LD R378, #0       ; R378 = 0
00389 LD R379, #0       ; R379 = 0
00390 LD R380, #0       ; R380 = 0
00391 LD R381, #0       ; R381 = 0
00392 LD R382, #0       ; R382 = 0
00393 LD R383, #0       ; R383 = 0
00394 LD R384, #0       ; R384 = 0
00395 LD R385, #0       ; R385 = 0
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00397 LD R387, #0       ; R387 = 0
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00405 LD R395, #0       ; R395 = 0
00406 LD R396, #0       ; R396 = 0
00407 LD R397, #0       ; R397 = 0
00408 LD R398, #0       ; R398 = 0
00409 LD R399, #0       ; R399 = 0
00410 LD R400, #0       ; R400 = 0
00411 LD R401, #0       ; R401 = 0
00412 LD R402, #0       ; R402 = 0
00413 LD R403, #0       ; R403 = 0
00414 LD R404, #0       ; R404 = 0
00415 LD R405, #0       ; R405 = 0
00416 LD R406, #0       ; R406 = 0
00417 LD R407, #0       ; R407 = 0
00418 LD R408, #0       ; R408 = 0
00419 LD R409, #0       ; R409 = 0
00420 LD R410, #0       ; R410 = 0
00421 LD R411, #0       ; R411 = 0
00422 LD R412, #0       ; R412 = 0
00423 LD R413, #0       ; R413 = 0
00424 LD R414, #0       ; R414 = 0
00425 LD R415, #0       ; R415 = 0
00426 LD R416, #0       ; R416 = 0
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00430 LD R420, #0       ; R420 = 0
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00432 LD R422, #0       ; R422 = 0
00433 LD R423, #0       ; R423 = 0
00434 LD R424, #0       ; R424 = 0
00435 LD R425, #0       ; R425 = 0
00436 LD R426, #0       ; R426 = 0
00437 LD R427, #0       ; R427 = 0
00438 LD R428, #0       ; R428 = 0
00439 LD R429, #0       ; R429 = 0
00440 LD R430, #0       ; R430 = 0
00441 LD R431, #0       ; R431 = 0
00442 LD R432, #0       ; R432 = 0
00443 LD R433, #0       ; R433 = 0
00444 LD R434, #0       ; R434 = 0
00445 LD R435, #0       ; R435 = 0
00446 LD R436, #0       ; R436 = 0
00447 LD R437, #0       ; R437 = 0
00448 LD R438, #0       ; R438 = 0
00449 LD R439, #0       ; R439 = 0
00450 LD R440, #0       ; R440 = 0
00451 LD R441, #0       ; R441 = 0
00452 LD R442, #0       ; R442 = 0
00453 LD R443, #0       ; R443 = 0
00454 LD R444, #0       ; R444 = 0
00455 LD R445, #0       ; R445 = 0
00456 LD R446, #0       ; R446 = 0
00457 LD R447, #0       ; R447 = 0
00458 LD R448, #0       ; R448 = 0
00459 LD R449, #0       ; R449 = 0
00460 LD R450, #0       ; R450 = 0
00461 LD R451, #0       ; R451 = 0
00462 LD R452, #0       ; R452 = 0
00463 LD R453, #0       ; R453 = 0
00464 LD R454, #0       ; R454 = 0
00465 LD R455, #0       ; R455 = 0
00466 LD R456, #0       ; R456 = 0
00467 LD R457, #0       ; R457 = 0
00468 LD R458, #0       ; R458 = 0
00469 LD R459, #0       ; R459 = 0
00470 LD R4
```