1.1.

a. Transfer the contents of register PC to register MAR
b. Issue a Read command to memory, and then wait until it has transferred the requested word into register MDR
c. Transfer the instruction from MDR into IR and decode it
d. Transfer the address LOCA from IR to MAR
e. Issue a Read command and wait until MDR is loaded
f. Transfer contents of MDR to the ALU
g. Transfer contents of R0 to the ALU
h. Perform addition of the two operands in the ALU and transfer result into R0
i. Transfer contents of PC to ALU
j. Add 1 to operand in ALU and transfer incremented address to PC

1.3 (a) Load A,R0
Load B,R1
Add R0,R1
Store R1,C

1.3 (b) Yes; Move B,C
Add A,C

1.5. (a) Let $T_R = (N_R \text{ X } S_R) / R_R$ and $T_C = (N_C \text{ X } S_C) / R_C$ be execution times on the RISC and CISC processors, respectively. Equating execution times and clock rates, we have

$$1.2N_R = 1.5N_C$$

Then

$$N_C / N_R = 1.2 / 1.5 = 0.8$$

Therefore, the largest allowable value for N_C is 80% of N_R.

1.5. (b) In this case

$$1.2N_R / 1.15 = 1.5N_C / 1.00$$

Then

$$N_C / N_R = 1.2 / (1.15 \text{ X } 1.5) = 0.696$$

Therefore, the largest allowable value for N_C is 69.6% of N_R.