Assignment 2

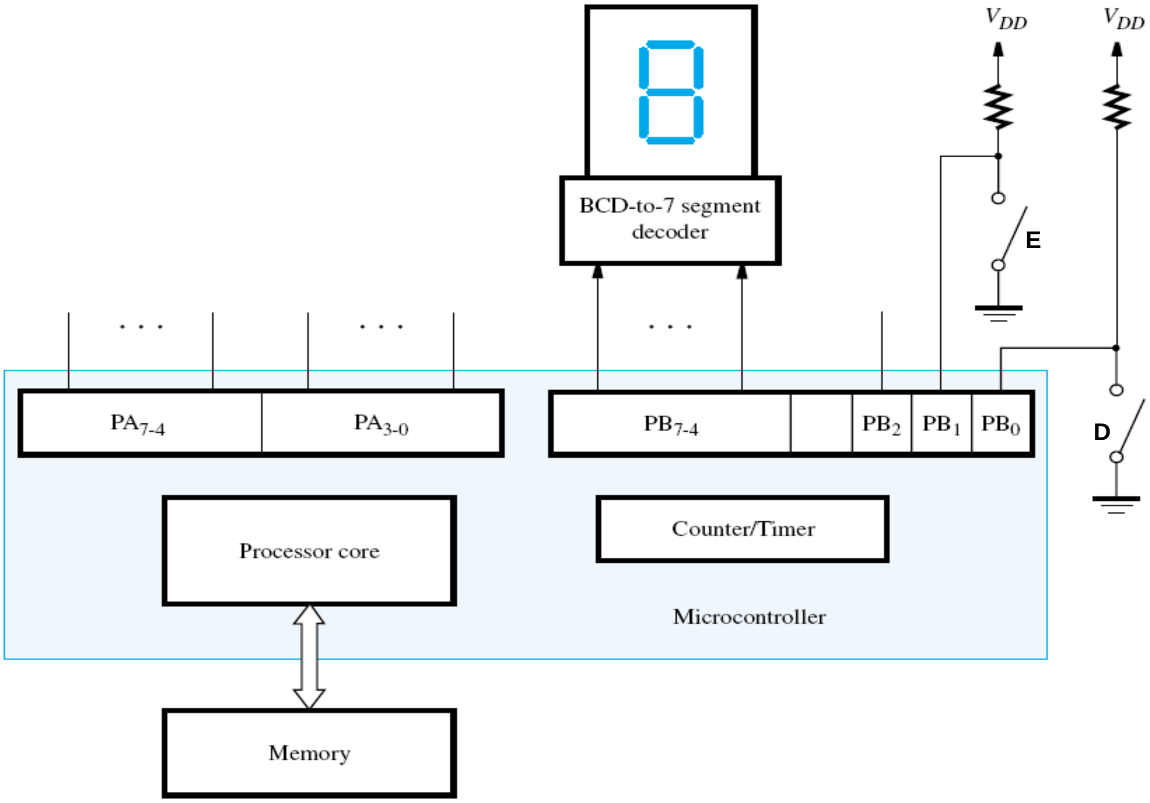
Due October 13, 13:59pm

NOTE: Late submissions will NOT be accepted. Please put your solutions in the CENG 355 **drop-box** (ELW, second floor) – they will be collected at **14:00**.

1. [10 points] The textbook's microcontroller below is responsible for 2 tasks: (1) conditionally incrementing the displayed digit every second, and (2) keeping track of the **E** and **D** switches: pressing **E** enables the process of incrementing the digit every second, while pressing **D** disables that process. Write the corresponding C program, assuming that the **first task** is the ISR whose address is stored at location **0x20**, and the **second task** is the main program. Assume that bit **PSR[6]** is the processor's interrupt-enable bit, and **Port B** is always ready to receive data from the processor. Initially, the 7-segment display shows **0**, and it is not being incremented.

- *Main Program*: If **D** has been pressed, the digit is not allowed to increment every second (until **E** is pressed). If **E** has been pressed, the digit is allowed to increment every second (until **D** is pressed).
- *ISR*: The 100-MHz Counter/Timer must be configured to generate interrupts every second. The displayed digit must be incremented, provided that **E** was pressed last (i.e., the process of incrementing the digit is enabled). If **D** was pressed last, the displayed digit is unchanged (i.e., the process of incrementing the digit is disabled).

Note: Incrementing **9** gives **0**.



2. [10 points] Recall **Question 1**, where the microcontroller was performing 2 tasks: (1) conditionally incrementing the displayed digit every second, and (2) keeping track of the **E** and **D** switches: pressing **E** enabled the process of incrementing the digit every second, while pressing **D** disabled that process. For this question, write the corresponding C program, assuming that the **first task** is the main program, and the **second task** is the ISR whose address is stored at location **0x20**. Assume that bit **PSR[6]** is the processor's interrupt-enable bit, and **Port B** is always ready to receive data from the processor. Initially, the 7-segment display shows **0**, and it is not being incremented.

- *Main Program*: The displayed digit must be incremented every second, provided that **E** was pressed last (i.e., the process of incrementing the digit is enabled). If **D** was pressed last, the displayed digit is unchanged (i.e., the process of incrementing the digit is disabled). Required 1-second timeouts must be implemented using the 100-MHz Counter/Timer. **Note:** Incrementing **9** gives **0**.
- *ISR*: **Port B** must be configured to generate interrupts whenever **PBIN** is updated. If **D** has been pressed, the digit is not allowed to increment every second (until **E** is pressed). If **E** has been pressed, the digit is allowed to increment every second (until **D** is pressed).

3. [5 points] Table below specifies a set of **3** independent pre-emptive tasks to be executed by a single processor. Show the task schedule using *Earliest Deadline First* (**EDF**) priority assignment. Note that the T3's deadline is 100 (not 120). If needed, break any prioritization ties as you wish.

Task **T_i**	Period **P_i**	WCET **C_i**	Deadline **D_i**	Initial Delay **ϕ_i**
T1	40	10	40	0
T2	60	20	60	0
T3	120	40	100	0