UNIVERISTY OF VICTORIA

CENG 355 MICROPROCESSOR-BASED SYSTEMS

MIDTERM EXAMINATION

25 OCTOBER 2012

NAME:_____ STUDENT NO._____

INSTRUCTOR: D.N.RAKHMATOV DURATION: 80 MINUTES

TO BE ANSWERED IN THE BOOKLET.

STUDENTS MUST COUNT THE NUMBER OF PAGES IN THIS EXAMINATION PAPER, AND REPORT ANY DISCREPANCY IMMEDIATELY TO THE INVIGILATOR.

THIS EXAMINATION PAPER HAS **3** PAGES AND **4** QUESTIONS.

In taking this examination, you agree that all work recorded herein is your own. A student caught in the act of cheating will be given a grade of **F** on this examination.

Show your work.

Read the questions carefully. If something appears ambiguous, write down your assumptions.

You are allowed to use books, notes, and/or calculators during this examination.

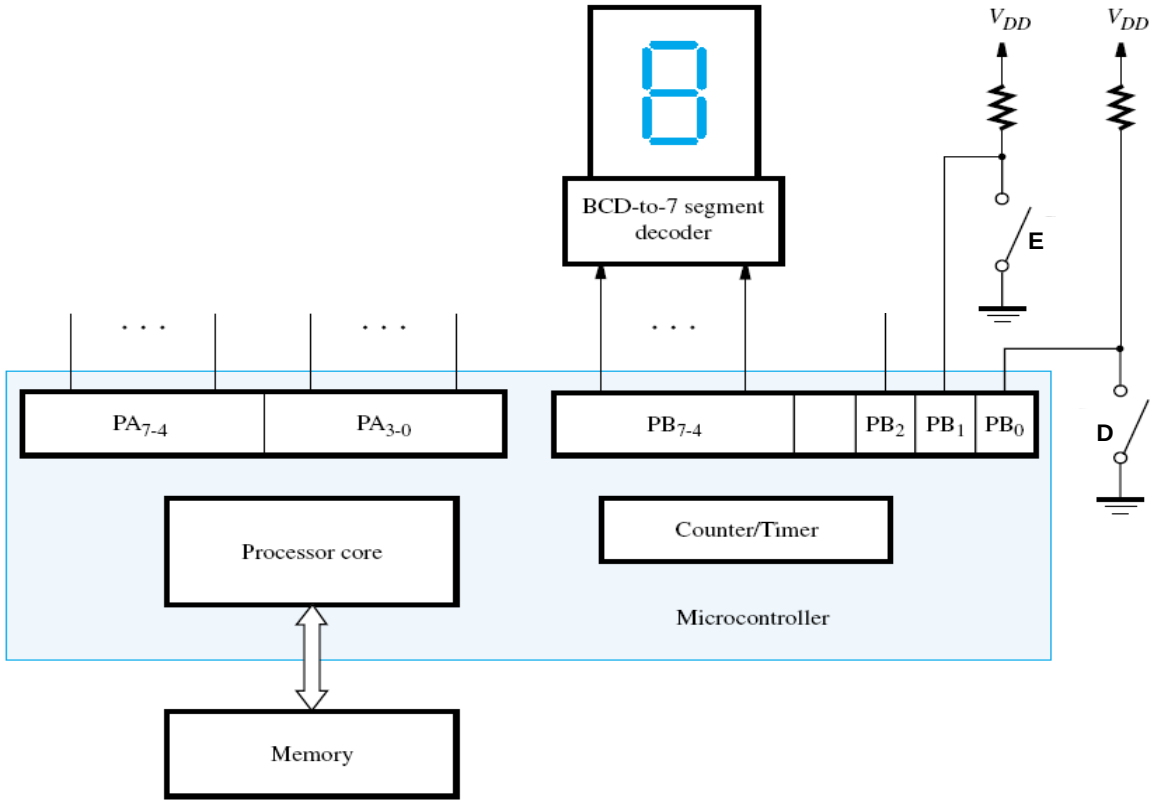
GOOD LUCK!

1. [15 points] The textbook's microcontroller below is responsible for 2 tasks: (1) conditionally incrementing the displayed digit every second, and (2) keeping track of the **E** and **D** switches: pressing **E** enables the process of incrementing the digit every second, while pressing **D** disables that process. Write the corresponding C program, assuming that the first task is the ISR whose address is stored at location **0x20**, and the second task is the main program. Assume that bit **PSR[6]** is the processor's interrupt-enable bit, and **Port B** is always ready to receive data from the processor. Initially, the 7-segment display shows digit **0**, and it is not being incremented.

• *Main Program*: If **D** has been pressed, the digit is not allowed to increment every second (until **E** is pressed). If **E** has been pressed, the digit is allowed to increment every second (until **D** is pressed).

• *ISR*: The 100-MHz Counter/Timer must be configured to generate interrupts every second. The displayed digit must be incremented, provided that **E** was pressed last (i.e., the process of incrementing the digit is enabled). If **D** was pressed last, the displayed digit is unchanged (i.e., the process of incrementing the digit is disabled).

Note: Incrementing **9** gives **0**.



2. [15 points] Assume a computer has 256-byte main memory and 64-byte cache with four blocks, where each block has four 32-bit words. While executing some program, the CPU reads 32-bit words from the following sequence of addresses:

24 8C 10 48 20 24 28 88 1C 40

Show the cache contents (e.g., **[00]** = address **00**'s contents) at the end of this sequence (10 addresses) and calculate the corresponding miss rate given that:

(a) Cache is direct-mapped.

(b) Cache is 2-way set-associative (2 blocks per set) with LRU replacement.

(c) Cache is fully-associative with LRU replacement.

3. [5 points] Some I/O device is active **10%** of the time and has the maximum data transfer rate of $\mathbf{R_{I/O} = 32KB/s}$. Each data transfer is in chunks of $\mathbf{d_{I/O} = 32B}$ when the I/O device is ready. If polling is used, the CPU performs either $\mathbf{A_{poll\text{-}ready} = 400}$ memory accesses per poll (when the device is ready), or $\mathbf{A_{poll\text{-}not\text{-}ready} = 200}$ memory accesses per poll (when the device is not ready). If interrupts are used, the CPU performs $\mathbf{A_{int} = 500}$ memory accesses per interrupt. Assume that the cache hit rate is $\mathbf{h_{poll} = 90\%}$ for polling and $\mathbf{h_{int} = 80\%}$ for interrupts. Assume that the cache access time is $\mathbf{C = 1\tau}$ (cache hit), and the main memory access time is $\mathbf{M = 10\tau}$ (cache miss). By what factor is the interrupt cost cheaper than the polling cost?

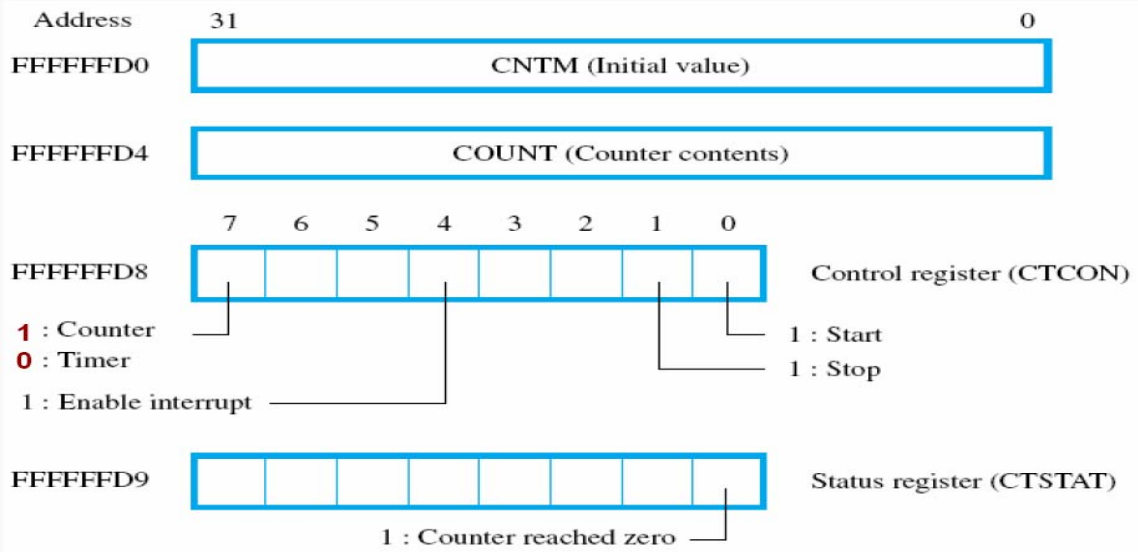
Hint: First, determine $\mathbf{T_{ave\text{-}poll}}$ and $\mathbf{T_{ave\text{-}int}}$ (i.e., the average access times for polling and interrupts), and then multiply by a total number of accesses in each case.

4. [5 points] Table below specifies a set of **3** independent pre-emptive tasks to be executed by a single processor. Show the **RM** (rate-monotonic) task schedule.

Task $\mathbf{T_i}$	Period $\mathbf{P_i}$	WCET $\mathbf{C_i}$	Deadline $\mathbf{D_i}$	Initial Delay $\mathbf{\phi_i}$
T1	40	10	40	0
T2	60	20	60	0
T3	120	30	120	0

END

Counter / Timer Registers



Parallel Port Registers