18 I/O and Peripherals
Part 4: DMA

CSC 230

Stallings: 7.5

M&H: 8.3.3

What about transfers from disk ➔ memory in large blocks?

- Interrupts frees CPU while waiting for general I/O
  - ✓ Yet CPU remains in charge of ALL I/O transfers

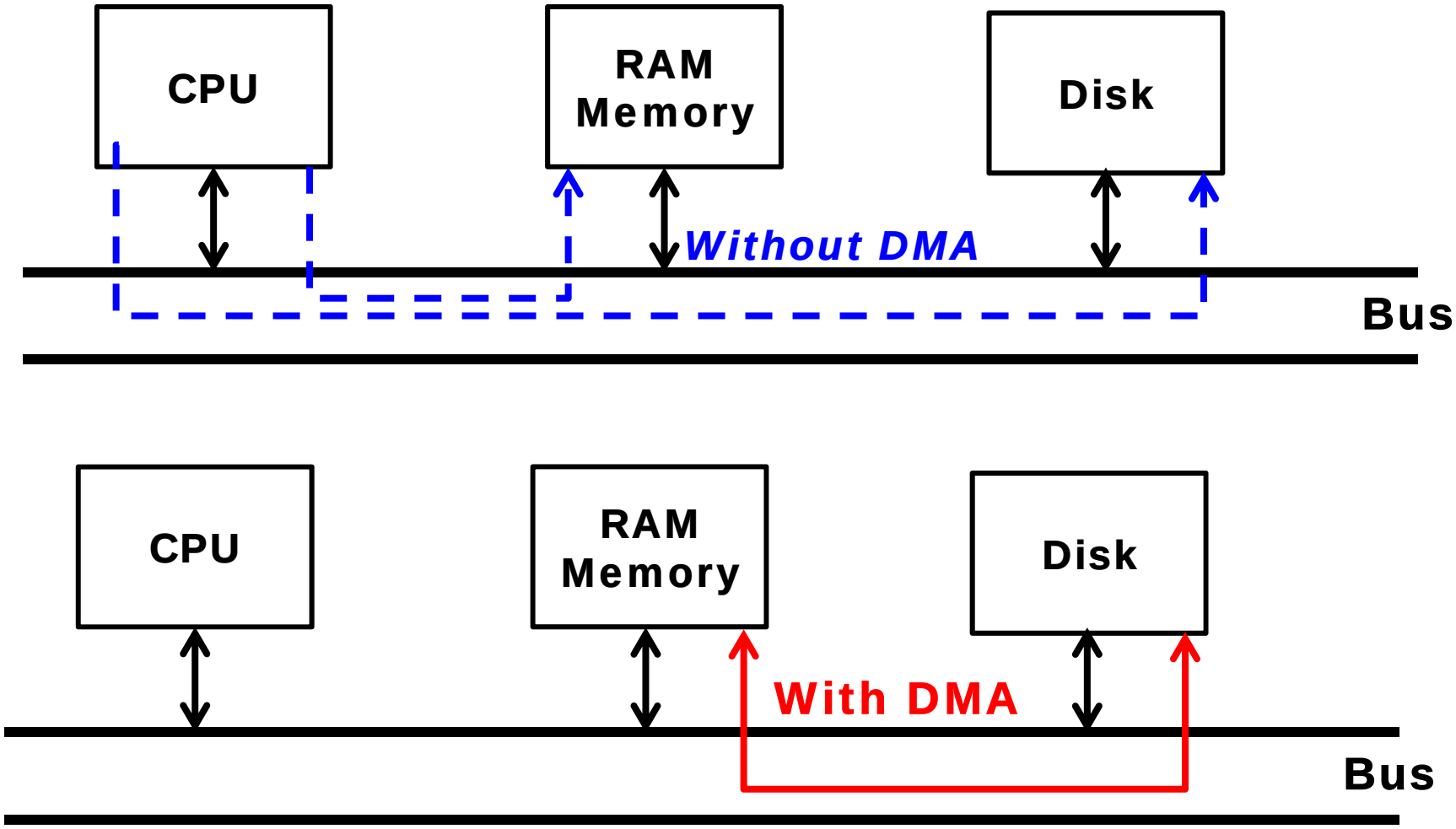
- Is there a better strategy for large transfers of data?

DMA = Direct Memory Access

Bypasses the CPU, after the initial setup by CPU

What is a DMA = Direct Memory Access

DMA Transfer from Disk to Memory Bypasses the CPU (after the initial setup)



DMA process and controls

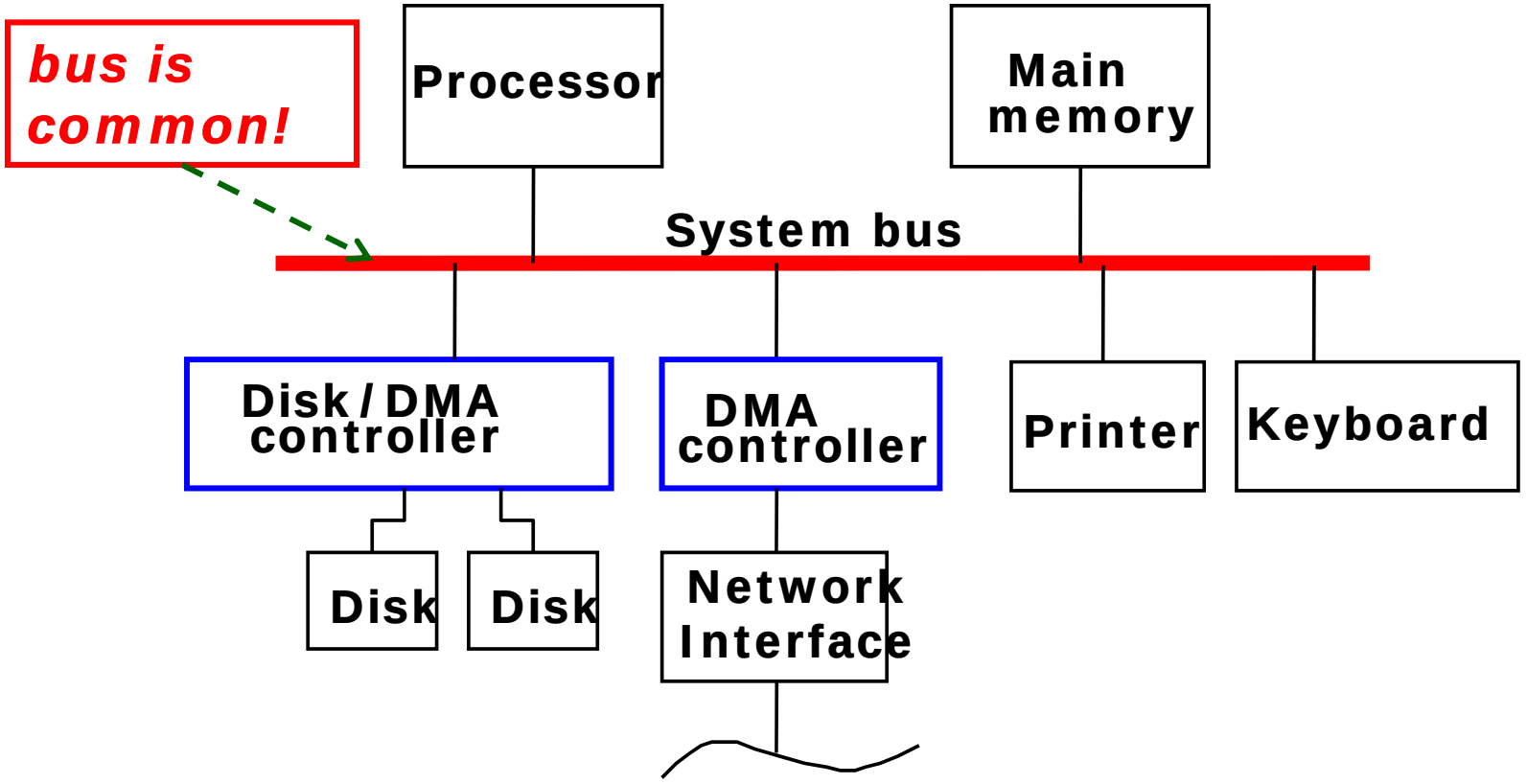
1) **Processor initiates** the data transfer by sending information to the DMA controller:
   a) which I/O device
   b) how many bytes to transfer to which location

2) **DMA controls** the data transfer between the device and memory while the processor is free for other work
   a) There is some form of handshaking between the DMA and the device to coordinate the transfer.
   b) Use of buses by processor and DMA controller may be interleaved
   c) The DMA sends an interrupt signal to the CPU when the data transfer is complete

3) **DMA interrupts** CPU when transfer is complete

The DMA device is really a simple special purpose processor

DMA Protocol Issue 1: who uses and controls the bus?



New strategy: cycle stealing, bus mastering

DMA Protocol Issue 2: extra bus, extra hardware?