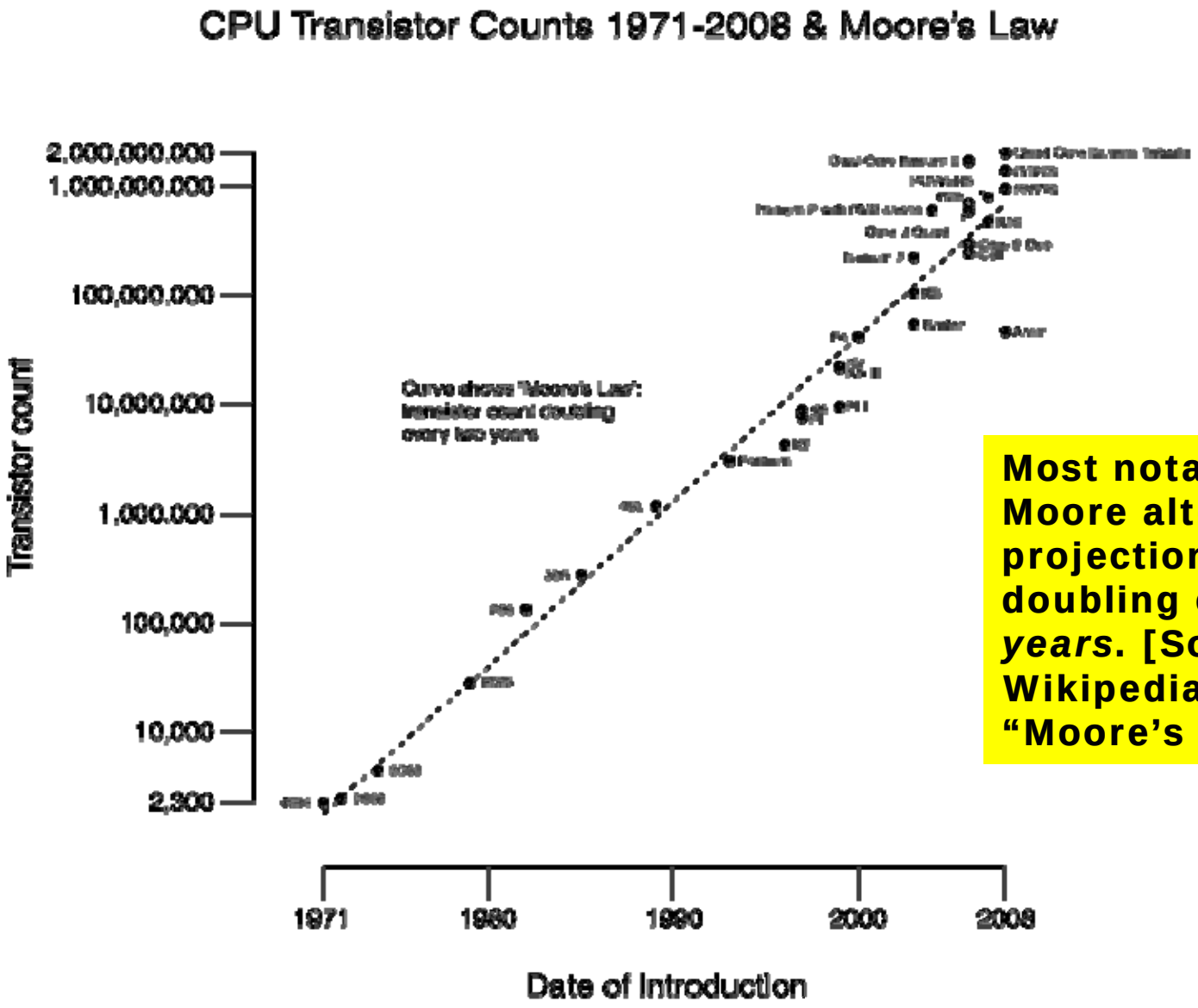
25 Processors
CSC 230

Department of Computer Science
University of Victoria



Most notably, 1975, Moore altered his projection to a doubling every *two years*. [Source: Wikipedia entry for "Moore's Law".]

Source: Wikipedia entry for "Transistor count"

INTEL ARCHITECTURE

[1969]

4004 ⇒ 8080 ⇒ 8085

IA really starts with the 8086 ⇒ 8088

[1971] 4004

4 bit registers - 4 bit external data bus - 12 bit addressing - 740kHz

[1974] 8080

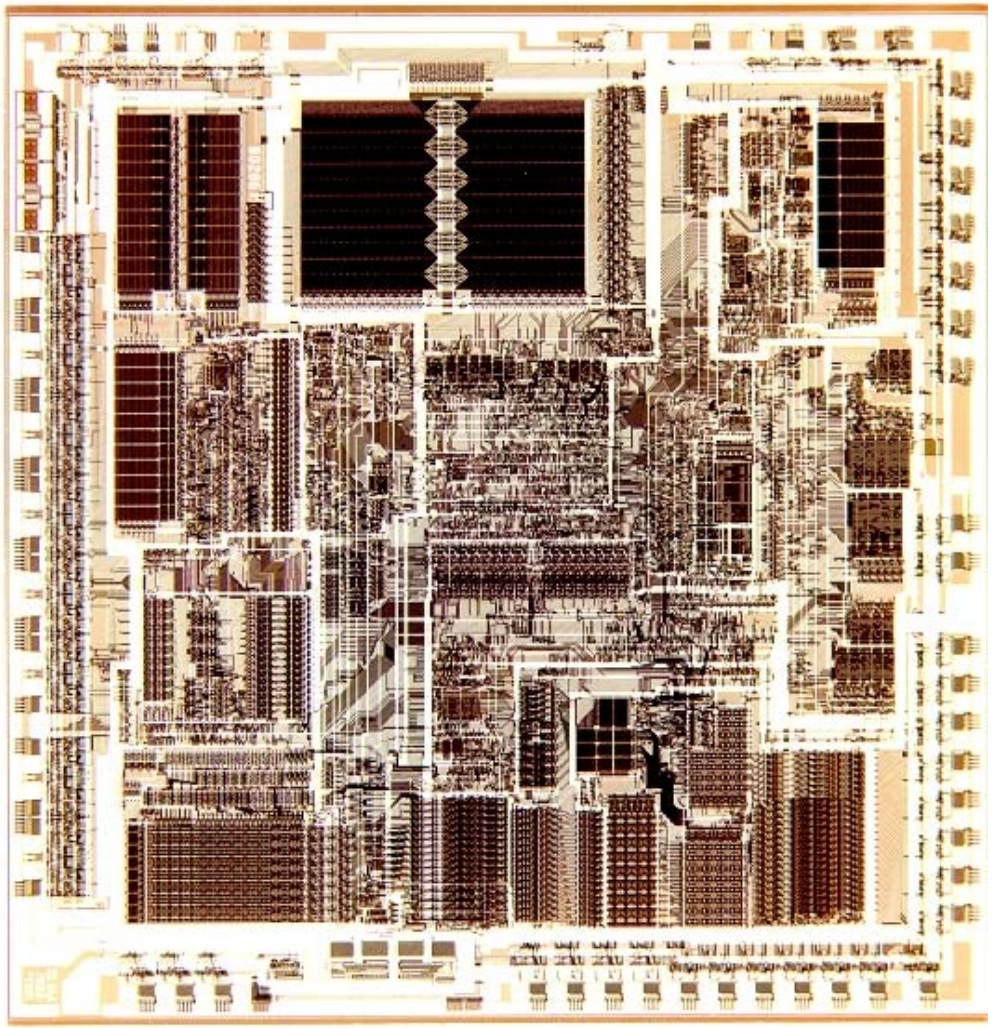
8 bit registers - 8 bit external data bus - 16 bit addressing - 2MHz

[1978] 8086

16 bit registers - 16 bit ext. data bus - 20 bit addressing - 4.77MHz to 10MHz

➔Programs from 1978 still execute on the latest members of the IA family

➔ downward compatibility



INTEL 80286 – 1982

- 32 bit registers for computation and addressing
- MMU added, giving paging with a fixed 4K page➔VM
- 6 parallel 'stages':
  - bus interface unit
  - code prefetch unit
  - instruction decode unit
  - execution unit
  - segment unit
  - paging unit

1.5µm silicon gate CMOS
1 polysilicon layer and 2 metal layers

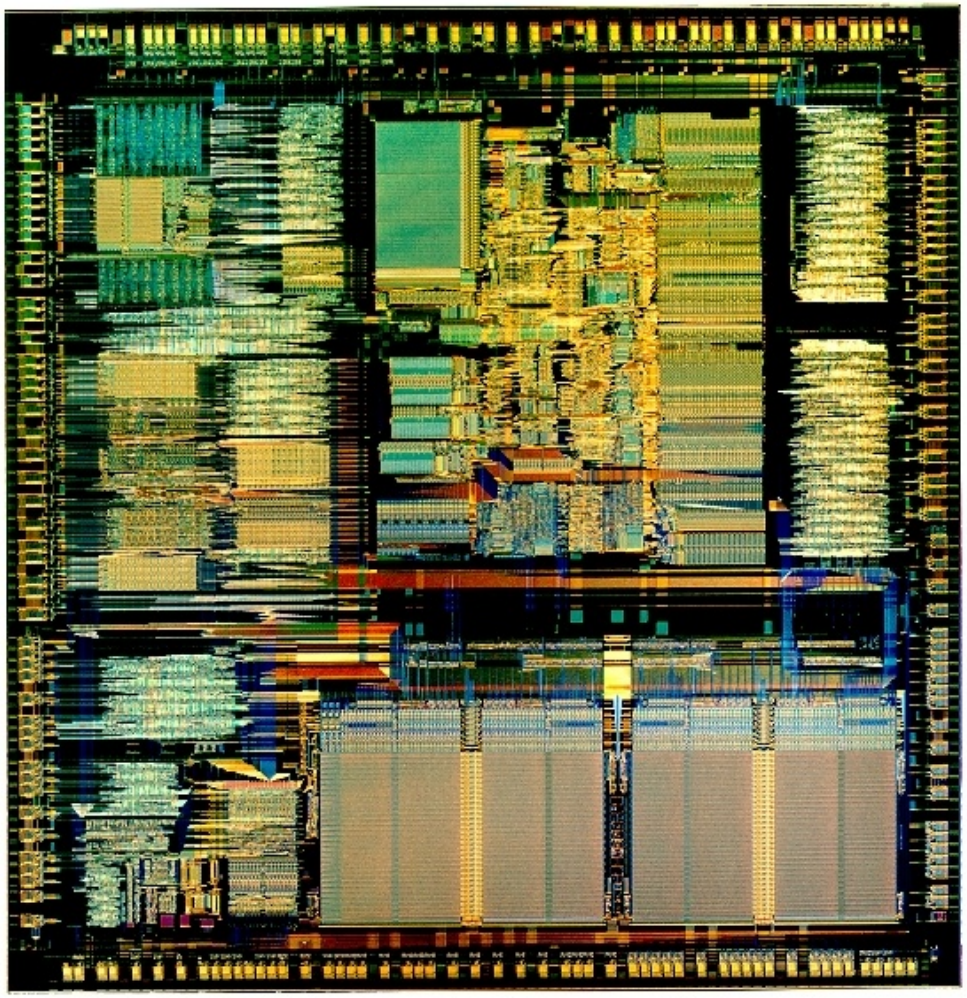
134,000 transistors
6 to 12 MHz clock speed

68.7mm² die size

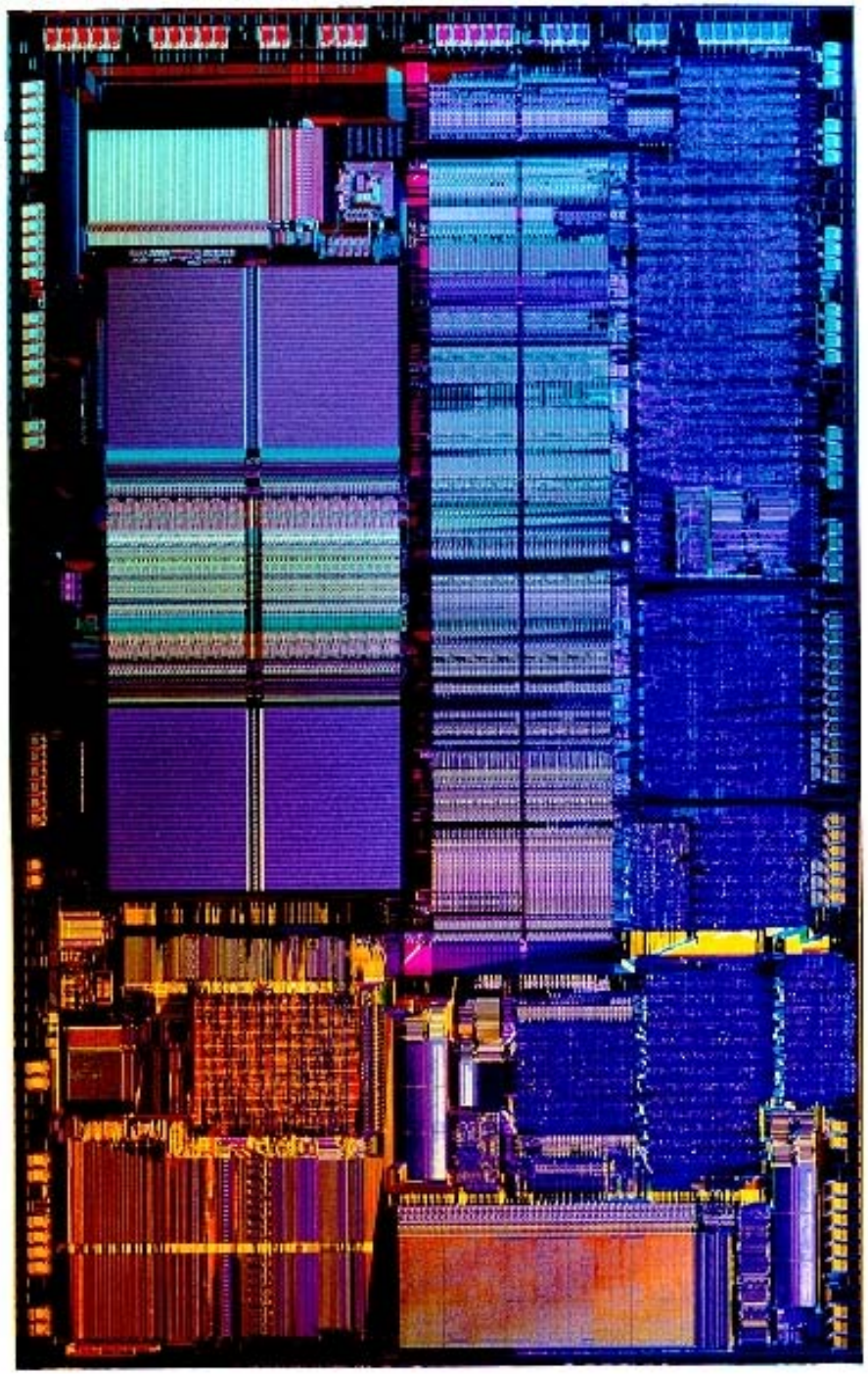
INTEL 80386 DX - 1985

first 32 bit processor

- 5 pipelined stages
  - each stage can work on one instruction per clock cycle
- 8K on-chip L1 cache was added
- Instructions were added to provide L2 (off-chip) cache support and multiprocessing



1.5µm silicon gate CMOS
10 mask layers
275,000 transistors
16 to 33MHz clock
104mm2 die size

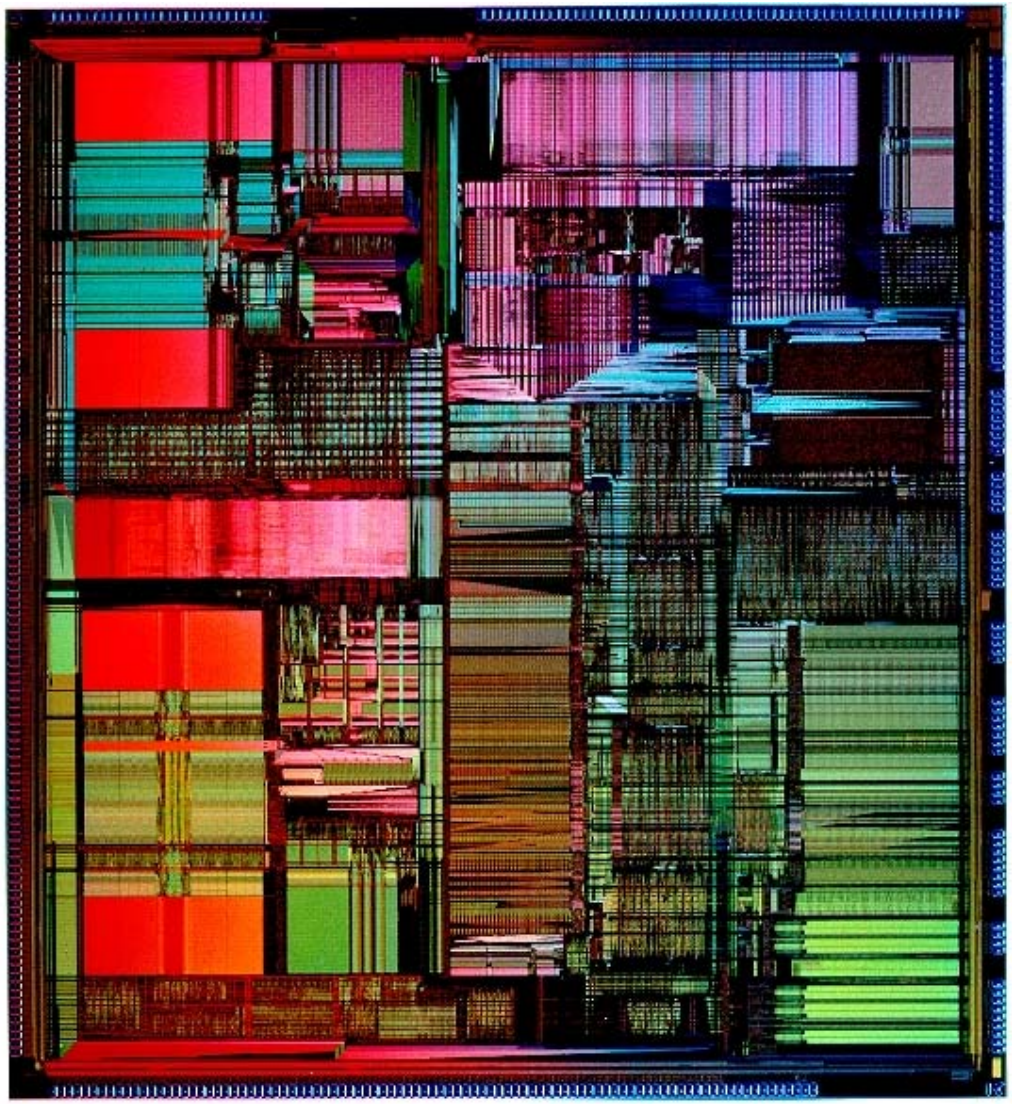


INTEL 80486 - 1989

first on-chip FP unit

1.0µm silicon gate CMOS
12 mask layers

1.2 million transistors
25 to 50MHz clock
163mm² die size



INTEL PENTIUM – 1993

0.8µm silicon gate BiCMOS
18 mask layers
3.1 million transistors
60 to 66 MHz clock
264mm² die size

- **second execution pipeline for superscalar performance**
- **8K L1 I-cache and 8K L1 D-cache**
- **Branch prediction hardware**
- **32 bit registers, but 128 and 256 bit internal data paths, external data bus is 64 bits**
- **two processor support**

Main Pentium Features

Multiple Branch Prediction:

- Predicts flow of the program through several branches.
- 90% or greater accuracy for finding next instruction.

Data Flow Analysis:

- Analyzes and schedules instructions to be executed in an optimal sequence, independent of the original program order.

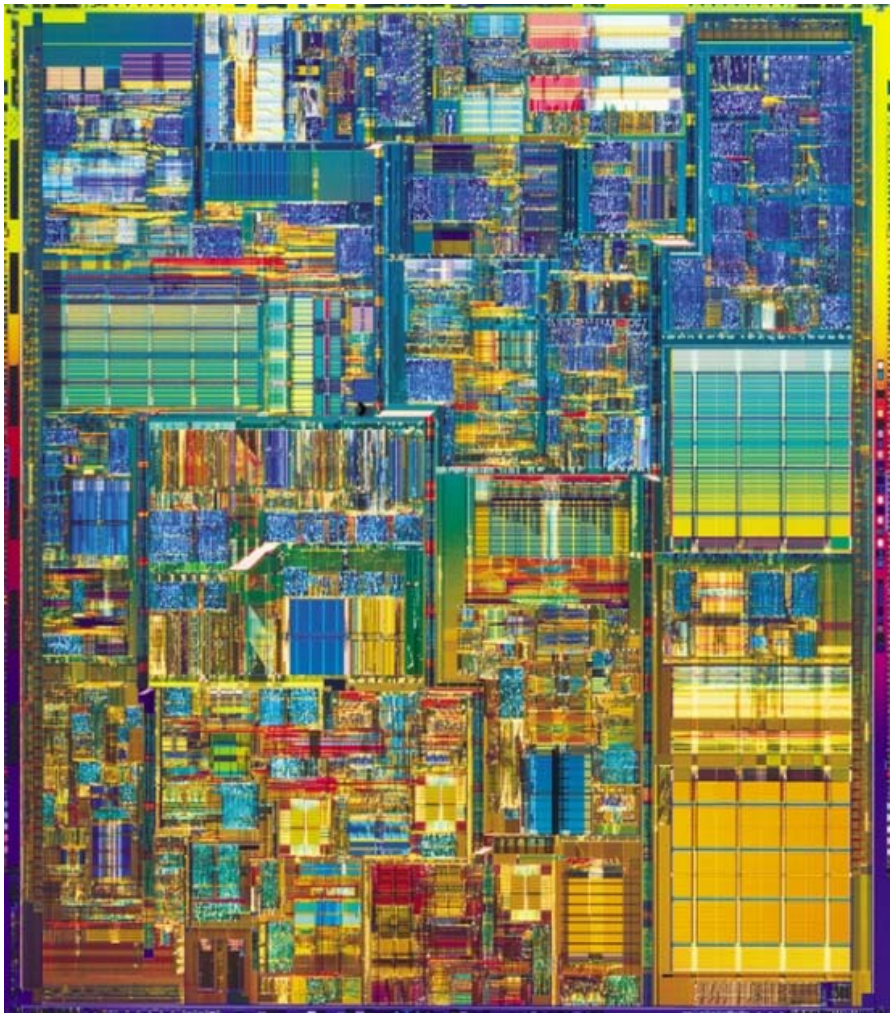
Speculative Execution:

- Looks ahead of the program counter and executes instructions that are likely to be needed.
- The processor executes up to five instructions at a time.

MMX technology:

- It improves video compression / decompression, image manipulation, encryption and I/O processing.
- MMX is an extra set of instructions to support SIMD operations.

See later....



INTEL PENTIUM 4 – 2000

- 0.18µm silicon gate CMOS
- 21 mask layers
- 1 polysilicon layer and
- 6 metal layers
- 224mm² die size

42 million transistors
1.4 to 1.5 GHz clock

Pentium 4 – 2000

CPU Speed 1.30 - 2.20 GHz

Intel® NetBurst™ Micro-architecture

The NetBurst™ micro-architecture delivers a number of new features including (Hyper Pipelined Technology, 400 MHz System Bus, Execution Trace Cache, and Rapid Execution Engine) as well as a number of enhanced features (Advanced Transfer Cache, Advanced Dynamic Execution, Enhanced Floating-point and Multi-media Unit, and Streaming SIMD Extensions 2 (SSE2)).

Hyper Pipelined Technology

Hyper-pipelined technology doubles the pipeline depth compared to the P6 micro-architecture used on Pentium® III processors. One of the key pipelines, the branch prediction / recovery pipeline, is implemented in 20 stages in the NetBurst™ micro-architecture, compared to 10 stages in the P6 micro-architecture.

400 MHz System Bus

The Intel® Pentium® 4 processor supports Intel's highest performance desktop system bus by delivering 3.2 GB of data per second into and out of the processor. This is accomplished through a physical signaling scheme of quad pumping the data transfers over a 100-MHz clocked system bus and a buffering scheme allowing for sustained 400-MHz data transfers. This compares to 1.06 GB/s delivered on the Pentium® III processor's 133-MHz system bus.

Level 1 Execution Trace Cache

In addition to the 8 KB data cache, the Pentium® 4 processor includes an Execution Trace Cache that stores up to 12 K decoded micro-ops in the order of program execution. This increases performance by removing the decoder from the main execution loop and makes more efficient usage of the cache storage space since instructions that are branched around are not stored. The result is a means to deliver a high volume of instructions to the processor's execution units and a reduction in the overall time required to recover from branches that have been mis-predicted.

Rapid Execution Engine

Two Arithmetic Logic Units (ALUs) on the Intel® Pentium® 4 processor are clocked at twice the core processor frequency. This allows basic integer instructions such as Add, Subtract, Logical AND, Logical OR, etc. to execute in ½ a clock cycle. For example, the Rapid Execution Engine on a 2.20 GHz Pentium® 4 processor runs at 4.4 GHz.

512KB or 256 KB, Level 2 Advanced Transfer Cache

Features of the ATC include:

- Non-Blocking, full speed, on-die level 2 cache
- 8-way set associative
- 256-bit data bus to the level 2 cache
- Data clocked into and out of the cache every clock cycle

Advanced Dynamic Execution

The Advance Dynamic Execution engine is a very deep, out-of-order speculative execution engine that keeps the execution units executing instructions. The Pentium 4 processor can also view 126 instructions in flight and handle up to 48 loads and 24 stores in the pipeline. It also includes an enhanced branch prediction algorithm that has the net effect of reducing the number of branch mis-predictions by about 33% over the P6 generation processor's branch prediction capability. It does this by implementing a 4 KB branch target buffer that stores more detail on the history of past branches, as well as more advanced branch prediction.

Enhanced Floating-point and Multi-media Unit

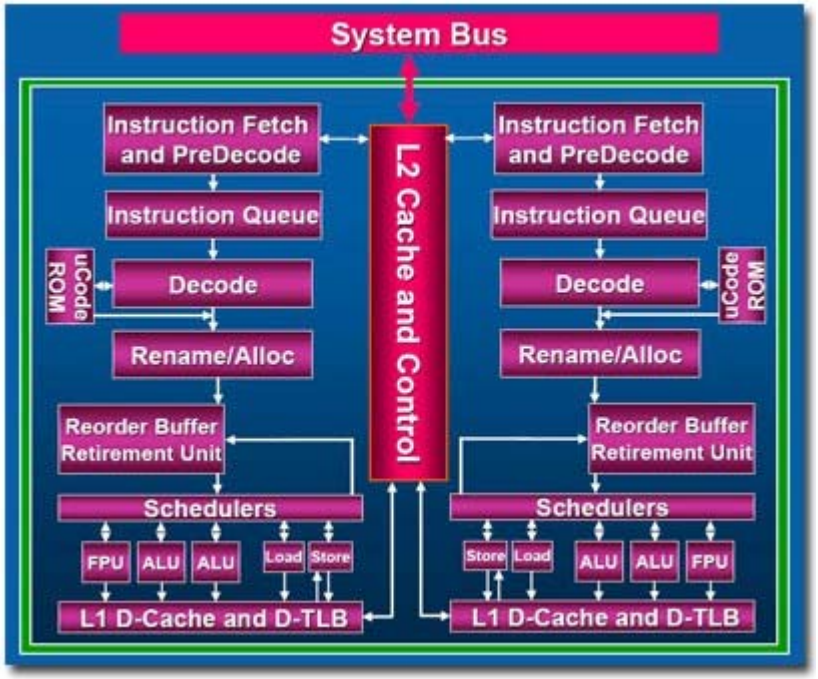
The Intel® Pentium® 4 processor expands the floating-point registers to a full 128-bit and adds an additional register for data movement which improves performance on both floating-point and multi-media applications.

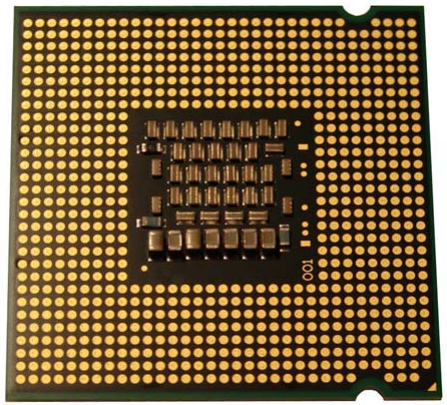
Internet Streaming SIMD Extensions 2 (SSE2)

With the introduction of SSE2, the NetBurst™ micro-architecture now extends the SIMD capabilities that MMX technology and SSE technology delivered by adding 144 new instructions. These instructions include 128-bit SIMD integer arithmetic and 128-bit SIMD double-precision floating-point operations. These new instructions reduce the overall number of instructions required to execute a particular program task and as a result can contribute to an overall performance increase.

Data Prefetch Logic

Functionality that anticipates the data needed by an application and pre-loads it into the Advanced Transfer Cache, further increasing processor and application performance.





Intel Core 2 Duo
E6750

INTEL CORE 2 DUO – 2006 to present

- 0.045µm and 0.065µm
- Two processors share up to 6MB L2 cache
- 64bit architecture
- Low power: 35 watts for notebook versions

291,000,000 transistors
2.33 to 3.33 GHz clock

CPU-Z

www.cpuid.com

CPU-Z set of utilities

➔ **Tells you everything you wish to know about the internals of your system**

INTEL CORE 2 QUAD (Q9000 series) – 2008

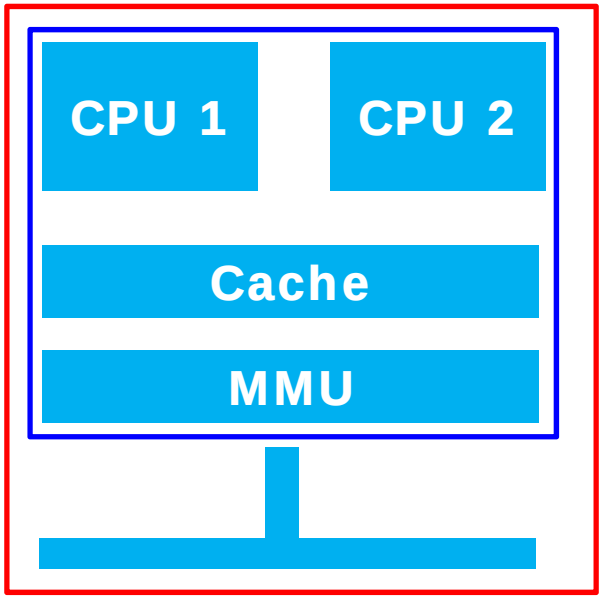
- 0.045µm
- Two 6MB L2 caches
- 105 watts with clock at 2.4GHz

  582,000,000 transistors

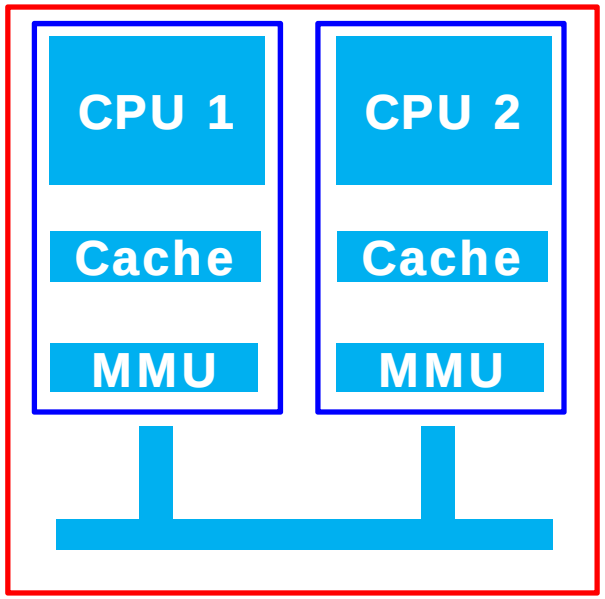
  2.33 to 3.0 GHz clock

Multicore Computers

- Two or more cores (CPUs) as a single integrated circuit.
- May have independent or shared on-board caches.
- Each core independently implements optimizations such as superscalar execution and pipelining.
- Number of cores is 2 for Intel Duo, 4 for Intel Core 2 Quad, 8 for PS3, … 32 for Intel Larrabee.



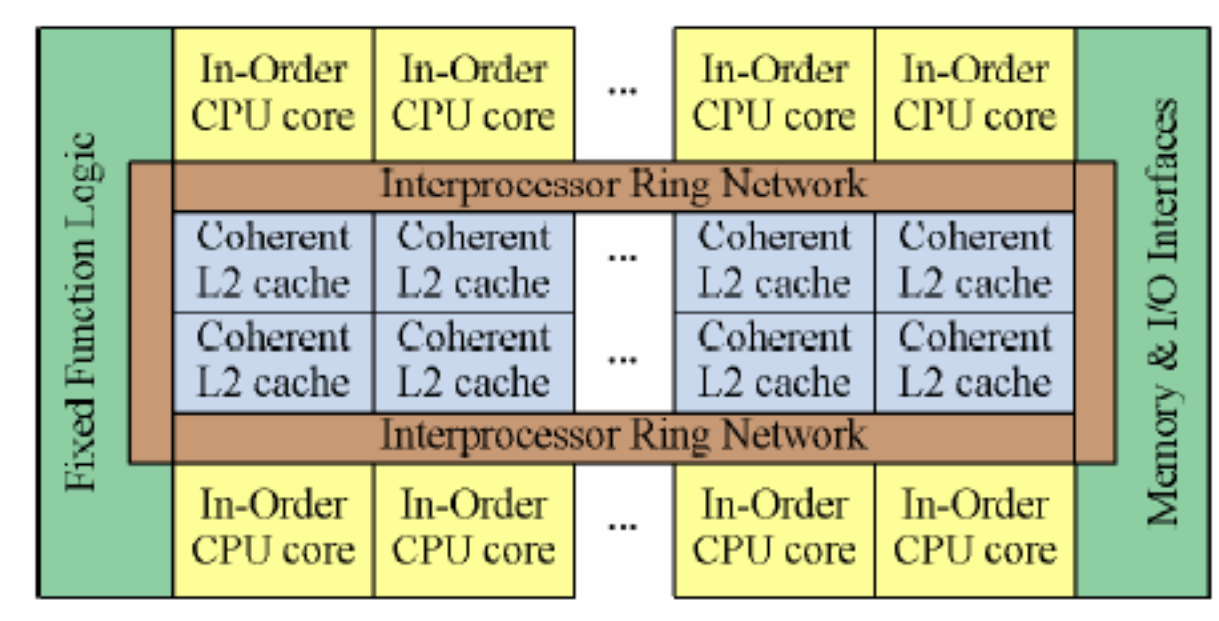
Multicore Design



Multiprocessor Design

Intel Larrabee

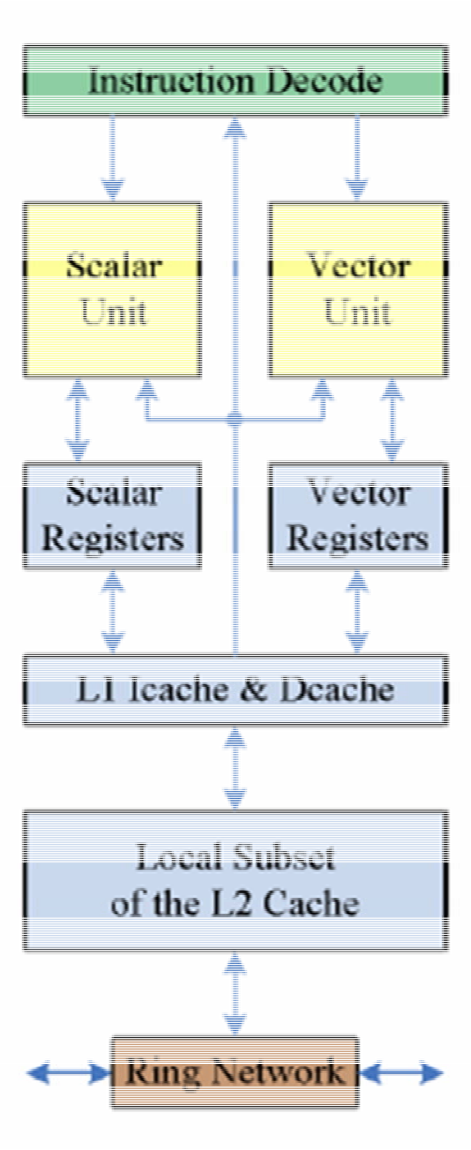
[Source: August 2008 issue of ACM Transactions on Graphics]



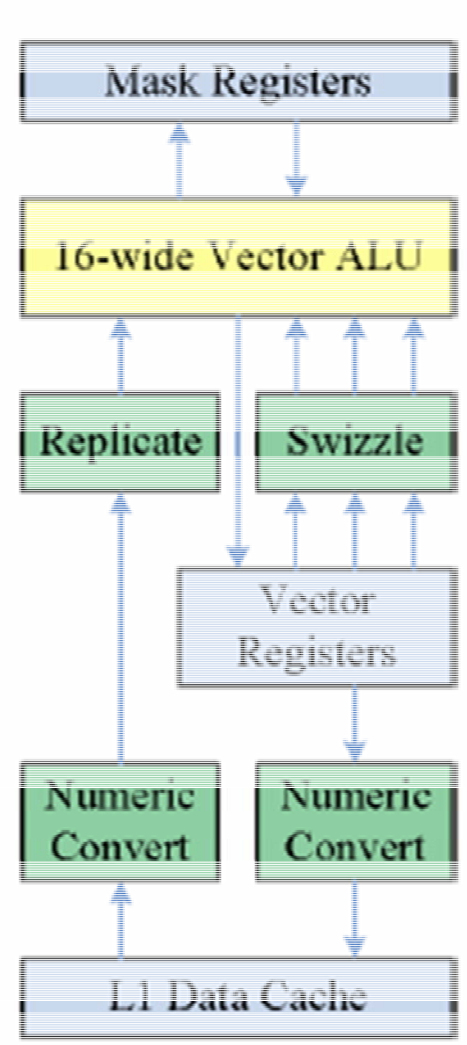
Each CPU core owns part of the L2 cache

- **Multicore – 32 cores?**
- **Intended for graphics processing**
- **Each core is a x86 CPU with extra instructions**
- **In-order instruction execution**

Intel Larrabee



CPU core with associated system blocks



Vector Processing Unit

Crusoe Processors

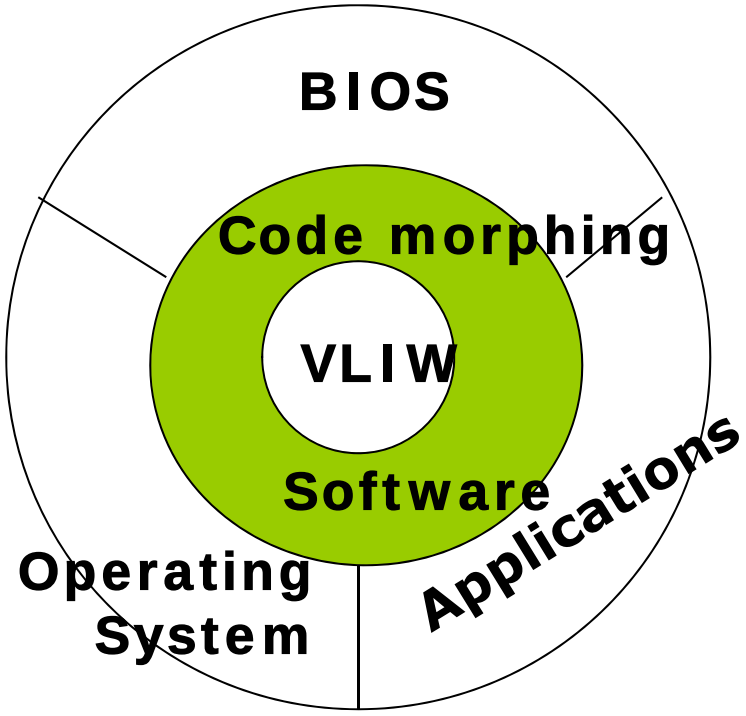
Introduced in January 2000 by Transmeta Corporation, the Crusoe processors are a family of X86 compatible processors with good performance and very low power consumption.

The power saving is achieved by replacing complex hardware operations with a software layer.

VLIW Engine

VLIW - very long instruction word

VLIW engine has two integer units, a floating point unit, a memory (load/store) unit and a branch unit.



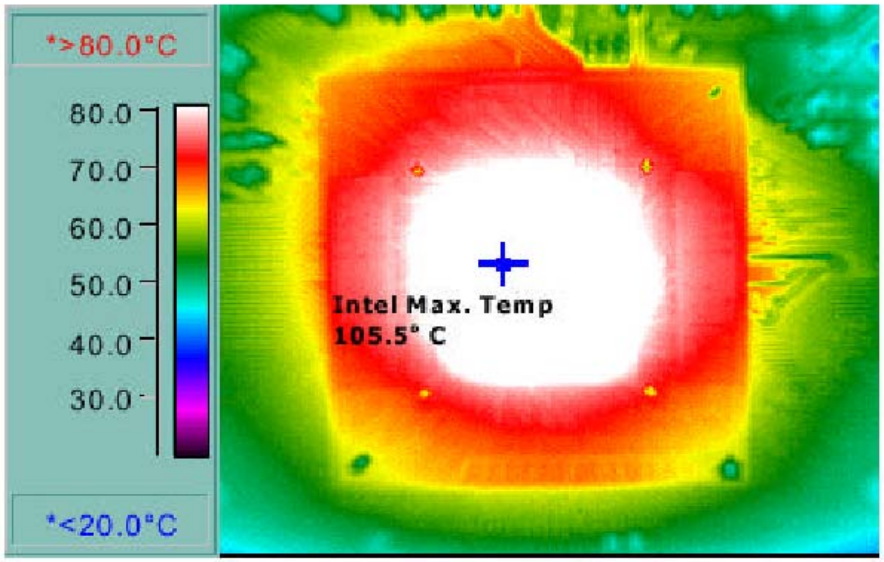


Figure 3. A Pentium III processor plays a DVD at 105° C (221° F).

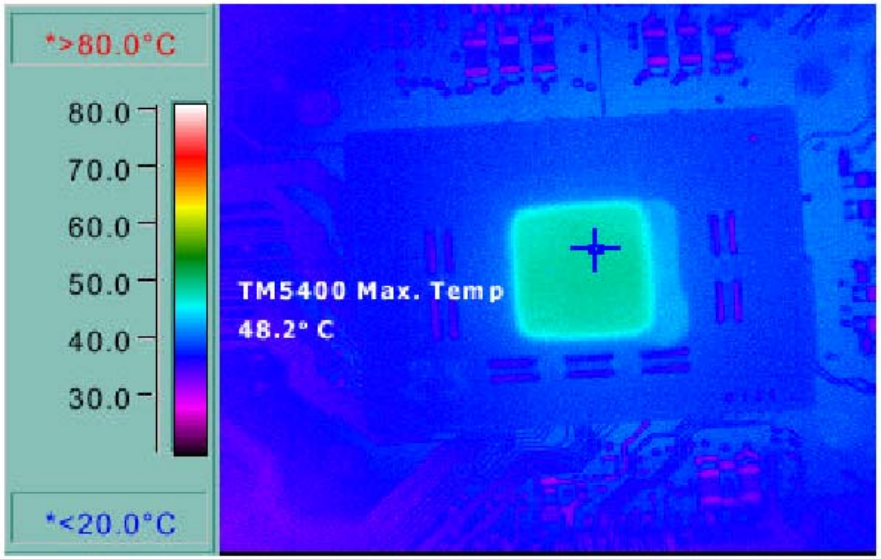


Figure 4. A Crusoe processor model TM5400 plays a DVD at 48° C (118° F).

Unfortunately, Transmeta no longer manufactures microprocessors!