Final Exam Study Questions

The questions on the final exam are based on all the material covered in class lectures and the textbook.

In addition to understanding the material, to prepare for final exam questions it is suggested to review all the assignment questions, quizzes and the midterm exam.

Below you will find some additional questions that will help you practice for the final exam.

Good luck!

---

1. Describe the following:
   - Instruction register (IR)
   - Program counter (PC)
   - Memory Address Register (MAR)
   - Memory Data Register (MDR)
   - Elapsed time
   - Processor time
   - Memory mapped I/O
   - I/O mapped I/O
   - Program controlled I/O
   - Interrupt driven I/O
   - Direct Memory Access (DMA)
   - Interrupt Service Routine (ISR)
   - Interrupt vector
   - Interrupt Daisy Chain
   - Exception
   - Internal trap
   - Memory access time
   - Memory cycle time
   - Memory latency
   - Random Access Memory (RAM)
   - Read Only Memory (ROM)
   - Cache
   - Virtual memory
   - Temporal locality of reference
   - Spatial locality of reference
   - Cache hit
   - Cache miss
   - Write through
   - Write back
   - Cache coherence
   - Least Recently Used (LRU) replacement
   - Cache hit rate
   - Page fault

2. Compare the following:
   - CISC vs. RISC
   - Memory mapped vs I/O mapped I/O
   - Static vs. dynamic RAM
   - Temporal vs. spatial locality of reference
   - Write through vs. write back

3. The stack of one implementation grows from a low address to a high address, and the current stack pointer is pointing to a valid item on the top of the stack. When an item is to be popped from the stack, should we pre-decrement, pre-increment, post-decrement, or post-increment the stack pointer? Explain.

4. A queue (Q) is a First-In-First-Out data structure. A new item is added to the back of the Q pointed to by the ↑Back pointer. An item is removed from the front of the Q pointed to by the ↑Front pointer. Why is it necessary to implement a Q as a circular buffer in practice?

5. In an asynchronous data transfer scheme, a slave needs to assert (i.e., make active/true) the 'slave-ready' signal in the process. Assuming the data transfer initiator/master is the processor, and the responder/slave is the memory module:
   (a) What does an asserted 'slave-ready' signal indicate in a memory read cycle?
   (b) What does an asserted 'slave-ready' signal indicate in a memory write cycle?

6. In the Direct-Mapped placement scheme, each block of the main memory can only be placed in one designated block location in the cache, while in the Associative-Mapped scheme a block from the main memory can be placed in any one of the block locations in the cache. In the Set-Associative mapping, all the blocks in the cache are configured into X sets with Y slots (or blocks) in each set. A main memory block must be placed in a designated set though it can be put in any one of the Y slots of that set. This last placement scheme combines the advantages of both Direct-Mapped and Associative-Mapped schemes.

   Comment on the consequence of setting X=1 in the Set-Associative scheme.
   Comment on the consequence of setting Y=1 in the Set-Associative scheme.

7. The ALU of a computer system is capable of performing the following operations: addition, shift left, shift right, logical AND, logical OR, test a bit and set the condition code. What will be the command(s) to the ALU if you want to multiply an unsigned integer, X, by 2?

8. ROM technology is expensive but it provides non-volatility (i.e., information stored are retained even without power). Almost every computer system has a small amount of ROM implemented. Why is this necessary?

9. Which update policy (write-back or write-through) is preferred for virtual memory? Why?