Rakhmatov has made it very clear on the website that the midterm will contain 3 questions -- one for each chapter we've covered thus far.

1. I/O Programming in C *(e.g. Q1 and Q2 in Assignment 1 and 2.)*
2. RM/EDF real-time task scheduling *(e.g. Q3 in Assignment 2.)*
3. Waveforms (arbitration and FSM) *(e.g. Q3 and Q4 in Assignment 3.)*

The past midterms that I had uploaded seem to show that in past years, the course covered memory hierarchy before interfacing, so there are many questions about cache and none about waveforms. The assignment, lecture examples, and class material should still give good examples of what to expect, though.

Question type 1 is pretty limited in the things that can be asked. It's mostly the same microcontroller setup with minor modifications in what the program actually does. It makes the most sense to me to **bring snippets of code corresponding to various repeated aspects across the examples we've been given**. *(e.g. Enabling CPU interrupts, Configuring PA/PB as Input/Output, Enabling interrupts in PA/PB/Timer, Setting up/starting/utilising the timer, Various switch/button trigger conditions, etc.)*

This lets us get the set-up out of the way easily and lets us construct a shell for the program before we even write the code for the actual functionality of the program. For me, this was the hardest part of the assignments. The actual main.c/ISR functionality only involved understanding how hex values affect PA/PB/control/status registers when wanting to R/W specific bits, and then first year CSC-level logic.

I'm also bringing completed samples of logic for solved variations of the C code examples. *(e.g. Counting logic, 2 buttons (press) vs. 1 button (hold/release), LED flashing code, Understanding how active high or active low components function, etc.)* but they might not be too useful when trying to work under a time limit. I'd rather learn to understand them well before the test, rather than try to use examples to figure out the exam questions in the heat of the moment.

I see this question being a sort of "build your own program" out of building blocks that have already been confirmed to be correct.

Question type 2 seems really straight-forward with almost no variation. The questions can be completed with an algorithm. **I'm going to bring two completed examples (RM, EDF) with step by step guides to follow. Creating step by step question guides really helps me to personally understand how a question works.** We did these same two types of examples in Monday's class to prepare for the midterm. There aren't really any possible curveballs imo.

Question type 3 is likely going to be very similar to Q4 in Assignment 3, as it's almost identical to the example done in Monday's class to prepare us for the midterm. **I'm going to bring a completed example with step by step instructions.** Some of the things I noted from the review class I'm going to want to make sure I understand are:

- How the question changes when different devices request the bus. This is the only way the question can be modified. This will come from trying different variations in how the problem is described.
- How rising/falling edges for each bit cascade through the rest of the arbitration scheme in order to change other bits. *(i.e. which bit changes trigger changes in other bits.)*
- How notation can dictate active high/active low.
- Which bits, when changed, have a delay of 1d, and which bits have a delay of 2d.

The website also indicates that rather than an arbitration waveform question, it could be an FSM waveform question. ~~This will likely look similar to Q3 in Assignment 3. I missed classes and didn't do Assignment 3 so I'm really lacking in understanding of Mealy/Moore FSM state diagrams, and will need to spend a lot of time going over them. I will update when I figure out what things are relevant to the course.~~ I went through this material, and the results of this can be found here:

https://docs.google.com/document/d/1pSZg50moWXs_hpK8peqE6HSBzZVGqtcHPQW1SBF0uPk/edit

(Scroll down)

Things that I don't think we will be tested on:

- Cache/memory hierarchy.
- Clock cycle arithmetic *(Q3 on Assignment 1)*
- Creating Mealy/Moore FSM state diagrams from a scenario. *(Q1 and Q2 on Assignment 3. Waveforms are explicitly stated to be on the exam, and I don't believe there is enough time to do both a Q1/Q2 type question and a Q3/Q4 type question. Correct me if I'm wrong, though.)*