Computer Science 230: Computer Architecture and Assembly Language

Background: Computer Organization and Systems

Stl: Chapter 1; 2.1 (history – actually quite important to read!); 2.2; (2.3 and 2.4 read); 2.5; part of 3.4

(Optional M&H: Chapter 1; 4.1)

What Exactly are?

Computer architecture:

deals with the *functional* behavior of a computer system as viewed by a programmer

e.g. the size of a data type – 32 bits to an integer

Computer organization:

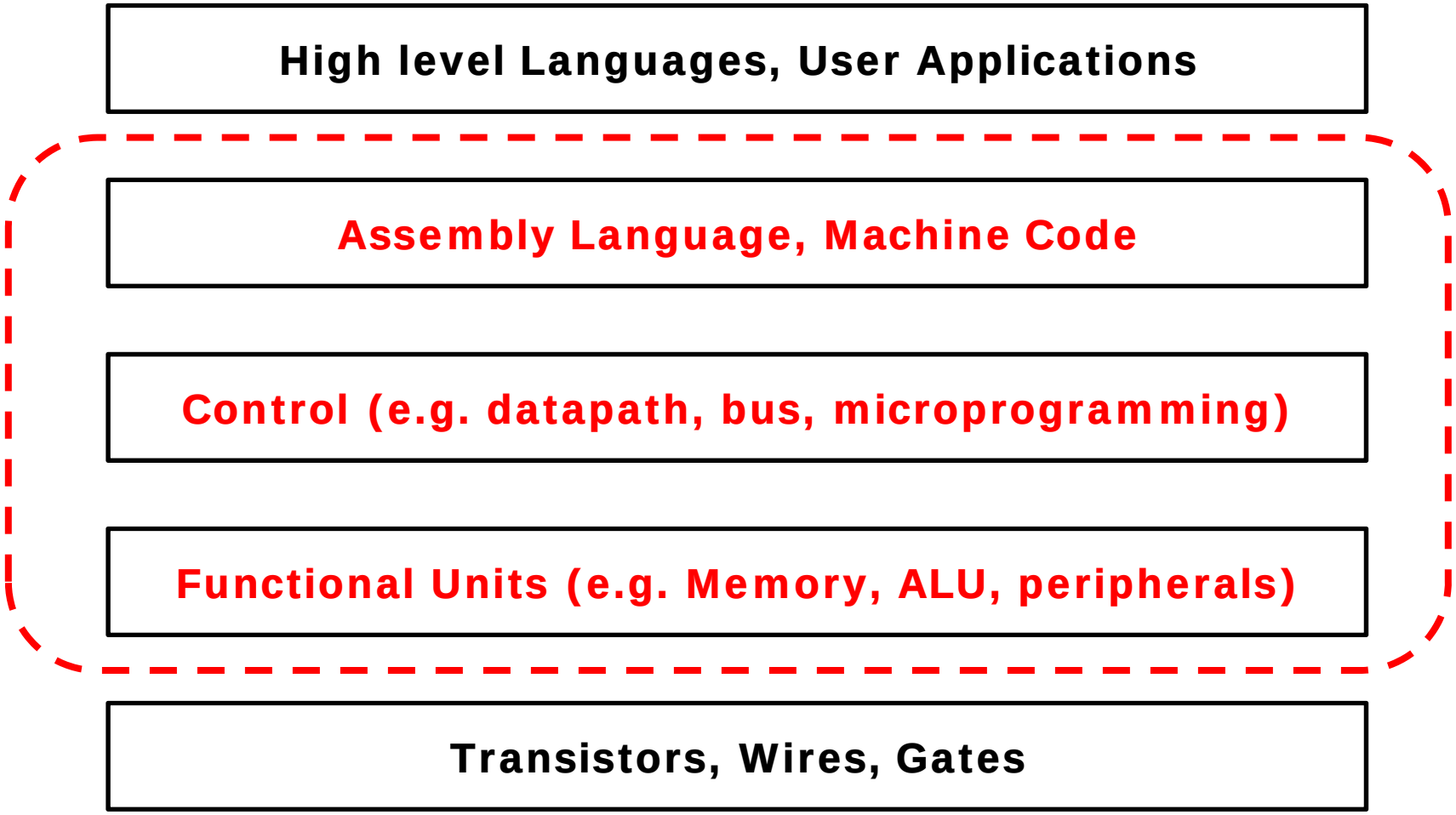
deals with *structural* relationships that are not visible to the programmer

e.g. clock frequency or the size of the physical memory

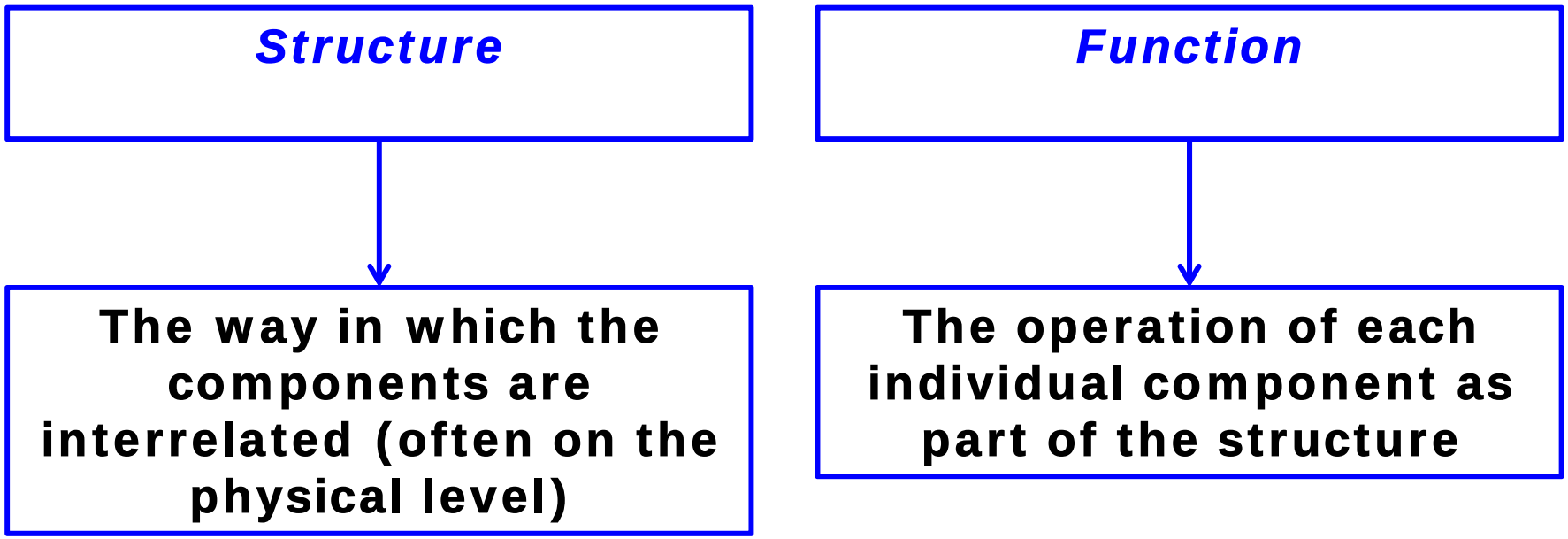
There are Many Levels at which to consider architecture:

highest level ➔ where the user is running programs
lowest level ➔ circuits

Levels of Machine Organization



How do we define?

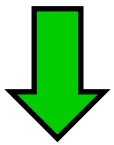


What is a microprocessor?

- 8-bit, 16-bit, 32-bit : refers to number of bits manipulated in one operation (usually the size of the registers).
- It requires external memory to execute programs.
- It cannot directly interface to I/O devices, thus peripheral chips are needed.

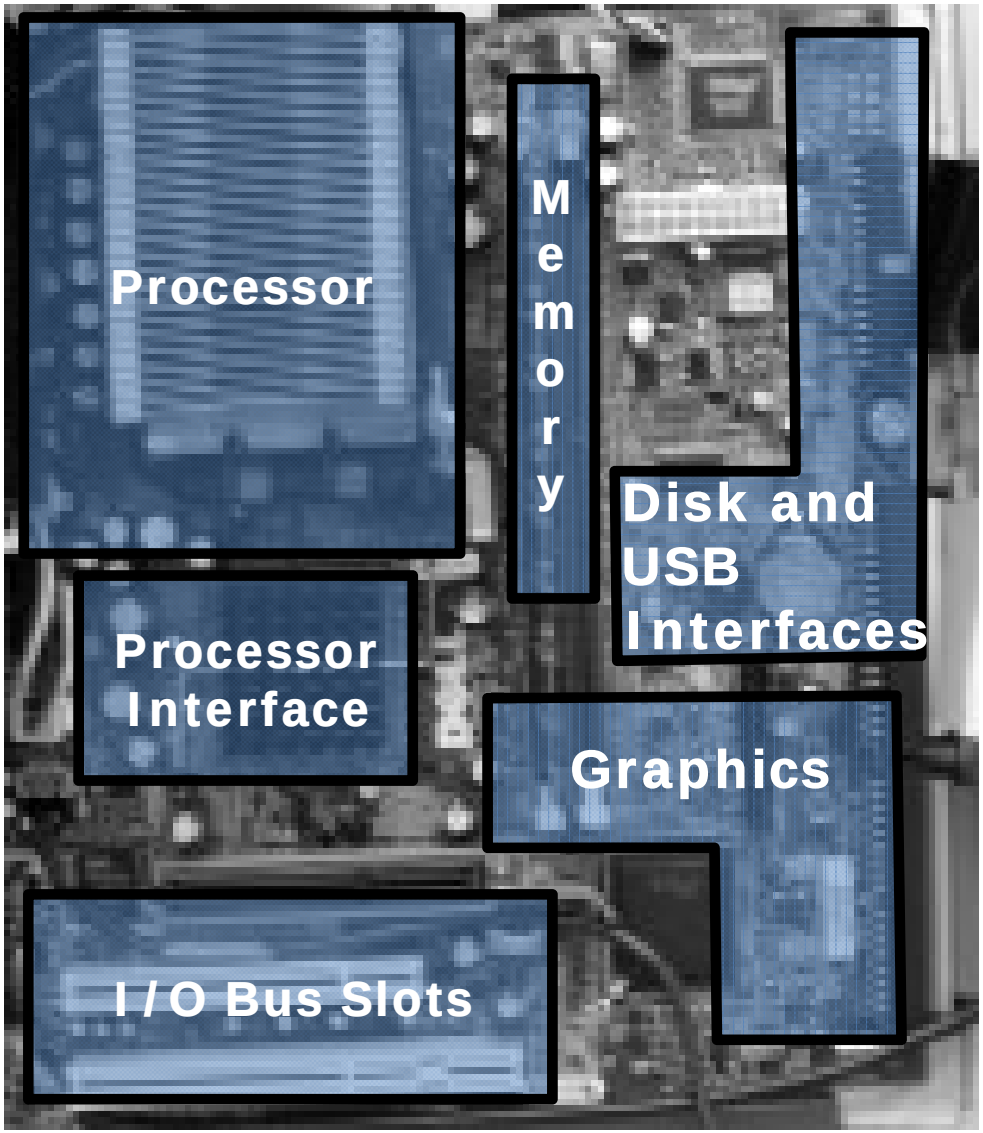
A **processor** is built from a large number of integrated circuits.

A **microprocessor** is a processor packaged as a single IC (Integrated Circuit = chip).



A **microcomputer** is a computer that uses a microprocessor as its CPU.

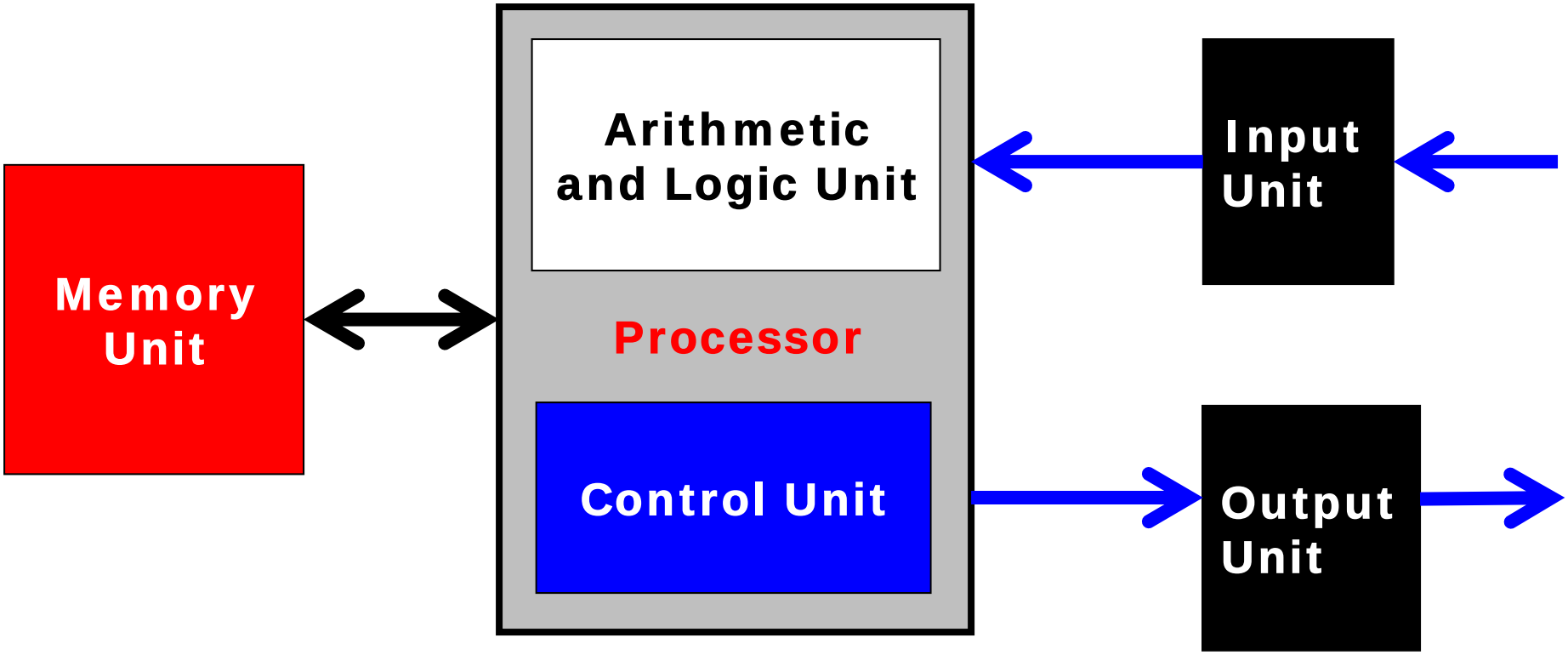
Close-up of a PC motherboard



A Typical Computer System

(Computer case source http://www.baber.com/cases/mpe_md14_silver.htm.
Motherboard source ftp://ftp.tyan.com/img_mobo/i_s2895.tif)

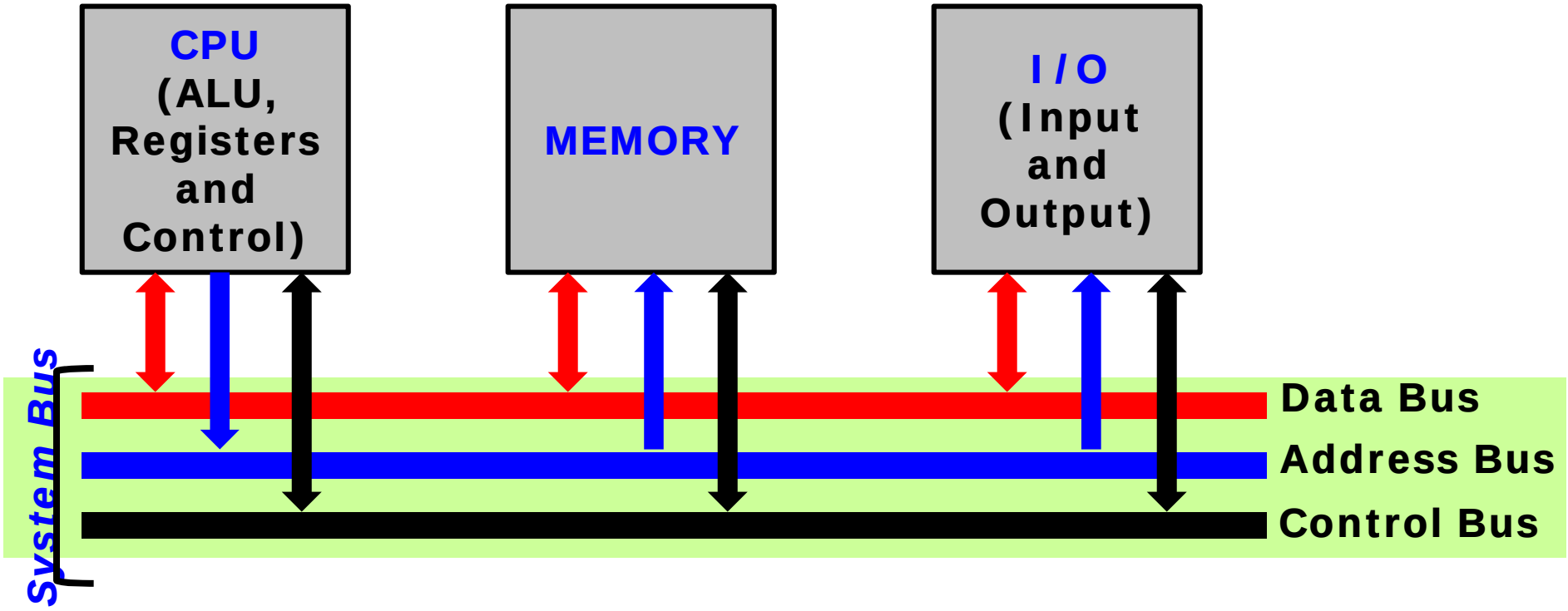
The von Neumann Model



1. Input
2. Output
3. ALU
4. Control Unit
5. Memory unit

The System Bus Model: Refining the von Neumann model

- CPU (ALU and control), memory, and an input/output unit.
- Communication is handled by a shared pathway called the *system bus*,
  - data bus, address bus, and control bus

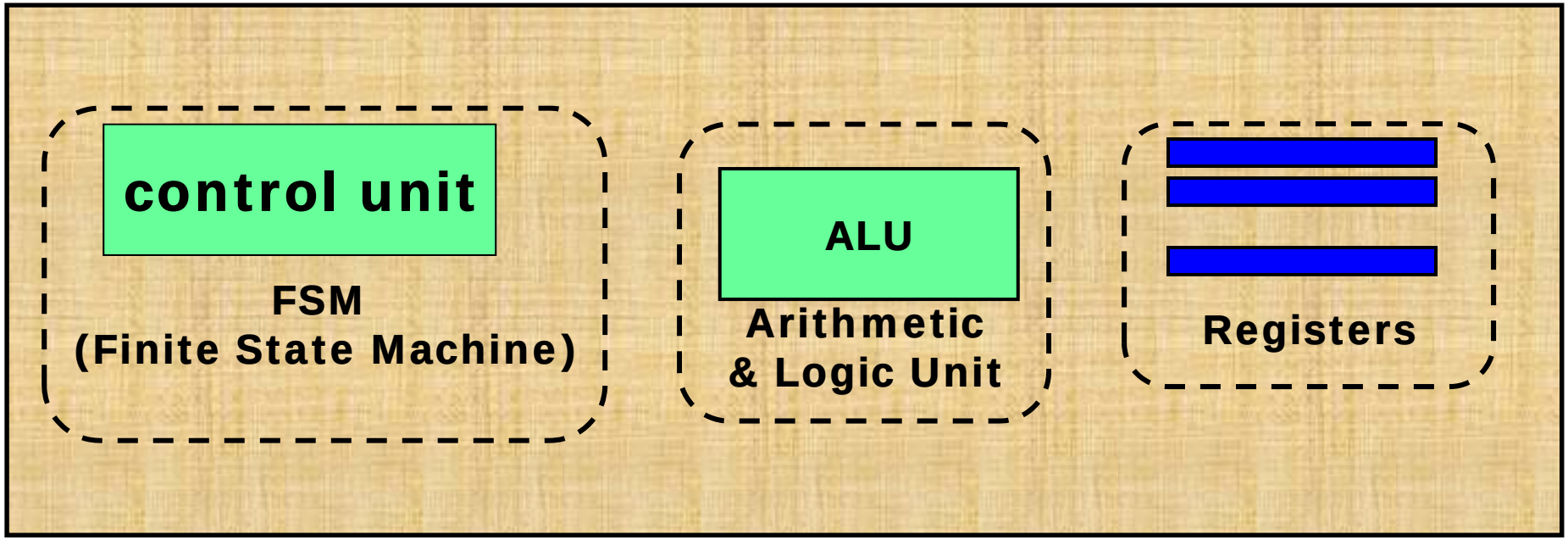


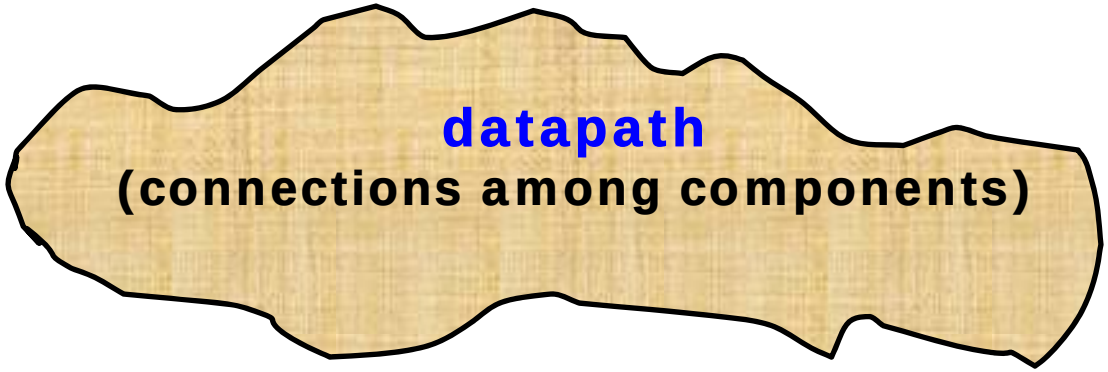
Quick Quiz

- The von Neumann Model consists of the Input Unit, Output Unit, ALU, Control Unit and _____.
- A _____ is a processor packaged as a single IC
- The system bus consists of the ___Bus, _____ Bus and _____Bus.

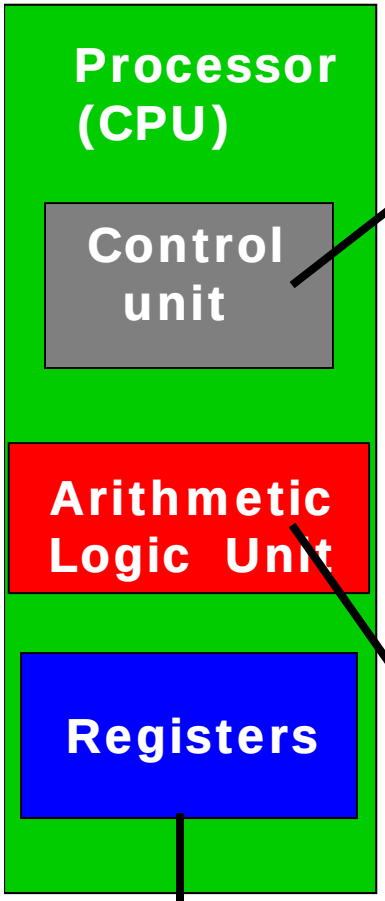
- True or False Functional Units (e.g. Memory, ALU, peripherals) are the lowest level of Machine Organization.
- If you have 32K bytes of byte-addressable memory to address, how many wires does the address bus need?

What's Inside the CPU?





The Processor

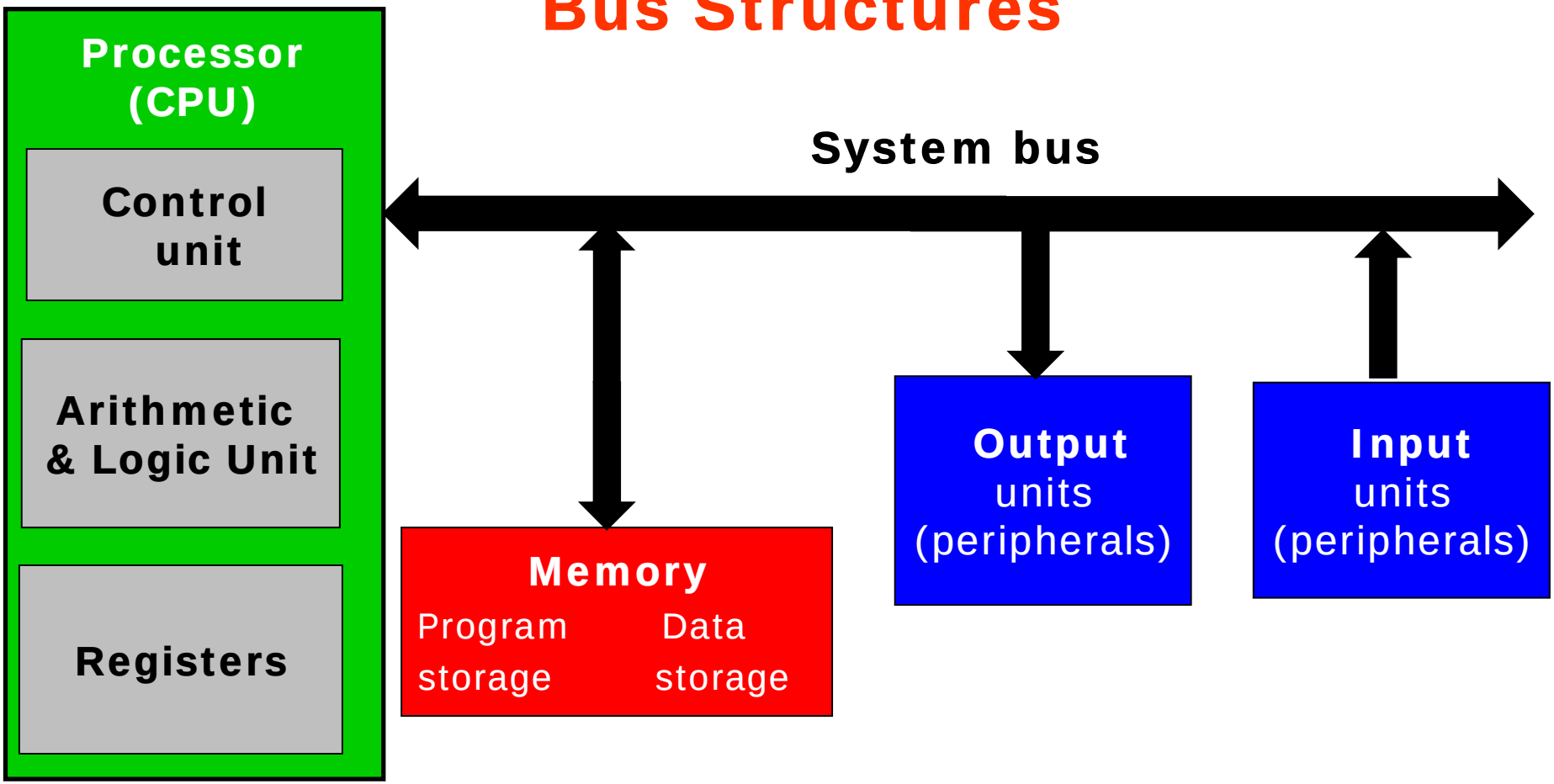


- It contains the hardware instruction logic
- It fetches machine language instructions from memory
- It directs the other units in the execution of those instructions
- It decodes and monitors the execution of instructions
- Activities are synchronized by the system clock and measured in clock cycles (2 GHz = 2000 million ticks, or cycles, per second)
- It uses a set of special purpose (housekeeping) registers:
  - PC = program counter
  - IR = instruction register
  - CCR = Condition Code Register (Status)

Registers hold data and address values. How many? It depends on the CPU design

It performs the arithmetic and logic operations

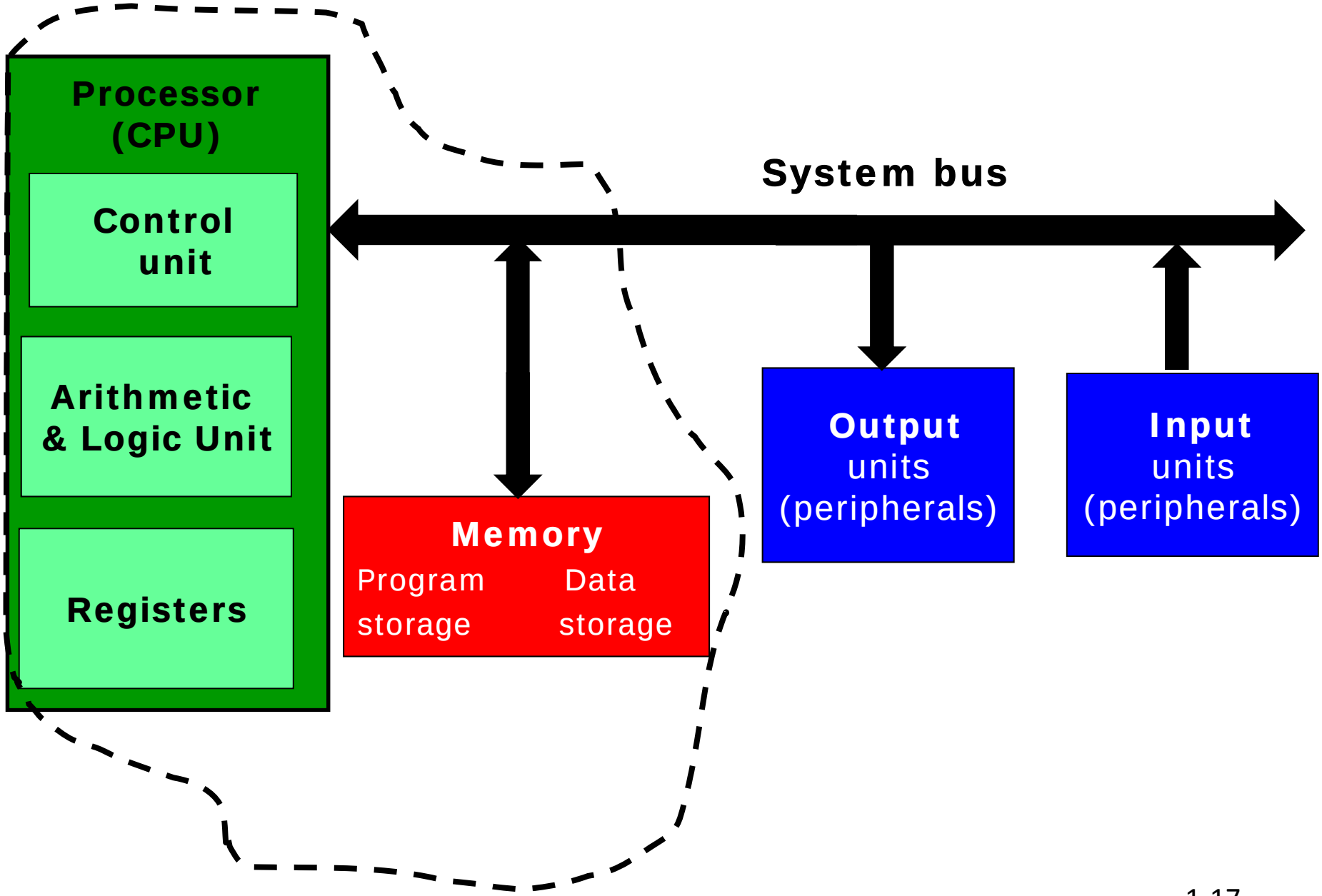
Bus Structures



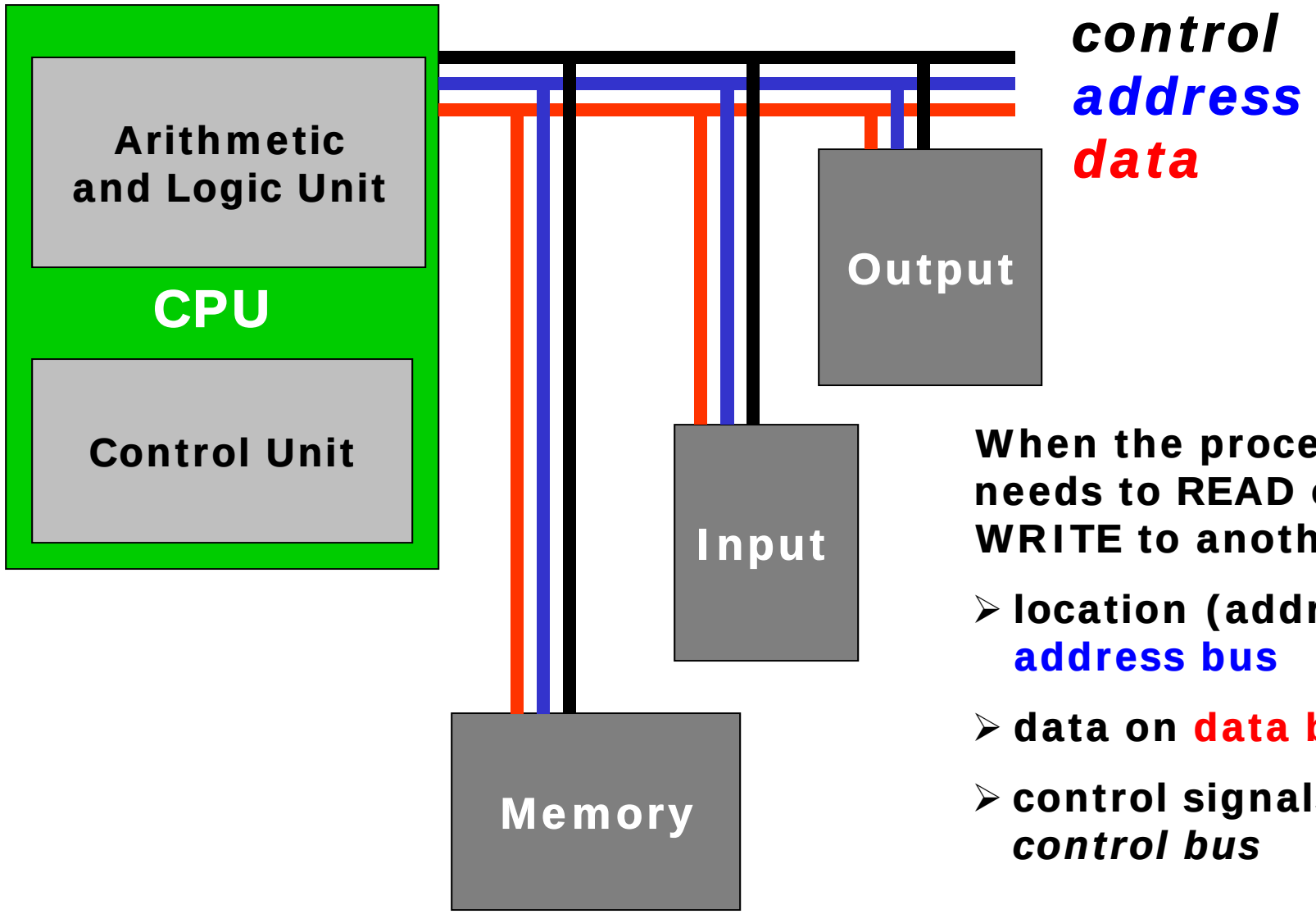
A **bus** is used to transfer information between the units.
The bus carries:

- **address**
- **data** and
- control information.

What is usually on the Motherboard?



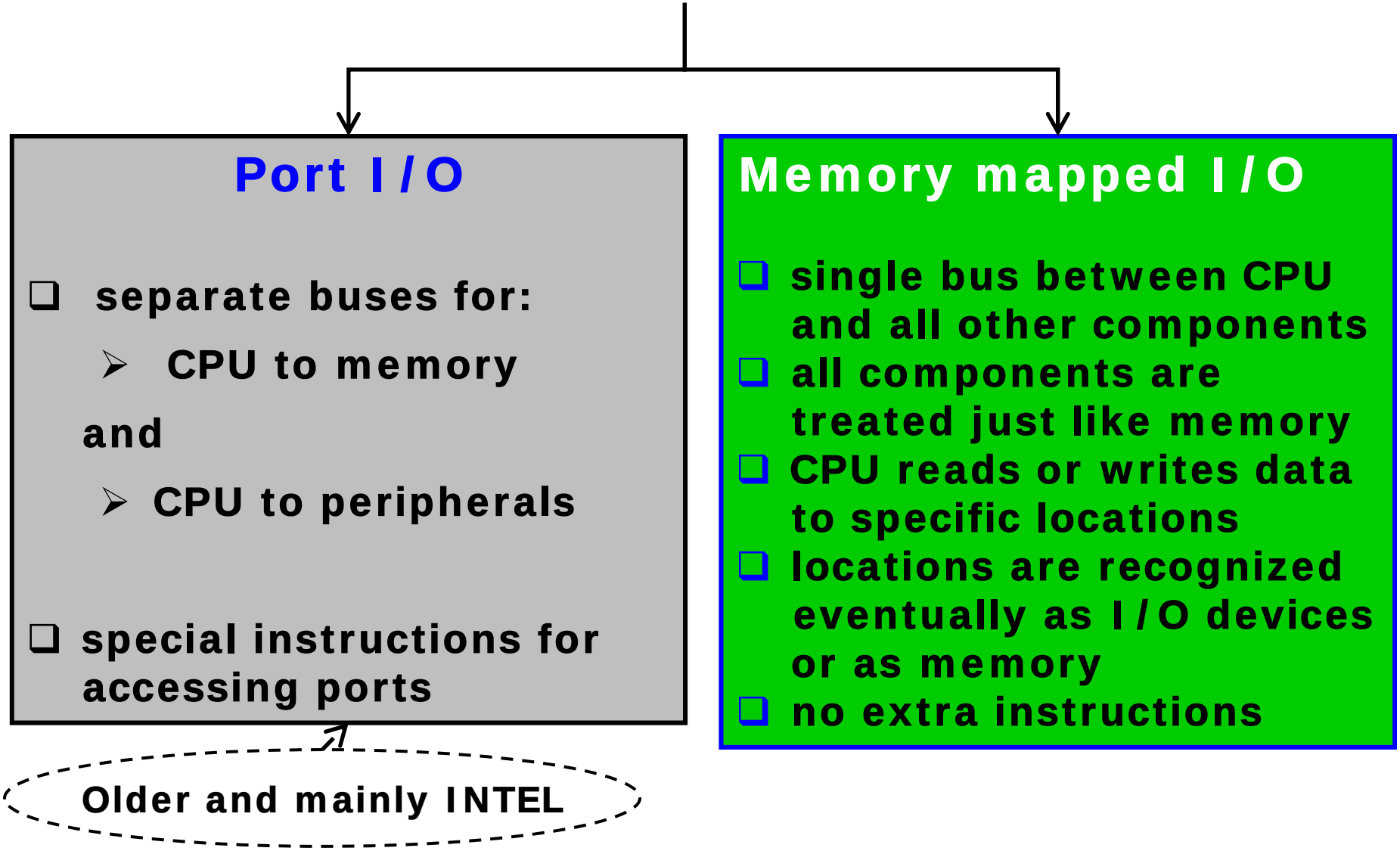
Functionality of the Bus



When the processor needs to READ or WRITE to another unit:

- **location (address) on address bus**
- **data on data bus**
- **control signals on *control bus***

Two main choices of architectures for bus structures



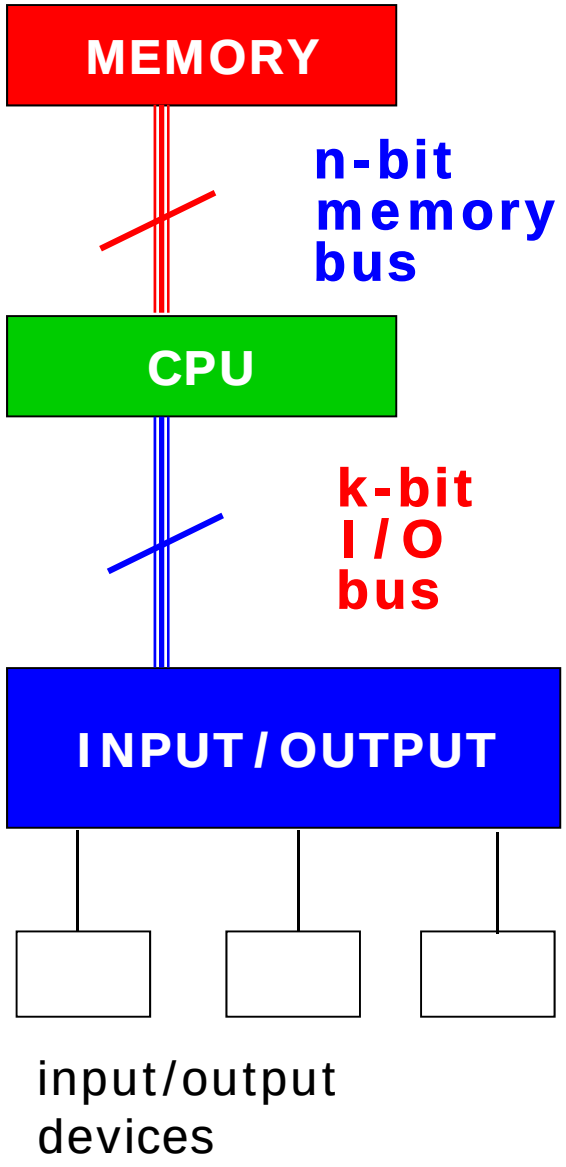
Port I/O

Older and mainly INTEL

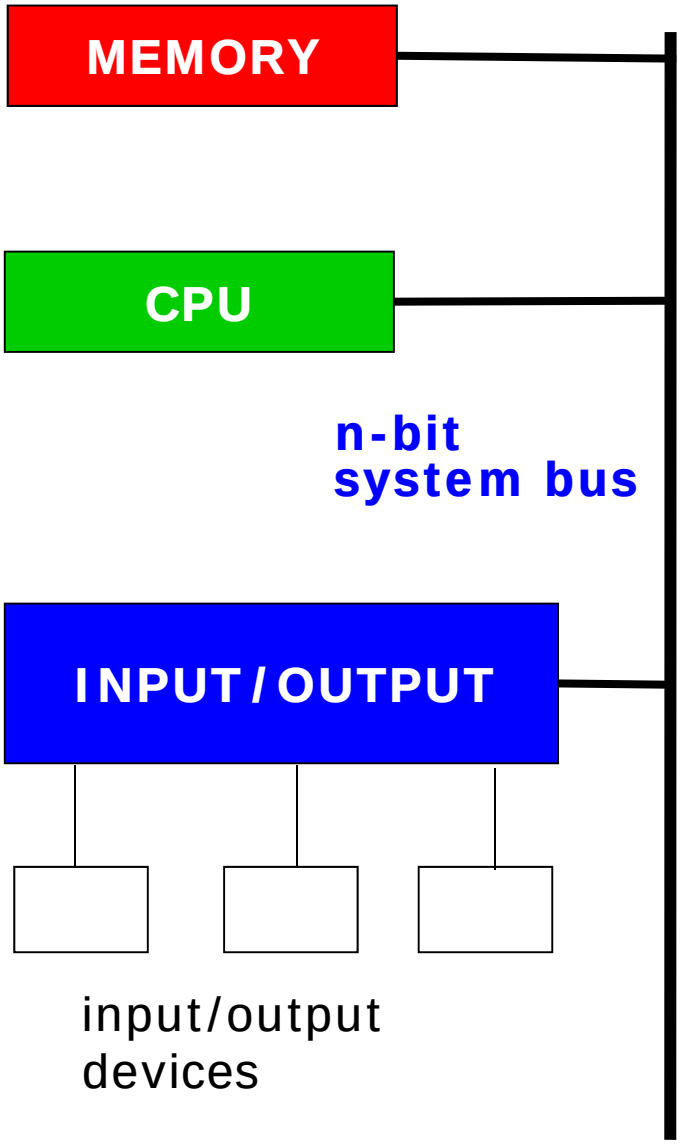
- separate buses for:
  - CPU to memory

  and
  - CPU to peripherals

- separate set of instructions
- possibly different sizes of buses
- each bus still logically composed of address, data and control

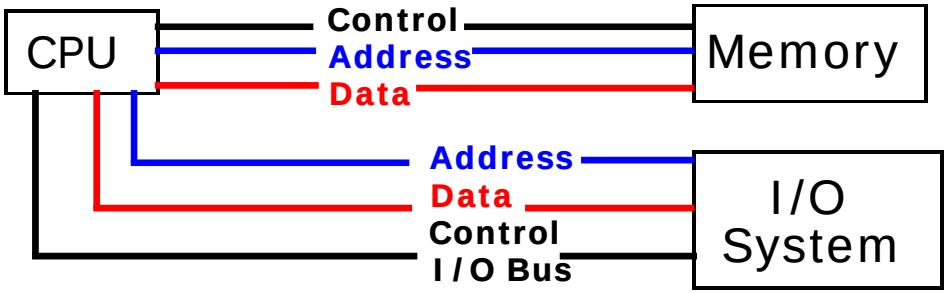


Memory Mapped I/O



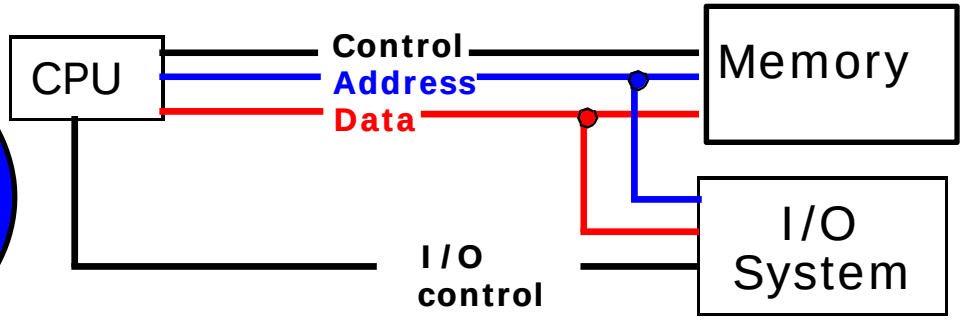
- single bus between CPU and all other elements
- logically composed of address, data and control
- given an address on the address bus, a location at that address is recognized eventually as an I/O device or memory

- e.g. office 520 or office 266
  - ✓ 5th floor, office 20
  - ✓ 2nd floor, office 66
  - ✓ the first digit distinguishes between the types of location (here a floor)



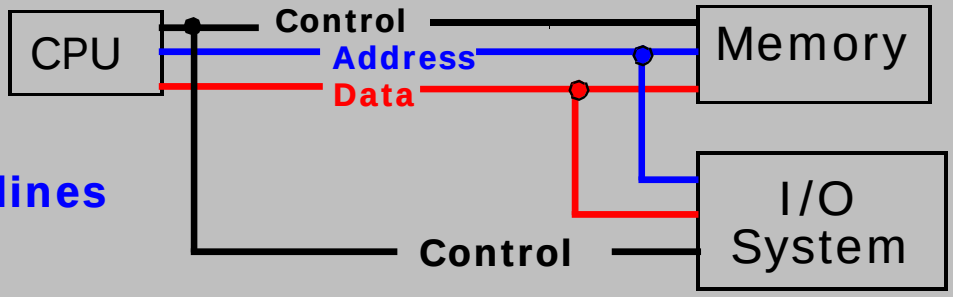
Separate memory and I/O buses (Port I/O)

Different possibilities

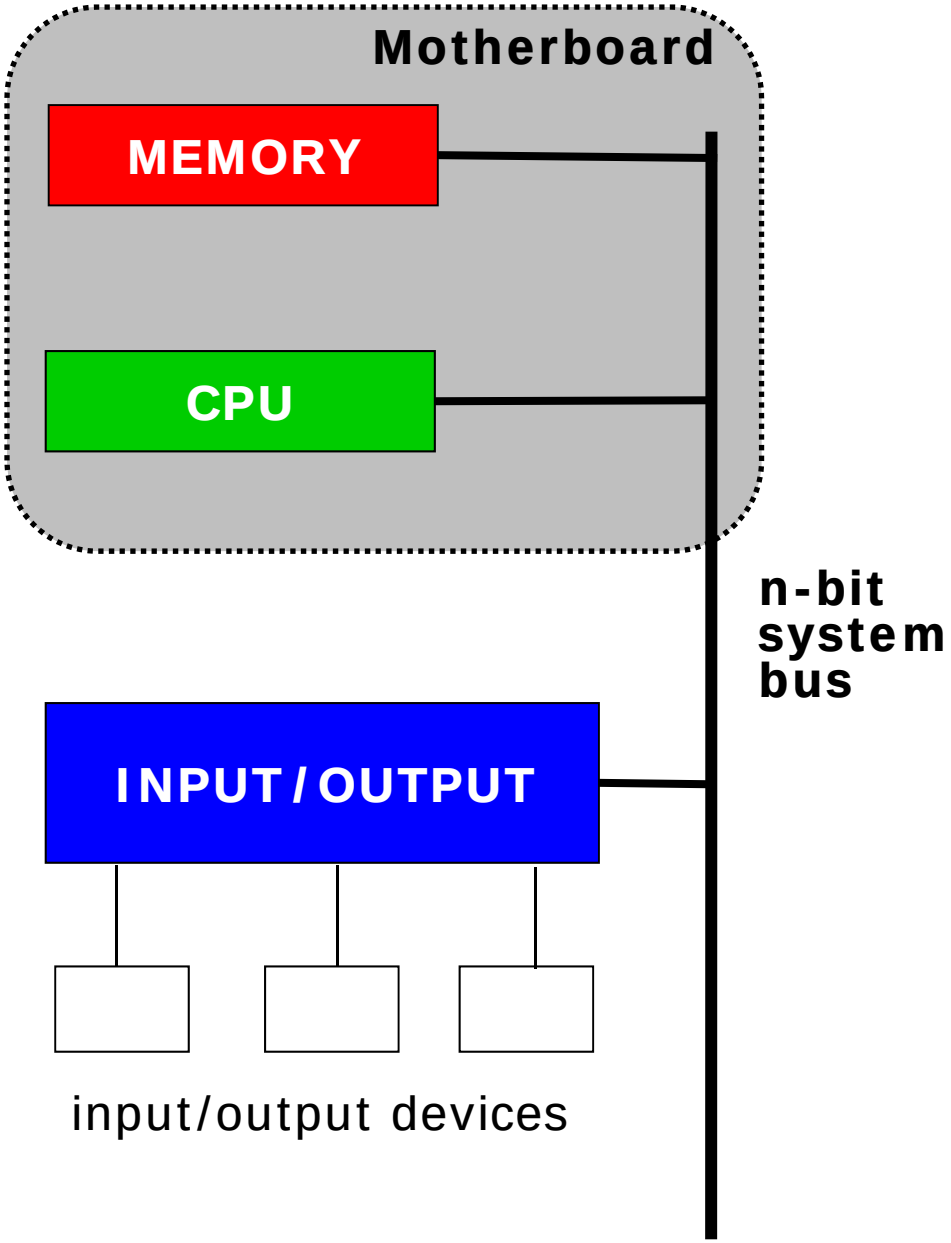


Shared address and data lines and separate control

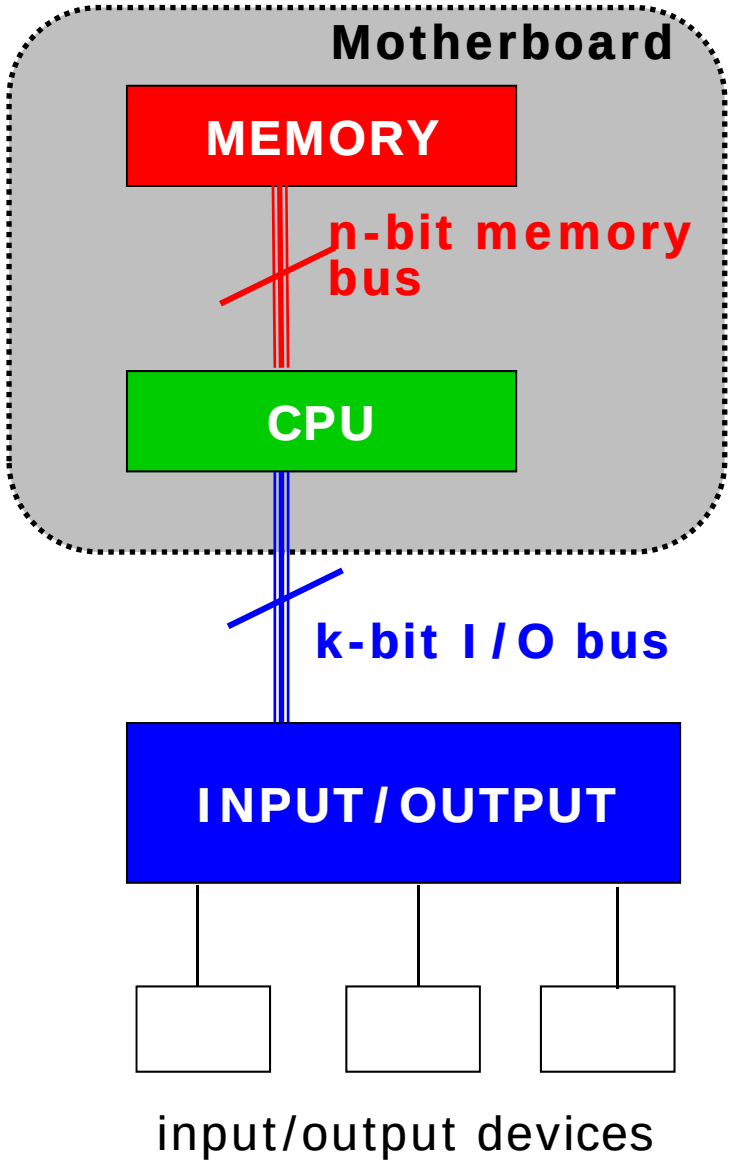
Shared address, data and control lines (memory-mapped I/O)



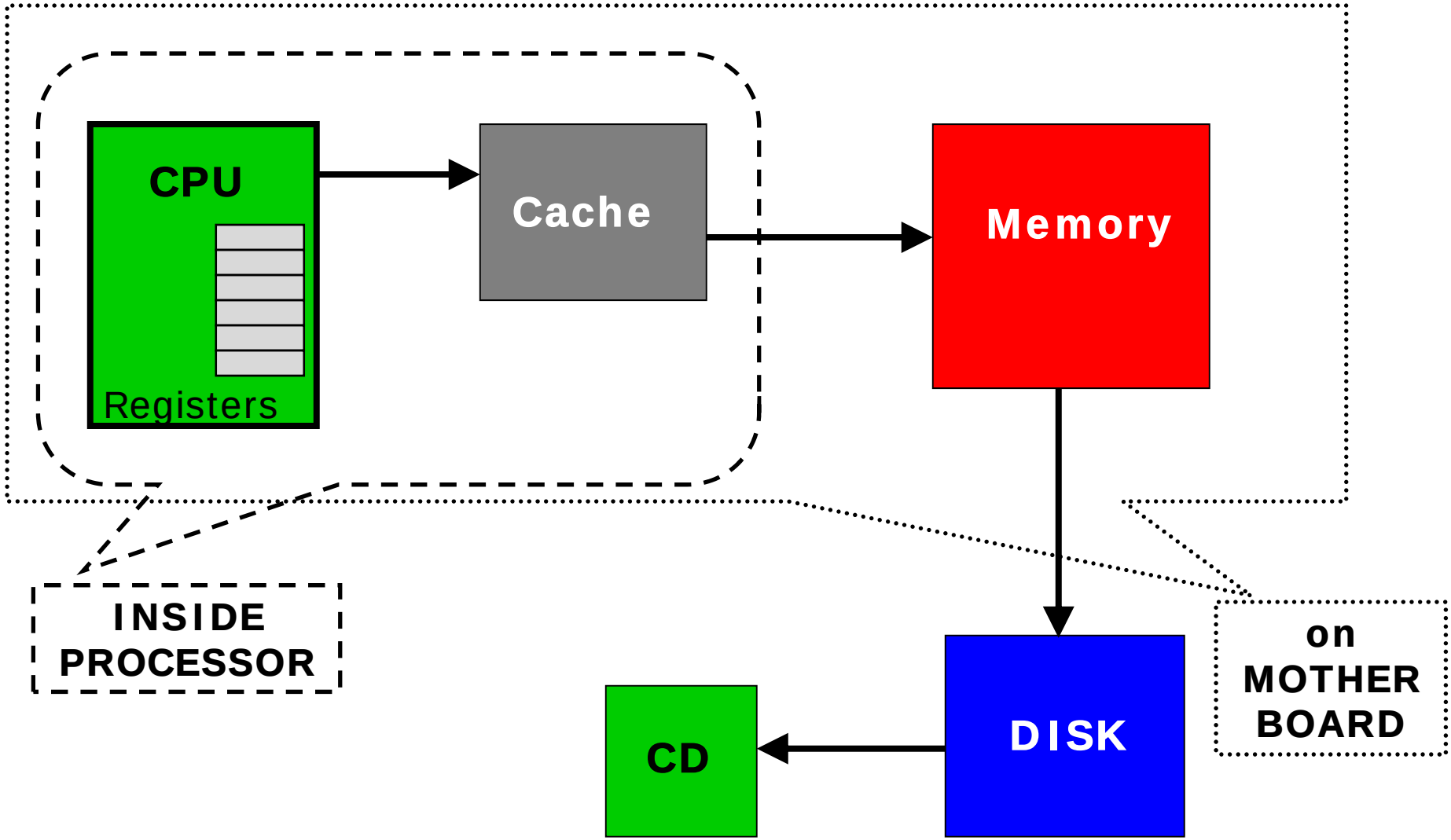
Reality 2



Reality 1



Storage Hierarchy

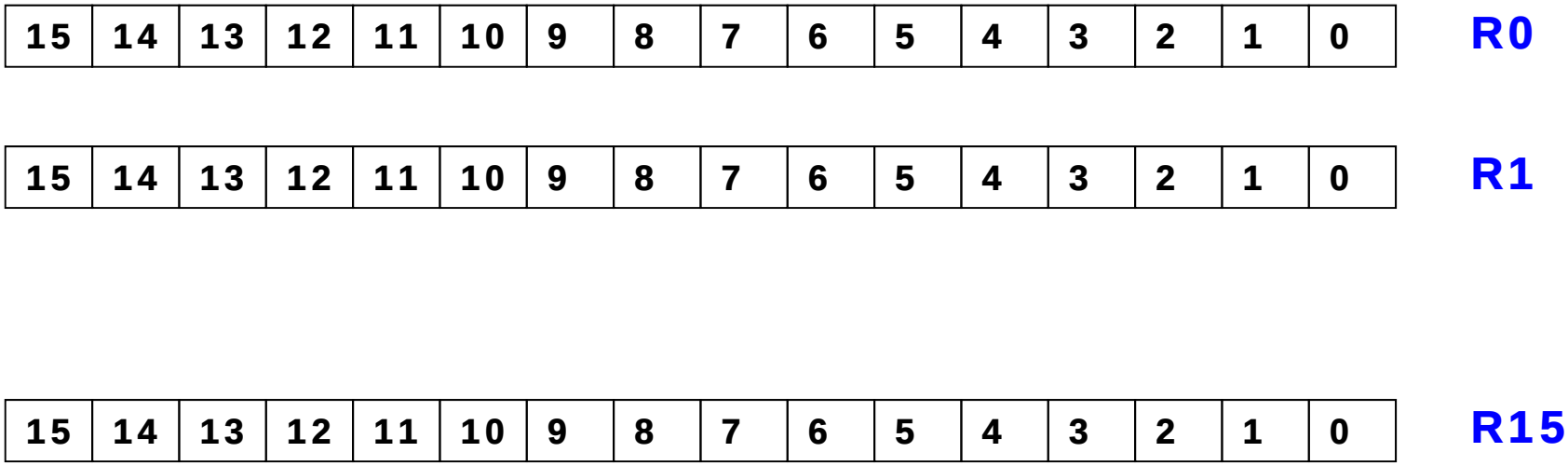


Component	Registers	Cache in CPU	RAM	Disk	CD
Access type	random	random	random	direct	direct
Capacity	64-1024	8-256KB	8K-?MB	1-80GB	740MB
Latency	1-10ns	20ns	50ns	10ms	10ms-1s
Block size	1 word	16 words	16 words	4KB	4KB
Bandwidth	system clock rate	8MB/s	1MB/s	1MB/s	1MB/s
Cost/MB	high	500	30	0.25	0.02

Registers – inside the CPU (Processor)

Registers in CPU: operational only, few of them

- ARM has 16 general purpose registers, each of 32 bits
- 68HC11 has 2
- Registers simply contain n bits (could be data or address)



R A M – Random Access Memory
(on the board, not inside the CPU)

➔ **array of cells accessed by their address (mailboxes?)**

- ***volatile / non-volatile*** **memory (retention or not of information after power is shut off)**
- ***access time*** **– time to select and read / write from a location**
- **random – all locations accessible in approximately same access time**
- **static versus dynamic (expanded on later)**

Types of Semiconductor Memory (definitions only here – more later)

- ✓ **RAM** - random access memory (static / dynamic)
- ✓ **ROM** - read only memory
- ✓ **PROM** - programmable ROM
- ✓ **EPROM** - erasable PROM (only a few times, using UV light)

Input / Output or, more generally, Peripherals (last part of the course)

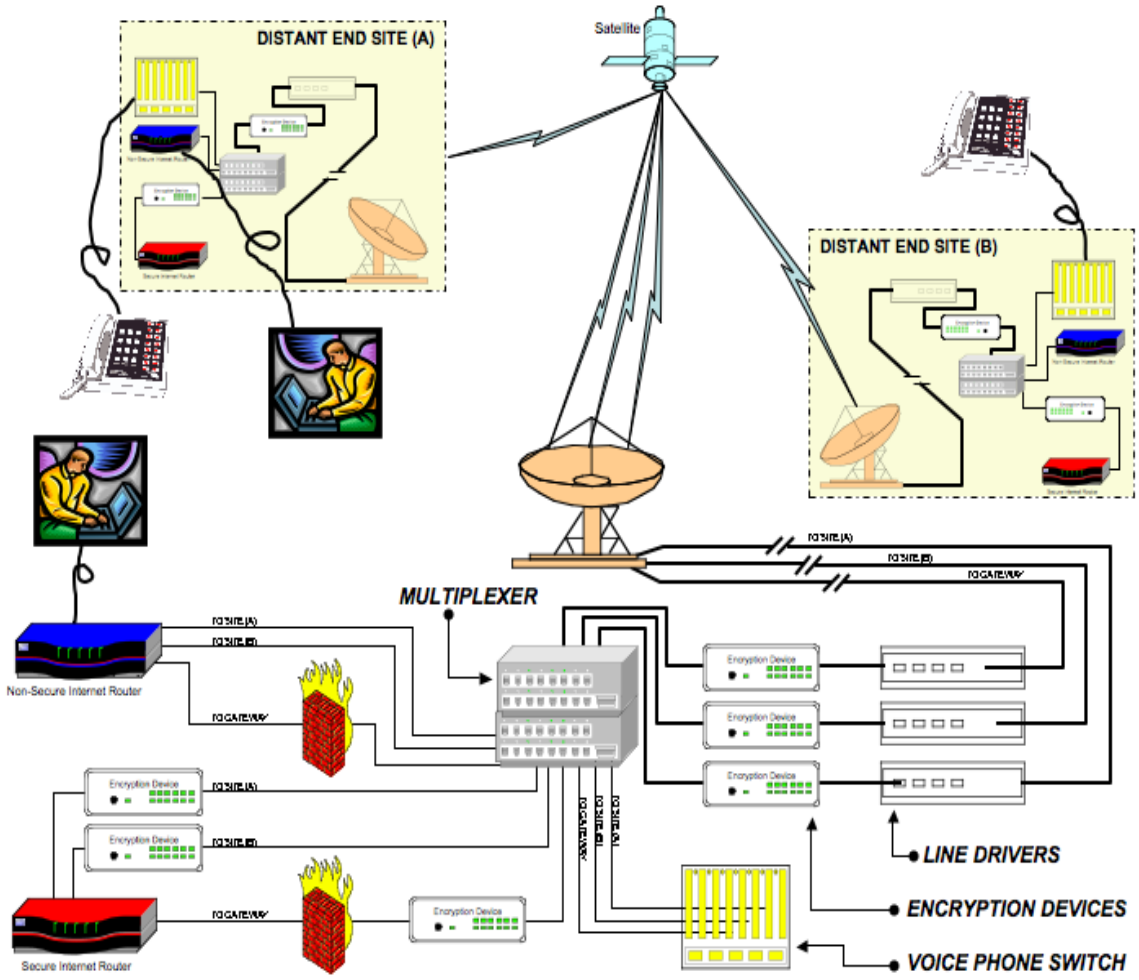
Input and output units enable the transfer of information between the system and the outside environment.

- **Example input devices: switches, keyboard, mouse, sensors.**
- **Example output devices: LEDs, video display, printer, motors.**

End-to-End Communication in Network

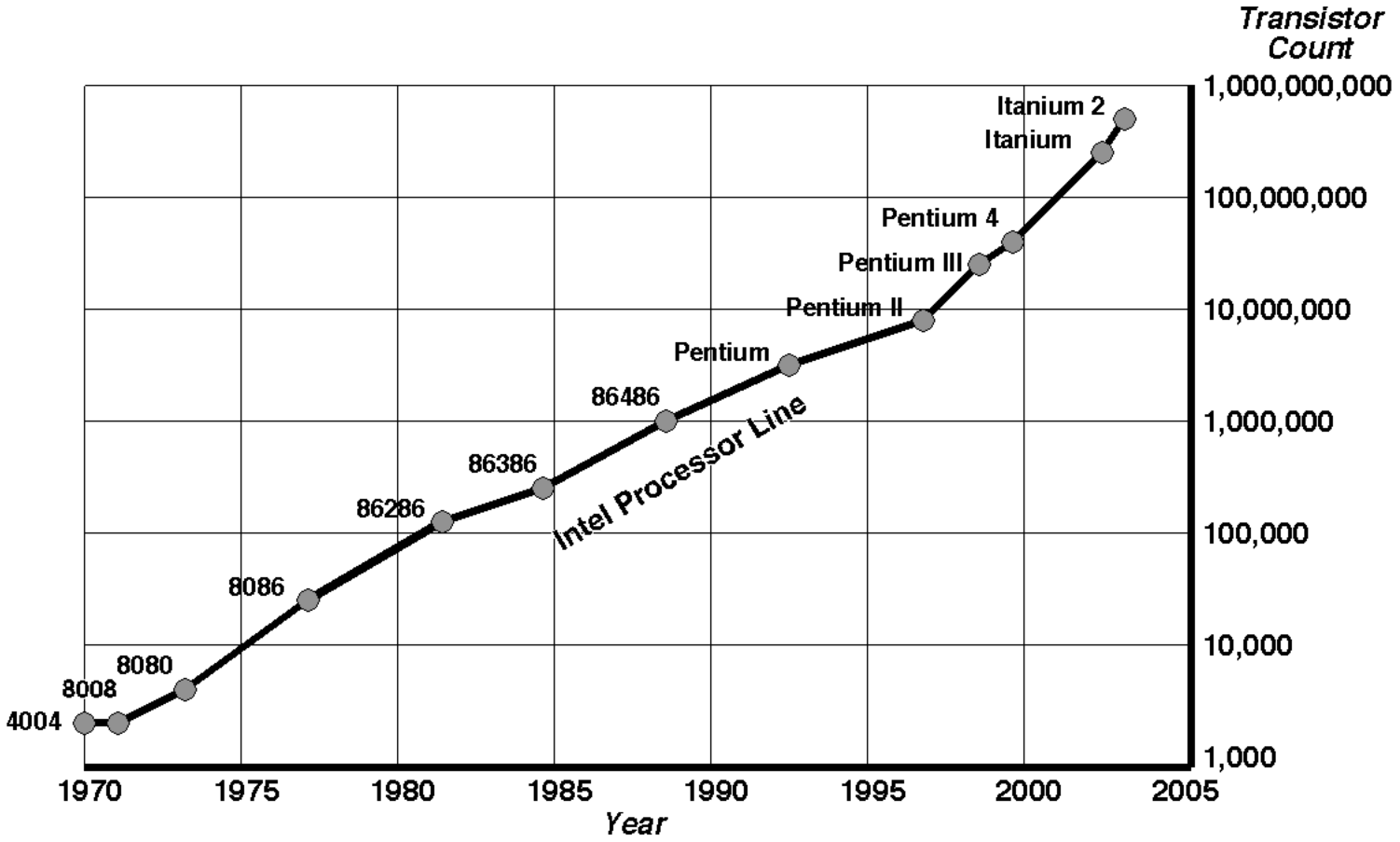
Architectural components include computers, hubs, switches, routers, firewalls, multiplexers, and phone switches.

Source: MSG
Scott Bramwell.



Moore's Law

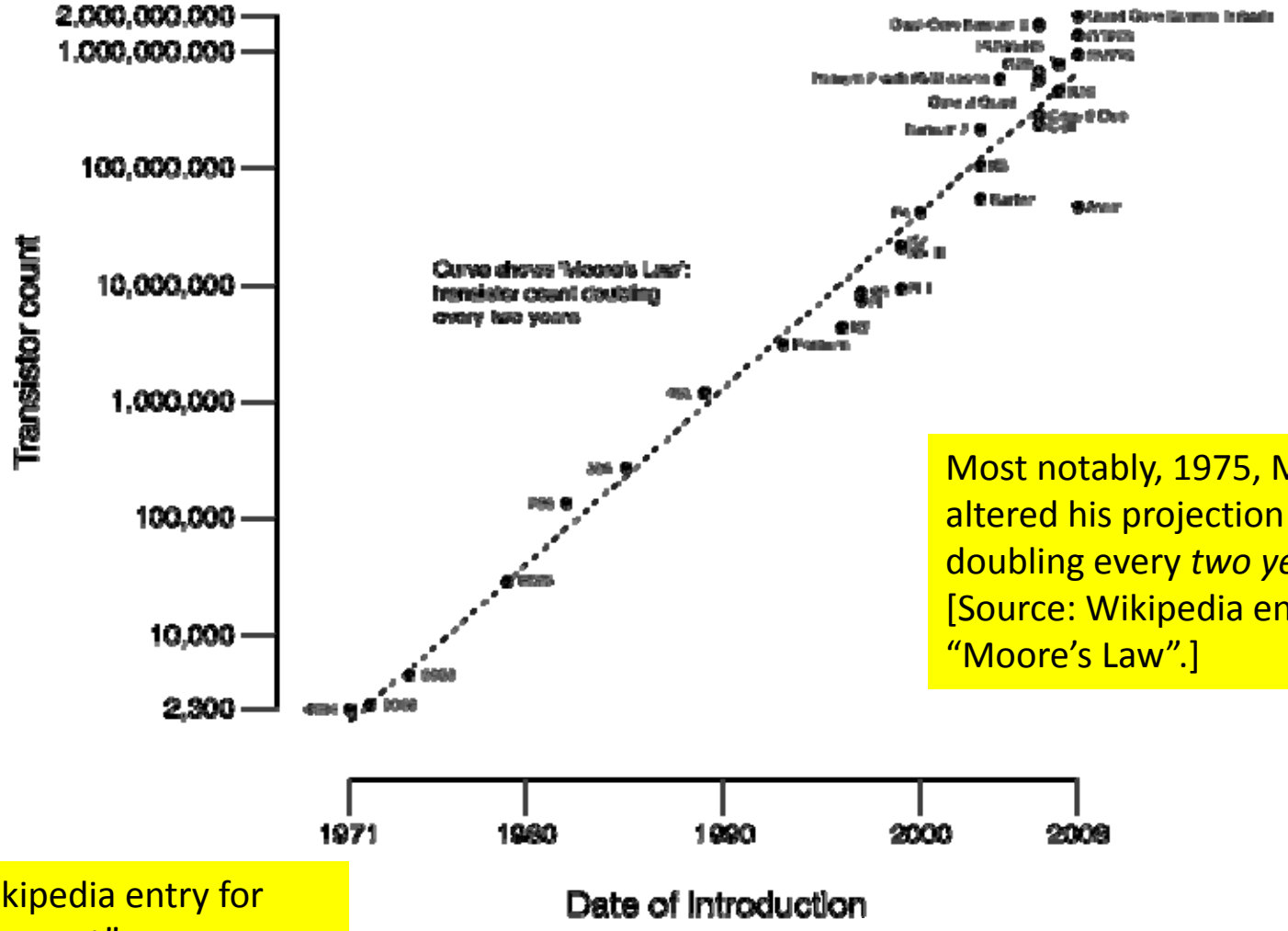
Computing power doubles every 18 months, for the same price.



Moore's Law Restated

- Computing power doubles every 18 months for the same price.
- Project planning needs to take this observation seriously: an architectural innovation that is being developed for a projected benefit that quadruples performance in three years may no longer be relevant
- The architectures that exist by then may already offer quadrupled performance and may look entirely different from what the innovation needs to be effective.

CPU Transistor Counts 1971-2008 & Moore's Law



Most notably, 1975, Moore altered his projection to a doubling every *two years*. [Source: Wikipedia entry for "Moore's Law".]

Source: Wikipedia entry for "Transistor count"

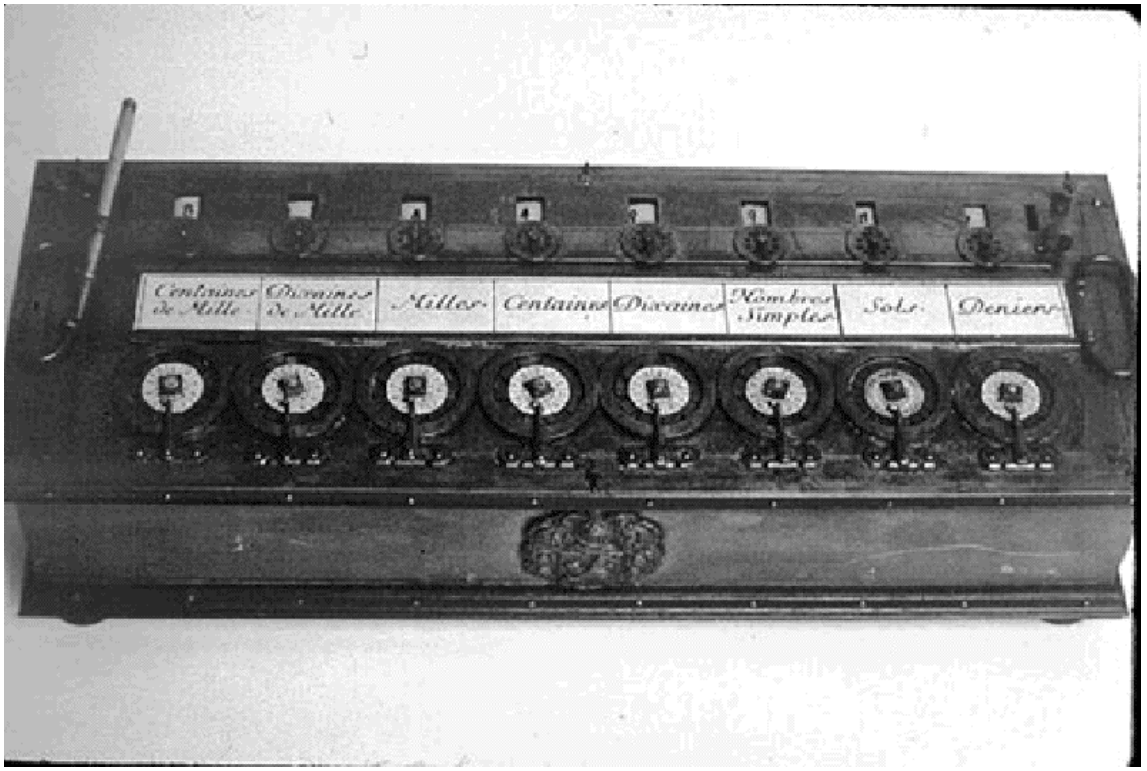
Quick Quiz

- The processor (CPU consists) of the Control Unit, the Arithmetic Logic Unit (ALU) and _____.
- The _____ and Memory are usually on the Motherboard.
- In a Port I/O architecture, there are separate buses for CPU to memory and CPU to _____.
- True or False Read Only Memory (ROM) is volatile.

Pascal's Calculating Machine (mid 1600's)

Performs basic arithmetic operations

(Source: IBM Archives photograph.)

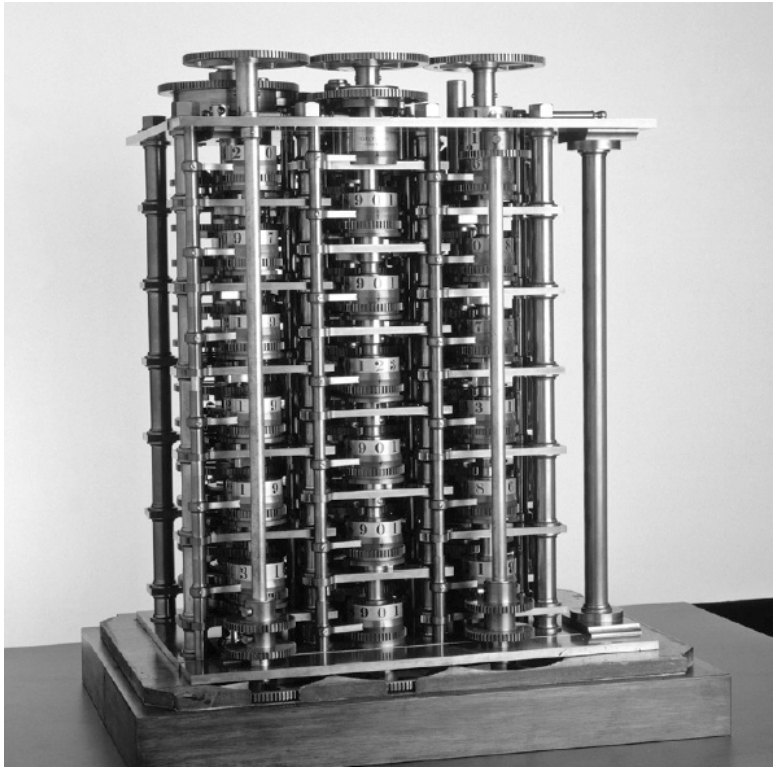


Does not have what may be considered the basic parts of a computer

Babbage's Difference Engine #1

The first known automatic calculator

(© SSPL/The ImageWorks.)



Does not have what may be considered the basic parts of a computer ➔ but "idea of algorithm"

The Jacquard Pattern Weaving Loom

The Jacquard pattern weaving loom (ca. 1804).

(Source: The Deutsches Museum.)

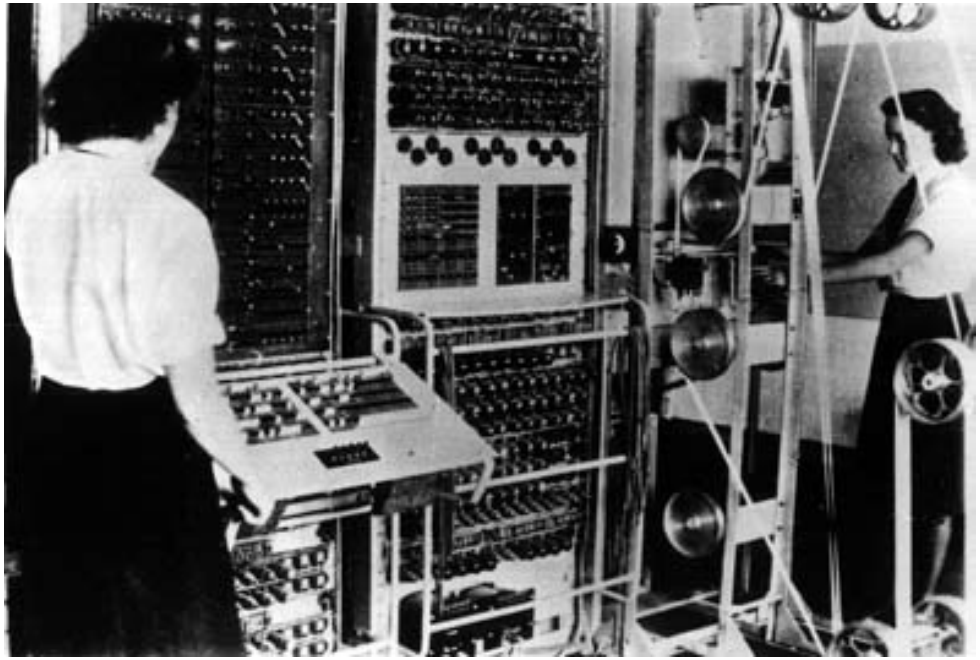
Possibly first "embedded system"?

Enigma and Colossus: the War Effort

Siemens Halkse T-52 Sturgeon (Enigma)

cipher machine.

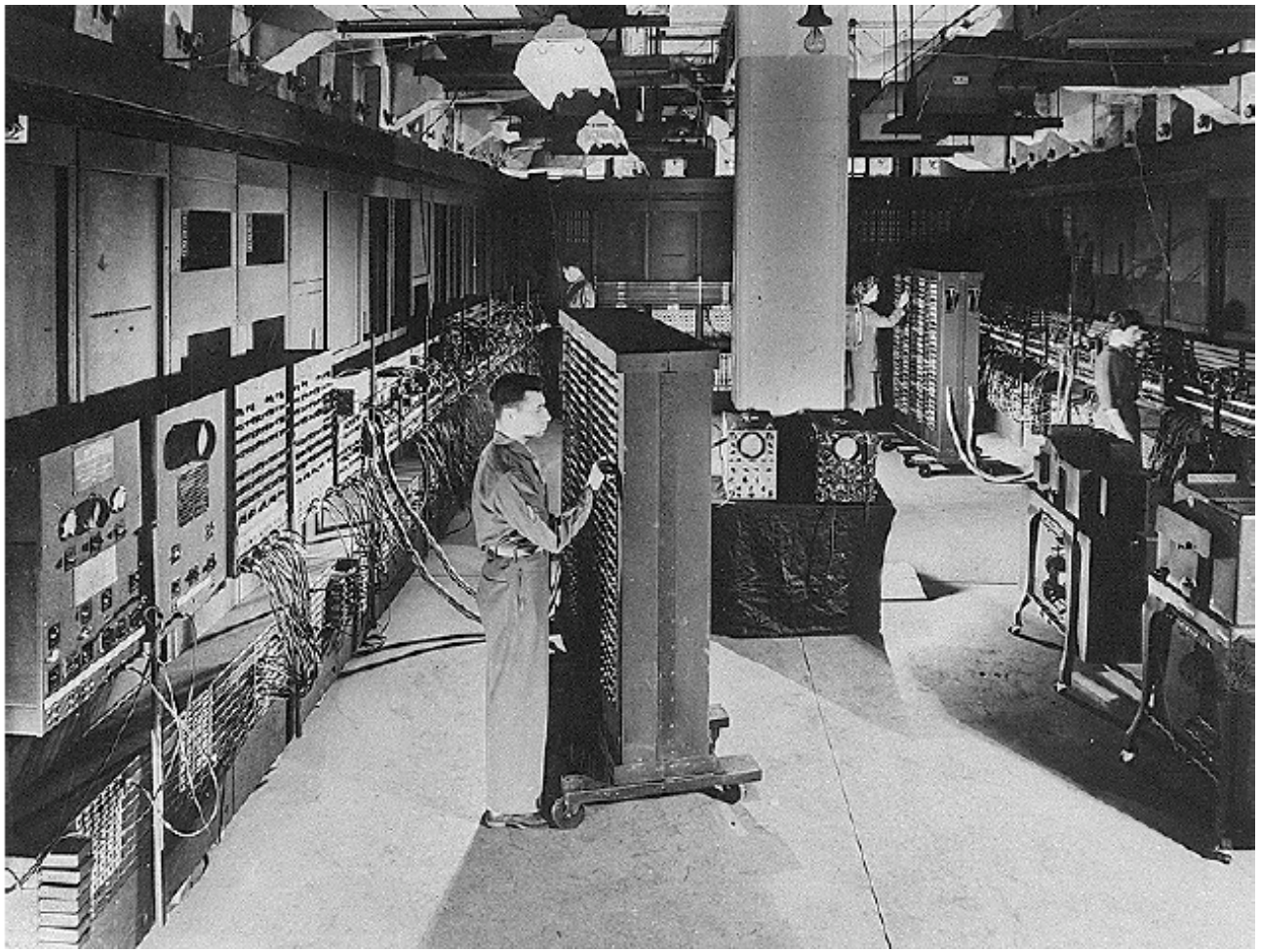
(Photo and copy courtesy
John Alexander, G7GCK
Leicester, England.)



(ca. 1944)

(Source: http://www.turing.org.uk/turing/scrapbook/electronic.html.)

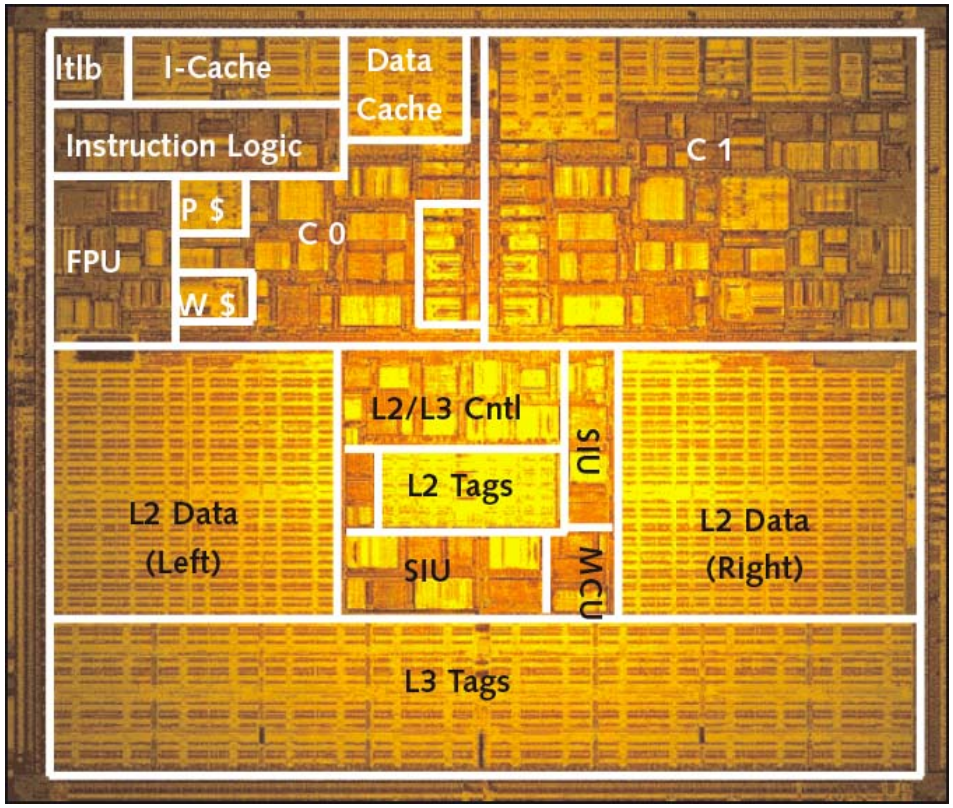
The ENIAC



(Time & Life Pictures/Getty Images.)

UltraSPARC IV+ Layout

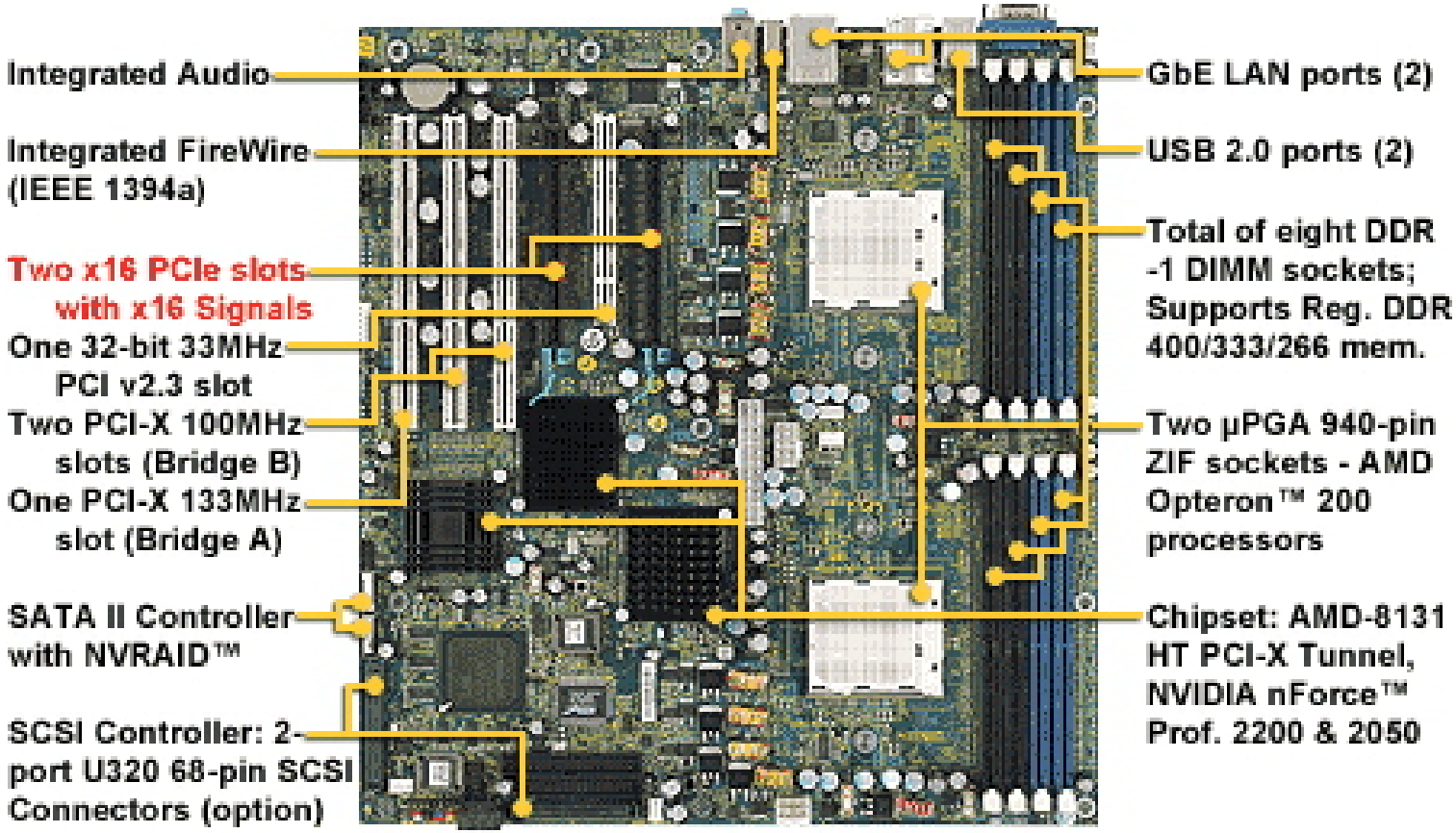
- Die photo of UltraSPARC IV+, 295 million transistors, 19.7 mm × 17.0 mm.



(Source: “Best Servers of 2004”, Kevin Krewell, 1/18/05, Microprocessor, www.MPRonline.com, Reed Electronics Group, ref: h10018.www1.hp.com/.)

The Motherboard

- An AMD Opteron 200 based motherboard.



Source: Courtesy Tyan Computer Corp. (USA).