UNIVERISTY OF VICTORIA

CENG 355 MICROPROCESSOR-BASED SYSTEMS

MIDTERM EXAMINATION

24 OCTOBER 2013

NAME:_____ STUDENT NO._____

INSTRUCTOR: D.N.RAKHMATOV DURATION: 80 MINUTES

TO BE ANSWERED IN THE BOOKLET.

STUDENTS MUST COUNT THE NUMBER OF PAGES IN THIS EXAMINATION PAPER, AND REPORT ANY DISCREPANCY IMMEDIATELY TO THE INVIGILATOR.

THIS EXAMINATION PAPER HAS **3** PAGES AND **3** QUESTIONS.

In taking this examination, you agree that all work recorded herein is your own. A student caught in the act of cheating will be given a grade of **F** on this examination.

Show your work.

Read the questions carefully. If something appears ambiguous, write down your assumptions.

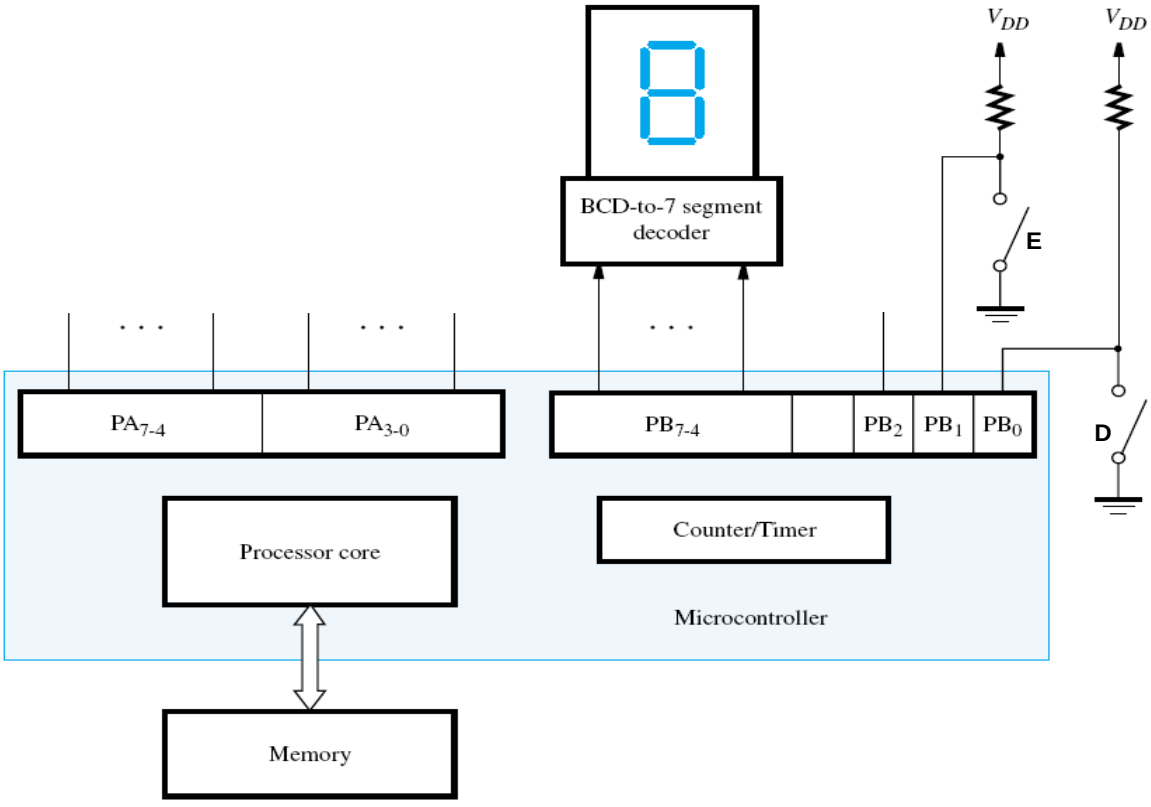
You are allowed to use books, notes, and/or calculators during this examination.

GOOD LUCK!

1. [15 points] The textbook's microcontroller below is responsible for 2 tasks: (1) conditionally incrementing the displayed digit every second, and (2) keeping track of the **E** and **D** switches: pressing **E** enables the process of incrementing the digit every second, while pressing **D** disables that process. Write the corresponding C program, assuming that the first task is the main program, and the second task is the ISR whose address is stored at location **0x20**. Assume that bit **PSR[6]** is the processor's interrupt-enable bit, and **Port B** is always ready to receive data from the processor. Initially, the 7-segment display shows **0**, and it is not being incremented.

• *Main Program*: The displayed digit must be incremented every second, provided that **E** was pressed last (i.e., the process of incrementing the digit is enabled). If **D** was pressed last, the displayed digit is unchanged (i.e., the process of incrementing the digit is disabled). Required 1-second timeouts must be implemented using the 100-MHz Counter/Timer. **Note:** Incrementing **9** gives **0**.

• *ISR*: **Port B** must be configured to generate interrupts whenever **PBIN** is changed. If **D** has been pressed, the digit is not allowed to increment every second (until **E** is pressed). If **E** has been pressed, the digit is allowed to increment every second (until **D** is pressed).



2. [10 points] Table below specifies a set of **4** independent pre-emptive tasks to be executed by a single processor. Show the task schedule using *Earliest Deadline First* (**EDF**) priority assignment.

Task T_i	P_i	C_i	D_i	ϕ_i
T1	20	4	16	0
T2	40	4	32	0
T3	40	12	40	0
T4	80	12	80	0

3. [15 points] Assume a computer has 256-byte main memory and 128-byte cache with eight blocks, where each block has four 32-bit words. While executing some program, the CPU reads 32-bit words from the following sequence of addresses:

80 48 44 20 00 40 48 C0 2C 88

Show the cache contents (e.g., **[00]** = address **00**'s contents) at the end of this sequence (10 addresses) and calculate the corresponding miss rate given that:

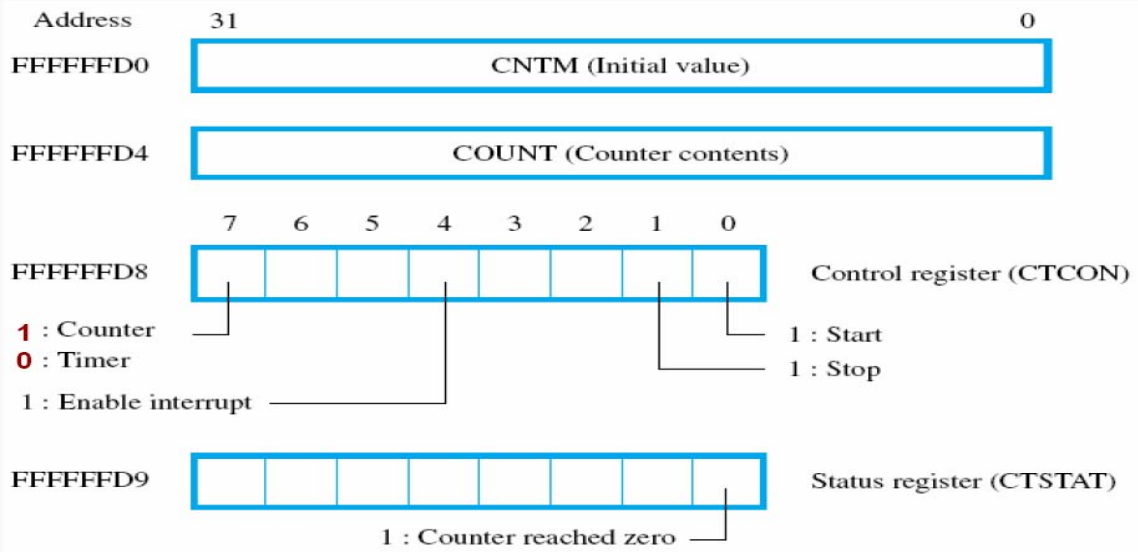
(a) Cache is direct-mapped.

(b) Cache is 4-way set-associative (4 blocks per set) with LRU replacement.

(c) Cache is fully-associative with LRU replacement.

END

Counter / Timer Registers



Parallel Port Registers